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15EC64

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Show the encapsulation and decapsulation representation in the TCP/IP model and explain. **(06 Marks)**

b. Define framing, explain role of bit stuffing in a framing. **(04 Marks)**

c. Mention the different network topology. List out advantages and disadvantages of each topology. **(06 Marks)**

OR

2 a. What are five components involved in data communication? Explain with a suitable diagram. **(05 Marks)**

b. Demonstrate stop and wait protocol by considering acknowledgement, timer and sequence no with the help of flow diagram. **(06 Marks)**

c. Describe link layer addressing with suitable illustration. **(05 Marks)**

Module-2

3 a. A ALOHA network transmits 200 bit frame using a shared channel with a 200 kbps band width. Find the through put of pure and slotted ALOHA if the system produces 500 frame per second. **(06 Marks)**

b. Describe the frame format of IEEE 802.3 Ethernet. What are minimum and maximum length of frame? **(07 Marks)**

c. Identify unicast, multicast and broad cast from the following MAC addresses:
4A : 30 : 10 : 21 : 10 : 1A
47 : 20 : 1B : 2E : 08 : EE
FF : FF : FF : FF : FF : FF. **(03 Marks)**

OR

4 a. A network using CSMA/CD has a band width of 10 Mbps. If the maximum propagation time is 25.6μs. What is the minimum size of the frame? **(05 Marks)**

b. Explain polling technique with suitable illustration. **(06 Marks)**

c. In the standard Ethernet with the transmission rate of 10 Mbps, length of cable is 2500 mt and frame size is 512 bits. The propagation speed of a signal in a cable is 2×10^8 m/s. Find efficiency of standard Ethernet. **(05 Marks)**

Module-3

5 a. Explain the following connecting devices: i) Hub ii) Link layer switch iii) Router. **(06 Marks)**

b. Define two types of Bluetooth networks. **(06 Marks)**

c. Differentiate between data gram network and virtual circuit network. **(04 Marks)**

OR

6 a. Define IEEE 802.11 addressing mechanism for four cases. **(06 Marks)**

b. Give a note on virtual LAN **(05 Marks)**

c. An organization is granted a block of address with the beginning addresses 14.24.74.0/24. The organization need to have 3 sub blocks of addresses to use in its three subnets: one sub block of 10 addresses, one sub block of 60 addresses, and one sub block of 120 addresses. Design the sub blocks. **(05 Marks)**

Module-4

7 a. Give a brief overview of IPV4 datagram. **(10 Marks)**

b. Find the shortest path from source 'A' to destination 'G' from given graph as shown in the Fig.Q7(b) using the Dijkstra algorithm. **(06 Marks)**

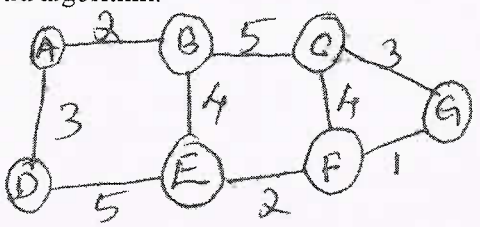

Fig.Q7(b)

OR

8 a. Explain three phases of communication between a remote host and mobile host. **(08 Marks)**

b. Explain distance-vector-routing using a Bellman Ford algorithm providing a suitable illustration. **(08 Marks)**

Module-5

9 a. Describe connectionless and connection – oriented services provided by the transport layer. **(08 Marks)**

b. Discuss TCP segment. **(08 Marks)**

OR

10 a. Demonstrate Go-back-n protocol with a forward channel is reliable but in the reverse channel, if an acknowledgment is delayed or lost. **(06 Marks)**

b. Explain a TCP connection establishment using three way hand shaking. **(10 Marks)**

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15EC655

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Derive the expression of $i_D - V_{DS}$ relationship for triode and saturation region of NMOS transistor. **(10 Marks)**

b. For the MOSFET with $\frac{W}{L} = \frac{8\,\mu m}{0.8\,\mu m}$. Calculate the values of V_{GS} and V_{DS} (min) needed to operate the transistor in the saturation region with a dc current I_D = 100 μA. Assume $K_n' = 194\mu A/V^2$ and $V_t = 0.7\,V$. **(06 Marks)**

OR

2 a. Explain channel length modulation effect and derive an expression for finite output resistance of a MOSFET in saturation region. **(10 Marks)**

b. Explain the breakdown effect that occurs in MOSFET and also the body effect. **(06 Marks)**

Module-2

3 a. Explain the operation of a MOSFET current mirror. **(06 Marks)**

b. Draw the circuit model of a MOSFET to show the development of the T equivalent. **(06 Marks)**

c. Using two transistors having equal lengths but widths related by $\left(\frac{W_2}{W_1}\right) = 5$, design the circuit to obtain I = 0.5 mA. Let $V_{DD} = -V_{SS} = 5V$, $K_n'\left(\frac{W}{L}\right)_1 = 0.8\ mA/V^2$, $V_t = 1\ V$ and $\lambda = 0$. Find the required value of resistance (R). What is the voltage at the gates of two transistors for biasing using constant-current source? **(04 Marks)**

OR

4 a. Consider a common source amplifier specified as follows:

$\left(\frac{W}{L}\right)K_n' = 1\,mA/V^2$, $V_{DD} = -V_{SS} = 10V$, R_D=15 KΩ, $R_{sig} = 100$ KΩ, $R_G = 4.7$ MΩ, $R_L = 15\,K\Omega$, I = 0.5 mA, V_t = 1.5 V, V_{GS} = 2.5 V

Peak to peak sinusoidal voltage (V_{sig}) = 0.4 V, assume V_A = 75 V. Find R_{in}, A_{vo} and R_{out} both without and with r_O taken into account. **(06 Marks)**

b. Derive the voltage gain and overall voltage gain equations of a source follower using MOSFET. **(10 Marks)**

Module-3

5 a. Compare NMOSFET and BJT in terms of current voltage characteristics, low frequency model, high frequency model and output resistance. **(08 Marks)**

b. Explain the operation of a MOSFET current steering circuits with necessary expressions. **(08 Marks)**

OR

6 a. Derive an expression for 3 dB frequency f_H for an amplifier having 2 poles and 2 zeros. **(10 Marks)**

b. Explain Millers theorem. **(06 Marks)**

Module-4

7 a. Briefly explain common source amplifier with active load. **(06 Marks)**

b. With neat circuit diagram, explain the MOS cascade amplifier to show that $V_0 = A_{V02} V_{01}$. **(10 Marks)**

OR

8 a. Consider common gate amplifier specified as follows:

$\left(\frac{W}{L}\right) = \frac{7.2\mu m}{0.36\mu m}$, $\mu_n C_{ox} = 387\mu A/V^2$, $r_0 = 18\ K\Omega$, $I_D = 100\ \mu A$, $g_m = 1.25$ m/V

$x = 0.2$, $R_S = 10\ K\Omega$, $R_L = 100\ K\Omega$, $C_{gs} = 20$ fF, $C_{gd} = 5$ fF and $C_L = 0$.

Find A_{VO}, R_{in}, R_{out}, G_V, G_{is}, G_i and f_H. **(06 Marks)**

b. Explain the common source amplifier with source degeneration resistance R_S. **(10 Marks)**

Module-5

9 a. Explain the operation of a basic circuit of MOS differential pair with a common mode input voltage. **(08 Marks)**

b. Obtain common mode gain and Common Mode Rejection Ratio (CMRR) of the MOS differential amplifier. **(08 Marks)**

OR

10 a. For the nMOS differential pair with a common mode voltage V_{cm} applied as shown in Fig. Q10 (a). Let $V_{DD} = V_{SS} = 1.5$ V, $K_n' \frac{W}{L} = 4$mA/V^2, $V_t = 0.5$ V, I = 0.4 mA, $R_D = 2.5\ K\Omega$ and neglect channel modulation.

(i) Find V_{OV} and V_{GS} for each transistor.

(ii) For $V_{CM} = 0$, find V_S, i_{D_1}, i_{D_2}, V_{D_1} and V_{D_2}.

(iii) Repeat (ii) for $V_{CM} = 1$ V. **(07 Marks)**

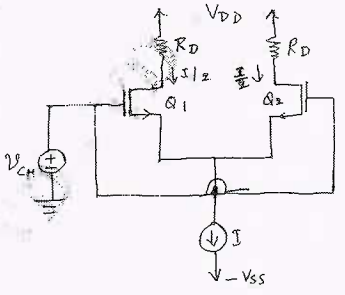

Fig. Q10 (a)

b. Draw the two-stage CMOS op-amp configuration and briefly explain. Obtain overall dc open-loop gain. **(09 Marks)**

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15EC52

Fifth Semester B.E. Degree Examination, June/July 2019
Digital Signal Processing

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Describe the process of frequency domain sampling and reconstruction of discrete time signals. **(10 Marks)**

b. Using linearity property find the DFT of the sequence $x(n) = \cos\left(\frac{\pi n}{4}\right) + \sin\left(\frac{\pi}{2} n\right)$ consider N =4. **(06 Marks)**

OR

2 a. State and prove the i) circular time shift ii) circular time reversal properties of DFT. **(08 Marks)**

b. Solve by concentric circle or graphical method to find circular convolution x(n) = {1, 3, 5, 3} and h(n) = {2, 3, 1, 1}. **(04 Marks)**

c. Derive the expression for the relationship of DFT with Z – transforms. **(04 Marks)**

Module-2

3 a. State and prove the following properties :
i) Circular correlation
ii) Parseval's theorem. **(06 marks)**

b. Consider a FIR filter with impulse response h(n) = {3, 2, 1, 1}. If the input is x(n) = {1, 2, 3, 3, 2, 1, –1, –2, –3, 5, 6, –1, 2, 0, 2, 1}. Find the output use overlap – same method. Assuming the length of block is 9. **(10 Marks)**

OR

4 a. Explain the linear filtering of long data sequences using overlap-add method. **(08 marks)**

b. An FIR filter has the impulse response of } $h(n) = \left\{\underset{\uparrow}{1},\ 2, 3\right\}$. Determine the response of the filter to the input sequence $x(n) = \left\{\underset{\uparrow}{1},\ 2\right\}$ use DFT and IDFT and verify the result using direct computation of linear convolution. **(08 Marks)**

Module-3

5 a. Develop DIT–FFT algorithm and obtain the signal flow diagram for N = 8. **(08 Marks)**

b. Determine the IDFT of X(K) = {4, 1 – j2.414, 0, 1 –j0.414, 0, 1 + j0.414, 0, 1 + j2.414} using inverse – radix 2 DIT – FFT algorithm. **(08 Marks)**

OR

6 a. Define chirp Z–transform. What are the applications of chirp–Z transform. **(04 Marks)**

b. The DFT of the following sequence using DIF – FFT algorithm
$x_1(n)$ = {1, 1, 1, 0, 0, 1, 1, 1} (ii) using the results in (i) Find DFT of signal $x_2(n)$ = {1, 1, 1, 1, 1, 0, 0, 1} consider N = 8. **(12 Marks)**

Module-4

7 a. Obtain the direct form I, direct form II, cascade and parallel form realization for the following system. $y(n) = 0.75y(n-1) - 0.125y(n-2) + 6x(n) + 7x(n-1) + x(n-2)$. **(08 Marks)**

b. Realize the system given by the difference equation :
$y(n) = -0.1y(n-1) + 0.72y(n-2) + 0.7x(n) - 0.252\,x(n-2)$
Use parallel form. Is this system stable? Determine its impulse response. **(08 Marks)**

OR

8 a. Design an IIR digital filter that when used in the prefilter A/D – H(z) – D/A structure will SATISFY the following equivalent along specifications. **(10 Marks)**

i) LPF with –1dB cutoff at 100π rad/sec
ii) stopband attenuation of 35dB or greater at 1000π rad/sec.
iii) monotonic stop band and pass band
iv) sampling rate of 2000 samples/sec.

b. Obtain H(z) using impulse invariance method for the following analog filter 5Hz sampling frequency $H_a(S) = \dfrac{2}{(S+1)(s+2)}$. **(06 Marks)**

Module-5

9 a. Realize a linear phase FIR filter with the following impulse response.
$h(n) = \sigma(n) + \frac{1}{4}\sigma(n-1) - \frac{1}{8}\sigma(n-2) + \frac{1}{4}\sigma(n-3) + \sigma(n-4)$. **(06 Marks)**

b. Consider a 3–stage FIR lattice structure having the coefficients $K_1 = 0.65$, $K_2 = -0.34$, $K_3 = 0.8$. Evaluate its impulse response by tracing a unit impulse $\sigma(n)$ at its input through the Lattice structure. Also, draw its direct form–I structure. **(10 Marks)**

OR

10 a. the desired frequency response of a LPF

$$H_d(w) = \begin{cases} e^{-j3w} & |w| < 3\pi/4 \\ 0 & 3\pi/4 < |w| < \pi \end{cases}.$$

Find the impulse response h(n) using Hamming window. Determine the frequency response of FIR filter. Consider N = 7. **(10 Marks)**

b. Explain the following terms :
i) Hamming window
ii) Hanning window
iii) Bartlet window. **(06 Marks)**

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15EC53

Fifth Semester B.E. Degree Examination, June/July 2019
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Discuss different type of module level with an example. **(08 Marks)**

b. List the basic type of design methodology. Differentiate between them. **(08 Marks)**

OR

2 a. What do you mean by instantiation and instances? Write a verilog code for 4 bit ripple carry counter to show instantiation and instances. **(08 Marks)**

b. What is the need of stimulus block in simulation, discuss with an example. **(08 Marks)**

Module-2

3 a. List and explain different system tasks and compiler directives of verilog. **(10 Marks)**

b. List the components of a verilog module. Write a verilog code to list the components of SR latch. **(06 Marks)**

OR

4 a. Explain, how integer, real and time register data types used in verilog. **(08 Marks)**

b. Show how connections between signals are specified in the module instantiation and the parts in a module definition. **(08 Marks)**

Module-3

5 a. Discuss on And/Or Gates with respect to logic symbols, gate instantiation and truth tables. **(08 Marks)**

b. Design AOI based 4:1 multiplexer, write verilog description for the same and its stimulus. **(08 Marks)**

OR

6 a. List the characteristics of continuous assignments. **(04 Marks)**

b. Write the verilog description of 4 bit full adder using dataflow operators and with carry look ahead mechanism. **(06 Marks)**

c. Discuss briefly available gate delays in verilog. **(06 Marks)**

Module-4

7 a. Explain multiway branchings loops with examples. **(14 Marks)**

b. Outline the characteristics of parallel blocks. **(02 Marks)**

OR

8 a. List and discuss different delay based timing control. **(09 Marks)**

b. Differentiate between blocking and non blocking assignments. **(07 Marks)**

Module-5

9 a. List and explain the short comings of VHDL. **(04 Marks)**

b. List the different steps of VHDL design process for design synthesis? Discuss briefly. **(12 Marks)**

OR

10 a. Write VHDL code for 4 bit comparator using behavioral description style. **(05 Marks)**

b. Write VHDL code for full adder in structural description style using 2 half adders. **(05 Marks)**

c. Explain scalar data types of VHDL with examples. **(06 Marks)**

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15EC54

Fifth Semester B.E. Degree Examination, June/July 2019
Information Theory and Coding

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define information content, entropy and information rate. **(03 Marks)**

b. A card is selected at random from a deck of playing cards. If you are told that it is in red colour, how much information is conveyed? How much additional information is needed to completely specify a card? **(05 Marks)**

c. Prove the maximal property of entropy. **(08 Marks)**

OR

2 a. A DMS has an alphabet X = $\{x_1, x_2, x_3, x_4\}$ with probability statistics $\left\{\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{8}\right\}$ show that $H(X^2) = 2.H(x)$. **(06 Marks)**

b. For the Markov source shown in Fig.Q.2(b). Find state probability, state entropy and source entropy. Also, write tree diagram to generate message of length 2. **(10 Marks)**

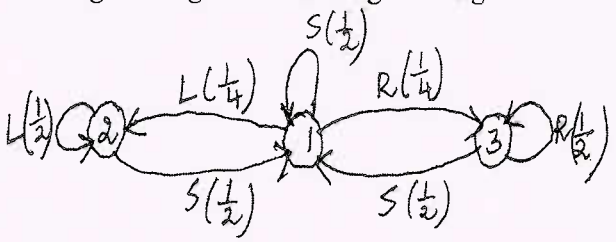

Fig.Q.2(b)

Module-2

3 a. Apply Shannon encoding algorithm and generation codes for the set of symbols S = $\{s_1, s_2, s_3, s_4, s_5, s_6\}$ with probability P = {0.3, 0.25, 0.20, 0.12, 0.08, 0.05}. Find code efficiency and variance. **(08 Marks)**

b. Using Shannon Fano algorithm, encode the following set of symbols and find the P(0) and P(1) {Probability of Zeros and ones}. **(05 Marks)**

Symbol	a	b	c	d	e	f	g
P	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.015625

c. Write the decision tree for the following set of codes and check for KMI property:

S_1	1
S_2	01
S_3	001
S_4	0001
S_5	00001

(03 Marks)

OR

4 a. A DMS has an alphabet of seven symbols with probability statistics as given below:
$S = \{s_1, s_2, s_3, s_4, s_5, s_6, s_7\}$

$$P = \left\{\frac{1}{4}, \frac{1}{4}, \frac{1}{8}, \frac{1}{8}, \frac{1}{8}, \frac{1}{16}, \frac{1}{16}\right\}$$

Compute Huffman code for these set of symbols by moving the combined symbols as high as possible. Explain why the efficiency of the coding is 100%. **(08 Marks)**

b. Write a note on Lempel – Ziv Algorithm. **(04 Marks)**

c. Design compact Huffman code by taking the code alphabet X = {0, 1, 2} for the set of symbols $S = \{s_1, s_2, s_3, s_4, s_5, s_6\}$, $P = \left\{\frac{1}{3}, \frac{1}{4}, \frac{1}{8}, \frac{1}{8}, \frac{1}{12}, \frac{1}{12}\right\}$. Find efficiency. **(04 Marks)**

Module-3

5 a. The TPM of a channel is given below. Compute H(x), H(y), H(x/y) and H(y/x)

$$P(xy) = \begin{bmatrix} 0.48 & 0.12 \\ 0.08 & 0.32 \end{bmatrix}$$ **(05 Marks)**

b. A binary symmetric channel has the following noise matrix. Compute mutual information, data transmission rate and channel capacity if $r_s = 10$ sym/sec

$$P(y/x) = \begin{bmatrix} 1/4 & 3/4 \\ 3/4 & 1/4 \end{bmatrix}$$

$$P(x) = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$ **(06 Marks)**

c. Derive an expression for the data transmission rate of binary Erasure channel. **(05 Marks)**

OR

6 a. An engineer says that he can design a system for transmitting computer output to a line printer operating at a speed of 30 lines/minute over a cabel having bandwidth of 3.5 kHz and $\frac{S}{N} = 30\text{dB}$. Assume that the printer needs 8 bits of data/character and prints out 80 characters/line. Would you believe the engineer? **(06 Marks)**

b. Write a note on differential entropy. **(05 Marks)**

c. Consider a binary symmetric channel whose channel matrix is given by $P(y/x) = \begin{bmatrix} 0.8 & 0.2 \\ 0.4 & 0.6 \end{bmatrix}$. Find channel capacity. **(05 Marks)**

Module-4

7 a. State error detecting and correcting capability of block codes. **(02 Marks)**

b. Consider a linear block code (6, 3). The check bits of this code are derived using the following relations:
$c_4 = d_1 + d_2$
$c_5 = d_1 + d_2 + d_3$
$c_6 = d_2 + d_3$
i) find generator matrix G
ii) find all code words of linear block code
iii) compute error detecting and correcting ability
iv) also find H and H^T. **(07 Marks)**

c. For a linear block code, the syndrome is given by:
$S_1 = r_1 + r_2 + r_3 + r_5$ $S_2 = r_1 + r_2 + r_4 + r_6$ $S_3 = r_1 + r_3 + r_4 + r_7$
i) Find H matrix ii) Draw syndrome calculator circuit iii) Draw encoder circuit. **(07 Marks)**

OR

8 a. A (7, 3) Hamming code is generated using $g(x) = 1 + x + x^2 + x^4$. Design a suitable encoder to generate systematic cyclic codes. Verify the circuit operation for D = [110]. Also, generate the code using mathematical computation. **(08 Marks)**

b. Design a syndrome calculator circuit for (7, 4) cyclic code having the generator polynomial $g(x) = 1 + x + x^3$. Verify the circuit operation using R = [1101001]. Also, perform the relevant mathematical computations. **(08 Marks)**

Module-5

9 a. Write an explanatory note on BCH codes. **(05 Marks)**

b. Consider the (3, 1, 2) convolutional encoder with $g^{(1)} = (110)$ $g^{(2)} = (101)$, $g^{(3)} = (111)$
i) Find constraint length
ii) Find rate efficiency
iii) Draw encoder diagram
iv) Find the generator matrix
v) Find the code for the message sequence (11101) using matrix and frequency domain approach. **(11 Marks)**

OR

10 a. For (2, 1, 3) convolutional encoder with $g^{(1)} = (1101)$, $g^{(2)} = (1011)$.
i) Write state transition table
ii) State diagram
iii) Draw the code tree
iv) Draw the trellis diagram
v) Find the encoded output for the message (11101) by traversing the code tree. **(10 Marks)**

b. Explain Viterbi decoding. **(06 Marks)**

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15EC562

Fifth Semester B.E. Degree Examination, June/July 2019
Object Oriented Programming Using C++

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is C++? How is it different form C? **(06 Marks)**

b. List and explain the various data types in C++? **(06 Marks)**

c. Write a note on : i) Enumerated Data Type ii) Const and Volatile. **(04 Marks)**

OR

2 a. Discuss the types of operators supported in C++. **(06 Marks)**

b. Illustrate the difference between pointers and reference variables in C++. **(04 Marks)**

c. Explain loops in C++? Give example. **(06 Marks)**

Module-2

3 a. Design a function call cal_SI( ), that has three parameters, principle, tenure. rate. Provide default argument to rate. Write a C++ program to find the simple interest using the above function. **(06 Marks)**

b. What are static variables and functions in C++. **(04 Marks)**

c. What are local classes in C++? Illustrate with an example program. **(06 Marks)**

OR

4 a. Define friend function. Demonstrate with an example program. **(06 Marks)**

b. With an example, mention the various circumstances in which, the scope resolution operators are used. **(06 Marks)**

c. Write a C++ program to overload tow function to find area of a circle and square. **(04 Marks)**

Module-3

5 a. What is a constructor? Write the need of constructor in a class. **(04 Marks)**

b. Can a class have many constructors? Justify. **(04 Marks)**

c. Create a class called Clock with data members as hour, minute and member functions readtime ( ), showtime ( ). Write a C++ program to input two clock objects and add using operator overloading +. **(08 Marks)**

OR

6 a. What is a destructor? Mention the destructor rules. **(04 Marks)**

b. Demonstrate unary operator and binary operator overloading. **(08 Marks)**

c. What is nesting of member functions? **(04 Marks)**

Module-4

7 a. Discuss base class and derived class with suitable example. **(04 Marks)**

b. What is Hybrid Inheritance? Explain the diamond problem of inheritance in C++ with suitable example. **(08 Marks)**

c. List the rules for virtual function in C++. **(04 Marks)**

OR

8 a. Give the significance of 'this' pointer with a program. **(06 Marks)**

b. What is an abstract class? Write the advantages with an example program. **(06 Marks)**

c. Differentiate virtual and pure virtual functions. **(04 Marks)**

Module-5

9 a. Explain the stream class hierarchy with a neat diagram. **(08 Marks)**

b. Describe the following unformatted I/O functions.
i) get( ) ii) put( ) iii) getline( ) d) write( ). **(08 Marks)**

OR

10 a. Write the syntax and example to create user defined manipulators. **(05 Marks)**

b. Write a C++ program to copy the content of one file to another. **(07 Marks)**

c. Why it is necessary to detect the EOF? Give example. **(04 Marks)**

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15EC61

Sixth Semester B.E. Degree Examination, June/July 2019
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Determine the Hilbert transform of the signal g(t) = sin c(t). **(04 Marks)**

b. Determine the pre-envelope and complex envelope of the signal shown in Fig.Q1(b). **(06 Marks)**

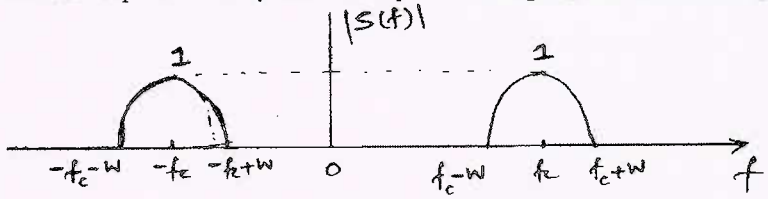

Fig.Q1(b)

c. Explain the time–domain procedure for the complex representation of band pass signals and systems. **(06 Marks)**

OR

2 a. For a binary sequence 0100000001011 construct i) RZBipolar format ii) Manchester format iii) B3Zs format iv) B6ZS format v) HDB3 format.
Also mention the application of B3ZS and B6Zs formats. **(07 Marks)**

b. Draw the power spectra of : i) RZAMI signal ii) NRZ polar signal. **(03 Marks)**

c. Consider a bandpass signal S(t) which is represented in terms of in-phase and quadrature components. Suggest a suitable scheme for :
i) extracting the in-phase and quadrature components from the band pass signal
ii) reconstructing the band pass signal from in-phase and quadrature components. **(06 Marks)**

Module-2

3 a. For the signals $s_1(t)$, $s_2(t)$, $s_3(t)$ and $s_4(t)$ shown in Fig.3(a), find a set of orthonormal basis functions using gram–Schmidt orthogonalization procedure. **(09 Marks)**

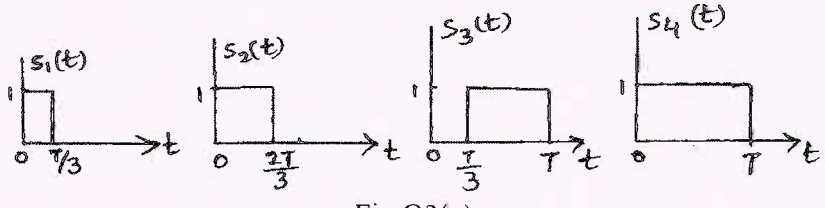

Fig.Q3(a)

b. Explain with neat diagram and necessary equations the matched filter receiver. **(07 Marks)**

OR

4 a. Obtain the decision rule for maximum likelihood decoding and explain the correlation receiver. **(08 Marks)**

b. Show that for a noisy input, the mean value of the j^{th} correlator output X_j depends only on S_{ij} and all the correlators outputs X_j, j = 1, 2, - - - - , N, have a variance equal to the PSD No/2 of the additive noise process w(t). **(08 Marks)**

Module-3

5 a. Sketch the QPSK wave form for the sequence 01101000. **(06 Marks)**

b. Obtain the expression for average probability of symbol error for BPSK using coherent detection. **(06 Marks)**

c. Obtain the constcleation of QAM for M = 16 and draw the signal space diagram. **(04 Marks)**

OR

6 a. Explain the generation and coherent detection of BFSK system. **(06 Marks)**

b. The binary sequence 1100100010 is applied to the DPSK transmitter

i) Sketch the resulting wave from at the transmitter output.

ii) Applying this waveform to the DPSK receiver, show that in the absence of noise, the original binary sequence is reconstructed at the receiver output. **(06 Marks)**

c. An FSK system transmits binary data at the rate of 2×10^6 bps. During the source of transmission, AWGN of zero mean and two sided PSD 10^{-20} Watts/Hz is added to the signal. The amplitude of the received sinusoidal wave for digit 1 or 0 is 1μv. Determine the average probability of symbol error assuming non-coherent detection. **(04 Marks)**

Module-4

7 a. Explain the following terms with related equations and diagram with respect to base band transmission.

i) ISI and Nyquist condition for zero ISI

ii) Duobinary signal pulse

iii) Modified duobinary signal pulse

iv) Partial response signals

v) Raised cosine spectrum. **(10 Marks)**

b. Explain the need for precoder in a duobinary signaling. The binary sequence 1110100100001101 is the input to the precoder whose output is used to modulate a duobinary transmitting filter. Obtain the precoded sequence, transmitted amplitude levels, the received signal levels and the decoded sequence. **(06 Marks)**

OR

8 a. With a neat diagram, explain the concept of linear traversal filter. **(06 Marks)**

b. Consider a channel distorted pulse x(t), at the input to the equalizer, given by $x(t) = \frac{1}{1+\left(\frac{2t}{T}\right)^2}$ where $1/T$ is the symbol rate. The pulse is sampled at the rate 2/T and equalized by a zero-forcing equalizer. Determine the coefficients of a five-tap zero-forcing equalizer. **(06 Marks)**

c. Write a note on eye diagram. **(04 Marks)**

Module-5

9 a. With a neat diagram explain the generation of PN sequences and state its properties. **(06 Marks)**

b. A DS spread–spectrum signal is designed so that the power ratio P_R/P_N at the intended receiver is 10^{-2}. If the desired $E_b/N_0 = 10$ for acceptable performance, determine the minimum value of the processing gain. **(04 Marks)**

c. Explain with neat block diagram FH spread –spectrum system. **(06 Marks**

OR

10 a. Explain the generation and demodulation of DS spread spectrum signal. **(06 Marks)**

b. Write a note on application of spread spectrum in wireless LANs. **(04 Marks)**

c. With a neat block diagram, explain the IS–95 reverse link. **(06 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, June/July 2019
ARM Micro Controller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the architecture of ARM cortex – M3 processor with neat diagram. **(08 Marks)**
b. With neat diagram, explain operation mode and privilege levels in cortex M3. **(08 Marks)**

OR

2 a. What is stack? Explain push and pop operation. With the help of a neat diagram. **(07 Marks)**
b. Explain in detail special registers used in ARM cortex M3 processor. **(09 Marks)**

Module-2

3 a. Write an ALP to calculate the sum of 1 to 10 numbers. **(08 Marks)**
b. Explain the following instruction set : i) BFC ii) SBFX iii)ASR iv) MRS. **(04 Marks)**
c. Explain how CMSIS provides standard access. Interface for Embedded software. **(04 Marks)**

OR

4 a. Write a program to blink a LED using 'C' language. **(08 Marks)**
b. Explain the following assembler directives AREA, ENTRY, DCB, ALIGN. **(04 Marks)**
c. Explain different bus interfaces supported by cortex M3. **(04 Marks)**

Module-3

5 a. Explain how embedded system are classified. **(08 marks)**
b. With neat block diagram, explain the element of embedded system. **(08 Marks)**

OR

6 a. Differentiate between RISC and CISC. **(04 Marks)**
b. Explain how program memory are classified. **(08 Marks)**
c. Explain how brown-out protection circuits works. **(04 Marks)**

Module-4

7 a. What are the operational and nonoperational attributes of an embedded systems. **(10 Marks)**
b. Explain different types of serial interface bus used in automotive communication. **(06 Marks)**

OR

8 a. Explain fundamental issues in hardware software co-design. **(06 Marks)**
b. Explain with a neat block diagram how source file to object file translation take place. **(06 marks)**
c. Explain super loop based approach of embedded firmware design. **(04 Marks)**

Module-5

9 a. With neat diagram explain operating system architecture. **(08 marks)**

b. Explain how operating systems are classified. **(04 marks)**

c. Differentiate between hard real time system and soft real time system with an example for each. **(04 Marks)**

OR

10 a. With neat diagram, explain embedded system development environment. **(08 marks)**

b. For the following jobs calculate the turnaround time, waiting time using preemptive SJF scheduling algorithm. **(04 Marks)**

Jobs	CPU bust time	Arrival time
1	10	0.0
2	2	3.0
3	1	4.0
4	4	5.0

c. Write a note on IAP [In Application Programming] and in system programming. **(04 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, June/July 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions. **(08 Marks)**

b. Explain the working of nMOS enhancement mode transistor with suitable diagrams. **(08 Marks)**

OR

2 a. Derive expression for drain current in linear and saturation region for nMOS transistor. **(08 Marks)**

b. With neat sketches explain the CMOs P-well process steps to fabricate a CMOS inverter. **(08 Marks)**

Module-2

3 a. Write the lambda based design rules for separation of layers and transistors. **(06 Marks)**

b. Draw circuit, stick and layout diagram for nMOS shift register cell. **(10 Marks)**

OR

4 a. Define sheet resistance (R_S) standard unit of capacitance ($\square Cg$) and delay unit (τ) **(06 Marks)**

b. Calculate the capacitance of the structure given below in Fig.Q4(b). **(10 Marks)**

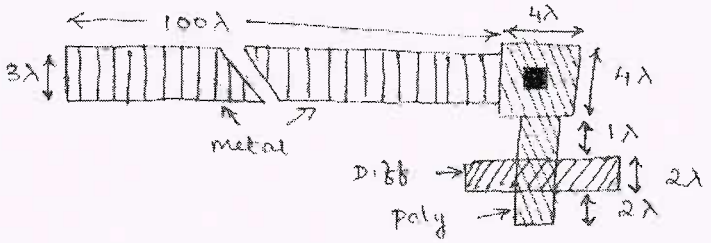

Fig.Q4(b)

Area capacitance value for metal 1 to substrate = 0.3pF × $10^{-4}/\mu m^2$(0.075 relative value)
Area capacitance value for diffusion to substrate = 1pf × $10^{-4}/\mu m^2$(0.25 relative value)
Area capacitance value for polysilicon to substrate = 0.4 pF × $10^{-4}/\mu m^2$(0.1 relative value).

Module-3

5 a. Obtain the scaling factor for the following device parameters :
   i) gate capacitance
   ii) gate area
   iii) saturation current (Idss)
   iv) channel resistance (R_{on})
   v) maximum operating frequency (f_0)
   vi) power dissipation per gate (Pg)
   vii) current density (J)
   viii) gate delay (T_d). **(08 Marks)**

b. With a neat diagram explain 4 × 4 Barrel shifter. **(08 Marks)**

OR

6 a. Explain the general arrangement of a 4 bit data path for processor. **(08 marks)**

b. Describe Manchester carry chain element. **(08 Marks)**

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI sub system. **(05 Marks)**

b. Explain in detail the general structure of an FPGA fabric. **(06 Marks)**

c. Explain switch logic implementation of CMOS 5 way selector with neat circuit diagram. **(05 Marks)**

OR

8 a. Explain the structured design approach for the implementation of a parity generator. **(08 marks)**

b. Explain dynamic CMOS logic with example. **(08 Marks)**

Module-5

9 a. Explain 3 transistor dynamic RAM cell with schematic diagram. **(06 Marks)**

b. Explain any two fault models in combinational circuits. **(06 Marks)**

c. Write a note on automatic test pattern generation. **(04 Marks)**

OR

10 a. write short notes on :
   i) observability and controllability
   ii) Built In Self Test (BIST). **(08 Marks)**

b. Explain nMOS pseudo static RAM cell with schematic diagram. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, June/July 2019
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Compare and contrast byte – stuffing and bit stuffing. **(06 Marks)**

b. With a neat diagram, explain encapsulation and decapsulatioin protocol layering. **(04 Marks)**

c. With a layer diagram, explain the responsibilities of each layer in TCP/IP protocol suite. **(06 Marks)**

OR

2 a. Discuss the ARP operation and show how ARP sends request and reply message with an example. **(08 Marks)**

b. Explain stop and wait protocol and show how adding sequence numbers can prevent duplicates with the help of flow diagram. **(08 Marks)**

Module-2

3 a. Explain the behaviour of CSMA protocol with a neat diagram and show the vulnerable time in CSMA. **(08 Marks)**

b. A pure ALOHA network transmits 200-bit frames on a shared channel of 200kbps. What is through put if the system (all stations together) produces?

i) 1000 frames per second?

ii) 500 frame per second? **(04 Marks)**

c. Explain reservation as a controlled access method. **(04 Marks)**

OR

4 a. Explain the format of standard Ethernet frame. What are the minimum and maximum frame lengths? **(07 Marks)**

b. Identify if the following Ethernet MAC addresses are unicast, multicast or broadcast

i) 47 : 20 : 1B : 2E : 08 : EE

ii) EE : FF : 10 : 01 : 11 : 00

iii) FF : FF : FF : FF : FF : FF **(03 Marks)**

c. What are the two effects of the bridges on an Ethernet LAN? Explain with a neat diagram. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain two types of networks defined in Bluetooth. **(04 Marks)**

b. What is hidden station problem in wireless LAN's? Give solution for it. **(06 Marks)**

c. Describe VLAN. How is it used in grouping of stations? **(06 Marks)**

OR

6 a. Explain the occupation of the address space in classful addressing. **(04 Marks)**

b. A block of addresses is granted to a small organization. We know that one of the addresses is 167·199·170·82/27. What is the first address, last address and total number of address of the block? **(06 Marks)**

c. With a neat diagram, explain how can a NAT help in address translation. **(06 Marks)**

Module-4

7 a. With a neat diagram explain IPV4 datagram format? **(08 Marks)**

b. What is the two addresses approach in mobile host? Explain the significance of home agent and foreign agent with a diagram. **(08 Marks)**

OR

8 a. With relevant diagrams describe Distance Vector Routing. What is two node instability in DVR? **(10 Marks)**

b. Explain operation of Border Gateway Protocol (BGP) with a diagram. **(06 Marks)**

Module-5

9 a. Explain connection less and connection oriented service showing the movement of packets using time line. **(08 Marks)**

b. Explain why the size of the send window in Go back N must be less than 2^m? **(08 Marks)**

OR

10 a. Explain TCP connection establishment and connection termination using three way hand shaking. **(10 Marks)**

b. Describe slow start algorithm for handling congestion in TCP. **(06 Marks)**

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15EC654

Sixth Semester B.E. Degree Examination, June/July 2019
Digital Switching Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With a neat diagram explain the working principle of four wire circuit. Also give the equations for echoes. **(10 Marks)**

b. Explain the hierarchy of national public switched telecommunication network with neat diagram. **(06 Marks)**

OR

2 a. Explain in brief, the regulation and standards in telecommunication network. **(08 Marks)**

b. Express the following power levels in dBm and dBw. i) 1mW ii)1W iii)2mW iv) 100mW. **(08 Marks)**

Module-2

3 a. Explain the functions of switching system. **(08 Marks)**

b. Explain the working of distribution frame in strowger exchange. **(08 Marks)**

OR

4 a. Explain in brief : i) message switching ii) circuit switching. **(08 Marks)**

b. Explain electronic switching along with different facilities provided. **(08 Marks)**

Module-3

5 a. Derive the Erlang's lost call formula with iterative application of recurrence relation. **(09 Marks)**

b. A group of 20 trunks provides a grade of service of 0.01 when offered 12E of traffic. How much is the grade of service improved if 2 extra trunks are added to the group? How much does the grade of service deteriorates if one trunk is out of service? **(07 Marks)**

OR

6 a. Design a grading for connecting 20 trunks to switches having ten outlets. **(08 Marks)**

b. Derive the expression for minimum number of cross points in a three stage network with M incoming trunks and N outgoing trunks for (M > N) case. **(08 Marks)**

Module-4

7 a. Explain Time-Space-Time switch with suitable diagram. **(08 Marks)**

b. Explain synchronization and frame alignment of PCM signals in digital exchange. **(08 Marks)**

OR

8 a. Briefly explain basic software architecture of a DSS. **(08 Marks)**

b. With the help of features flow diagram, explain call forwarding feature. **(08 Marks)**

Module-5

9 a. Describe the various organizational interfaces of DSS central office. **(10 Marks)**

b. Briefly explain strategy for improving software quality with diagram. **(06 Marks)**

OR

10 a. Explain generic switch hardware architecture with neat diagram. **(08 Marks)**

b. Write short note on : i) Reliability analysis ii) Recovery strategy. **(08 Marks)**

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15EC655

Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression of drain current of a MOS device for triode and saturation region. **(08 Marks)**

b. Consider a CMOS process for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450 cm^2/v.s$ and $v_t = 0.7V$

i) Find C_{ox} and k_n^1

ii) For an NMOS transistor $\frac{W}{L} = \frac{8\mu m}{0.8\mu m}$. Calculate the values of V_{GS} and V_{DSmin} needed to operate a transistor in saturation region with a DC current $I_D = 100\mu A$.

iii) For the derive in (ii), find the value of V_{GS} required to cause the device to operate as 1000Ω resistor for a very small V_{DS}. **(08 Marks)**

OR

2 a. With the neat diagram obtain the expression for finite O/P resistance in saturation region. **(07 Marks)**

b. Define the following parameter with respect to MOSFET:
i) Threshold voltage ii) Body Effect. **(05 Marks)**

c. For the circuit shown in Fig.Q.2(c), find the values of R and V_D to obtain a current I_D of $80\mu A$. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $L = 0.8\mu m$ and $W = 4\mu m$. Assume $\lambda = 0$. **(04 Marks)**

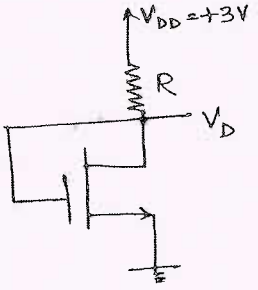

Fig.Q.2(c)

Module-2

3 a. Draw the circuit diagram of source follower amplifier. Draw its small signal equivalent circuit with r_o. Obtain the expression for R_{in}, R_{out}, A_v, A_{v_o} and Gv. **(10 Marks)**

b. List the various techniques used for biasing in MOS amplifier circuits and explain any two in detail. **(06 Marks)**

OR

4 a. Draw the development of T-Equivalent circuit model for the MOSFET. **(05 Marks)**

b. Explain the high frequency model of MOSFET with a neat diagram and internal capacitances. **(06 Marks)**

c. Derive the expression for transconductance g_m and voltage gain A_v for a common source amplifier with small input signal. **(05 Marks)**

Module-3

5 a. Determine the G_v, A_v, R_{out}, R_{in}, A_{v_o} for a common source MOS amplifier. **(08 Marks)**

b. Derive the expression for determining 3-dB frequency (W_H) of an amplifier. **(08 Marks)**

OR

6 a. Explain the operation of a MOSFET current steering circuits with necessary expressions. **(08 Marks)**

b. Fig.Q.6(b) shows an ideal voltage amplifier having a gain of -100V/V with an impedance Z is

i) A 1MΩ resistance

ii) A 1pF capacitance. In each case, use the equivalent circuit to determine V_o/V_{sig}. **(08 Marks)**

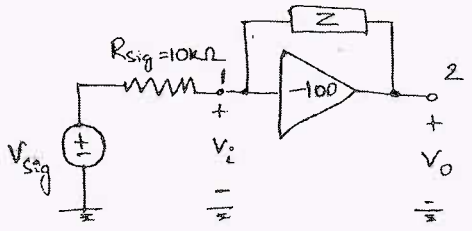

Fig.Q.6(b)

Module-4

7 a. Consider a CMOS CS amplifier in Fig.Q.7(a) for the case V_{DD} = 3V, $V_{tn} = |V_{tp}| = 0.6V$, $\mu_n C_{ox}$ = 200μA/V², $\mu_p C_{ox}$ = 65 μA/V² for all transistors L = 0.4μm, W = 4μm. Also $V_{An} = 20V$, $|V_{AP}| = 10V$, I_{REF} = 100μA. Find g_{m1}, r_{o1}, r_{o2} and small signal voltage gain. **(06 Marks)**

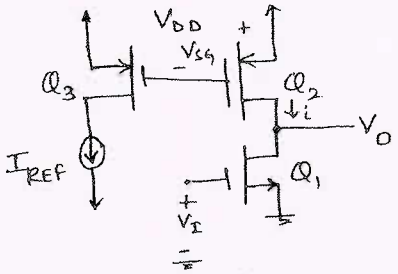

Fig.Q.7(a)

b. For a common gate amplifier with active load determine the expression for R_i, A_{vo}, A_v, G_{vo}, G_v, R_o. **(10 Marks)**

OR

8 a. Explain the following: i) Double cascode ii) Folded cascode. **(08 Marks)**

b. Explain the high frequency response of MOS cascode amplifier with necessary diagram and expressions. **(08 Marks)**

Module-5

9 a. Explain the operation of MOS differential pair with a differential input voltage. **(08 Marks)**

b. Prove that $A_{CM} = \frac{-r_{o4}}{2R_{ss}} \times \frac{1}{1+g_{m3}r_{o3}}$ for the active loaded MOS differential amplifier. **(08 Marks)**

OR

10 a. For the nMOS differential pair with a common mode voltage V_{CM} applied as shown in Fig.Q.10(a). Let $V_{DD} = V_{SS} = 2.5V$ $K_n^1 \frac{W}{L} = 3mA/v^2$, $V_{tn} = 0.7V$, $I = 0.2mA$, $R_D = 5K\Omega$. Neglect channel length modulation

i) Find V_{OV} and V_{GS} for each transistor

ii) For $V_{CM} = 0$, Find Vs, i_{D1}, i_{D2}, V_{D1} and V_{D2}

iii) What is highest value of V_{cm} for which Q_1 and Q_2 remain in saturation, if current source I requires a minimum voltage of 0.3V to operate properly. What is the lowest value for V_s and hence for V_{cm}?

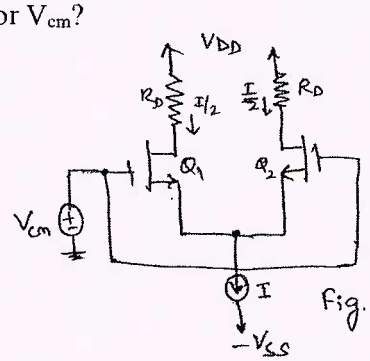

Fig.Q.10(a)

(08 Marks)

b. With neat circuit diagram, explain the operation of two stage CMOS Op-amp configuration. **(08 Marks)**

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15EC52

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Signal Processing

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the DFT expression from the DTFT. **(04 Marks)**

b. Compute the 'N' point DFT of the sequence
$x(n) = a.n\ 0 \le n \le N-1$. **(06 Marks)**

c. Find the circular convolution between the sequences using DFT and IDFT method
$x_1(n) = (1, 2, 3, 1)$ and $x_2(n) = (4, 3, 2, 1)$ **(06 Marks)**

OR

2 a. State and prove that circular (i) Folding ii) Frequency shift properties of an 'N' point sequence. **(06 Marks)**

b. Consider the finite length sequence $x(n) = \delta(n) + 2\delta(n-j)$ Find :
(i) 10 point DFT of x(n)
(ii) $y(k) = e^{-j\left(\frac{4\pi k}{10}\right)}X(k)$ where X(k) is 10 point DFT of x(n) find y(n)
(iii) Find z(n) that has DFT z(k) = X(k).w(k) where w(k) is the 10 point DFT of $w(n) = u(n) - u(n-7)$ **(07 Marks)**

c. Let x(n) be a finite length sequence with $x(k) = \{1, 4j, 0, -4j\}$, find the DFT's of
(i) $x_1(n) = e^{j\frac{\pi}{2}n}x(n)$ (ii) $x_2(n) = \cos\left(\frac{\pi}{2}n\right)x(n)$ (iii) $x_3(n) = x((n-1)_4)$ **(03 Marks)**

Module-2

3 a. Explain the disadvantages of direct computation of DFT and advantage of FFT. **(04 Marks)**

b. Find the output y(n) of a filter whose impulse response $h(n) = \{3, 2, 1\}$ and input $x(n) = \{2, 1, -1, -2, -3, 5, 6, -1, 2, 0, 2, 1\}$. Using overlap and save method. Use 8 point circular convolution in your approach. **(10 Marks)**

c. State and prove symmetric property of twiddle factor w_N. **(02 Marks)**

OR

4 a. Find the number of complex multiplications and additions required to computer 128 point DFT using (i) Direct method (ii) FFT (iii) what is the speed improvement factor (iv) Number of real registers needed (v) Number of trigonometric functions needed. **(06 Marks)**

b. A long sequence x(n) is filtered with a filter with impulse response h(n) to produce output y(n). If $x(n) = \{1, 4, 3, 0, 7, 4, -7, -7, -1, 3, 4, 3\}$ and $h(n) = \{1, 2\}$. Compute y(n) using overlap and add method. Use only 5 point circular convolution in your approach. **(10 Marks)**

Module-3

5 a. Develop 8 point DIT-FFT radix – 2 algorithm and draw the signal flow graph. **(08 Marks)**

b. Find the 8 point DFT of the sequence $x(n) = \{1, 1, 1, 1, 0, 0, 0, 0\}$ using radix – 2 DIF FFT algorithm. **(08 Marks)**

OR

6 a. Find the 4 point circular convolution of x(n) and h(n) given below using radix – 2 DIT FFT algorithm. x(n) = {1, 1, 1, 1} h(n) = {1, 0, 1, 0}. **(06 Marks)**

b. First five points of 8-point DFT's of a real valued sequence is given by x(0) = 0 x(1) = 2 + 2j, x(2) = -4j, x(3) = 2 – 2j, x(4) = 0. Determine the remaining points. Hence find the sequence x(n) using radix – 2 DIT FFT algorithm. **(10 Marks)**

Module-4

7 a. Compare Butterworth and Chebyshev filters. **(04 Marks)**

b. Design an analog lowpass Butterworth filter for the following specifications
$0.8 \le |H_a(s)| \le 1, 0 \le \Omega \le 0.2\pi, \ |H_a(s)| \le 0.2, 0.6\pi \le \Omega \le \pi$. **(08 Marks)**

c. Explain Analog to Analog transformation. **(04 Marks)**

OR

8 a. Design a digital lowpass filter using BLT to satisfy the following chart.
i) Monotonic pass and stop band
ii) -3dB cut –off of 0.5π rad
iii) Magnitude down atleast 15dB at 0.75π rad **(08 Marks)**

b. Find H(z) for the given T.F $H(s) = \frac{s+a}{(s+a)^2 + b^2}$ using Impulse Invariant Transformation (IIT) technique. **(08 Marks)**

Module-5

9 a. Obtain direct form – I, Form – II, Cascade and parallel form of realization for the following system. y(n) = 0.75 y(n – 1) – 0.125 y(n – 2) + 6x(n) + 7x (n – 1) + x(n – 2). **(12 Marks)**

b. Realize an FIR filter given by $h(n) = \left(\frac{1}{2}\right)^n [u(n) - u(n-4)]$ using direct form – I. **(04 Marks)**

OR

10 a. Write equations of any four different windows used in design of FIR filters. **(10 Marks)**

b. Design the symmetric FIR, lowpass filter whose desired frequency response is given as

$$H_d(w) = \begin{cases} e^{-jw\tau} \text{ for } |w| \le w_c \\ 0 \text{ otherwise} \end{cases}$$

The length of the filter should be 7 and w_c = 1 radian/sample use rectangular window. **(06 Marks)**

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15EC54

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Information Theory and Coding

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

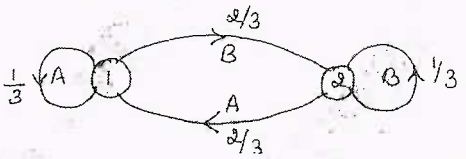
Module-1

1 a. The output of an information source contains 160 symbols, 128 of which occur with a probability of $\frac{1}{256}$ and remaining with a probability of $\frac{1}{64}$ each. Find the average information rate of the source if the source emits 10,000 sym/s. **(02 Marks)**

b. In a facsimile transmission of a picture, there are 4×10^6 pixels/frame. For a good reconstruction of the image atleast eight brightness levels are necessary. Assuming all these levels are equally likely to occur. Find the average information rate if one picture is transmitted every 4s. **(04 Marks)**

c. Consider the following Markov source shown in fig. Q1(c). Find i) State probabilities ii) State entropies iii) Source entropy iv) G_1, G_2 v) Show that $G_1 > G_2 > H$. **(10 Marks)**

Fig.Q1(c)



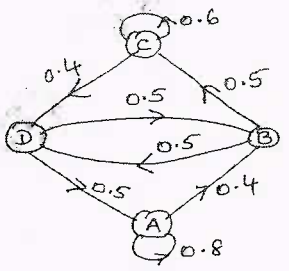
OR

2 a. The international Morse code uses a sequence of symbols of dots and dashes to transmit letters of English alphabet. The dash is represented by a current pulse of duration 2ms and dot of 1ms. The probability of dash is half as that of dot. Consider 1ms duration of gap is given in between the symbols. Calculate i) Self – information of a dot and a dash ii) Average information content of a dot – dash code iii) Average rate of information. **(06 Marks)**

b. State the properties of Entropy. **(04 Marks)**

c. Consider the Markov source shown in fig. Q2(c). find i) State probabilities ii) State entropies iii) Source entropy. **(06 Marks)**

Fig.Q2(c)



Module-2

3 a. With an example, explain Prefix codes. **(04 Marks)**

b. Consider the following source S = {A, B, C, D, E} with probabilities P = {0.5, 0.25, 0.125, 0.0625, 0.0625}. Find the code words for the symbols using Shannon's encoding algorithm. Also, find the source efficiency and redundancy. **(06 Marks)**

c. An information source produces a sequence of independent symbols having the following probabilities. Construct binary code using Huffman encoding and find its efficiency. **(06 Marks)**

A	B	C	D	E	F	G
1/3	1/27	1/3	1/9	1/9	1/27	1/27

OR

4 a. State Kraft McMillan Inequality property. **(04 Marks)**

b. Consider a discrete memory less source with S = (X, Y, Z) with the corresponding probabilities P = (0.5, 0.3, 0.2). Find the code words for the symbols using Shannon's algorithm. Also, find the source efficiency and redundancy. **(06 Marks)**

c. Consider a discrete memory less source with S = (X, Y, Z) with respective probabilities P = (0.6, 0.2, 0.2). Find the codeword for the message 'YXZXY' using arithmetic coding. **(06 Marks)**

Module-3

5 a. A binary channel has the following characteristics

$$P(Y/X) = \begin{bmatrix} 2/3 & 1/3 \\ 1/3 & 2/3 \end{bmatrix}$$

. If input symbols are transmitted with probabilities ¾ and ¼ respectively. Find entropies, H(X) , H(X, Y) and H(Y/X). **(03 Marks)**

b. Prove that the mutual information is always a non - negative entity $I(X ; Y) \geq 0$. **(06 Marks)**

c. The noise characteristics of a channel are as shown in fig.Q5(c). Find the capacity of the channel using Muroga's method. **(07 Marks)**

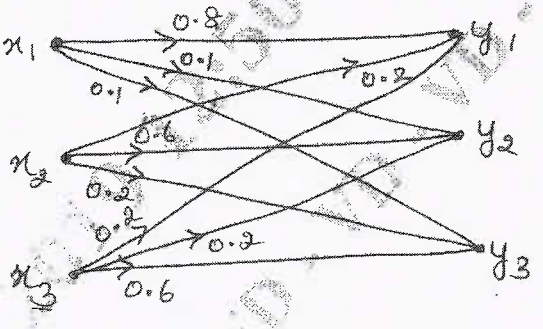


Fig.Q5(c)

OR

6 a. State the properties of Joint Probability Matrix. **(04 Marks)**

b. Find the mutual information for the channel shown in fig.6(b). Let $P(x_1) = 0.6$ and $P(x_2) = 0.4$. **(06 Marks)**

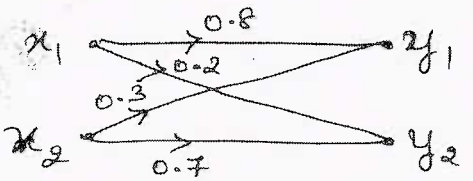


Fig.Q6(b)

c. Derive the expression for the channel capacity of a Binary Symmetric Channel. **(06 Marks)**

Module-4

7 a. For a (6, 3) code find all the code vectors if the co-efficient matrix P is given by

$$P = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

i) Find code vector ii) Implement the encoder iii) Find the syndrome vector (S).
iv) Implement the syndrome circuit. **(08 Marks)**

b. Obtain the generator and parity check matrices for an (n, k) cyclic code with $g(x) = 1+x+x^3$. **(08 Marks)**

OR

8 a. In an LBC, the syndrome is given by

$S_1 = r_1 + r_2 + r_3 + r_5$; $S_2 = r_1 + r_2 + r_4 + r_6$; $S_3 = r_1 + r_3 + r_4 + r_7$.

i) Find the parity check matrix (H) ii) Draw the encoder circuit
iii) Find the code word for all input sequences.
iv) What is the syndrome for the received data 1011011? **(08 Marks)**

b. In a (15,5) cyclic code, the generator polynomial is given by $g(x) = 1+x+ x^2+x^4+x^5+ x^8+ x^{10}$. Draw the block diagram of an encoder and syndrome calculator for this code. Find whether $r(x) = 1+ x^4+ x^6 + x^8 + x^{14}$ a valid code word. **(08 Marks)**

Module-5

9 a. Design a (15,7) binary BCH code with r = 2. **(06 Marks)**

b. Consider the (3, 1, 2) convolution code with $g^{(1)} = (1\ 1\ 0)$, $g^{(2)} = (1\ 0\ 1)$, $g^{(3)} = (1\ 1\ 1)$.
i) Find the constraint length ii) Find the rate iii) Draw the encoder block diagram
iv) Find the generator matrix v) Find the code word for the message sequence (1 1 1 0 1) using time – domain and transfer – domain approach. **(10 Marks)**

OR

10 a. Explain why (23, 12) Golay code is called as perfect code. **(04 Marks)**

b. Consider the convolution encoder shown in fig. Q10(b).
i) Write the impulse response of the encoder.
ii) Find the output for the message (1 0 0 1 1) using time – domain approach.
iii) Find the output for the message (1 0 0 1 1) using transfer – domain approach. **(12 Marks)**

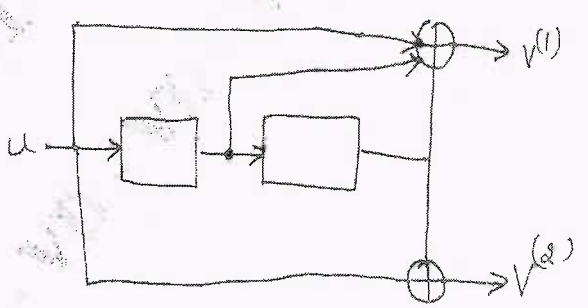


Fig.Q10(b)

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15EC553

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Operating Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Define operating system. Explain the key concerns of an operating system. **(10 Marks)**

b. Explain the different computational structures of operating system. **(06 Marks)**

OR

2 a. Explain different classes of operating system. **(10 Marks)**

b. Explain various resource allocation strategies. **(06 Marks)**

Module-2

3 a. Define process, process states and transition with suitable algorithm. **(08 Marks)**

b. Explain Process Control Block. **(08 Marks)**

OR

4 a. For a given set of process FCFS and SRN scheduling compare their performance in terms of mean turnaround time and weighted turnaround time. **(10 Marks)**

Process	P_1	P_2	P_3	P_4	P_5
Admission time	0	2	3	5	9
Service time	3	3	2	5	3

b. Explain long-term and short term scheduling. **(06 Marks)**

Module-3

5 a. Compare contiguous and non-contiguous memory allocation techniques. **(08 Marks)**

b. Write a short note on : i) paging ii) segmentation. **(08 Marks)**

OR

6 a. Explain demand paging preliminaries. **(10 Marks)**

b. Write short note on :

i) First–In–First–Out (FIFO) page replacement policy. **(03 Marks)**

ii) Least Recently Used (LRU) page replacement policy. **(03 Marks)**

Module-4

7 a. Explain file system and IOCS. **(08 Marks)**

b. Explain fundamental file organizations. **(08 Marks)**

OR

8 a. Explain directory structures. **(08 Marks)**

b. Explain file system action at a file operation. **(08 Marks)**

Module-5

9 a. Define message passing. Explain how to implement the message passing. **(08 Marks)**

b. Explain mail boxes and message passing in unix. **(08 Marks)**

OR

10 a. Define deadlock. Explain deadlock in resource allocation. **(08 Marks)**

b. Explain deadlock detection algorithm. **(08 Marks)**

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15EC561

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Automotive Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain with necessary diagrams, working of a four stroke IC engine. **(08 Marks)**

b. Explain the operating principle of starter battery. **(08 Marks)**

OR

2 a. Define air fuel ratio. Explain the performance of an engine with respect to air-fuel ratio. **(08 Marks)**

b. What are the major controller inputs and outputs from/to engine? Show how they are connected between engine and controller. **(08 Marks)**

Module-2

3 a. With necessary diagrams, explain the working principle of MAP sensor. **(08 Marks)**

b. With neat diagram, explain optical crankshaft position sensor. **(08 Marks)**

OR

4 a. Explain magnetic reluctance position sensor with relevant diagrams. **(08 Marks)**

b. Explain hall effect sensor. **(08 Marks)**

Module-3

5 What are the seven modes of fuel control? Explain them in detail. **(16 Marks)**

OR

6 a. Explain with a neat diagram how the secondary air is controlled/ **(08 Marks)**

b. Explain in detail system diagnostics. **(08 Marks)**

Module-4

7 a. What are the CAN protocol layers? Explain. **(06 Marks)**

b. Explain LIN Bus and MOST Bus. **(10 Marks)**

OR

8 a. Explain with neat diagram : ABS (Anti Braking System) **(08 Marks)**

b. Explain digital speed sensor. **(08 Marks)**

Module-5

9 a. Explain in detail ON-board diagnostics performed in car. **(08 Marks)**

b. Explain low tire-pressure warning system with relevant diagrams. **(08 Marks)**

OR

10 a. Explain with necessary diagrams generic automatic navigation system. **(08 Marks)**

b. Write a note on advanced cruise control. **(04 Marks)**

c. Write explanatory notes on electric and hybrid vehicles. **(04 Marks)**

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15EC562

Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Object Oriented Programming using C++

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What is C++? List the applications of C++. **(04 Marks)**

b. Describe the structure of a C++ program with an example. **(08 Marks)**

c. When do we use cascading of input/output operators? Give example. **(04 Marks)**

OR

2 a. Write a C++ program to find the sum of digits of a given number.
e.g If input number = 16738
output is 25 i.e. 1 + 6 + 7 + 3 + 8. **(04 Marks)**

b. Explain the different types of expressions in C++. Give examples for each type. (any four) **(08 Marks)**

c. With an example, describe the purpose of new and delete operators in C++. **(04 Marks)**

Module-2

3 a. Mention the restrictions posed by the complier on inline functions. **(04 Marks)**

b. Design a class 'triangle' containing data items 'base' 'height' and four member functions setdata( ), getdata( ), displaydata( ) and findarea( ), to set values to 'base' and 'height', to get the user input, to display and find area of triangle (i.e. $\frac{1}{2}$ * base*height) respectively. Write the main function which creates the object and uses the members of the class. **(08 Marks)**

c. Discuss the different types of function overloading in C++. **(04 Marks)**

OR

4 a. When do we use default arguments? State the rules that need to be followed while using default arguments. **(04 Marks)**

b. Draw a neat diagram and explain the process of memory allocation to objects in C++. **(06 Marks)**

c. Develop a C++ program to define two classes namely husband and wife that hold a private member 'salary' respectively. Calculate and display the total income of the family using friend function. **(06 Marks)**

Module-3

5 a. How are constructors differ from member functions of a class? **(04 Marks)**

b. What is operator overloading? Give syntax and example. List the operators that cannot be overloaded. **(06 Marks)**

c. Explain the significance of friend functions to overload operators. **(06 Marks)**

OR

6 a. Discuss the importance of dynamic constructors and destructor in a C++ class. **(08 Marks)**

b. Write a C++ program to add two complex numbers by overloading the + operator. Also overload << and >> operators for reading and displaying the complex numbers. **(08 Marks)**

Module-4

7	a.	What is inheritance? List its advantages.	(04 Marks)
	b.	Explain the visibility inheritance modes. Give an example.	(08 Marks)
	c.	Compare multiple inheritances with multilevel inheritance.	(04 Marks)

OR

8	a.	What is abstract class? Give an example.	(04 Marks)
	b.	Demonstrate the working of pointers as objects with a relevant example.	(08 Marks)
	c.	State the differences between virtual and pure virtual functions.	(04 Marks)

Module-5

9	a.	What is a data stream? Describe the hierarchy of file stream classes in C++.	(08 Marks)
	b.	Explain the following unformatted I/O functions : i) getline( ) ii) write( ).	(04 Marks)
	c.	Compare and contrast width( ) and setw( ).	(04 Marks)

OR

10	a.	How file opening and closing is done? What are the functions required for reading and writing data in a file. Explain with an example.	(08 Marks)
	b.	Create a C++ program to read a text file and find number of characters, words and lines in a file.	(08 Marks)

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15EC61

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert transform. What are its applications. Prove that a signal g(t) and its Hilbert transform $\tilde{g}(t)$ are orthogonal over the entire time interval $(-\infty, \infty)$. **(05 Marks)**

b. Determine the pre-envelope and complex envelope of the RF pulse defined by $x(t) = A\,\text{rect}\left(\frac{t}{T}\right)\cos(2\pi f_c t)$. **(06 Marks)**

c. Compare the power spectra of various line codes in terms of bandwidth, DC component, Noise immunity and synchronization capability, with neat sketch. **(05 Marks)**

OR

2 a. Express bandpass signal s(t) in canonical form. Also explain the scheme for deriving the inphase and quadrature components of the bandpass signal s(t). **(06 Marks)**

b. Explain with relevant expressions, the procedure for computational analysis of a bandpass system driven by a bandpass signal. **(06 Marks)**

c. What is the advantage of HDB3 code over conventional alternate mark inversion(AMI) code. Code the pattern "1010000011000011000000" using HDB3 encoding and AMI encoding. **(04 Marks)**

Module-2

3 a. Explain the geometric representation of set of M energy signals as linear combination of N orthonormal basis functions. illustrate for the case N = 2 and M = 3, with necessary diagrams and expressions. **(08 Marks)**

b. Using the Gram–Schmidt orthogonalization procedure, find a set of orthonormal basic functions to represent the three signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ shown in Fig.Q3(b). also express each of these signals in terms of the set of basis functions. **(08 Marks)**

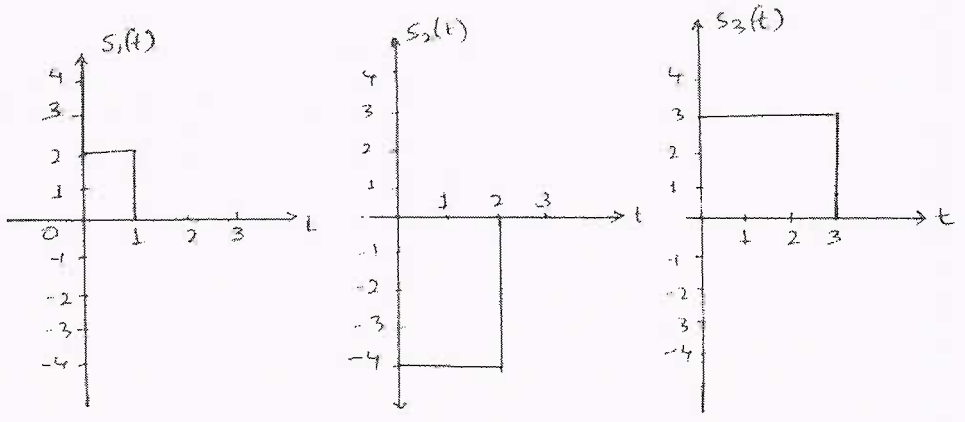

Fig.Q3(b)

OR

4 a. Explain the correlation receiver with neat diagrams and explanation of detector and the maximum –linklihood decoder blocks. **(08 Marks)**

b. Explain the matched filter receiver. Obtain the expression for the impulse response of the matched filter. **(08 Marks)**

Module-3

5 a. Derive the expression for error probability of binary PSK using coherent detection. **(06 Marks)**

b. Binary data are transmitted over a microwave link at the rate of 10^6 bits/sec and the power spectral density of the noise at the receiver input is 10^{-10} ω/Hz. find the average carrier power required to maintain an average probability of error $Pe \leq 10^{-4}$ for the following cases.
Binary PSK using coherent detection
DPSK
Note : take $erfc(2.63) = 2 \times 10^{-4}$, $Q(3.7) = 10^{-4}$. **(06 Marks)**

c. Define bandwidth efficiency. Tabulate and comment on the bandwidth efficiency of M-ary PSK signals for different values of M. **(04 Marks)**

OR

6 a. With neat diagram and expressions, explain binary FSK generation and non-coherent detection scheme. **(06 Marks)**

b. Explain the generation and optimum detection of differential phase – shift keying with neat block diagram. **(06 Marks)**

c. What is the advantage of M-ary QAM over M-ary PSK system? Obtain the constellation of QAM for M = 4 and draw signal space diagram. **(04 Marks)**

Module-4

7 a. With a neat block diagram, explain the digital PAM transmission through band limited baseband channels. Also obtain the expression for inter symbol interference. **(06 Marks)**

b. Explain the modified duo-binary signaling scheme, with pre-coding. Illustrate the encoding for the binary sequence "011100101". Assume previous pre-coder outputs as 1. **(07 Marks)**
With neat diagram, explain the timing features pertaining to eye diagram and it interpretation for baseband binary data transmission system. **(03 Marks)**

OR

8 a. With neat sketches and expressions, explain raised cosine spectrum solution to reduce ISI. **(06 Marks)**

b. What is the advantage of controlled ISI partial response signaling scheme? With block diagram, explain the duo-binary encoder with pre-coder. Mention the frequency response, impulse response and its features. **(06 Marks)**

c. With neat diagram and relevant expressions, explain the concept of adaptive equalization. **(04 Marks)**

Module-5

9 a. Explain the working of Direct Sequence Spread Spectrum transmitter and receiver with neat diagram, waveform and expressions. **(08 Marks)**

b. A slow frequency Hopped/MFSK system has the following parameters,
   i) The number of bits/MFSK symbol = 4
   ii) The number of MFSK symbols per hop = 5
   iii) Calculate the processing gain of the system in decibels. **(03 Marks)**

c. List and briefly explain any 3 applications of direct sequence spread spectrum. **(05 Marks)**

OR

10 a. With a neat block diagram, explain frequency Hopped spread spectrum technique. Explain the terms chip rate, Jamming Margin and processing gain. **(08 Marks)**

b. What is a PN sequence? Explain the generation of maximum-length sequences (ML-sequence). What are the properties of ML sequences? **(04 Marks)**

c. In a DS/BPSK system, the feedback shift register used to generate the PN sequence has length m = 19. The system is required to have an average probability of symbol error due to externally generated interfering signals that does not exceed 10^{-5}. Calculate the following system parameters in decibels :
   i) Processing gain
   ii) Antijam margin
   (Assume Q(4.25) = 10 –5 or erfc(3) = 2×10^{-5}). **(04 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan. 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention any two differences between CMOS and Bipolar technology. **(02 Marks)**

b. Write all the mask steps of p-well process. **(06 Marks)**

c. With neat diagrams, explain the cut off, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds}. **(08 Marks)**

OR

2 a. Explain body effect as non ideal IV effects of MOSFET. **(03 Marks)**

b. Explain Noise margin, with respect to CMOS inverter. **(05 Marks)**

c. Explain the steps of n-MOS fabrication with neat diagram. **(08 Marks)**

Module-2

3 a. With a neat diagram, explain λ - rules for buried and butting contact and show thE cross sectional view of same. (white any one structure burreid contact). **(08 Marks)**

b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. **(08 Marks)**

OR

4 a. Define sheet resistance, with equation. **(02 Marks)**

b. Calculate the area capacitance of the layer below [Refer Fig.Q4(b)] :

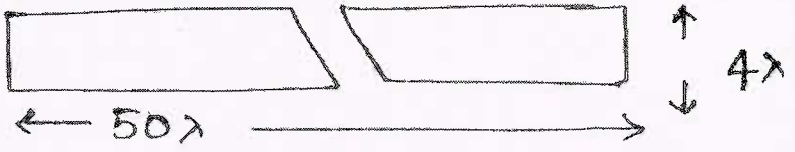

Fig.Q4(b)

i) If the layer is metal – 1 and relative capacitance value is 0.075 C_g

ii) if the layer is polysilicon and relative capacitance value is 0.1 C_g. **(06 Marks)**

c. Write the schematic and stick diagram for Boolean expression $y = \overline{(a + bc)}$.(implement using CMOS logic). **(08 Marks)**

Module-3

5 a. Design a 4bit, 4 × 4 barrel shifter. Write the nMOS implementation and strategy for the same. **(08 Marks)**

b. Explain carry select adder with neat block diagram. **(08 Marks)**

OR

6 a. Define regularity. **(02 Marks)**

b. Derive the scaling factor for the device parameter :
   i) Parasitic capacitance
   ii) Channel resistance
   iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like EX-OR, EX-NOR AND and OR operations with an adder. Write the block diagram of 4-bit ALU using adder element. **(08 Marks)**

Module-4

7 a. Explain the following logics :
   i) Clocked CMOS logic
   ii) n-p CMOS logic. **(08 Marks)**

b. Explain parity generator, with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

OR

8 a. Explain Pseudo-nMOS logic. Find Z_{pu}/Z_{pd} when $V_{inr} = 0.5V_{DD}$, $V_{tn} = |V_{t_p}| = 0.2V_{DD}$, $V_{DD} = 5V$ and $\mu_n = 2.5\mu p$. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

Module-5

9 a. Write the system timing considerations. **(08 Marks)**

b. Explain logic verification principle. **(08 Marks)**

OR

10 a. Explain three transistor dynamic RAM with neat circuit and stick diagram. **(06 Marks)**

b. What are design manufacturability. **(10 Marks)**

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