CBCS SCHEME

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the step-by-step CMOS P-Well fabrication process. **(08 Marks)**

b. With the mathematical equations, explain velocity saturation and mobility degradation effect due to increase in saturation current. **(08 Marks)**

OR

2 a. With the transfer characteristic of skewed inverter, explain the beta ratio effects. **(06 Marks)**

b. Compare CMOS and bipolar technologies. **(06 Marks)**

c. Consider the nMOS transistor in a 180 nm process with a nominal threshold of 0.4V and doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1V instead of '0'? **(04 Marks)**

Module-2

3 a. Discuss the λ-based design rules (i) Butting contact (ii) Transistors (nMOS, pMOS and CMOS) **(08 Marks)**

b. Derive the expression of delay interms of τ for CMOS inverter pair. **(08 Marks)**

OR

4 a. Draw the layout for $\overline{Y} = A + BC$ using CMOS. **(08 Marks)**

b. Find the C_{in} for the layout shown in Fig.Q4(b).

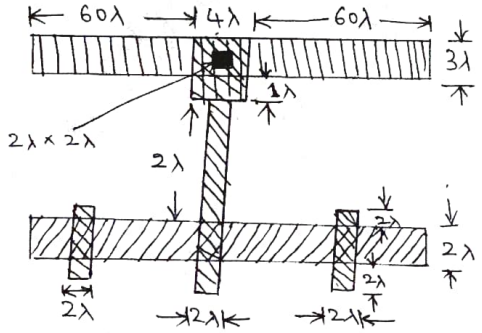

Fig.Q4(b) **(08 Marks)**

Module-3

5 a. Define scaling. Explain the scaling factors for device parameters. **(08 Marks)**

b. What is Manchester Carry Chain? Explain it. **(08 Marks)**

OR

6 a. What are the problems associated with VLSI design and how to reduce by using standard practice? **(06 Marks)**

b. Draw the 4 × 4 cross bar switch using MOS switches and explain it. **(06 Marks)**

c. Calculate the Regularity for 4 × 4 bit and 8 × 8 bit shifter. **(04 Marks)**

23.07.2021
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Solutions Submitted By:
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22/07/2021

Module-4

7 a. Construct a stick diagram for an nMOS parity generator as shown in Fig.Q7(a). The required response is such that $z = 1$ if there is an even number (including zero) of 1s on the input and $z = 0$ if there is an odd number.

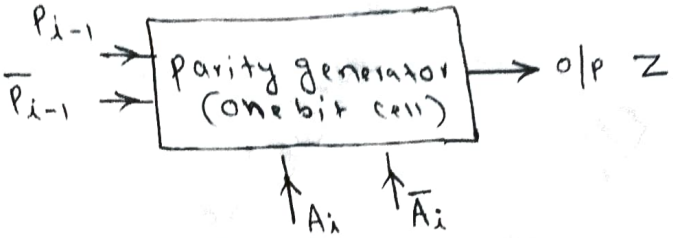


Fig.Q7(a) **(08 Marks)**

b. Draw the block diagram of Generic structure of an FPGA fabric and explain it. **(08 Marks)**

OR

8 a. Construct a stick diagram for an multiplexer shown in Fig.Q8(a) using CMOS.

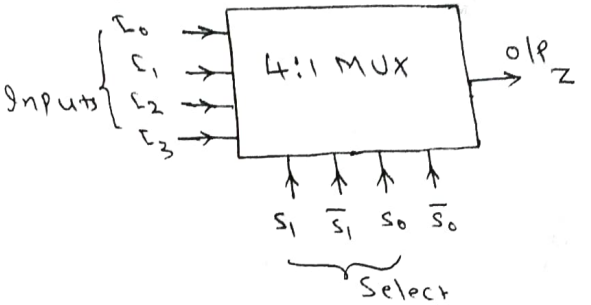


Fig.Q8(a) **(08 Marks)**

b. Explain the goals and techniques of FPGA based system design. **(08 Marks)**

Module-5

9 a. What are the requirements for system timing considerations? **(06 Marks)**

b. Explain the operation of a three transistor dynamic RAM cell. **(06 Marks)**

c. Write a note on stuck - at faults. **(04 Marks)**

OR

10 a. With the help of block diagram, explain the process of logic verification. **(08 Marks)**

b. Explain the operation of CMOS pseudo-static memory cell. **(08 Marks)**

* * * * *

Solutions to 6th Semester B.E. Degree Examination, Dec. 2019 | Jan. 2020

Faculty – Prof. Meenaxi. Torase

Subject – VLSI Design Subject Code – 15EC53

Module – 1

1a Explain the step-by-step CMOS p-well fabrication process. (8 Marks)

⟹

→ P-well acts as substrate for n-device within parent n-type substrate.

Mask-1 : Defines the area in which deep p-well diffusions are to take place

Mask-2 : Defines thinox regions, namely those areas where thick-oxide is to be stripped and thin-oxide grown to accomodate p and n-transistors.

Mask-3 : used to pattern polysilicon layer.

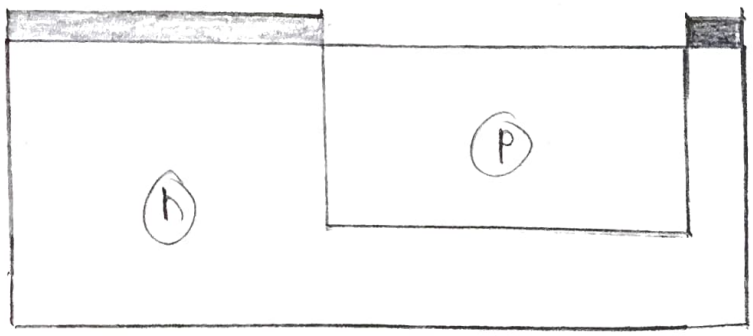
Mask-4 : p^+ mask is used to define areas where p-diffusion is to take place.

Mask-5 : negative p^+ mask is used to define areas where n-diffusion is to take place.

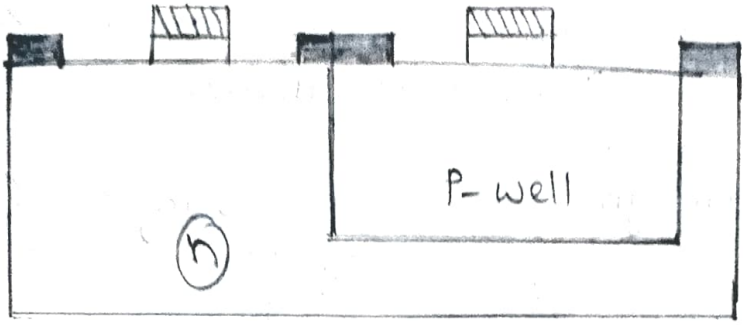
Mask-6 : Contact cuts are defined.

Mask-7 : Metal layer pattern is defined.

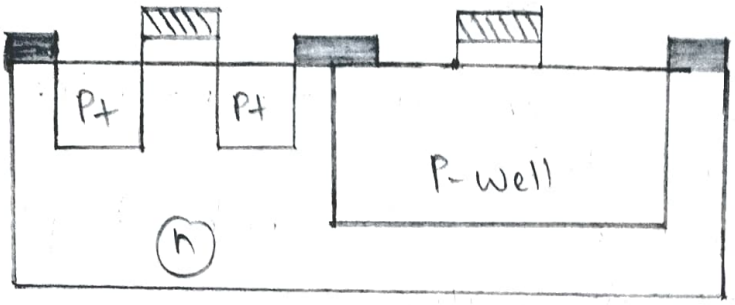
Mask-8 : Overglass with Contact cuts for bonding pads.



Prof – Meenaxi. T

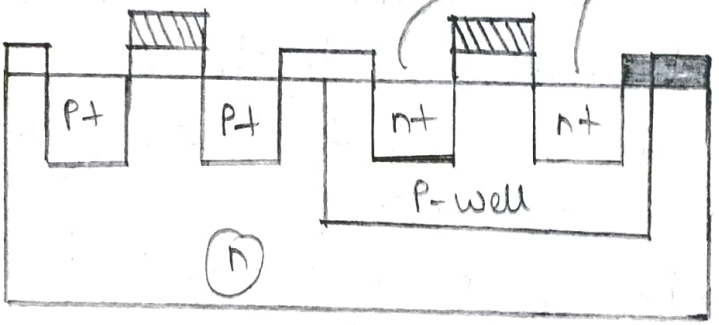


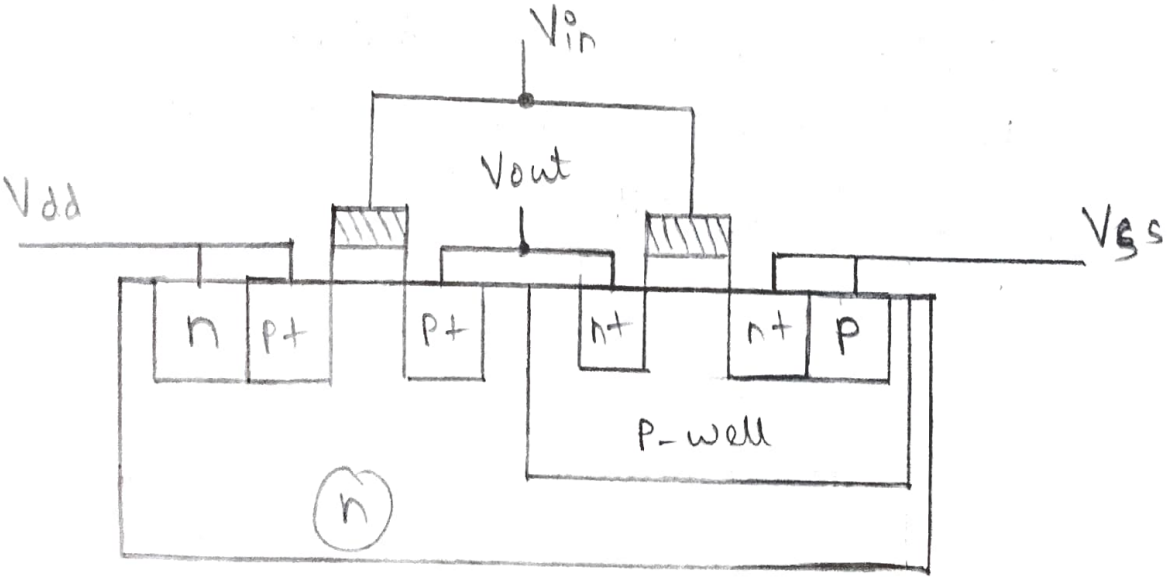
P+ mask
(+)ve



P+ mask
(-ve)

n-diffusion





1b With the mathematical equations, explain velocity saturation and mobility degradation effect due to increase in saturation current. (8 Marks)

$\Rightarrow$ $\boxed{V = \mu \mathcal{E}}$ where μ is carrier mobility, the constant of proportionality

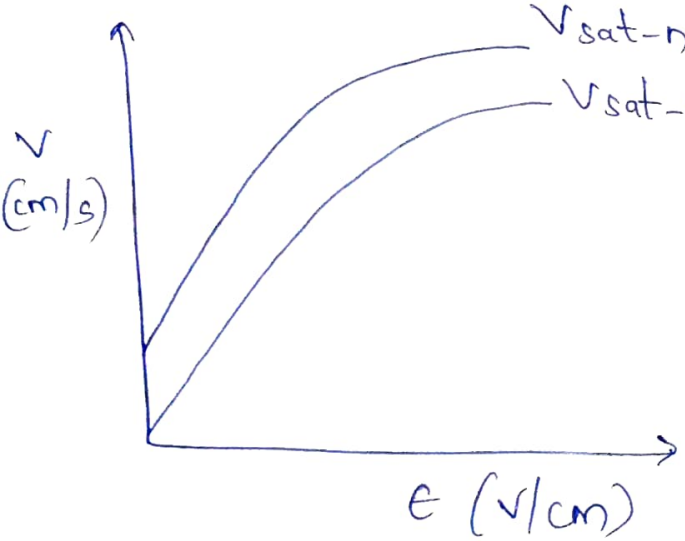
→ The carrier drift velocity and hence current is proportional to lateral electric field $\left(\mathcal{E} = \frac{V_{ds}}{L}\right)$ between source and drain.

→ The long-channel model assumed that carrier mobility is independent of applied fields. This is a good approximation for low fields, but breaks down when strong lateral or vertical fields are applied.

→ A high-voltage at the gate of transistor attracts the carriers to the edge of the channel, causing collisions with the oxide interface that slow the carriers. This is called Mobility degradation

→ Carriers approach a maximum velocity (V_{sat}) when high fields are applied. This phenomenon is called velocity saturation.

→ At low fields, the velocity increases linearly with the field. The slope is mobility μ_{eff}.



$$V = \begin{cases} \dfrac{\mu_{eff}\,\mathcal{E}}{1 + \dfrac{\mathcal{E}}{\mathcal{E}_c}}, & \mathcal{E} < \mathcal{E}_c \\ V_{sat}, & \mathcal{E} \geq \mathcal{E}_c \end{cases}$$

Critical electric field is

$$\mathcal{E}_c = \frac{2V_{sat}}{\mu_{eff}}$$

Prof. Meenaxi

2a with the transfer characteristics of skewed inverter, explain the beta ratio effects. – (6marks)

⟹

→ for $\beta_p = \beta_n$, the inverter threshold voltage V_{inv} is $\frac{V_{dd}}{2}$

→ This may be desirable because it maximizes noise margin and allows a capacitive load to charge and discharge in equal times by providing equal current source and sink capabilities.

→ Inverters with different beta ratios $r = \frac{\beta_p}{\beta_n}$ are called skewed inverters.

→ If $r > 1$, the inverter is HI-skewed.

→ If $r < 1$, the inverter is LO-skewed

→ If $r = 1$, the inverter has normal skew or is unskewed

→ A HI-skewed inverter has a strong pmos transistor Therefore, if the input is $\frac{V_{dd}}{2}$, output will be greater than $\frac{V_{dd}}{2}$. The input threshold must be higher than unskewed inverter.

→ A LO-skew inverter has weaker pmos transistor and thus a lower switching threshold.

→ As the beta ratio is changed, the switching threshold moves. However the output voltage transition remains sharp.

→ Gates are usually skewed, by adjusting width of transistors while maintaining minimum length for speed.

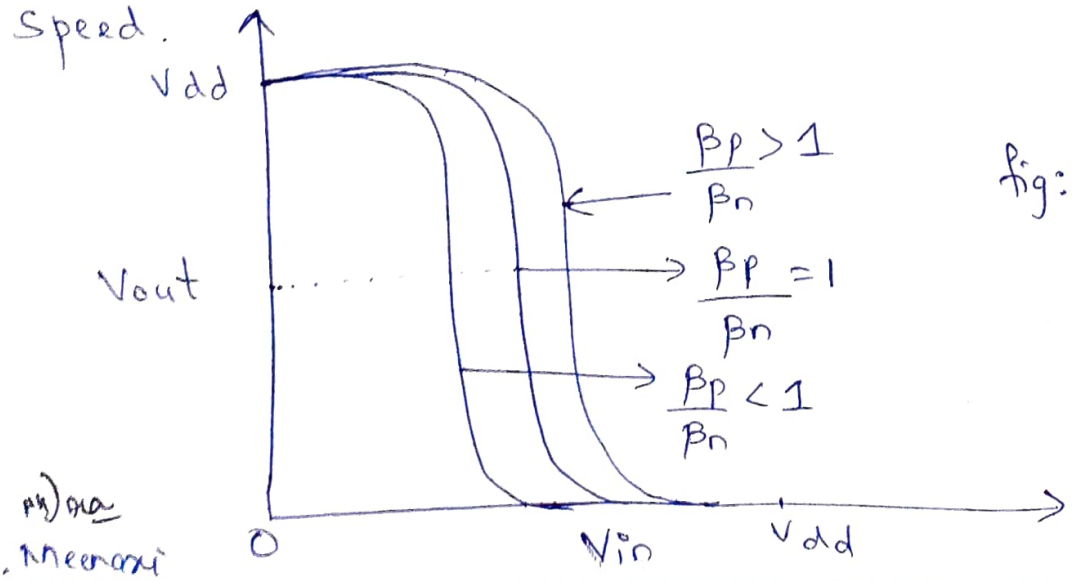
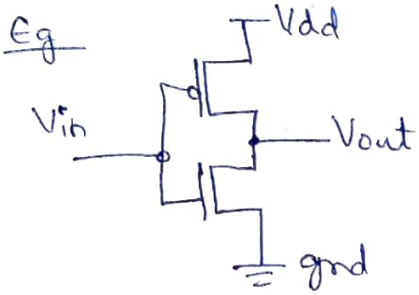
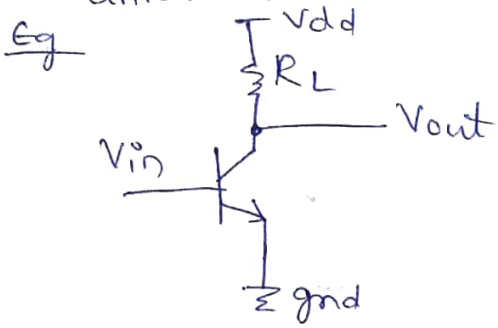


fig: Transfer characteristics of skewed inverters

2b Compare CMOS and bipolar technologies. (6marks)

⟹

CMOS	bipolar
→ low static power dissipation	→ High static power dissipation
→ High input impedance	→ low input impedance
→ low drive current	→ High drive current
→ High packing density	→ low packing density
→ low gm	→ high gm
→ low output drive current	→ high output drive current
→ high delay sensitivity to load.	→ low delay sensitivity to load
→ Bi-directional	→ unidirectional
Eg 	Eg 

2c Consider the nmos transistor in a 180nm process with a nominal threshold of 0.4V and doping level of $8 \times 10^{17}\ cm^{-3}$. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1V instead of '0'. (4 marks)

⟹ At room temperature, thermal voltage $\frac{KT}{q} = 26mV$

$n_i = 1.45 \times 10^{10}\ /cm^3$

$N_A = 8 \times 10^{17}\ /cm^3$

$V_{tho} = 0.4$

Threshold voltage increases by $0.472 - 0.4$

$= 0.072V$

$$V_t = V_{tho} + \gamma\left(\sqrt{2\phi_b + V_{SB}} - \sqrt{2\phi_b}\right)$$

$$\phi_b = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 26mV \ln\left(\frac{8\times10^{17}}{1.45\times10^{10}}\right)$$

$$\boxed{\phi_b = 0.463V}$$

$$\gamma = \frac{\sqrt{2\epsilon_{si} q \cdot N_A}}{C_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$= \frac{3.9\times8.854\times10^{-14}}{10.5\times10^{-8}}$$

$$C_{ox} = 3.26\times10^{-6}$$

$$\gamma = \frac{\sqrt{2\times11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times8\times10^{17}}}{3.26\times10^{-6}}$$

$$\boxed{\gamma = 0.157}$$

$$\therefore V_t = 0.4 + 0.157\left(\sqrt{2(0.463)+1.1} - \sqrt{2(0.463)}\right)$$

$$= 0.4 + 0.157\left(1.423 - 0.962\right)$$

$$\boxed{V_t = 0.472}$$

Now

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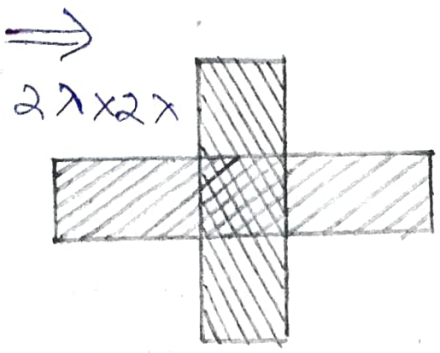
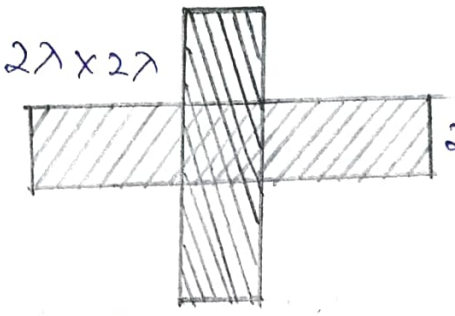
Module-2

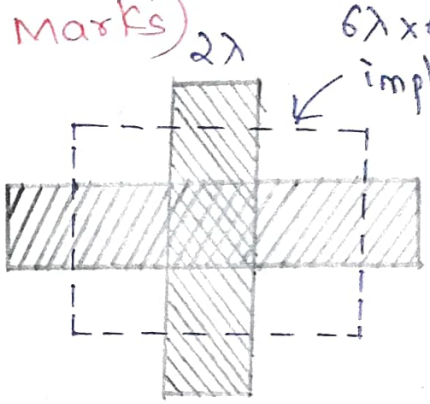
3a Discuss the λ-based design rules (i) Butting Contact (ii) Transistors (nmos, pmos and cmos) (8 Marks)



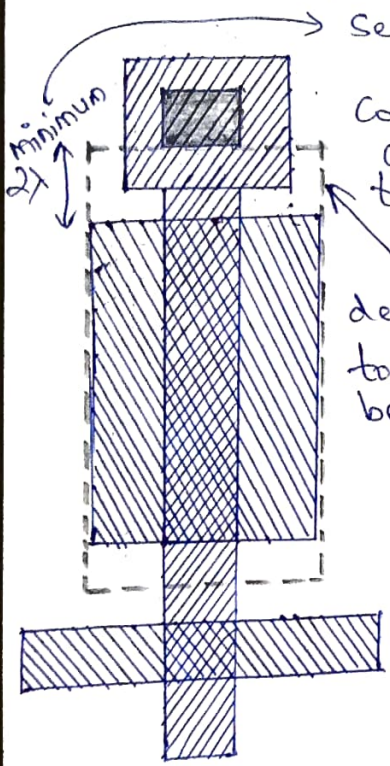
nmos enhancement

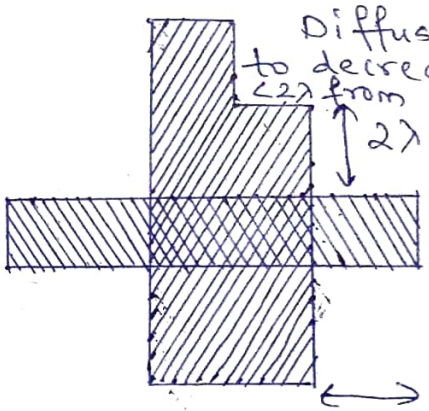


Pmos enhancement

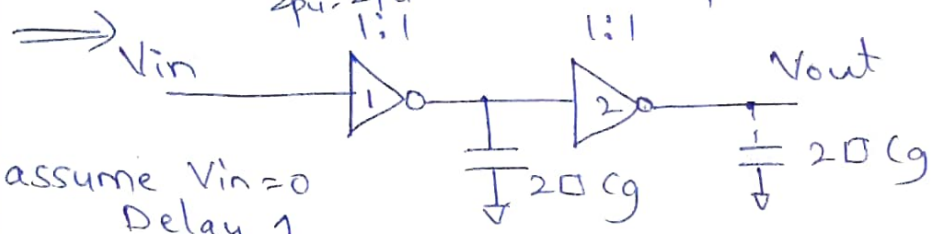


nmos depletion





3b Derive the expression of delay interms of τ for CMOS inverter pair. — (8 Marks)



assume Vin = 0

Delay 1

$= 2.5 R_s \times 20 C_g$

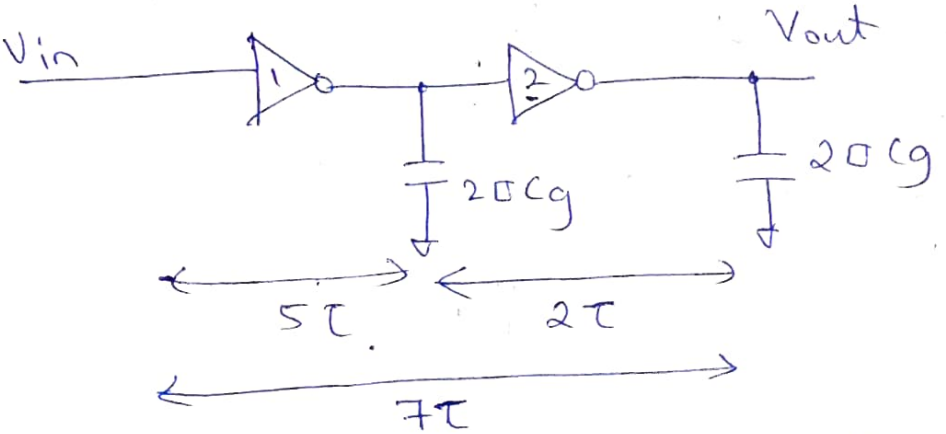
Delay1 = 5τ

$\therefore$ Delay 2 = $1 R_s \times 20 C_g$

Delay2 = 2τ

$\therefore$ Total delay = $5\tau + 2\tau$

Total delay = 7τ



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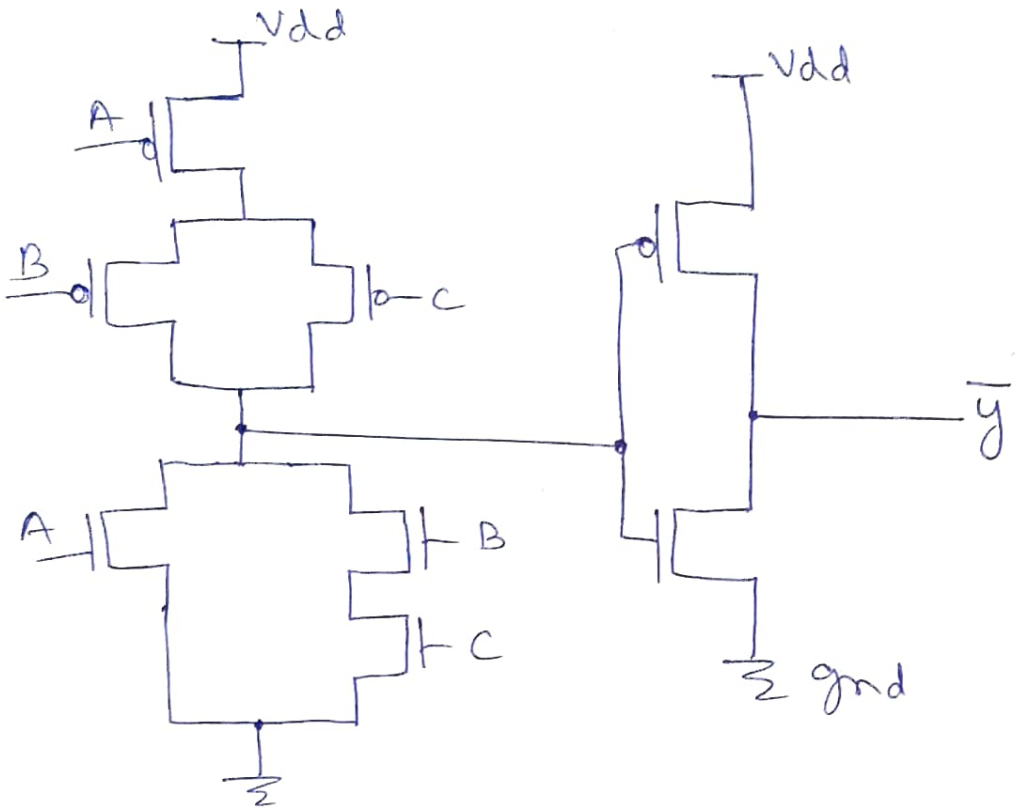
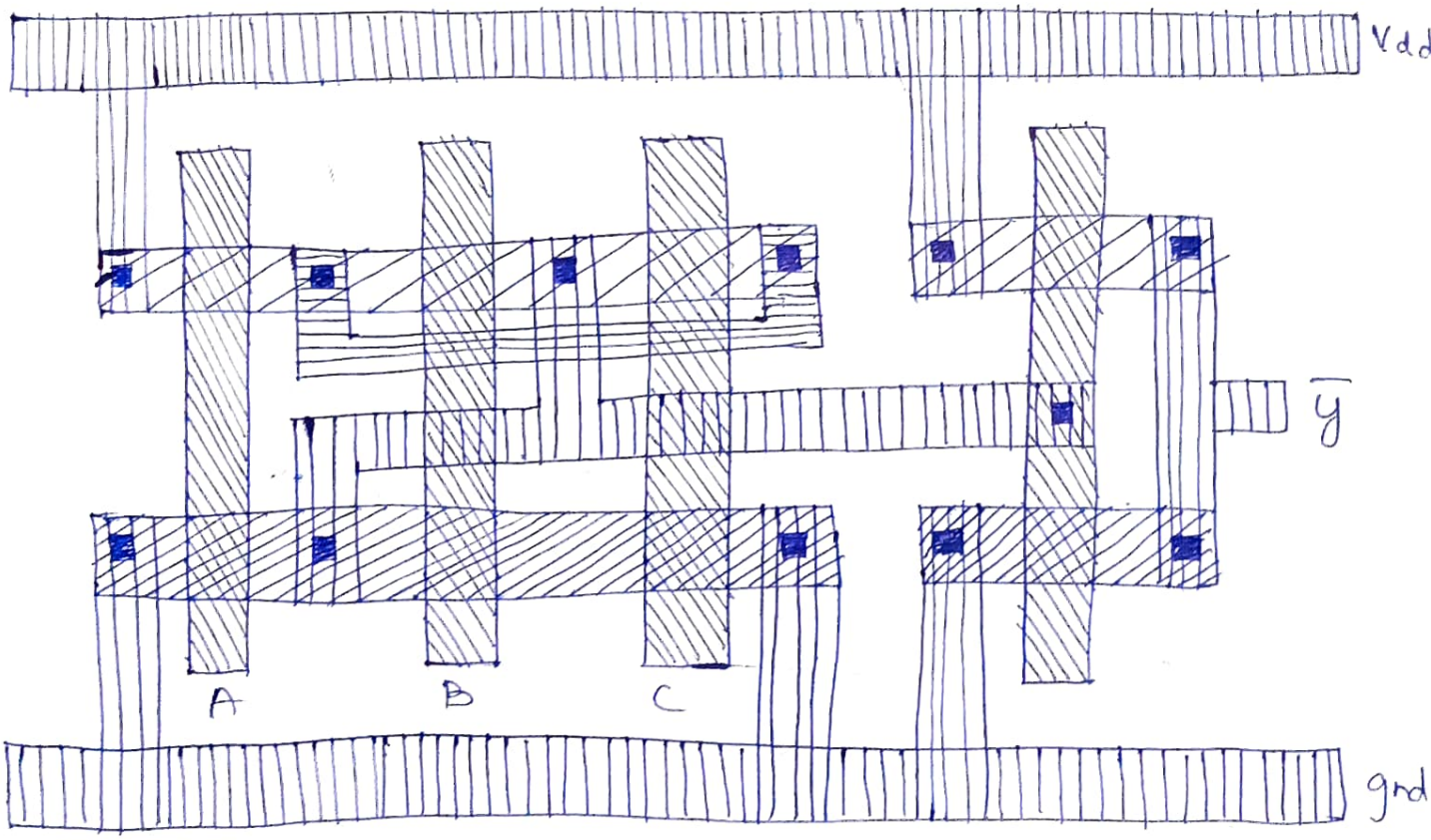
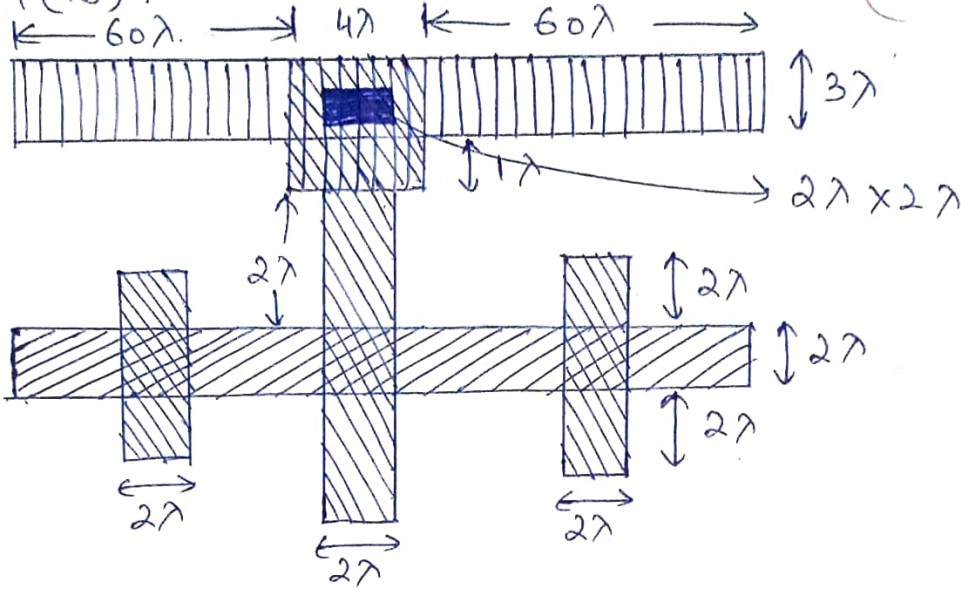
4a Draw the layout for $\bar{y} = A + BC$ using CMOS. (8 Marks)

$\Rightarrow$ $\bar{y} = A + BC$





4b Find the C_{in} for the layout shown in fig. Q(4b). (8 Marks)



Solution

C_{in} = metal capacitance (C_m) + Polysilicon capacitance (C_p) + Gate capacitance (C_g)

$$C_{in} = C_m + C_p + C_g$$

$$C_m = \frac{2 \times (60\lambda \times 3\lambda)}{2\lambda \times 2\lambda} \times \text{Relative 'c' value}$$

$$= \frac{360\lambda^2}{4\lambda^2} \times 0.075 \square C_g$$

$$C_m = 6.75 \square C_g$$

$$C_p = \text{Relative area} \times \text{Relative 'c' value}$$

$$= \frac{[(4 \times 4) + (2 \times 2) + (2 \times 1)]\lambda^2}{(2\lambda \times 2\lambda)} \times 0.1 \square C_g$$

$$C_p = 0.55 \square C_g$$

$$C_g = 1 \square C_g$$

$$\therefore C_{in} = C_m + C_p + C_g$$

$$= 6.75 \square C_g + 0.55 \square C_g + 1 \square C_g$$

$$\boxed{C_{in} = 8.3 \square C_g}$$

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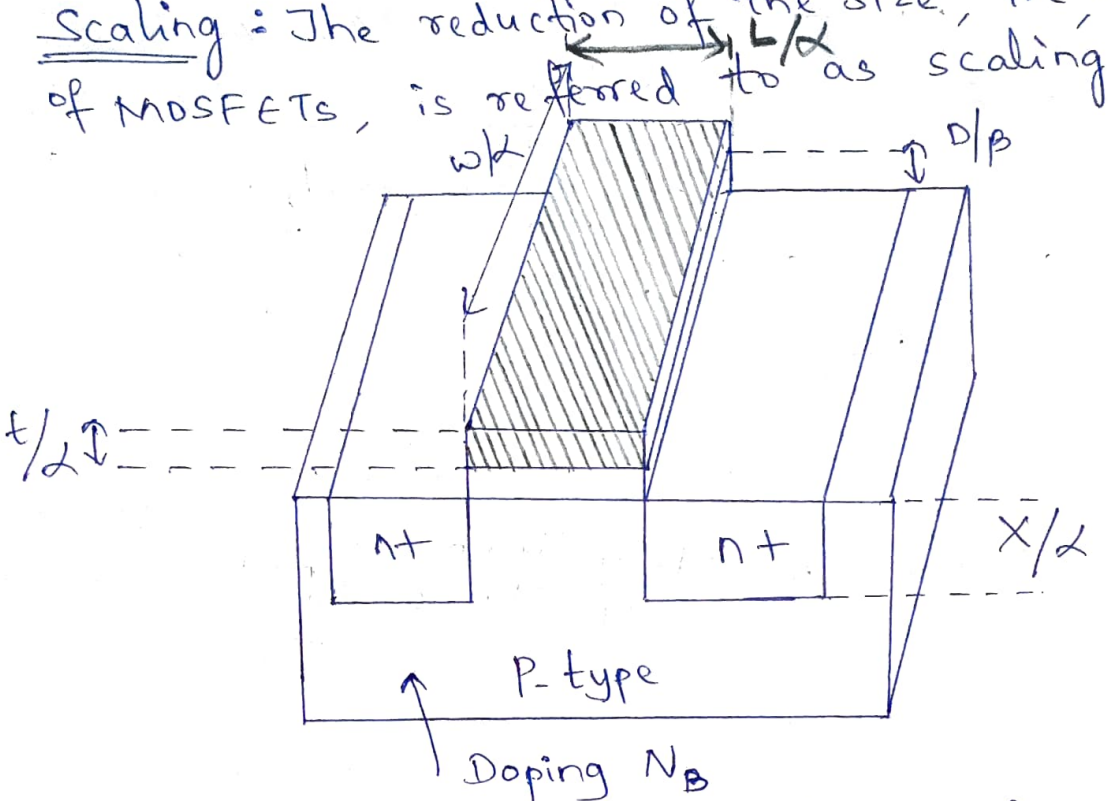
Module-3

5a Define scaling. Explain the scaling factors for device parameters. (8 Marks)

⇒

Scaling: The reduction of the size, i.e the dimensions of MOSFETs, is referred to as scaling.



Gate-Area (Ag)

$A_g = L \cdot w$

$A_g = \frac{1}{\alpha} \cdot \frac{1}{\alpha}$

$$A_g = \frac{1}{\alpha^2}$$

Scaling factors for device parameters

Gate-capacitance per unit area C_o or C_{ox}

$$C_o = \frac{\varepsilon_{ox}}{D}$$

$$= \frac{1}{1/\beta}$$

$$C_o = \beta$$

Gate - Capacitance (C_g)

$$C_g = C_o \cdot L \cdot W$$

$$= \beta \cdot \frac{1}{\alpha} \cdot \frac{1}{\alpha}$$

$$\boxed{C_g = \frac{\beta}{\alpha^2}}$$

Parasitic Capacitance (C_x)

$$C_x = \frac{A_x}{d} = \frac{1/\alpha^2}{1/\alpha}$$

$$\boxed{C_x = \frac{1}{\alpha}}$$

Carrier Density in channel (Q_{on})

$$Q_{on} = C_o \cdot V_{gs}$$

$$= \beta \cdot \frac{1}{\beta}$$

$$\boxed{Q_{on} = 1}$$

channel Resistance (R_{on})

$$R_{on} = \frac{L}{W} \cdot \frac{1}{Q_{on} \cdot \mu}$$

$$\boxed{R_{on} = 1}$$

Gate - Delay (T_d)

$$T_d = R_{on} \cdot C_g$$

$$= 1 \cdot \frac{\beta}{\alpha^2}$$

$$\boxed{T_d = \frac{\beta}{\alpha^2}}$$

Maximum Operating frequency (f_o)

$$f_o = \frac{W}{L} \cdot \frac{\mu C_o V_{dd}}{C_g} = \frac{1}{T_d}$$

$$f_o = \frac{1}{\beta/\alpha^2}$$

$$\boxed{f_o = \alpha^2/\beta}$$

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Saturation current (I_{dss})

$$I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2$$

$$= \frac{KW}{L}(V_{gs}-V_t)^2$$

$$= \frac{\mu C_{ox} W}{L}(V_{gs}-V_t)^2$$

$$= \frac{\beta \cdot 1/\alpha}{1/\alpha} \cdot \frac{1}{\beta^2}$$

$$\boxed{I_{ds} = \frac{1}{\beta}}$$

Current Density (J)

$$J = \frac{I_{ds}}{A} = \frac{1/\beta}{1/\alpha^2}$$

$$\boxed{J = \frac{\alpha^2}{\beta}}$$

Switching Energy per gate (ϵ_g)

$$\epsilon_g = \frac{1}{2} C_g V_{dd}^2$$

$$= \frac{\beta}{\alpha^2} \cdot \frac{1}{\beta^2}$$

$$\boxed{\epsilon_g = \frac{1}{\alpha^2 \beta}}$$

Power dissipation per gate (P_g)

$$P_g = P_{gs} + P_{gd}$$

P_{gs} = static component

$$= \frac{V_{dd}^2}{R_{on}} = \frac{1/\beta^2}{1}$$

$$\boxed{P_{gs} = \frac{1}{\beta^2}}$$

P_{gd} = dynamic Component

$$= \epsilon_g \cdot f_o$$

$$= 1/\alpha^2\beta \cdot \alpha^2/\beta$$

$$\therefore \boxed{P_{gd} = \frac{1}{\beta^2}}$$

$$\therefore P_g = \frac{1}{\beta^2} + \frac{1}{\beta^2}$$

$$\boxed{P_g = \frac{1}{\beta^2}}$$

Power dissipation Per unit area

$$P_a = \frac{P_g}{A_g} = \frac{1/\beta^2}{1/\alpha^2}$$

$$\therefore \boxed{P_a = \frac{\alpha^2}{\beta^2}}$$

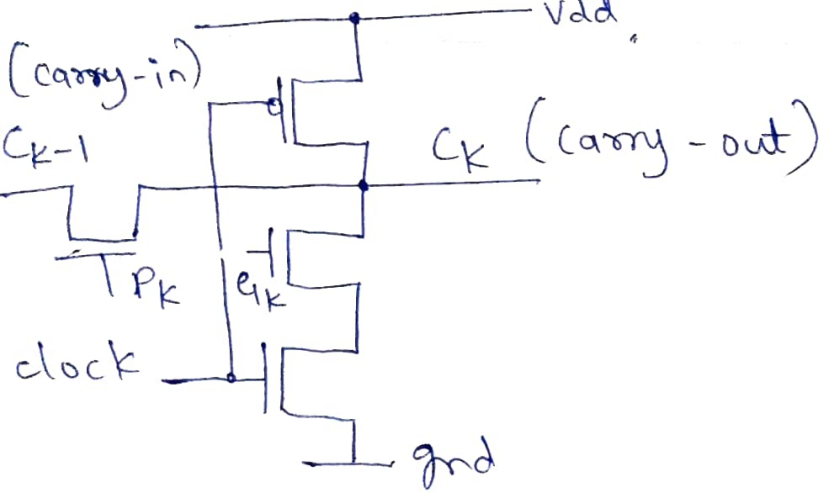
Power Speed Product (P_T)

$$P_T = P_g \cdot T_d = \frac{1}{\beta^2} \cdot \frac{\beta}{\alpha^2}$$

$$\therefore \boxed{P_T = \frac{1}{\alpha^2 \beta}}$$

5b What is Manchester Carry chain? Explain it (8 Marks)

⟹ Manchester carry-chain Adder is a chain of pass-transistors that are used to implement the carry chain.



$P_k = A_k \oplus B_k$

P_k = Propagate

g_k = Generate

$g_k = \overline{A}_k \cdot B_k$

→ It is a fast-adder circuit

→ when clock is 0, output will be charged to logic high, because pmos will be ON state.

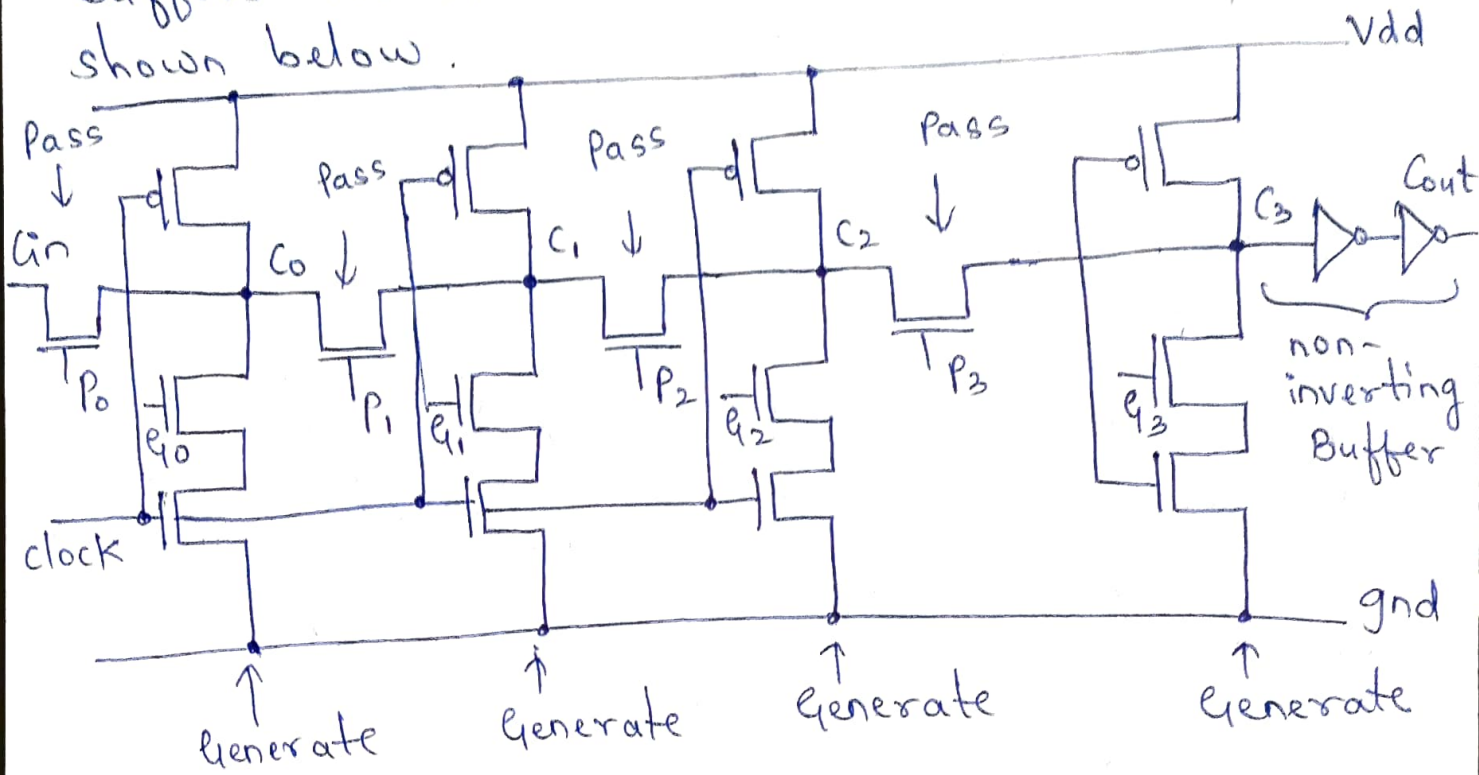
→ when clock is 1, pmos will be off. If $\boxed{P_k = 1}$ then carry-will propagate.

→ If $\boxed{P_k = 0}$ then C_{k-1} will not be propagated.

→ Depending on inputs at g_k ($A_k = B_k = 1$, carry will be generated). ($A_k = B_k = 0$ no carry generation)

→ Even though Manchester carry are faster while cascading delay is observed, cascading is done by connecting pass-transistors in series.

→ As n-pass transistors are cascaded, delay also increases as square of n. Thus to reduce delay, buffers are included after every 4 chain as shown below.



6a What are the problems associated with VLSI design and how to reduce by using standard practice? (6 Marks)

⇒ Some of the problems associated with VLSI design are:

→ How to design large complex systems in a reasonable time and with reasonable effort. This is a problem shared with other approaches to system design

→ The nature of architectures best suited to take full advantage of VLSI and the technology.

→ The testability of large/complex systems once implemented in silicon

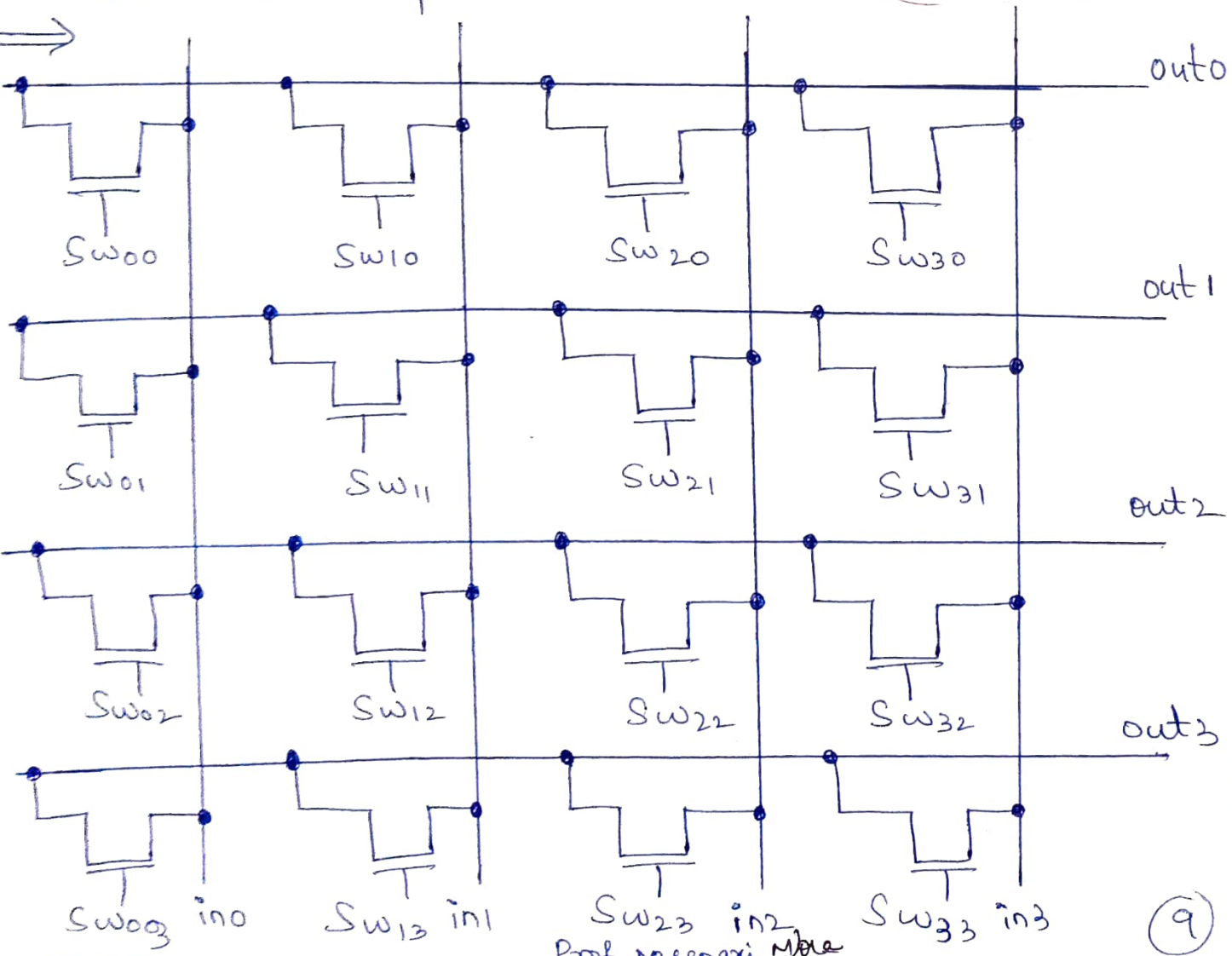
Problems are reduced if two aspects of standard practice are accepted:

→ Approach the design in a top-down manner and with adequate Computer-aided tools to do the job. Partition the system sensibly, aiming for simple interconnection between susbsystems and high regularity within subsystems. Generate and then verify each section of the design.

→ Design testability into the system from the outset & be prepared to devote a significant proportion of the total chip area to test & diagnostic facilities.

6b Draw the 4x4 cross-bar switch using Mos switches and explain it. (6 Marks)

⟹



→ Any general purpose n-bit shifter should be able to shift incoming data by upto (n-1) places in right-shift or Left-shift direction.

→ shifter must have
* input from a four-line parallel data-bus.
* four output lines for shifted data.
* means of transfering input data to output lines.

Cross bar switch results in few limitations.

→ any input line can be connected to any or all output lines.

→ If all switches are closed, then all inputs are connected to all outputs in one short circuit

→ 16 control signals (sw_{00} - sw_{15}) are required for each transistor switch and such complexity is highly undesirable.

→ Hence barrel shifter is more efficient which overcomes drawbacks of cross-bar switch.

6c Calculate the Regularity for 4x4 bit and 8x8 bit shifter. (4 marks)

⟹

→ Regularity = $\frac{\text{Total number of transistors on chip}}{\text{Number of transistor circuits that must be designed in detail.}}$

→ Regularity should be as high as possible to minimize the design effort required for any system

for 4x4 bit shifter

$$\text{Regularity} = \frac{\text{Total number of transistors on chip}}{\text{Number of transistors circuits that must be designed in detail}}$$

$$\therefore \text{Regularity} = \frac{16}{1}$$

$$\therefore \boxed{\text{Regularity} = 16}$$

for 8x8 bit shifter

$$\text{Regularity} = \frac{64}{1}$$

$$\therefore \boxed{\text{Regularity} = 64}$$

Module-4

7a Construct a stick diagram for an nmos parity generator as shown in Fig. Q7(a). The required response is such that z=1 if there is an even number (including zero) of 1's on the input and z=0 if there is an odd number. (8 Marks)

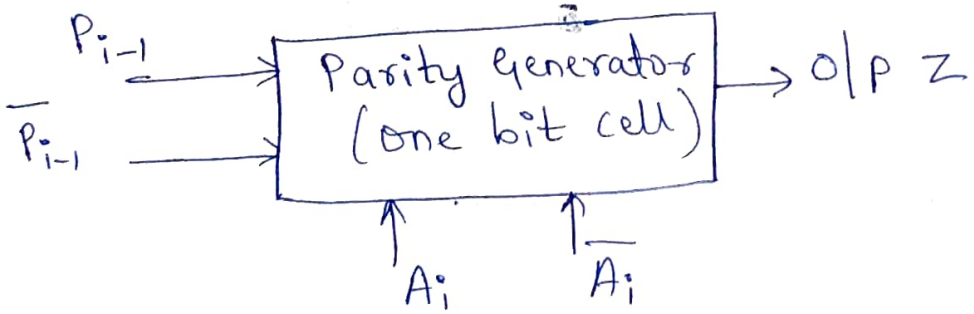


Fig. Q7(a)

H)ola

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$$Z = \overline{P_{i-1}} \cdot A_i + P_{i-1} \cdot \overline{A_i}$$

$$\overline{Z} = \overline{\overline{P_{i-1}} A_i + P_{i-1} \overline{A_i}}$$

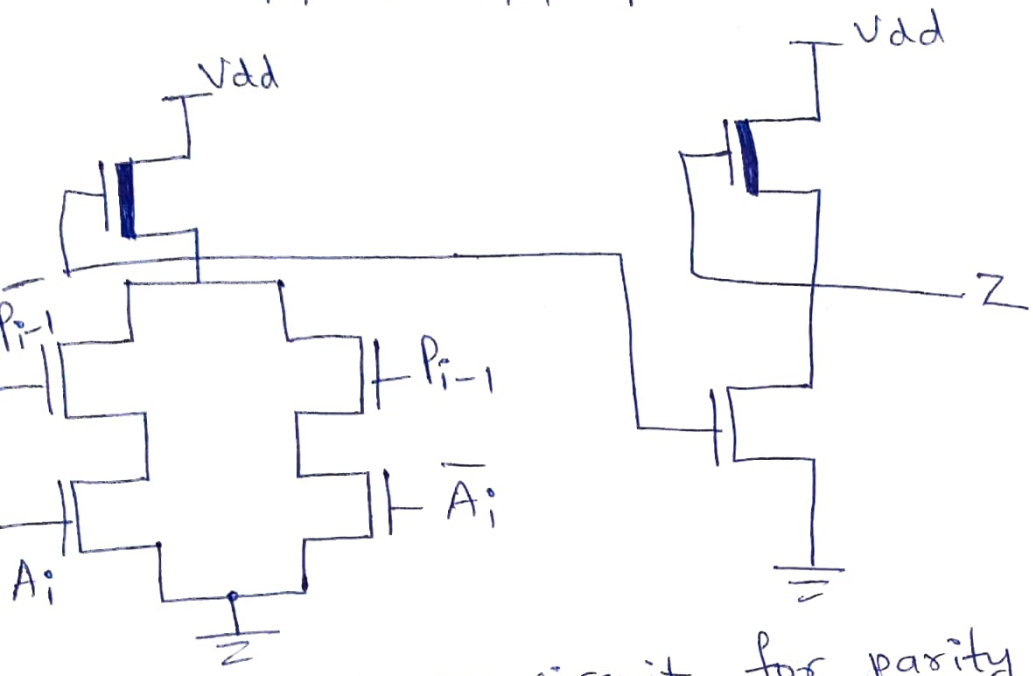


Fig: nmos circuit for parity Generator

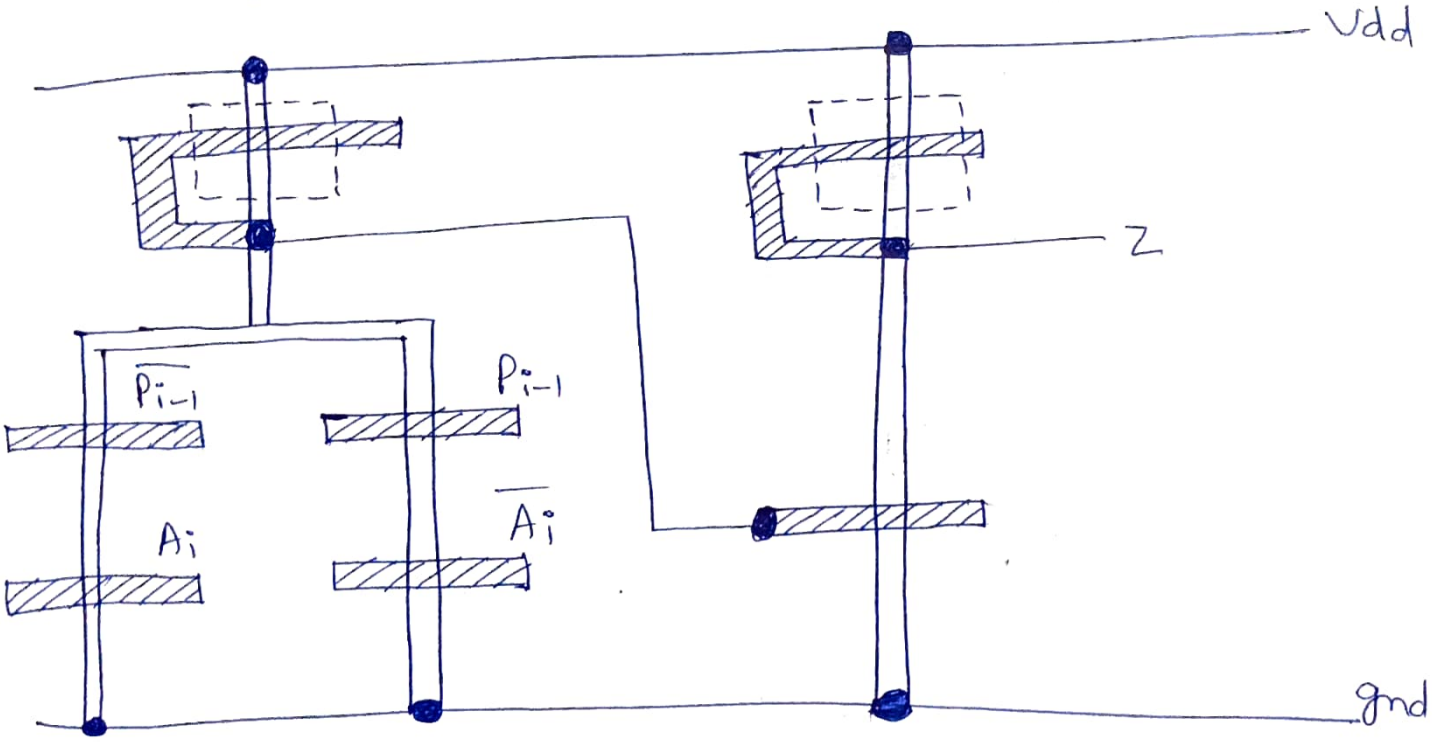
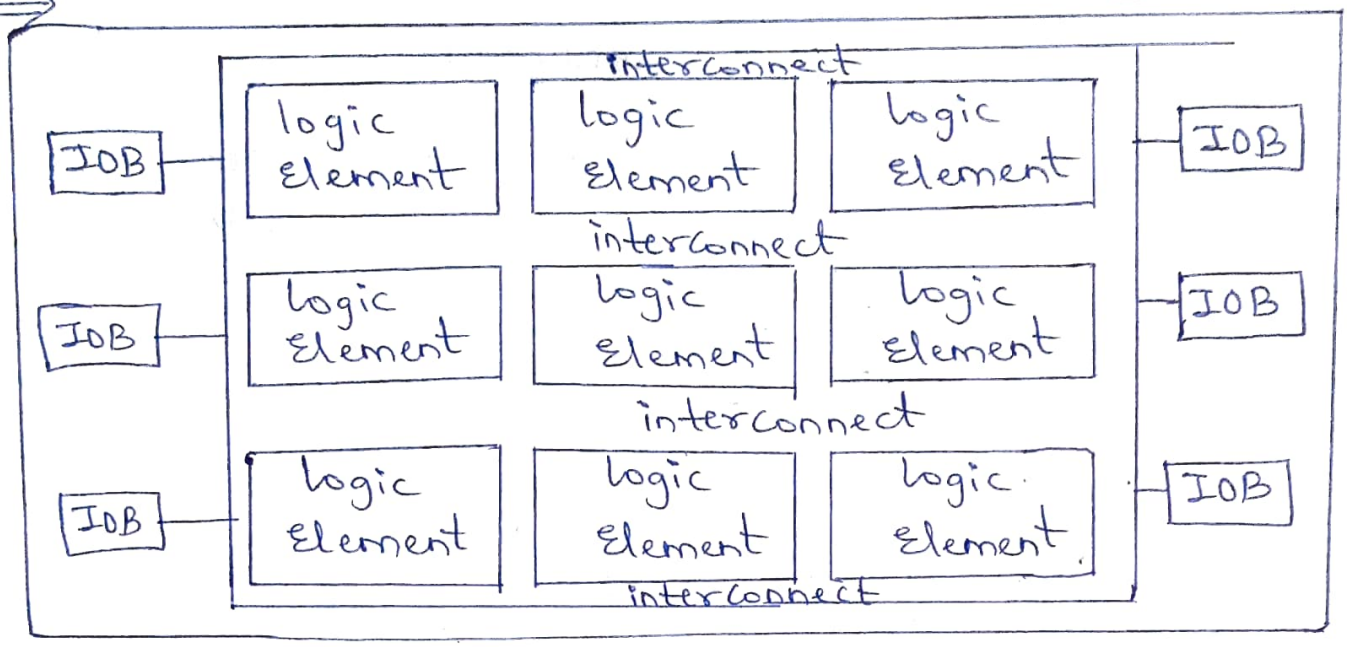


Fig: Stick diagram for parity Generator

7b Draw the block diagram of Generic structure of an FPGA fabric and explain it (8 Marks)

⟹



→ FPGA Consists of 3 major Elements
  * Combinational logic
  * Interconnect
  * I/o pins

→ Combinational logic is divided into small units which is known as logic element (LE) or Combinational logic blocks (CLB)

→ LE or CLB forms the functions of several logic gates.

→ Interconnection between these logic elements are made using programmable interconnects.

→ These interconnects are logically organized into channels or other units.

→ FPGA offers several interconnects depending on the distance between CLB's that are to be Connected.

→ clock signals are provided with their own interconnection networks

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→ I/o pins are referred as I/o Blocks (IOB) These are generally programmable for inputs or outputs and often provides other features such as low power or high speed connection

8a Construct a stick diagram for an multiplexer shown in fig. Q8(a) using CMOS. (8 Marks)

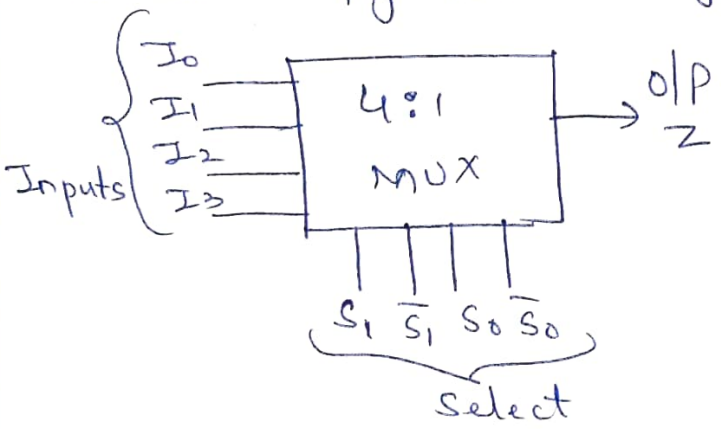
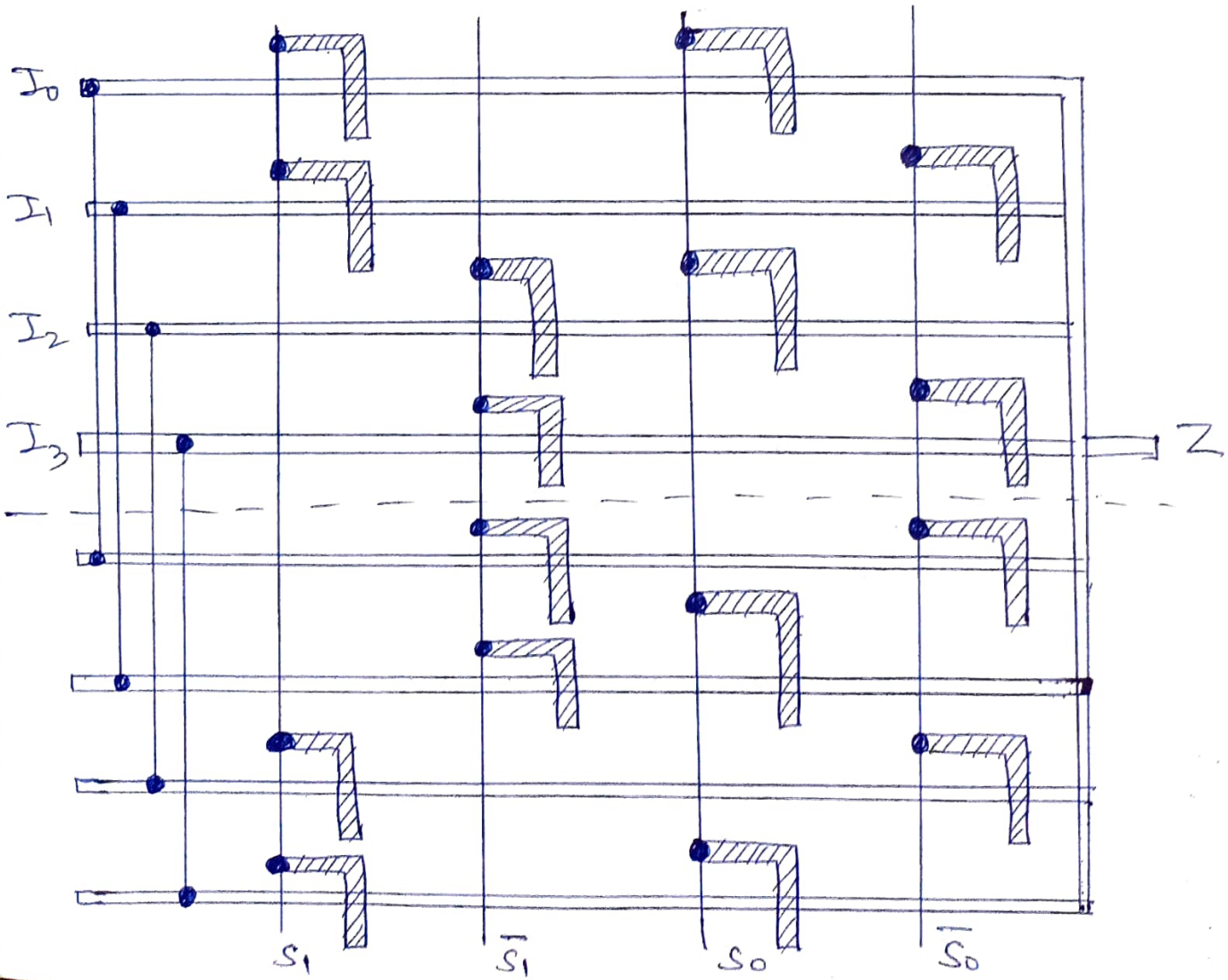


Fig. Q8(a)

⟹ CMOS stick-diagram for 4:1 MUX



8b Explain the goals and techniques of FPGA based system design (8 Marks)

⟹

→ The logic function to be performed is only one of the goals that must be met by an FPGA or any digital system design.

Performance: The logic must run at a required rate. Performance can be measured in several ways, such as throughput and latency. Clock rate is often used as a measure of performance.

Power | energy: The chip must often run within an energy or power budget. Energy consumption is clearly critical in battery-powered systems. Even if the system is to run-off the power grid, heat dissipation costs money and must be controlled.

Design time: You can't take forever to design the system, FPGAs, because they are standard parts, have several advantages in design time. They can be used as prototypes, they can be programmed quickly, and they can be used as parts in the final design.

Design Cost: Design time is one important component of design cost. FPGA tools are often less expensive than custom VLSI tools.

Manufacturing Cost: The manufacturing cost is the cost of replicating the system many times. FPGAs are more expensive than ASICs.

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Module-5

9a What are the requirements for system timing considerations? (6 Marks)

$\Longrightarrow$

→ A two-phase non-overlapping clock signal is assumed to be available and this clock alone will be used throughout the system.

→ clock phases are to be identified as ϕ_1 & ϕ_2 where ϕ_1 is assumed to lead ϕ_2

→ Bits (or data) to be stored are written to registers, storage elements and subsystems on ϕ_1 of clock; i.e, write signals WR are Anded with ϕ_1.

→ Bits (or data) written into storage elements may be assumed to have settled before the immediately following ϕ_2 signal and ϕ_2 signal is used to refresh data

→ Delays through data paths, combinational logic are assumed to be less than the interval between the leading edge of ϕ_1 of the clock and leading edge of the following ϕ_2 signal

→ Bits or data may be read from storage elements on the next ϕ_1 of the clock; i.e read signals RD are Anded with ϕ_1.

→ RD and WR are mutually exclusive to any one storage element.

→ A general requirement for system stability is that there must be atleast one clocked storage element in series with every closed loop signal path

More

9b Explain the operation of three transistor dynamic RAM cell. (6 Marks)

⟹

3T DRAM cell

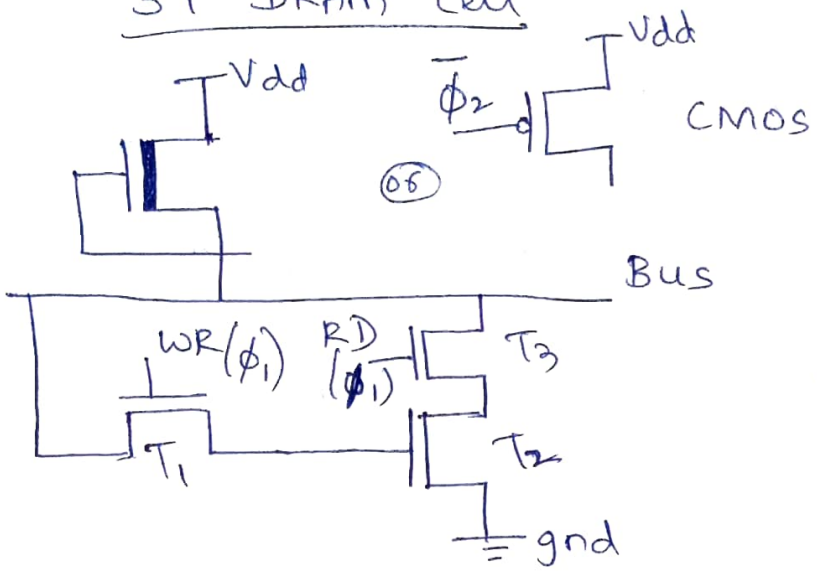
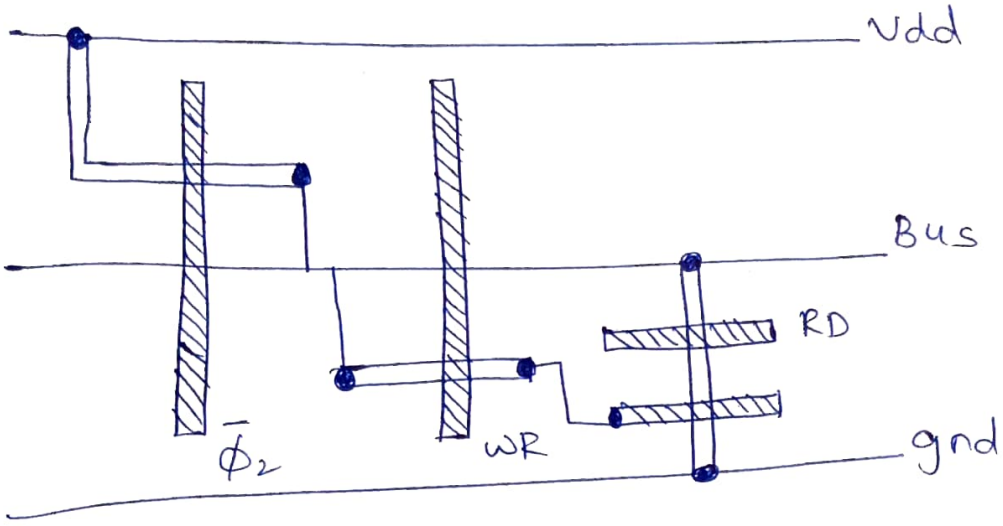


fig: NMOS 3T DRAM cell



Stick Diagram of 3T DRAM

→ with RD control line in low state, WR in high state (RD=0, WR=1) the logic level on bus is communicated to gate capacitance of T_2. Then WR is made low again

→ when both RD & WR are in low state, bit value is stored for some time by C_g of T_2

→ To read stored bit, make RD high and WR low and bus will be pulled to gnd through T_3 & T_2 if a 1 was stored

Otherwise T_2 will be non-conducting & bus will remain high due to pull-up circuit

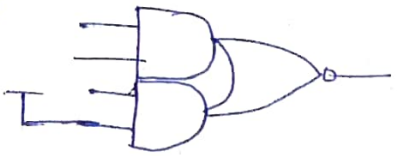
→ Complement of stored bit is read onto bus.
→ Cell is dynamic and will hold data only as long as sufficient charge remains on C_g of T_2

9c Write a note on stuck-at faults. (4 marks)

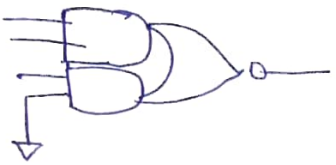
⟹ In the stuck-at model, a faulty gate input is modeled as a stuck-at zero (S-A-0) or stuck-at one (S-A-1)

→ These faults most frequently occur due to gate oxide shorts (nmos gate to gnd or pmos gate to Vdd) or metal-to-metal shorts.

Eg:



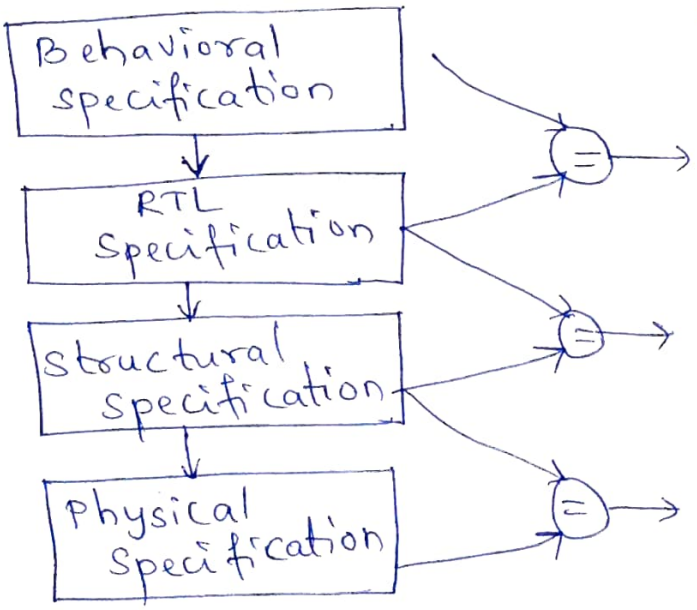
Stuck-at-1
S-A-1 fault



S-A-0 Fault.

10a With the help of block diagram, explain the process of logic verification. (8 Marks)

⟹



Formal verification
Test vector equivalence

Timing Analysis
Noise Analysis

Layout Versus Schematic (LVS)

Power analysis
DRC
ERC
Parasitic Extraction

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→ verification tests is necessary to prove that a synthesized gate description was functionally equivalent to source RTL.

→ Behaviour specification might be a description in a high-level computer language as C, a system modeling language as systemC, hardware description language as VHDL, verilog or simply a table with required inputs and outputs.

→ Designers have a golden model and this becomes the reference against which other designs are checked.

→ Functional equivalence involves running a simulator on 2 descriptions of chip & ensuring that o/p's are equivalent at some convenient check points in time for all inputs applied. This is most conveniently done in an HDL by employing a test-bench.

→ You can check functional equivalence through simulation at various levels of design hierarchy.

→ If the description is at RTL level, the behavior at system level may be able to be fully verified.

10b Explain the operation of CMOS pseudo-static memory cell (8-Marks)

⟹

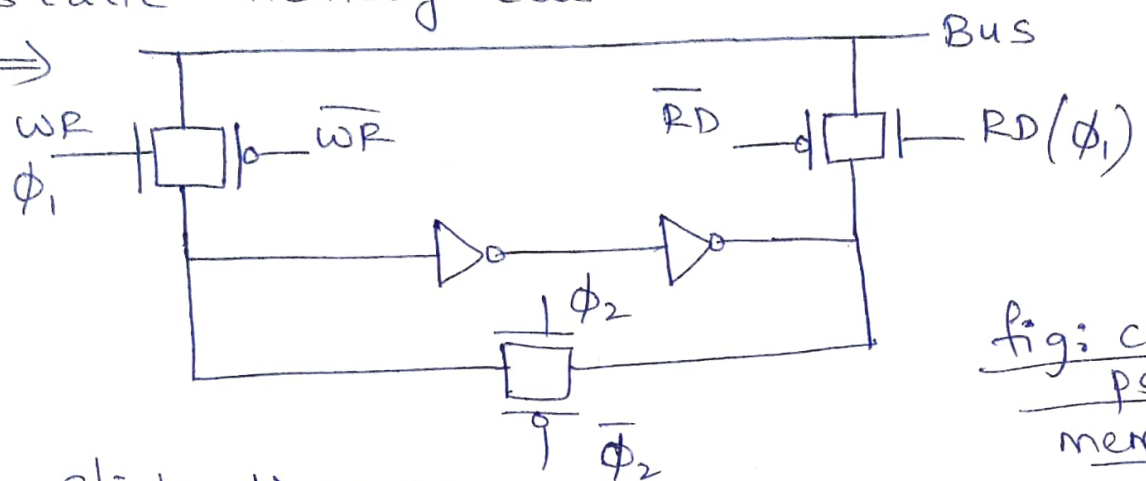
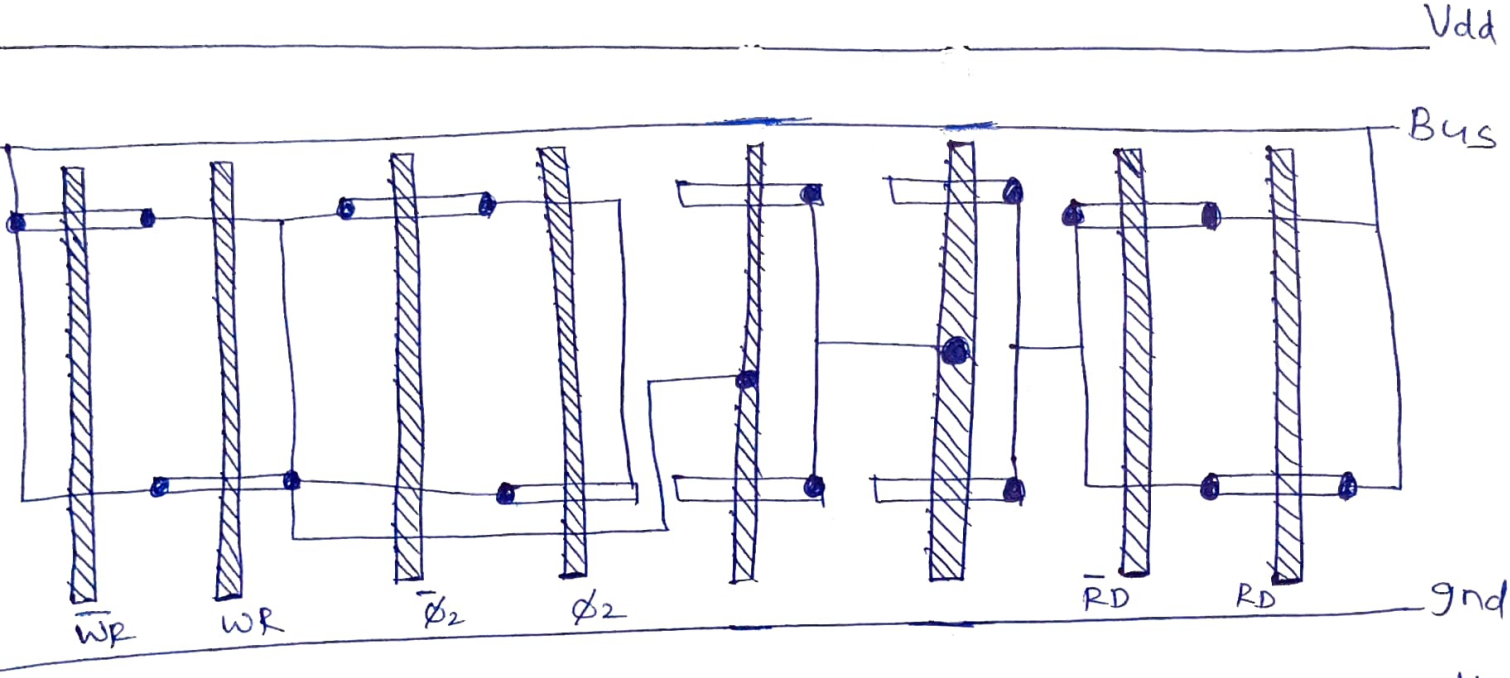


fig: CMOS pseudo-static memory cell

stick diagram



CMOS stick-diagram of Pseudo-static memory cell

→ DRAM need to be refreshed periodically and hence not convenient, hence pseudo-static RAM is designed which holds data indefinitely

→ 2 back-to-back inverters form a basic bistable element which is our memory.

→ ϕ_2 is used to refresh the data every clock cycle

→ Bit is written on activating WR line which occurs with ϕ_1 of clock

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→ Bit is stored on gate capacitance (C_g) of inverter-1, which will produce complemented output at inverter-1 and true at output of inverter-2

→ At every ϕ_2, stored bit is refreshed through gated feedback path

→ To read stored bit, RD is activated ($R_D = 1$) which occurs with ϕ_1 of clock

→ ϕ_2 is used for refreshing, hence no data to be read if so charge-sharing effect occurs, leading to destruction of stored bit ∴

→ W_R and RD must be mutually exclusive