Department of Electronics & Communication Engineering

BASIC ELECTRONICS (18ELN14/24)

SCHEME & SOLUTION

Aug/Sept 2020

Prepared By

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(Val.L)

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First/Second Semester B.E. Degree Examination, Aug./Sept.2020
Basic Electronics

Time: 3 hrs.   Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1   a. Explain the operation of PN – junction diode under forward and reverse bias condition.
                                                                                    (08 Marks)
     b. Explain how zener diode can be used as voltage regulator.   (06 Marks)
     c. A silicon diode has I_S = 10nA. operating at 25°C. Calculate diode current I_D for a forward bias of 0.6V.   (06 Marks)

OR

2   a. With neat circuit diagram, explain the operation of center tapped full wave rectifier. Draw input and output waveforms.   (08 Marks)
     b. Explain photo diode and LED in brief.   (06 Marks)
     c. Explain LM7805 fixed voltage regulator.   (06 Marks)

Module-2

3   a. Explain construction and operation of n–channel JFET. Draw transfer and drain characteristic.   (08 Marks)
     b. Explain the operation of CMOS inverter.   (06 Marks)

     c. A n–channel JFET has I_{Dss} = 8mA. V_p = –4V. Determine I_D for V_{GS} = –1V and V_{GS} = –2V.   (06 Marks)

OR

4   a. Explain construction and operation of n – channel depletion MOSFET.   (08 Marks)
     b. Explain the operation of SCR using 2 – Transistor model.   (06 Marks)
     c. Explain natural and forced commutation turn off methods of SCR.   (06 Marks)

Module-3

5   a. Define following terms with respect to OP –Amp : i) CMRR   ii) Input offset voltage iii) Slew rate. Also mention op-amp ideal characteristics.   (08 Marks)
     b. A certain op-amp has an open loop differentials voltage gain of 1,00,000 and CMRR = 4,00,000. Determine common mode gain and express CMRR in decibels.
                                                                                    (06 Marks)
     c. Explain op-amp as integrator.   (06 Marks)

OR

6   a. With neat circuit, explain the operation of three input adder circuit. Derive expression for V_0.   (08 Marks)
     b. A non inverting amplifier has closed loop gain of 25. If input voltage V_i = 10mv, R_f = 10KΩ determine the value of R_1 and output voltage V_0.   (06 Marks)
     c. Explain difference amplifier using op-amp.   (06 Marks)

Module-4

7 a. With neat circuit, explain transistor as an amplifier. Derive expression for voltage gain.
(08 Marks)

    b. Mention types of feedback amplifier. With block diagram, explain voltage series feedback amplifier.
(06 Marks)

    c. A negative feedback amplifier has gain $A = 1000$ and bandwidth of 200KHz. Calculate gain and bandwidth with feedback if feedback factor $\beta = 20\%$.
(06 Marks)

OR

8 a. What is phase shift oscillator? Explain with circuit, RC phase shift oscillator. **(08 Marks)**

    b. Explain with circuit, Astable multivibrator using IC 555. **(06 Marks)**

    c. An Astable multivibrator circuit has $R_1 = 6.8K\Omega$, $R_2 = 4.7K\Omega$, $C = 0.1\mu F$. Calculate frequency of oscillation and duty cycle **(06 Marks)**

Module-5

9 a. Convert :

      i) $(2467.125)_{10} = (?)_2 = (?)_{16}$

      ii) $(765.16)_8 = (?)_{10} = (?)_2$

      iii) $(101111.101)_2 = (?)_8 = (?)_{10}$. **(08 Marks)**

    b. Explain full adder using truth table and expression. Implement sum and carry expressions.
(06 Marks)

    c. Implement half adder using NAND gates. **(06 Marks)**

OR

10 a. State and prove De-Morgan's theorems for two variables. **(08 Marks)**

    b. With the help of logic diagram and truth table, explain the working of clocked SR – Flip flop.
(06 Marks)

    c. Explain the basic block diagram of communication system. **(06 Marks)**

1.A Explain the operation of PN junction diode under forward and reverse bias condition.

8 Marks

Soln
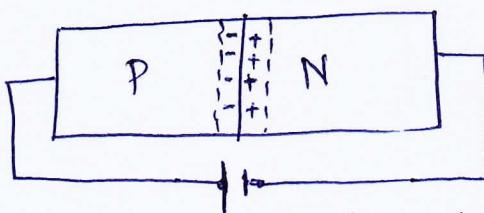
Fig. 1(a)   Diode under forward bias
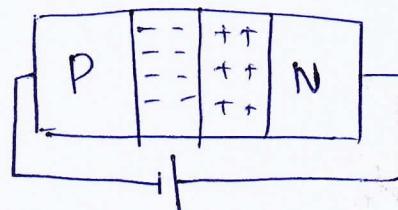
Fig 1(b) Diode under reverse bias

under forward bias

Fig 1(a) shows ~~the~~ PN junction diode under forward bias condition

- The diode is said to be in f/b when P side of the diode is at highest potential & N-side of the diode is at lowest potential.

- ~~With~~ Under this scenario, the depletion width reduces & helps in conduction of the current.

- The min voltage required to break the depletion width is 0.7V in Silicon & 0.3 in Germanium.

under reverse bias

- when P side of the ~~battery~~ diode is connected to -ve side of the battery & N-side of the diode is connected to +ve side of battery, the diode is said to be in reverse bias.

- During reverse bias mode, the depletion width reduces & there will be no current or very very less current flowing through the diode. Fig. 1(b).

I_F

(Breakdown voltage)

V_{BR}

FIB

Forward voltage $= 0.7 - Si$
$0.3 - Ge$

V_f

V_T

FIB.

I_R
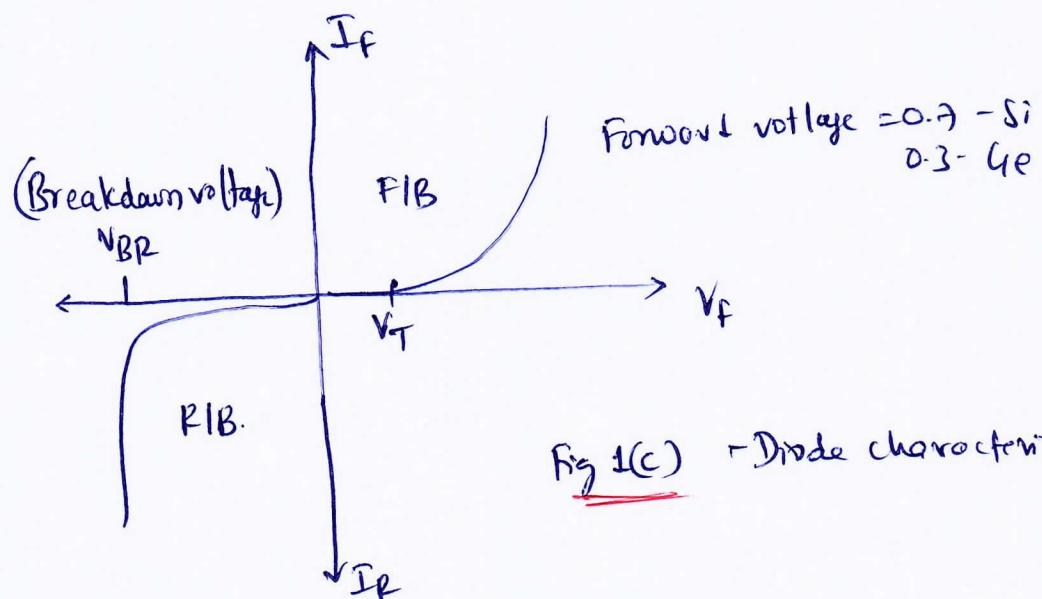
Fig 1(c) — Diode characteristics

Diode symbol

P ▷ N

Fig 1(d) Diode symbol

Jalil

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1.B Explain how zener diode can be used as voltage regulator.   6 Marks

Zener diode accept unregulated DC supply as i/P & provides Constant DC o/P irrespective of changes in the load current & line voltage.
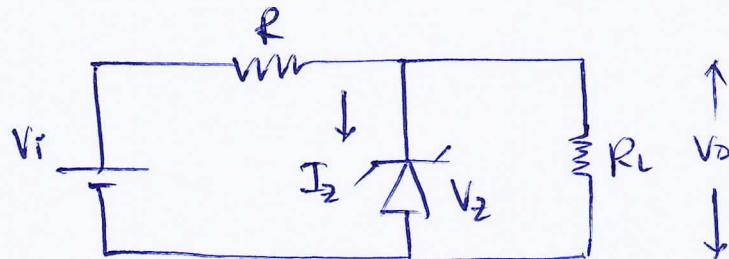

Fig 1 (d) Zener diode as voltage regulator

- Zener diode operates in reverse breakdown region & has Constant voltage V_z across its terminals.
- For zener diode to operate in breakdown, the dc i/p V_i must be greater than the zener breakdown voltage V_z
    i.e $V_i > V_z$

Analysis : Since R_L & zener diode are in Parallel . voltage across R_L = voltage across Zener diode i.e $V_0 = V_z$ – ①

∴ V_0 will be Constant because V_z is Constant.

∴ V_0 will remain Constant even if there is any fluctuations in V_i until $V_i > V_z$ Condition is maintained.

from fig 1(d) $I = I_z + I_L$ – ②

$I_z = I - I_L$ – ③

but $I = \dfrac{V_i - V_0}{R}$ – ④

using ④ in ③ $I_z = \left[\dfrac{V_i - V_0}{R}\right] - I_L$ – ⑤

⑤ represents Current through Zener diode

Considering V_i varies b/n V_{imin} & V_{imax} & I_L varies b/n I_{Lmin} & I_{Lmax} , I_z b/n I_{zmin} & I_{zmax}

we can write $\quad I_{zmin} < I_z < I_{zmax}$ — ⑥

now I_{zmax} — max zener current flows when

$V_i = V_{imax}$

& w.k.т $I = I_z + I_L$

↑

Constant

- if I_z is max I_L will be min such that I is constant

- I_{zmax} flows when $V_i = V_{imax}$

& if I_{zmax} is max then I_L will be minimum

so form ⑥ & ⑤

$$I_z < I_{zmax}$$

$$\left[\frac{V_{imax} - V_o}{R}\right] - I_{Lmin} < I_{zmax} \quad — ⑦$$

Similarly for $I_z > I_{zmin}$

$$\left[\frac{V_{imin} - V_o}{R}\right] - I_{Lmax} > I_{zmin} \quad — ⑧$$

Thus zener diode regulates the current through it using
Conditions ⑦ & ⑧ //

1.C A silicon diode has I_S=10 nA operating at 25°C. Calculate diode current I_D for a forward bias of 0.6 V.   6 Marks

Soln   Let $\eta = 2$

$$T_K = 25° + 273° = 298$$

$$k = \frac{11.600}{2} = 5800$$

$$\frac{kV_D}{T_k} = \frac{5800 \times 0.6}{298} = 11.68$$

$$e^{11.68} = 117930$$

$$\therefore I_D = I_S \left(e^{kV_D/T_k} - 1 \right)$$

$$I_D = 10n \left(117930 - 1 \right) = 1.18mA \; //$$

2.A With a neat circuit diagram, explain the operation of centre-tapped full-wave rectifier. Draw input and output waveforms.   (8 Marks)
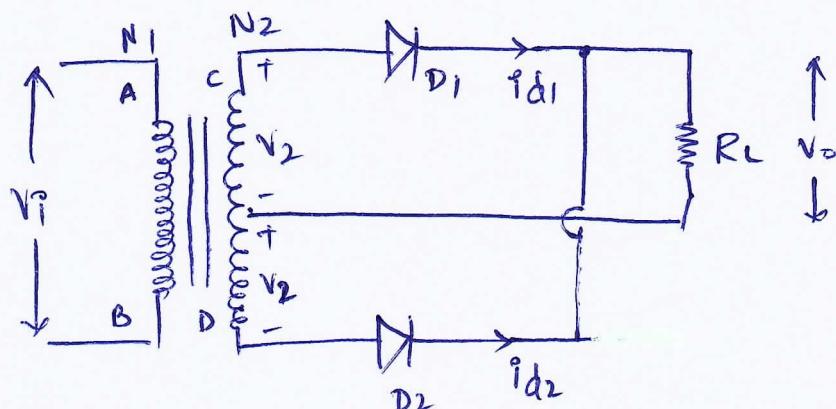
Fig. 2(a) – Centre tapped Full wave rectifier

- Fig 2(a) shows the centre tapped full wave rectifier using two diodes
- A step down transformer is used to reduce the ac to required level.
- Centre tapping is done in the secondary of the transformer to obtain two voltages but of opposite phase.

Positive half cycle – During +ve half cycle of i/p voltage

Diode D1 is forward bias & Diode D2 is reverse bias. In this case the voltage at point C is +ve and voltage at point D is -ve ∴ D1 is flw biased. Hence the current flows only thgh diode D1 & to RL Resulting in o/p voltage Vo.

Negative half cycle – During -ve half cycle of i/p point D is at +ve & point C is at -ve. Therefore diode D2 is forward biased & D1 is reverse biased resulting in a flow of current only thrgh diode D2. & thrgh RL.
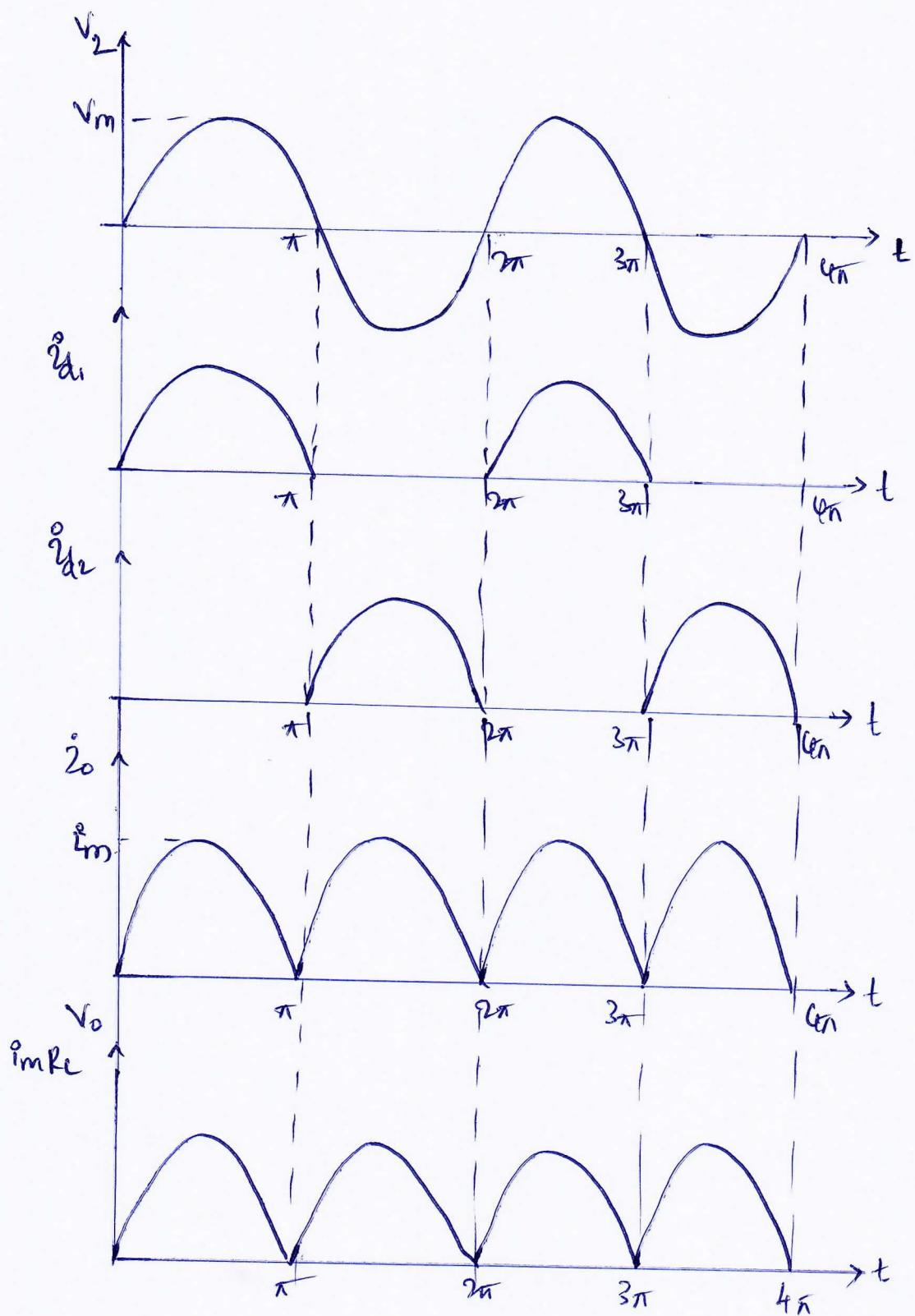
Fig 2 (b) Waveforms of Full wave Centre tap rectifier

2.B Explain photo diode and LED in brief.   (6 marks)

Photo diode — A photodiode is a semiconductor device that converts light into electric current. It is also called photo detector, photo sensor or light detector.

It is a PN junction operated in reverse bias regim as shown in Fig 2(d)
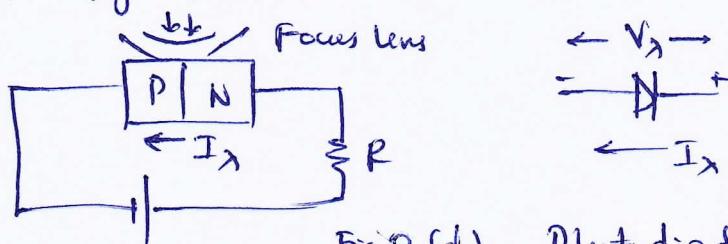

Fig 2.(d) Photo diode in reverse bias

In photo diode the reverse saturation current I_λ is limited by the availability of thermally generated minority carriers. A light is made to impinge on the junction, the light photons impart energy to the valence electrons causing more e^- hole pairs to be released. As a result the concentration of minority carriers increases & so does the current I_λ.
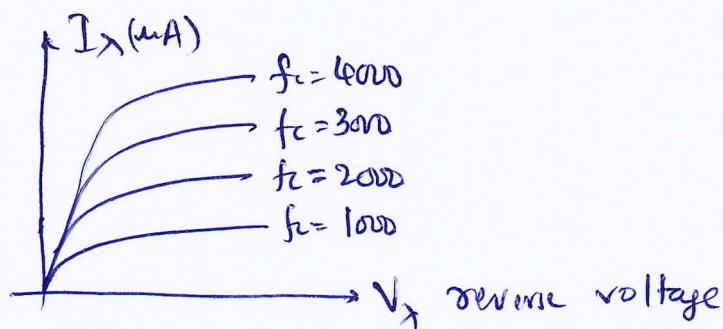

Fig 2(e) V-I characteristics of photo diode

LED -

In forward biased P-N jn, diode, recombination of e⁻ & holes takes place at the junction & within the body of the crystal, particularly at the location of a crystal defect. Upon capture of a free electron by a hole, the electron goes into a new state & its kinetic energy is given off as heat & as light photons. In a Si diode, most of this energy is given off as heat but in other materials such as GaAs or GaP sufficient no. of photons (light) are generated so as to create a visible source.

This process of light emission is known as tight term electroluminescence.
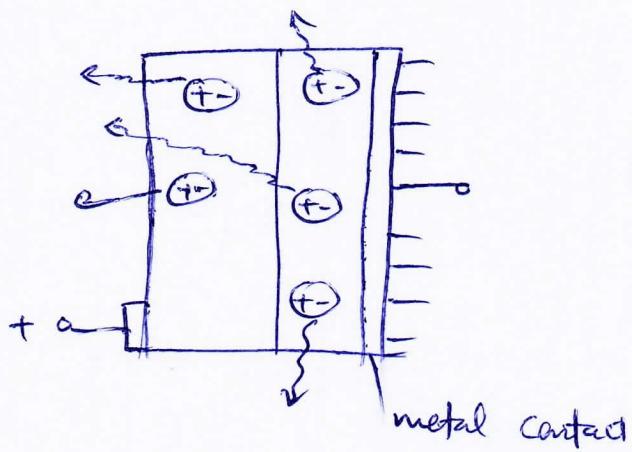
Fig 2 (c) light emission in LED

metal contact

The LM7805 fixed voltage regulator has an o/p voltage of +5V & a max load current of 1A.

LM- linear monolithic

The typical load regulation is 10mV for a load current b/w 5mA & 1·5A. The typical line regulation is 3mV for i/p voltage b/w 7 to 25V.

Ripple rejection ratio is 80dB which means it will reduce i/p-ripple by a factor of 10000.

Rout is approximately 0.01Ω //.

Fig. 2(g) shows 7805 used for voltage regulation.

Bypass capacitor C1 is used to prevent the oscillations in i/p. Bypass capacitor C2 is used to improve the transient response. The typical values of C1 & C2 are 0.1µF to 1µf
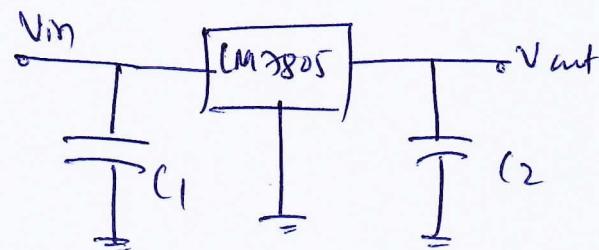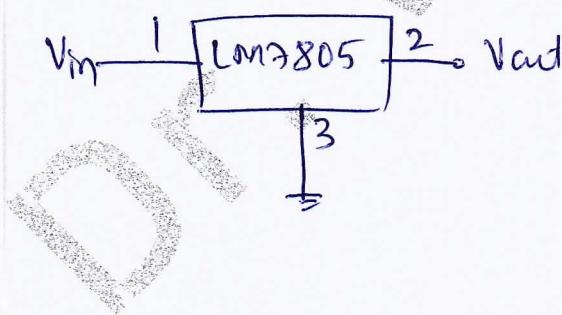

Fig 2(g) 7805 used for voltage regulation

3. A Explain the construction and operation of a N-channel JFET. Draw transfer and drain characteristics.   **8 marks**

Construction
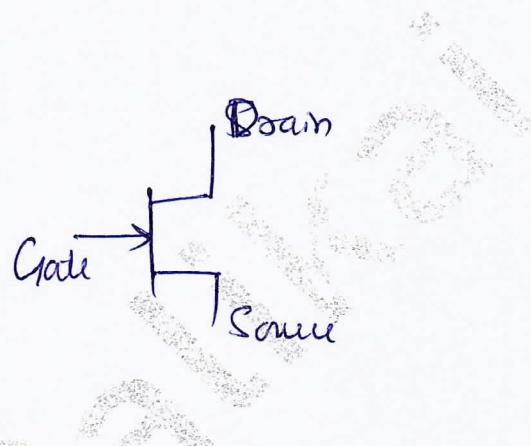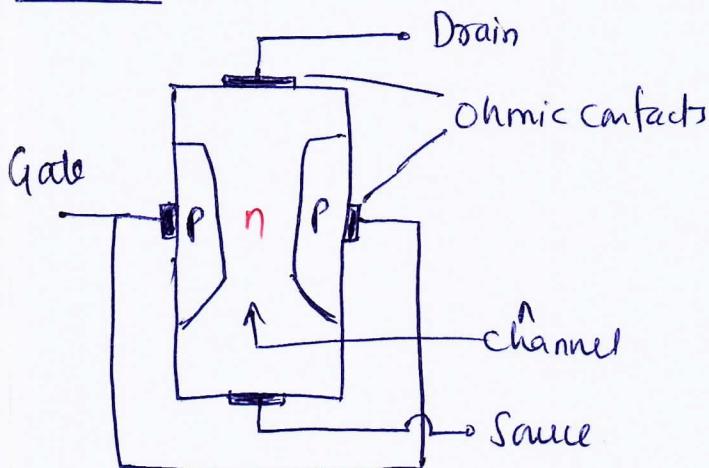
Fig 3 (a) Structure & Symbol of n-channel JFET

Fig 3(a) shows structure & symbol of n-channel JFET. A small bar of extrinsic semiconductor material, of n-type is taken & at its two ends, two ohmic contacts are made which are the drain & source terminals.

- Heavily doped electrodes of p-type material form p-n junctions on each side of the bar. The thin region b/w the two p-gates is called the channel. Since this channel is of n-type or since the channel is in n-type bar, the JFET is known as n-channel JFET.

- The electrons enter the channel through the terminal called source & leave through the terminal drain. The terminals taken out from heavily doped electrodes of p-type material are called gates. Usually these electrodes are & connected together & only one terminal is taken out.

Working

- When voltage is applied betn the drain & Source with DC Supply V_{DS}. electrons flow from source to drain through the narrow Channel which is betn the two depletion regions. This causes a drain current I_D to flow from Drain to Source

- When the gate is shorted to Source as shown below. 3(b) ~~or when no gate voltage is applied, there will no~~ current. there is minimum reverse bias betn gate & Same p-n jⁿ making ~~depletion width region~~ the channel width more, hence more current flow

- When V_{GS} is increased with -ve voltage (i.e $V_{GS}=-ve$) Fig 3(c), the depletion width of p-n jⁿ increases there by reducing the channel width, hence less current flow.

- When V_{GS} is more & more -ve then the two depletion width touches each other making JFET to enter to Cutoff state. ,,
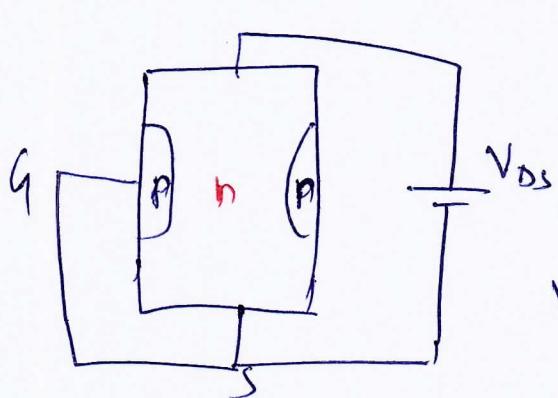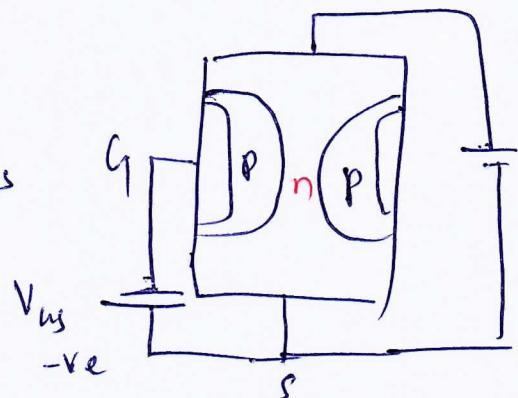

Fig. 3(b)   Fig 3(c)

Working of n-Channel JFET

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3.B Explain the operation of a CMOS inverter.   6 Marks
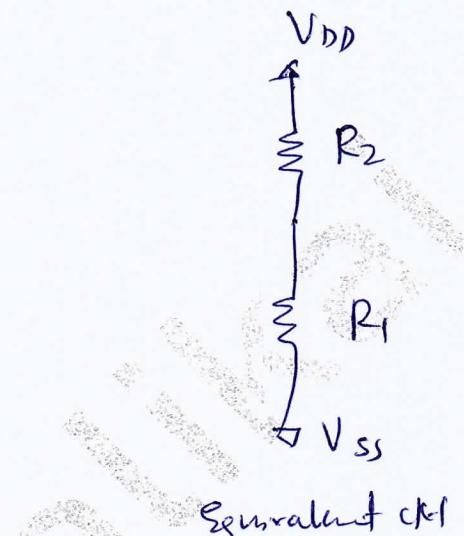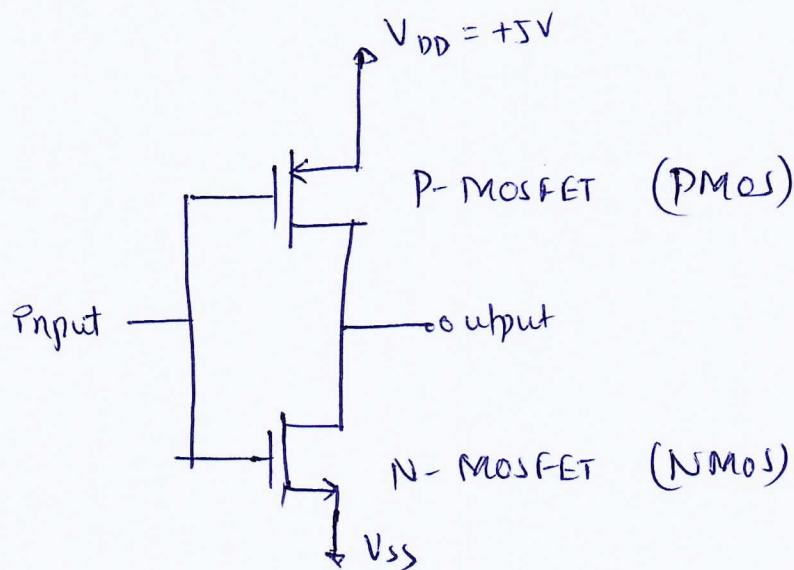
Fig 3(a) CMOS inverter.

Fig 3(a) describes a simple CMOS inverter. Complimentary metal Oxide Semiconductor Field Effect transistor C-MOSFET Inverter Consists of one P-channel MOSFET & N-channel MOSFET. Hence the name Complimentary MOS.

Operation

When i/p is High the gate of PMOS is at logic 0 while the gate of NMOS & is also at logic 0

When logic 0 falls at the gate of PMOS, then PMOS is turned on thereby Creating a channel & as a result PMOS Conducts

under this scenario PMOS is on ∴

$$V_0 = \frac{R_2 \cdot V_{DD}}{R_1 + R_2} \cong V_{DD}$$

∴ $V_0 = +5V$

∴ For $V_{in} = 0, V_0 = +5V$

$V_{in} = $ logic 0

$V_{out} = $ logic 1 //

when i/p is logic 1 then NMOS is turned on & channel is created, as a result NMOS Conducts & resulting in o/p $ OV.

i.e $V_D = \dfrac{R_1 \cdot V_{SS}}{R_1 + R_2}$ & $V_{SS} = 0V$

for $V_{in} = 1$ $V_0 = 0V$

or $V_{in} = logic\ 1$ $V_0 = logic\ 0$ //

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3. A   <u>Continued</u> . . .

Transfer & Drain Characteristics

Fig 3(c) V-I Characteristics — Drain
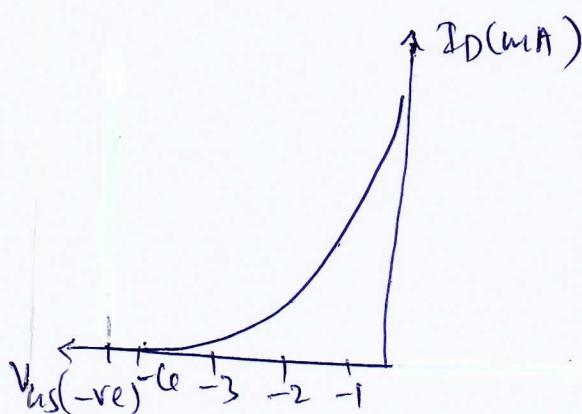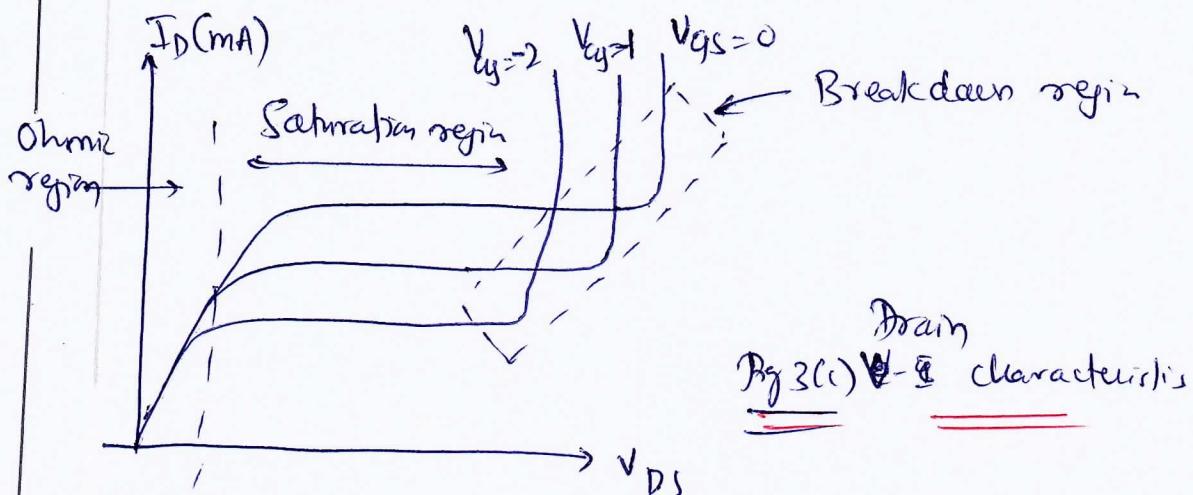
Fig 3(d) Transfer Characteristics of n-JFET

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3. C n-channel JFET has I_{Dss} = 8mA, Vp=-4V. Determine I_D for V_{GS}=-1 and V_{GS}=-2V.

6 Marks

Soln $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$ for $V_{GS} = -1$

$= 8m\left[1 - \dfrac{(-1)}{(-4)}\right]^2 \Rightarrow I_D = 4.5\,mA //$

$I_D = 8m\left[1 - \dfrac{(-2)}{(-4)}\right]^2$ for $V_{GS} = -2$

$I_D = 2m\,A //$

4. A Explain the construction and working of n-channel depletion type MOSFET. 8 Marks
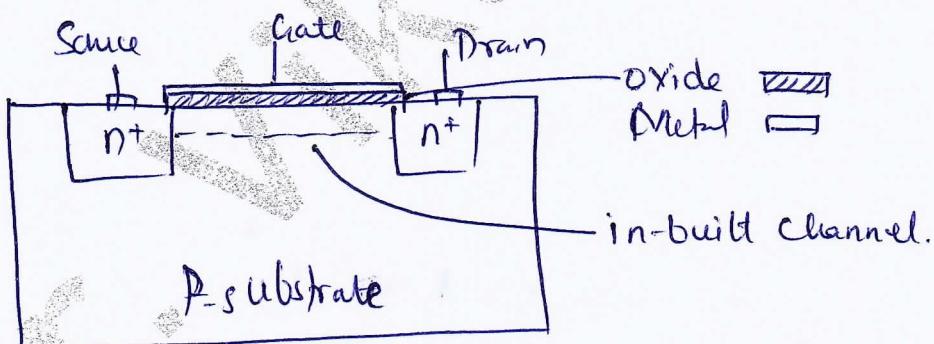
Fig 4(a) n-channel depletion mosfet

Fig 4(a) shows the basic construction of n-channel depletion type mosfet. Two heavily doped n-regions are diffused into a lightly doped p-type substrate. These two heavily doped n-regions represent Source & Drain.

The Source & drain regions are connected through metallic contacts to n- regions.

- The gate is also connected to a metal contact surface but remains insulated from the n channel by very thin dielectric material (SiO_2)

Working

When $V_{GS} = 0V$. V_{DS} = applied

Since there is an in-built channel already present in the MOSFET therefore even there is no V_{GS} being applied the current flows from Source to Drain due to V_{DS}

When $V_{GS} = +ve$ voltage V_{DS} = applied

When V_{GS} becomes +ve then the +ve voltage on gate attracts more & more electrons beneath the oxide layer resulting in a much wider channel. As a result of this more current flows due to increase in the width of the channel.

When $V_{GS} = -ve$

When V_{GS} becomes -ve then the channel width reduces as the -ve charges on the gate repels the negative charges from gate due to which the channel width reduces. Hence the current flow is minimized.
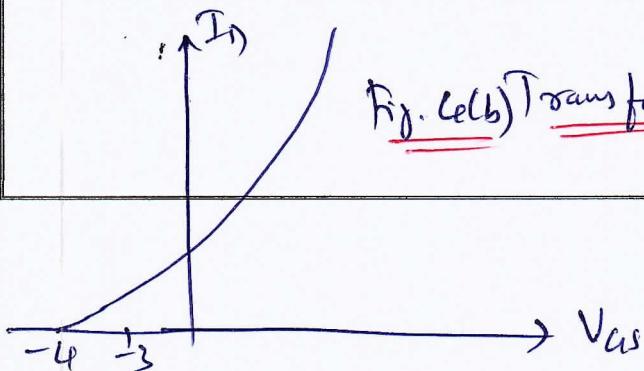
Fig. (e(b)) Transfer Characteristics of n-channel MOSFET

Explain Working of Silicon Controlled Rectifier using 2-T model

Soln SCR is a switching device widely used in power Control applications. The basic operation of an SCR can be best explained by splitting the 4-layer PNPN structure into two-three layer structure as shown in Fig 20.

G marks
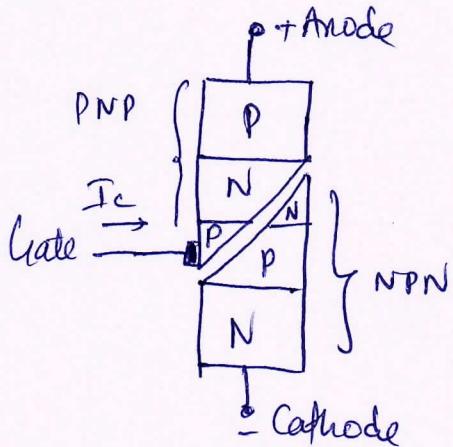
Fig 4(c) Cross sectional view
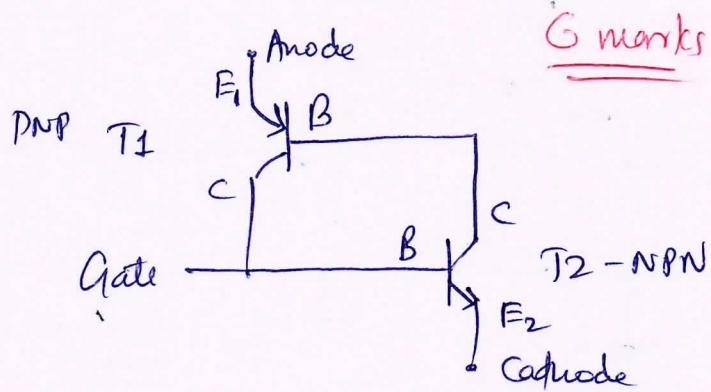
Fig 4(d) Equivalent ckt

Thus the equivalent ckt of SCR is composed of pnp transistor & npn transistor as seen in Fig 20.

Switching action (operation)

Let a positive voltage V be applied to the anode (E1) & let the cathode (E2) & gate (G) be both grounded as shown in fig 4(d)

As $V_G = V_{BE2} = 0$ the transistor T2 is in Off state. It means that the C-B jn of T2 through E-B jn of T1 is R/B. Therefore $I_{B1} =$ very low or no base current hence the anode current $I_A = I_{B1} = 0$. Thus making SCR to off.

Now let $V_G > 0$ be applied at gate. As $V_{BE2} = V_G$ when V_G is sufficiently large I_{B2} will cause T2 to turn ON & I_{C2} becomes large. As $I_{B1} = I_{C2}$, T1 turns on causing I_{C1} to flow. this inturn increases I_{B2} causing a regenerative action. As a result SCR turns ON

So/n

The mechanism of turning off the SCR is called Commutation

Natural Commutation

The natural Commutation is also called as line Commutation because it uses supply line voltage for turning off SCR.

- The supply voltage naturally passes through zero due to which current through SCR becomes zero at the instant when line voltage becomes zero.

- As current flows through SCR becomes zero, the SCR naturally turns off.

- After passing through zero, the ac voltage becomes negative which appears across the SCR & it does not conduct.

Forced Commutation

- The forced Commutation is used when supply is DC

- This Commutation requires external ckt which is connected across SCR.
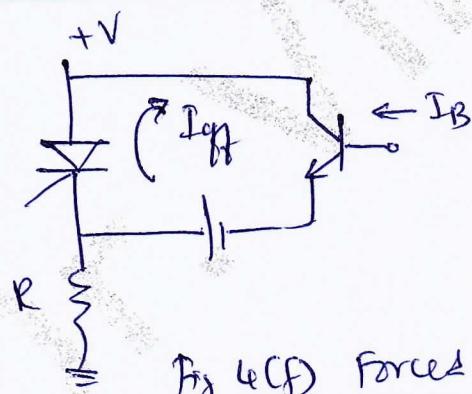
Fig 4(f) Forced Commutation mechanism

The current through SCR is forced to become zero by passing a current in opposite direction using external ckt.

- When SCR conducts $I_B = 0$ & $Q_1 = off$.

- To turn off SCR +ve pulse is applied to base of Q_1 which drives Q_1 in saturation & circulates high current I_{off}

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MODULE 03

5. A Explain the following terms related to op-amp: (i) CMRR (ii) Input Offset Voltage (iii) Slew rate. Also mention op-amp ideal characteristics.   8 Marks

Soln

CMRR – The ability of an opamp to reject a common mode signal is expressed by a ratio known as Common mode rejection ratio.

$$CMRR = \frac{\text{differential voltage gain } (A_d)}{\text{Common mode gain } (A_c)} = 20 \log \left| \frac{A_d}{A_c} \right| dB$$

- Practically CMRR value is very large
- ideally CMRR is ∞.

Input offset voltage – whenever both the i/p terminals of the opamp are grounded, the o/p must be zero ideally. However, in practical reality there exists a small offset value at the o/p.

- To make this o/p value to zero, a small voltage is applied at the i/p. & This voltage makes o/p to zero.
- This dc i/p voltage which makes o/p zero ~~when~~ is known as i/p offset voltage

Slew rate – Maximum rate of change of output voltage with time $S = \left. \dfrac{dV_0}{dt} \right|_{max}$ V/µsec

opamp ideal Characteristics
1) Infinite i/p impedance   3) Infinite CMRR   5) Infinite Slew rate
2) Zero o/p impedence   4) Infinite B/w   6) Infinite gain //

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5. B A certain op-amp has an open loop voltage gain of 1,00,000 and a common mode gain of 0.2. Determine the CMRR and express it in decibels   **6 Marks**

Soln   given $A_d = 100000 = \phi$

$A_c = 0.2$

$$CMRR = \frac{A_d}{A_c} = 20\log\left(\frac{A_d}{A_c}\right) \, dB$$

$$20\log\left(\frac{100000}{0.2}\right) = 114 \, dB \, //$$

5 C. Explain opamp integrator   **6 Marks**
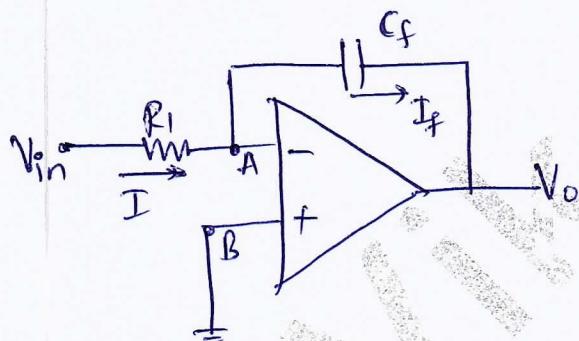
Fig 5(a)   opamp integrator

Fig 5(a) depicts the opamp integrator.

Applying KCL.

$I_1 = I_f$ Since no current enters opamp due to high i/p resistance

$$I_1 = \frac{V_{in} - V_A}{R_1} \quad —① \qquad I_f = \frac{d(V_A - V_0)}{dt} \cdot C_f \quad —②$$

$$\frac{V_{in} - V_A}{R_1} = \frac{d(V_A - V_0)}{dt} C_f$$

due to concept of virtual ground $V_A = V_B = 0$

$$\therefore \frac{V_{in}}{R_1} = -\frac{dV_0}{dt} \cdot C_f \quad \Rightarrow \quad \frac{dV_0}{dt} = \frac{-V_{in}}{R_1 C_f}$$

$$\int_0^t \frac{dV_0}{dt} = \int_0^t \frac{V_{in}}{R_1 C_f} \quad \Rightarrow \quad V_0 = \frac{-1}{R_1 C_f}\int_0^t V_{in}$$

(21)
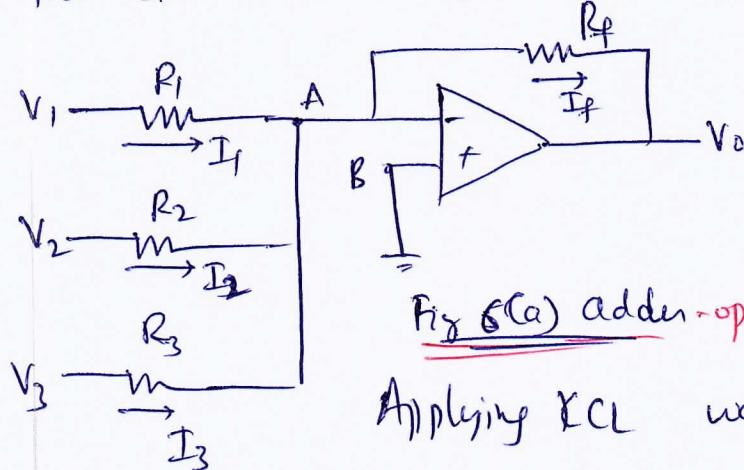
6. A Wth neat circuit, explain the operation of three input adder circuit. Derive expression for Vo.   8 marks

So$|^n$ In this ckt all the i/p signals to be added are applied to the inverting i/p terminal of the opamp.

- The ckt with 3 i/p is as shown below.

Fig 6(a) adder-opamp

Here V_1, V_2 V_3 are 3 i/p, R_1 R_2 R_3 are the 3 resistances.

R_f - feedback resistance

Applying KCL we have $I_1 + I_2 + I_3 = I_f$ — ①

$I_1 = \dfrac{V_1 - V_A}{R_1}$ — ② $I_2 = \dfrac{V_2 - V_A}{R_2}$ — ③ $I_3 = \dfrac{V_3 - V_A}{R_3}$ — ④

but from the concept of virtual ground $V_A = V_B = 0$

∴ $V_A = 0$ ⟹ $I_1 = \dfrac{V_1}{R_1}$ $I_2 = \dfrac{V_2}{R_2}$ $I_3 = \dfrac{V_3}{R_3}$

① ⟹ $\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3} = \dfrac{V_A - V_0}{R_f}$ ⟹ $\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3} = \dfrac{-V_0}{R_f}$

$$\boxed{V_0 = -R_f \left[\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3} \right]}$$

if $R_1 = R_2 = R_3 = R$ then $\boxed{V_0 = \dfrac{-R_f}{R}\left(V_1 + V_2 + V_3\right)}$ — ⑤

⑤ indicates addition of voltages in opamp adder //

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6 B. A non-inverting amplifier has closed loop gain of 25. If input voltage Vi=10mV,

Rf =10kΩ, determine the value of R1 and output voltage Vo   6 Marks

Soln

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{in} \quad —\text{①}$$

given $R_f = 10k$ $\frac{V_0}{V_{in}} = 25$ $V_i = 10m$

$$\therefore \frac{V_0}{V_{in}} = 1 + \frac{R_f}{R_1} \quad —\text{②}$$

from $\frac{V_0}{V_{in}} = 25 \Rightarrow \frac{V_0}{10m} = 25$

$$\boxed{V_0 = 250mV}$$
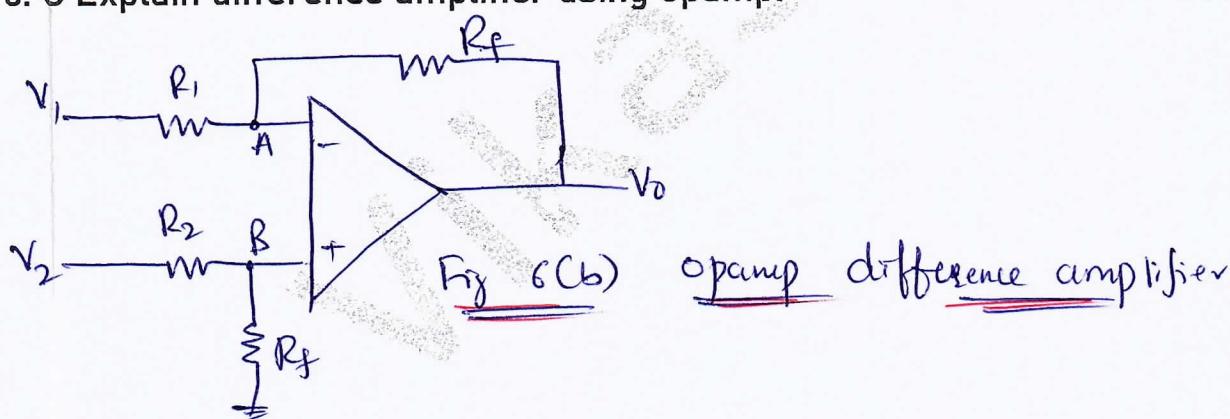
$$\text{②} \Rightarrow \frac{\cancel{250mV}^{25}}{} = \left(1 + \frac{10k}{R_1}\right) \Rightarrow 24 = \frac{10k}{R_1}$$
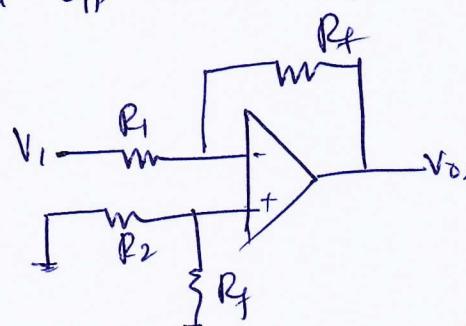
$$\therefore R_1 = \frac{10k}{24} \Rightarrow \boxed{R_1 = 416.6\,\Omega}$$

**6. C Explain difference amplifier using opamp.   6 Marks**

Fig 6(b) opamp difference amplifier

Applying superposition theorem
let V_{01} be the o/p with input V_1 acting alone assuming V_2
to be zero
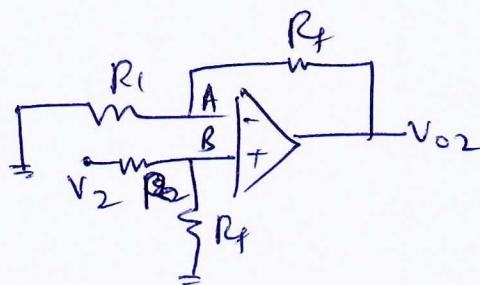
$$V_{01} = -\frac{R_f}{R_1} V_1 \quad —\text{①}$$

under this scenario the
ckt behaves as inverting amplr

let V_{o2} be o/p with V_2 alone acting

then

Here the ckt behaves as non-inv amplifier

with $V_{o2} = V_B \left(1 + \dfrac{R_f}{R_1}\right)$ — ②

now $\quad V_B = \dfrac{V_2 \cdot R_f}{R_2 + R_f}$ — ③

use ③ in ②

$$V_{o2} = V_2 \left(\frac{R_f}{R_2 + R_f}\right)\left(1 + \frac{R_f}{R_1}\right) \Rightarrow V_{o2}\left(\frac{R_f}{R_2 + R_f}\right)\left(\frac{R_1 + R_f}{R_1}\right)$$

$$\quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad L ④$$

① + ④ $\Rightarrow V_o = -\dfrac{R_f}{R_1} V_{.1} + V_2\left[\dfrac{R_f}{R_2 + R_f}\right]\left[\dfrac{R_1 + R_f}{R_1}\right]$

if all resistances are selected as $R_1 = R_2$ then

$$V_o = -\frac{R_f}{R_1} V_{.1} + V_2 \left[\frac{R_f}{R_2 + R_f}\right]\left[\frac{R_2 + R_f}{R_1}\right]$$

$$V_o = -\frac{R_f}{R_1} V_{.1} + V_{.2} \frac{R_f}{R_1}$$

$\therefore \quad V_o = \dfrac{-R_f}{R_1}\left(V_{.1} + V_{.2}\right)$

$$V_o = \frac{R_f}{R_1}\left(V_{.2} - V_1\right) \quad //$$
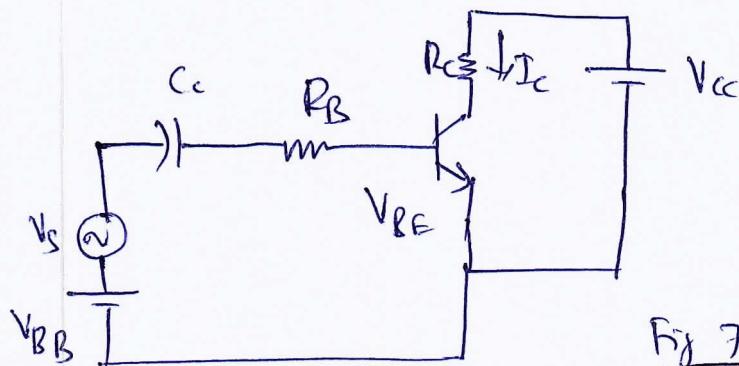
MODULE 04

7.A With neat circuit, explain transistor as an amplifier. Derive the expression for voltage gain.   **8 Marks**

Sol? Considering npn transistor in Common emitter Configuration the ckt for BJT as amplifier is as shown in Fig 7(a)

BJT amplify current because the collector current is equal to the base current multiplied by β.

Fig 7(a) BJT as amplifier

The base current in transistor is very small compared to the collector current & emitter current. Because of this the collector current is approximately equal to emitter current.

Fig 7(a) shows basic tx amplifier ckt with Vs as ac i/p & VBB as DC bias voltage. Capacitance Cc acts as ~~easy~~ DC block for the BJT. RB is base resistor Rc – collector resistor.

The B-E jn has very low resistance to ac signal. This internal resistance is denoted by r_e' & appears in series with RB. The ac base voltage is

$$V_b = I_e r_e' \quad -①$$

Since $I_c \approx I_e$

$$V_c = I_e R_c \quad -②$$

$$V_b = V_s - I_b R_B \quad -③$$

$$A_v = \frac{V_c}{V_b} \approx \frac{I_e R_c}{I_e r_e'} \quad \therefore \boxed{A_v = \frac{R_c}{r_e'}} \quad //$$

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7.B Mention types of feedback amplifier. With block diagram, explain voltage series feedback amplifier   **8 Marks**

Soln   Types of feedback amplifier

- Voltage amplifier
- Current amplifier
- Transconductance amplifier
- Transimpedence amplifier.

<u>voltage series feedback amplifier</u>
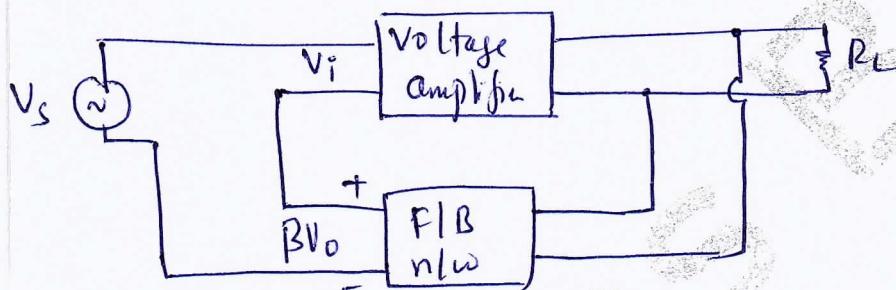
Fig 7(b) – Voltage-Series feedback amplifier

V_i - i/p to voltage amplifier V_s - i/p to feedback amplifier.
V_0 - o/p voltage

$$V_i = V_{in} - \beta V_0 \quad - \text{①} \quad - \text{after feedback i/p becomes}$$

W.K.T $V_0 = A V_i \quad - \text{②}$

Substitute ① in ②

$$V_0 = A (V_{in} - \beta V_0)$$

$$V_0 = A V_{in} - A\beta V_0$$

$$A V_{in} = V_0 + A\beta V_0 \quad \Rightarrow \quad V_0(1 + A\beta) = A V_{in}$$

$$\boxed{\frac{V_0}{V_{in}} = \frac{A}{1 + A\beta}} \quad \text{- gain of voltage series f/b amplifier //}$$

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7. C A negative feedback amplifier has gain A =1000 and bandwidth of 200kHz. Calculate gain and bandwidth with feedback if feedback factor β=20%   6 Marks

Soln $A = 1000$

$B/w = 200kHz$

$\beta = 20\% = 0.2$

$A_f = \dfrac{A}{1 + A\beta} = \dfrac{1000}{1 + (1000)(0.2)} = 4.975 \,//$

B/w with feedback $f_{H_f} - f_{L_f}$

$f_{H_f} = (1 + A\beta)f_H$ $f_{L_f} = \dfrac{f_L}{(1 + A\beta)}$

$f_{H_f} = 1 + (1000)(0.2)f_H \Rightarrow 201 f_H$ —②

$f_{L_f} = \dfrac{f_L}{1 + (1000)(0.2)} = \dfrac{f_L}{201}$ —①

B/w with feedback = ② − ① ⇒ $201 f_H - \dfrac{f_L}{201}$

$(B/w)_f = \dfrac{201 \times 201 \, f_H - f_L}{201}$
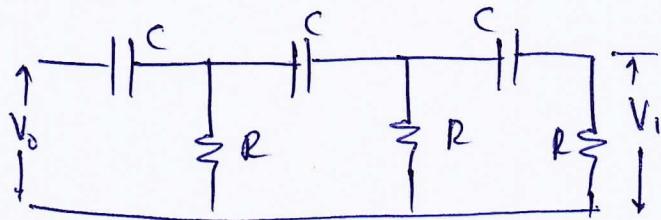
$(B/w)_f = \dfrac{40401 \, f_H - f_L}{201} \,//$

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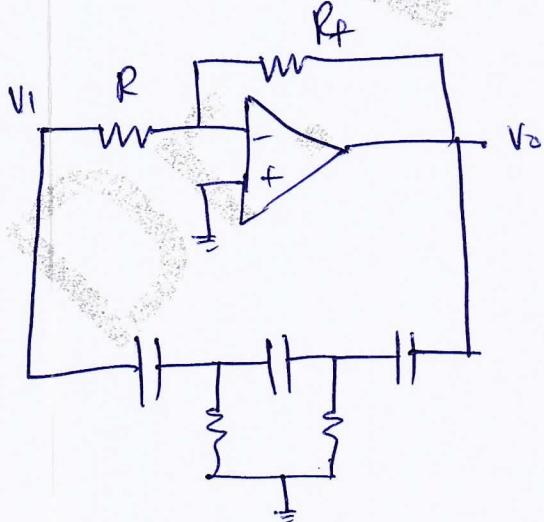
8. A What is phase shift oscillator? Explain with circuit RC phase shift oscillator.

8 Marks

A phase shift oscillator is an oscillator which produces the o/p based on the phase shifts that occur in the ckt. RC phase shift oscillator is a simple phase-shift oscillator that uses 3 RC sections in its feedback using opamp in inverting mode to give a ~~phase~~ total phase shift of 180°. thus generating the oscillations.

- Each RC section produces 60° phase shift hence the total phase shift introduced by the f/b path is 180°.

- To satisfy the Barkhausen criteria, the amplifier path must introduce 180° phase shift in forward path. Thus total phase shift becomes 360°.

- The opamp in inverting mode is used here. to get 180° phase shift.

The freq of oscillation will be $\omega_0 = \dfrac{1}{RC\sqrt{6}}$
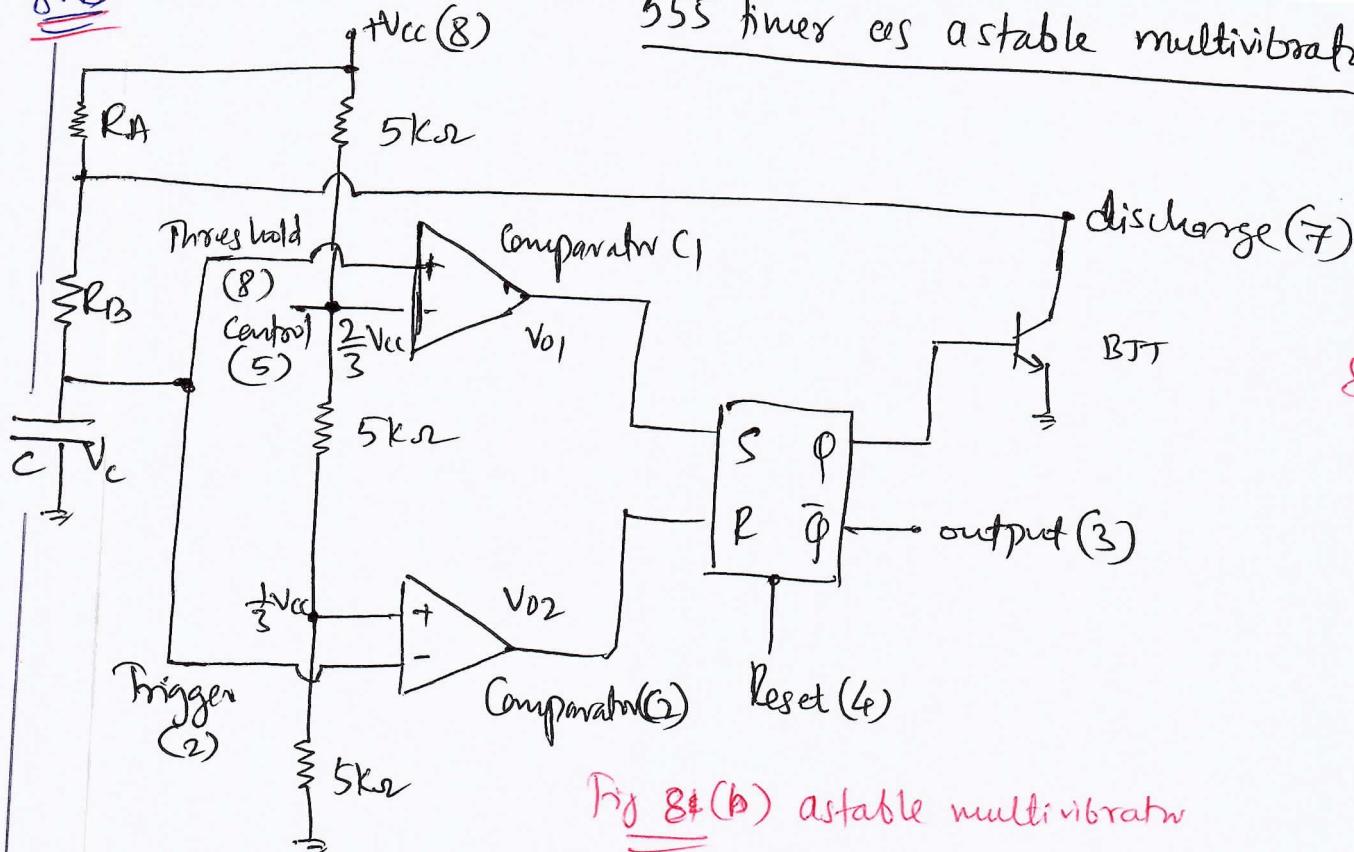
i.e $f_0 = \dfrac{1}{2\pi RC\sqrt{6}}$ //

$|A\beta| = 1$ $\therefore$ $(A) = \dfrac{1}{(\beta)} = 29$. The gain must be 29.

$\therefore$ $|A| = \dfrac{R_f}{R} = ~~\cancel{28}~~ 29$ // $R_f \geqslant 29R$ //

555 timer as astable multivibrator

+Vcc (8)

RA   5kΩ

Threshold   Comparator C1

(8)   Vo1

RB   Control $\frac{2}{3}$Vcc
(5)

discharge (7)

BJT

$\overline{C}$|Vc   5kΩ

8 marks

$\frac{1}{3}$Vcc   +   Vo2

S   Q
R $\overline{Q}$ output (3)

Trigger   Comparator C2   Reset (4)
(2)

5kΩ

Fig 8.(b) astable multivibrator

- Here trigger & threshold are tied together.
- Initially we assume Capacitor C = 0. (no charge)

When C=0, for Comparator C2   -ve terminal at 0V
                                +ve terminal at $\frac{1}{3}$Vcc

Hence Vo2 = +Vcc = logic 1. ∴ R = 1

This makes o/p & S-R flip flop Q = 0 or $\overline{Q}$ = 1

- Once Q = 0, the BJT is off. & it behaves as open
Switch.

- Because the Capacitor is initially empty, now it starts to
Charge through RA & RB from Vcc.

- The Capacitor Charges till $\frac{2}{3}$Vcc, & as soon as the
Capacitor charge goes above $\frac{2}{3}$Vcc, the Comparator 1
will do the comparison.

8. C An astable multivibrator circuit has R1=6.8kΩ, R2=4.7kΩ, C=0.1uF. Calculate frequency of oscillation and duty cycle　　　　　　6 Marks

Sol^n　$f = \dfrac{1}{0.693(R_A + 2R_B)C}$

given　$R_1 = R_A = 6.8K$　　$R_2 = R_B = 4.7K$　　$C = 0.1uf$

∴　$f = \dfrac{1}{0.693(6.8K + 2(4.7K))0.1u}$

$f = \text{1112×10}^{-3}$　$890.7\ Hz$ //

---

9. (a)

Continued...

(iii)　$(101111.101)_2 = (?)_8 = (?)_{10}$

Considering binary no.　|　Considering binary no.

$101\ 111.\ 101$　　　　|
$(5\ 7.\ 5)_8$ //　　　　　|　$1\times 2^5 + 0\times 2^4 + 1\times 2^3 + 1\times 2^2 + 1\times 2^1 + 1\times 2^0 . 1\times 2^{-1} +$
　　　　　　　　　　　　|　　　　　　　　　$0\times 2^{-2} + 1\times 2^{-3}$

　　　　　　　　　　　　$= (32 + 0 + 8 + 4 + 2 + 1).(0.5 + 0 + 0.125)$

　　　　　　　　　　　　$= 47.625$ //

(50)

9   a.   Convert :

  i) $(2467.125)_{10} = (?)_2 = (?)_{16}$

  ii) $(765.16)_8 = (?)_{10} = (?)_2$

  iii) $(101111.101)_2 = (?)_8 = (?)_{10}.$

                                                                8 Marks

Soln $(2467.125)_{10}$

(i)

2	2467
2	1233 – 1
2	616 – 1
2	308 – 0
2	154 – 0
2	77 – 0
2	38 – 1
2	19 – 0
2	9 – 1
2	4 – 1
2	2 – 0
	1 – 0

$0.125 \times 2 = 0.25 \quad - 0$

$0.25 \times 2 = 0.5 \quad - 0$

$0.5 \times 2 = 1.0 \quad \rightarrow 1$

$\therefore (2467.125)_{10} = 10011010011.001$ //

$10011010\ 0011.001$

$(9A3.2)_H$ //

_____

(ii) $(765.16)_8 = (?)_{10} = (?)_2$

$7 \times 8^2 + 6 \times 8^1 + 5 \times 8^0 . 1 \times 8^{-1} + 6 \times 8^{-2}$

$(7 \times 64) + (6 \times 8) + (5 \times 1) . \frac{1}{8} + \frac{6}{64}$

$448 + 48 + 5 . 0.21875$

$(501.21875)_{10}$ //

taking octal no.

$(111\ 110\ 101.001\ 110)_2$ //

9.B Explain full adder using truth table and expression. Implement sum and carry expressions. **6** Marks

Sol) Full adder is a combinational ckt that performs arithmetic sum of three i/p bits. It consists of 3 i/p & 2 o/p. Two of the i/p variables are denoted by A & B represent two significant bits to be added. The third i/p C_{in} represents the carry from the previous lower significant position.

I/P

A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Sum = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C_{in}} + A\bar{B}\bar{C_{in}} + ABC_{in}$$

$$\Rightarrow C_{in}(\bar{A}\bar{B}+AB) + \bar{C_{in}}(\bar{A}B+A\bar{B})$$

$$\Rightarrow C_{in}(\overline{A\oplus B}) + C_{in}(A\oplus B)$$

Let $A\oplus B = X$

$$Sum = C_{in}\bar{X} + C_{in}X$$
$$= C_{in}\oplus X$$

resubstitute X

$$\therefore \boxed{Sum = C_{in} + A\oplus B \quad or \quad A\oplus B\oplus C_{in}}$$
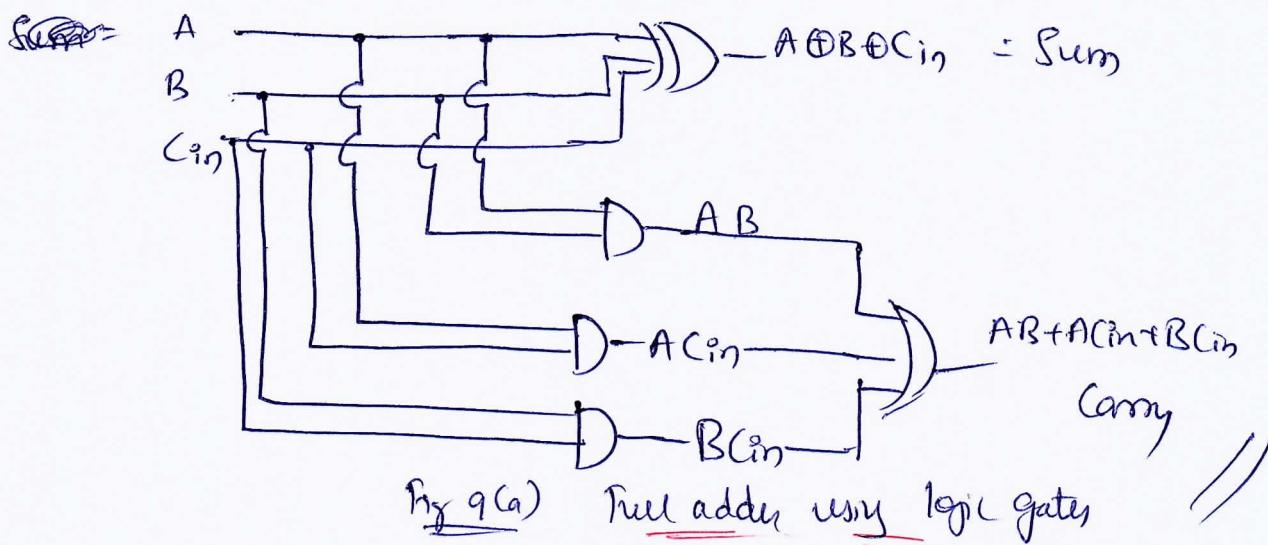
Carry: $\bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$= \bar{A}BC_{in} + ABC_{in} + A\bar{B}C_{in} + ABC_{in} + AB\bar{C}_{in} + ABC_{in}$ $\Leftarrow \because A+A=A$

$= BC_{in}(\bar{A}+A) + AC_{in}(\bar{B}+B) + AB(\bar{C}_{in}+C_{in})$

$= BC_{in} + AC_{in} + AB$

logic diagrams

$A \oplus B \oplus C_{in}$ = Sum

AB

AC_{in}

BC_{in}

$AB + AC_{in} + BC_{in}$
Carry

Fig 9(a)   Full adder using logic gates

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9. C Implement half adder using NAND gates.   8 Marks
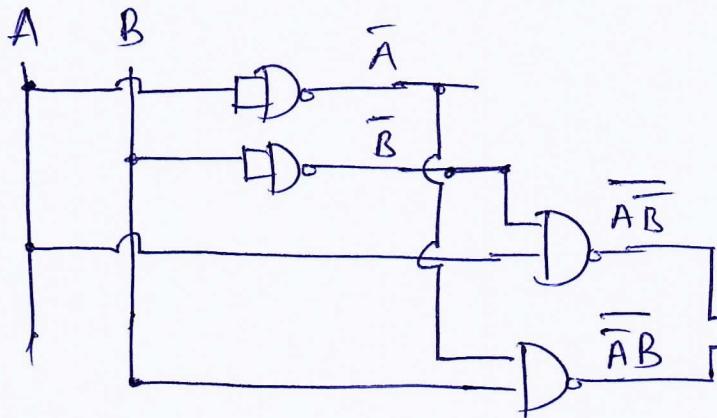
Sum = $A \oplus B$ = $\bar{A}B + A\bar{B}$

Carry = AB

Sum = $A\bar{B} + \bar{A}B$

$\overline{Sum}$ = $\overline{A\bar{B} + \bar{A}B}$ = $\overline{A\bar{B}} \cdot \overline{\bar{A}B}$
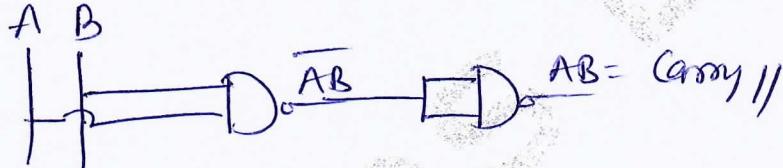
Sum = $\overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}$

$\overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}$ = $A\bar{B} + \bar{A}B$ //

Fig 9(b) – Half adder using nand gates

Carry =

AB = Carry //

10. A State and prove DeMorgan's theorems for 2 variables.

Sol^n

Theorem 1 - $\overline{AB} = \overline{A} + \overline{B}$

The Compliment of a product is equal to the sum of their individual Compliments

Theorem 2 - $\overline{A+B} = \overline{A}\,\overline{B}$

The Compliment of a sum is equal to the product of the Compliments

A	B	$\overline{A}$	$\overline{B}$	A.B	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

Hence proved //
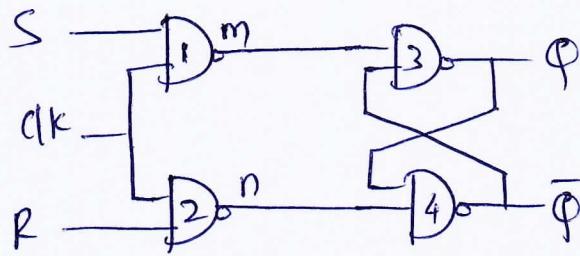
A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$	A+B	$\overline{A+B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

Hence proved //

10. B With the help of a logic diagram and truth table, explain the operation of an SR flip-flop

6 Marks

Soln

Fig 10(a) S-R-flip flop

S	R	Q	$\bar{Q}$
0	0	No change	
0	1	(Reset) $Q=0$ $\bar{Q}=1$	
1	0	(Set) $Q=1$ $\bar{Q}=0$	
1	1	Forbidden	

nand

A	B	o/p
0	0	1
0	1	1
1	0	1
1	1	0

Case (i)   S=0 R=1   Clk=1

When S=0   o/p of gate ① ⇒ m = 1

R=1   o/p of gate ② ⇒ n = 0

& for gate ④ one of the i/p is n=0

∴ o/p of gate ④ $\bar{Q} = 1$

for gate ③ & the i/ps are 1 & 1 ∴ $Q = 0$

∴ ⌐For S=0 R=1 $Q=0$ $\bar{Q}=1$⌐

Case (ii)   S=1 R=0 clk=1

gate ① S=1 o/p of gate ① ⇒ m= 0

R=0 o/p of gate ② ⇒ n = 1

For gate ③ one of the i/p is 0 i.e m=0 hence $Q=1$

for gate ④ the i/p are 1 & 1 ∴ $\bar{Q} = 0$

for ⌐S=1 R=0 $Q=1$ $\bar{Q}=0$⌐

Case (iii)   S=0 R=0 clk=1 & previous value of $Q=1$ $\bar{Q}=0$

gate ① ⇒ 1   gate ② ⇒ 1   gate ③ ⇒ $\begin{matrix}m=1\\\bar{Q}=0\end{matrix}$ } $Q=1$
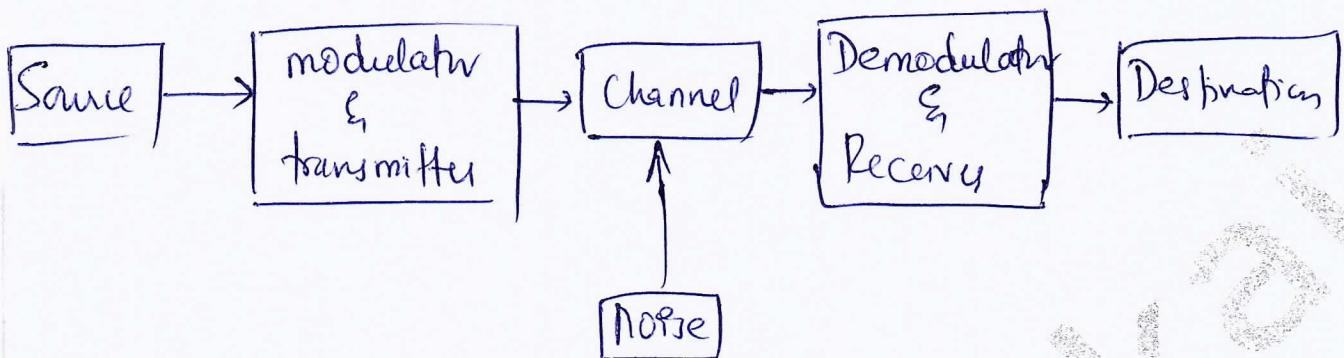
   m=1   n=1

gate ④ ⇒ n=1 } $\bar{Q}=0$

$\bar{Q}=0$

∴ for S=0 R=0 $Q=\bar{Q}$ = previous state.

//

Source → modulator & transmitter → Channel → Demodulator & Recever → Destination

Noise → Channel

Fig 10 (b) Communication System

Source - The aim of the Communication System is to convey a message & this message originates from Source. Common examples of Source are analog audio, video or some digital data

Modulator & transmitter :- It processes the message signal & this message signal is transmitted. The modulator makes sure that the information content is made to sit on carrier signal & can be reached to a longer distance.

Channel : It is a medium through which the information is transmitted Ex Air, optical Cables, Pair of Conducting wires etc

Noise :- During the transmission, Sometimes unwanted energy gets added to the information & it hampers the quality of the signal. Such a Signal is known as noise

Demodulator & Recever :- Performs the reverse action as that of modulator. It extracts the actual information content from the Carrier signal & sends it for reception, which is received by the receiver //.