



Karnatak Law Society's
Vishwanathrao Deshpande Institute of Technology, Haliyal
 (Approved by AICTE, New Delhi. Affiliated to VTU, Belagavi)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

10TH July 2021

ACTIVITY REPORT

BRIEF REPORT ON

“AN OVERVIEW OF PCB INDUSTRY: CONCEPT TO MANUFACTURING”

PROCEEDINGS	DESCRIPTION
EVENT TITLE:	AN OVERVIEW OF PCB INDUSTRY: CONCEPT TO MANUFACTURING
GUEST SPEAKER:	AMIT SOMANAGOUDAR, APPLICATION ENGINEER SIEMENS EDA, BANGALORE
EVENT DATE:	10TH JULY 2021
EVENT TIME:	11:30 AM TO 01:30 PM
EVENT DURATION:	1HR 30 MIN
TARGET AUDIENCE:	4th & 6th Semester
PLATFORMS:	GOOGLE MEET
MEET LINK:	<u>LINK:</u> Video call link: https://meet.google.com/akw-nztk-vep Or dial: (US) +1 304-918-0441 PIN: 946 204 465#
EVENT CO-ORDINATORS:	PROF. PLASIN DIAS & PROF. VINAY CHITARE, ALUMNI CO-ORDINATORS, DEPARTMENT OF E&CE
MASTER OF CEREMONY & WELCOME ADDRESS:	PROF. VINAY CHITARE
INTRODUCTION OF GUEST SPEAKER:	PROF. PLASIN DIAS
ADDRESS BY GUEST SPEAKER (PRIME HIGHLIGHTS):	1. Illustrated PCB Design Layout 2. Importance of System Integrity 3. Career Opportunities in Core Company 4. Emphasized on Basic Concepts related to Circuit Analysis
PRESIDENTIAL REMARKS:	DR. MAHENDRA M. DIXIT, HOD, DEPARTMENT OF E&CE
VOTE OF THANKS:	PROF. PLASIN DIAS
TOTAL NUMBER OF PARTICIPANTS:	80+
OUTCOME OF WEBINAR:	Conceptual understanding of PCB Design Layouts and Career Opportunities in core Companies
BRIEF BIODATA OF RESOURCE PERSON:	ENCLOSED
TOPICS COVERED:	ENCLOSED
LIST OF PARTICIPANTS:	ENCLOSED
EVENT SNAPSHOTS:	ENCLOSED

**Prof. Plasin Dias,
 Prof. Vinay Chitare,
 Alumni Co-Ordinators,
 E&CE Department,
 KLS VDI T, Haliyal**

**Dr. Mahendra M. Dixit,
 HOD, E&CE Department,
 Dean (R&D),
 KLS VDI T, Haliyal**



Karnatak Law society's
Vishwanathrao Deshpande Institute of Technology, Haliyal



Department of Electronics and Communication Engineering



In Association with IEI Students' Chapter

Alumni Talk Series #6

An Overview Of PCB Industry: Concept To Manufacturing



Resource Person

AMIT SOMNAGOUDAR,

Application Engineer,
Siemens EDA, Bangalore

Our Proud Alumni
2007-2011 Batch



Target audience
4th & 6th Sem

Live on



Google Meet

Free Registration

Date : 10 July 2021 , Time : 11:30AM - 12:30PM

Prof Plasin Dias
Prof Vinay Chitare
Alumni Co-ordinators

Dr. Mahendra M. Dixit
HoD, E&CE

Dr. V. A. Kulkarni
Principal

BRIEF BIODATA OF RESOURCE PERSON

Amit Somanagoudar, Application Engineer Siemens EDA, Bangalore

Experience:

Company Name : VELANKANI ELECTRONICS PVT LTD.
Designation : Signal Integrity Analysis Engineer.
Location : Bangalore, Karnataka
Experience : From June 15th 2017 to till date.
Company Name : SIENNA ECAD Technologies Pvt Ltd.
Designation : Signal Integrity Analysis Engineer.
Location : Bangalore, Karnataka
Total Experience : From July 17th 2014 to MAY 30 2017

Education:

1.	M-Tech	BELLARI INSTITUTE OF TECHNOLOGY AND MANAGEMENT	Visvesvaraya Technological University, Belgaum	COMPUTER NETWORKING	2013
2.	BE	KLS's VDRIT, HALIYAL	Visvesvaraya Technological University, Belgaum	ELECTRONICS AND COMMUNICATION	2011

ROLES & RESPONSIBILITY:

- Pre and Post Layout Simulation of Signal Integrity, Power Analysis and Board and System Level Thermal Analysis.
- Handling High Speed Digital Signal Integrity issues i.e. Jitter, Timing, Delay and Crosstalk.
- Power issues like IR drop and Decoupling Analysis.
- Handling Board level and System Level thermal issues.
- Reliability Analysis of the components in the board.
- Insertion Loss and Return Loss modelling and improvement with S-Parameters for Transmission Path.
- Verify & validate the models and assure safe signal margins are obtained.
- Layout review before start the analysis activity.
- Interact with H/W Team and Layout Team in Completing Analysis activity.
- Prepare Pre & Post detailed analysis reports.
- Suggest design recommendations so that analysis is successful.

MAJOR PROJECTS HANDLED:

Intel Server (Skylake Processor)

Communication card with 40-layer Stack-up. Blind buried via technology.

Interfaces:

RF Traces, PCIe Gen 4, 100 Gbps Ethernet, AURORA, USB 3.0 and LPDDR4

Challenges:

SerDes Signal losses was to be minimal, hence blind buried via technology, common antipad structure for the vias was suggested. Via structure was modelled using 3D Full Wave Solvers. Four LPDDR4 memory chips was to be used hence Top-Bottom placement was suggested to minimize the length of traces. Impedance details for USB interface was suggested.

Stationary launched pad missile guidance system

Interfaces:

RF Traces, PCIe Gen 4, 25 Gbps Ethernet, USB 3.0 and LPDDR4

Challenges: 32 DDR4 memory chips had to be analysed for length matching, placement, and routing. Dense design of 62 layers. Blind & buried via design, Power Aware analysis, and Crosstalk mitigation

Head Mounted Display

Interfaces:

PCIe Gen 4 and USB 3.0.

Challenges: The board size was the major issue to overcome, placement optimization with routing and via technology planning.

Camera Module for the Lunar rover

Interfaces:

SDRAM, NAND Flash, eMMC and ADC.

Challenges:

SDRAM signal routing with series terminations, Crosstalk reduction.

Career Highlights:

- Winner of the quarterly best performance award 3 times in a row.
- Winner for all India Technical Excellence Award for 2020

LIST OF PARTICIPANTS (TEACHING STAFF)

SL. NO.	PARTICIPANT NAME	AFFILIATION
1	PROF. PLASIN DIAS	KLS VEDIT HALIYAL
2	PROF. VINAY CHITARE	KLS VEDIT HALIYAL

LIST OF PARTICIPANTS (STUDENTS)

SL. NO.	PARTICIPANT NAME	AFFILIATION
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53	LAXMI NIRVANI	KLS VEDIT HALIYAL
54	DEEPIKA RATHI	KLS VEDIT HALIYAL
55	FREEDA A FERNANDES	KLS VEDIT HALIYAL
56	SONAL PAI	KLS VEDIT HALIYAL
57	PRACHI BHANDARE	KLS VEDIT HALIYAL
58	ARAVIND	KLS VEDIT HALIYAL
59	SHREYA PAI	KLS VEDIT HALIYAL
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TOPICS COVERED

- Industry and Education System - How it comes together?
- Systematic Breakdown of Responsibilities
- Deep dive into key areas of Expertise and Roles
- What is ECAD and How it is driving the Electronics Industry
- How are ECAD tool assisting the Electronics Engineers in Schematics, Layout, Verification, Fabrication, Testing
- Career Opportunities - Different career options, Trends and direction in which the industry is headed

GALLERY – EVENT SNAPSHOTS



