CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, June/July 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions. (08 Marks)

b. Explain the working of nMOS enhancement mode transistor with suitable diagrams. (08 Marks)

OR

2 a. Derive expression for drain current in linear and saturation region for nMOS transistor. (08 Marks)

b. With neat sketches explain the CMOs P-well process steps to fabricate a CMOS inverter. (08 Marks)

Module-2

3 a. Write the lambda based design rules for separation of layers and transistors. (06 Marks)

b Draw circuit, stick and layout diagram for nMOS shift register cell (10 Marks)

OR

4 a. Define sheet resistance (R_S) standard unit of capacitance (□Cg) and delay unit (τ) (06 Marks)

b. Calculate the capacitance of the structure given below in Fig.Q4(b). (10 Marks)

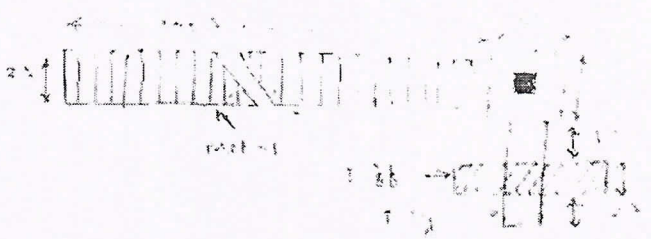


Fig.Q4(b)

Area capacitance value for metal 1 to substrate = 0.3pF × 10^{-4} μm² (0.075 relative value)
Area capacitance value for diffusion to substrate = 1pF × 10^{-4} μm² (0.25 relative value)
Area capacitance value for polysilicon to substrate = 0.4 pF × 10^{-4} μm² (0.1 relative value).

Head of the Department
Dept. of Electronic & Communication Engg
KLS V.D.I.T., HALIYAL (U.K.)

Scheme and Solutions Prepared by

Prof Meenakshi .T.

Module-3

5 a. Obtain the scaling factor for the following device parameters :
   i) gate capacitance
   ii) gate area
   iii) saturation current (Idss)
   iv) channel resistance (R_{on})
   v) maximum operating frequency (f_{ll})
   vi) power dissipation per gate (Pg)
   vii) current density (J)
   viii) gate delay (T_d). (08 Marks)

b. With a neat diagram explain 4 × 4 Barrel shifter. (08 Marks)

OR

6 a. Explain the general arrangement of a 4 bit data path for processor. (08 marks)

b. Describe Manchester carry chain element. (08 Marks)

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI sub system. (05 Marks)

b. Explain in detail the general structure of an FPGA fabric. (06 Marks)

c. Explain switch logic implementation of CMOS 5 way selector with neat circuit diagram. (05 Marks)

OR

8 a. Explain the structured design approach for the implementation of a parity generator. (08 marks)

b. Explain dynamic CMOS logic with example. (08 Marks)

Module-5

9 a Explain 3 transistor dynamic RAM cell with schematic diagram. (06 Marks)

b. Explain any two fault models in combinational circuits. (06 Marks)

c Write a note on automatic test pattern generation. (04 Marks)

OR

10 a. write short notes on :
   i) observability and controllability
   ii) Built In Self Test (BIST). (08 Marks)

b. Explain nMOS pseudo static RAM cell with schematic diagram. (08 Marks)

* * * * *

6th Semester B.E. Degree Examination, June/July 20

Subject - VLSI Design Subject Code - 15EC6

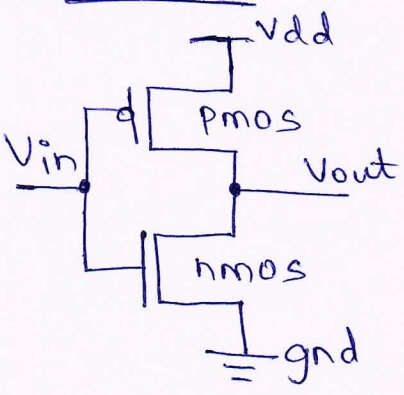
Solutions to June/July. 2019 Question Paper.

Module - 1

Faculty - Meena

19 Derive the CMOS inverter DC characteristics graphically from p-device and n-device characteristics and show all operating regions. — 8 Marks

Solution



→ CMOS inverter consists of pmos and nmos transistors connected at gate and drain terminals.

→ Vdd connected to pmos source and gnd connected to nmos source.

→ V_{tn} is threshold voltage for nmos and V_{tp} is threshold voltage for pmos.

→ V_{tp} is negative for pmos.

→ $V_{gsn} = V_{in}$, $V_{gsp} = V_{in} - V_{dd}$

$V_{dsn} = V_{out}$, $V_{dsp} = V_{out} - V_{dd}$

	Cutoff	Linear	saturation
nmos	$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$
pmos	$V_{gsp} > V_{tp}$ $V_{in} > V_{tp} + V_{dd}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{dd}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{dd}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

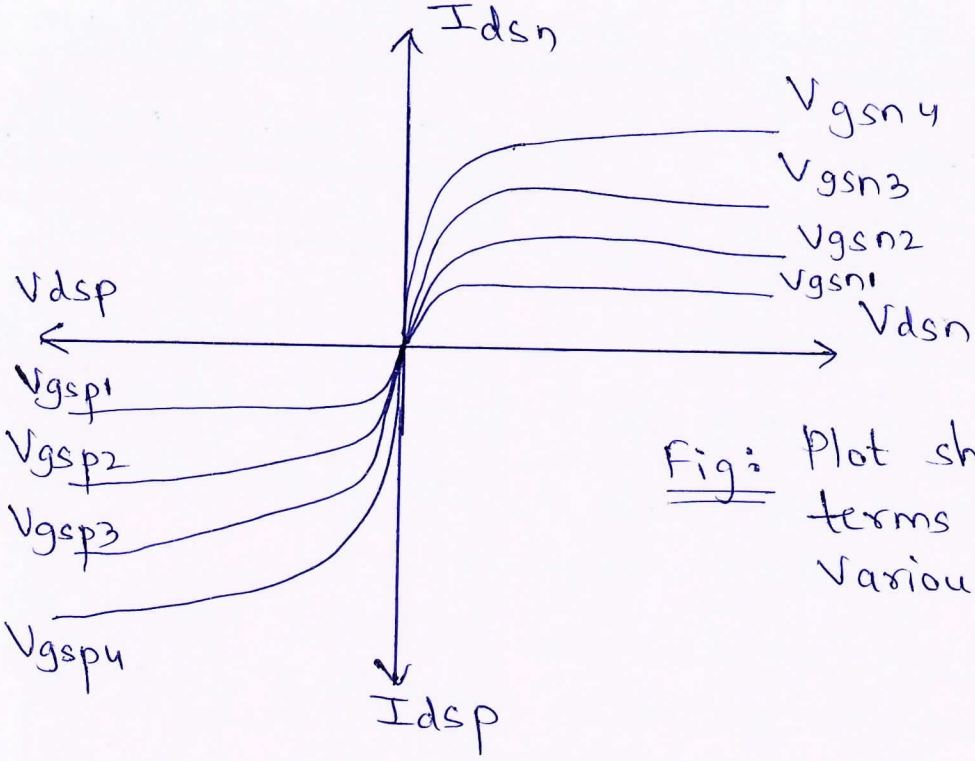


Fig: Plot shows Idsn & Idsp in terms of Vdsn & Vdsp for various values of Vgsn & Vgs

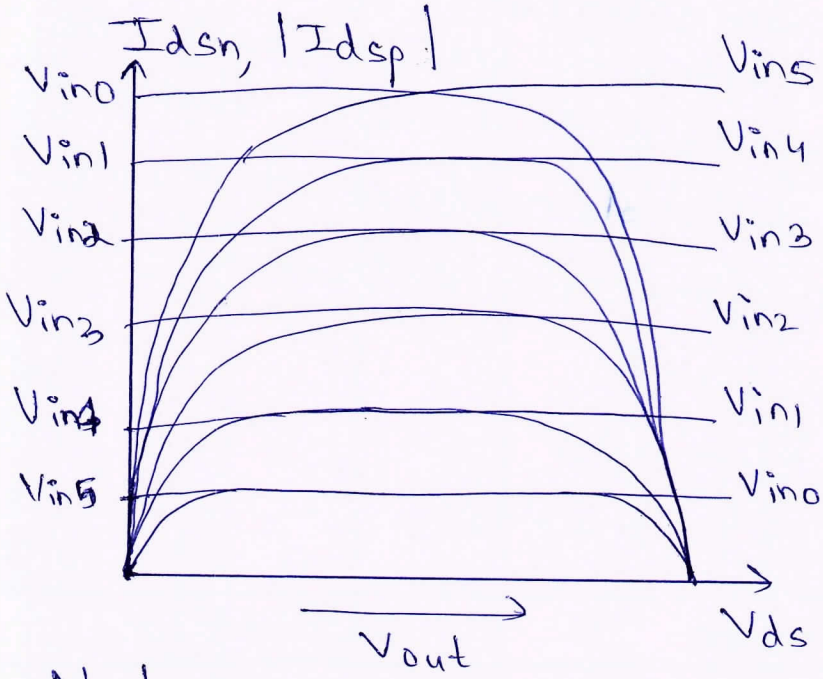


Fig: Plot shows Idsn & Idsp in terms of Vout for various values of Vin

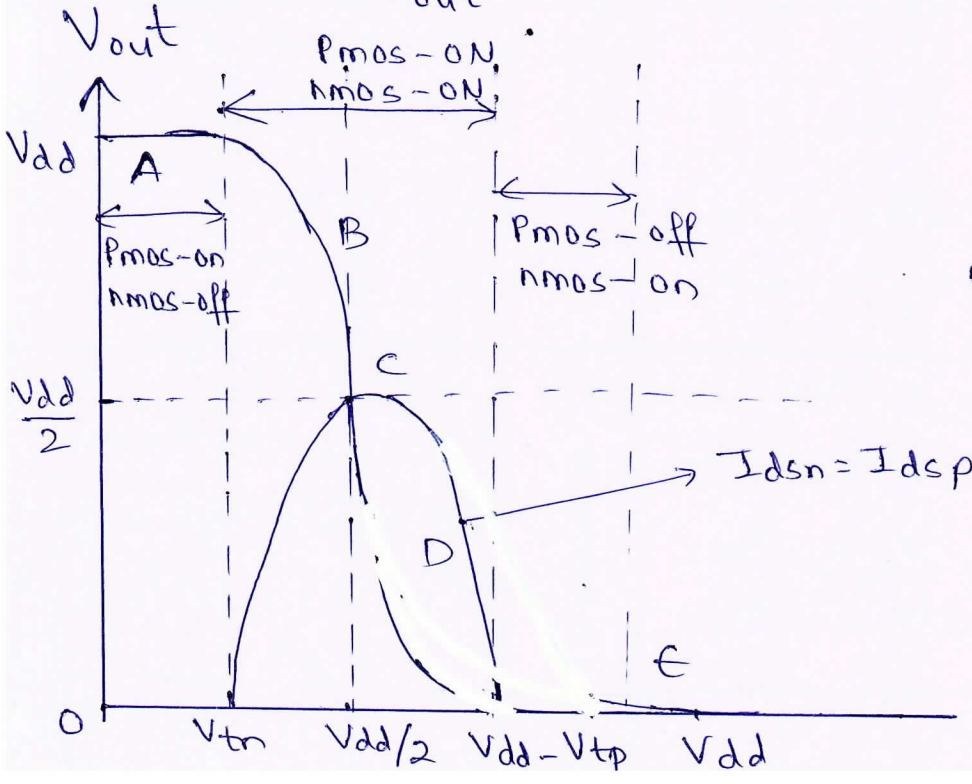


Fig: Dc characteristics of CMOS Inverter

Region	Condition	Pmos	nmos	Output
A	$0 \le V_{in} \le V_{tn}$	Linear	cut-off	$V_{out} = V_{dd}$
B	$V_{tn} \le V_{in} < \frac{V_{dd}}{2}$	Linear	saturation	$V_{out} > \frac{V_{dd}}{2}$
C	$V_{in} = \frac{V_{dd}}{2}$	saturation	saturation	$V_{out} = \frac{V_{dd}}{2}$
D	$\frac{V_{dd}}{2} < V_{in} < \frac{V_{dd}}{2} - \lvert V_{tp} \rvert$	saturation	Linear	$V_{out} < \frac{V_{dd}}{2}$
E	$V_{in} > \frac{V_{dd}}{2} - \lvert V_{tp} \rvert$	cutoff	Linear	$V_{out} = 0$

1b Explain the working of nmos enhancement mode transistor with suitable diagram. — 8 Marks

Solution

→ MOSFET operates in 3 regions — cut-off
— linear | resistive | Triode | non-saturation
— Saturation

→ It consists of moderately doped p-type substrate into which 2 heavily doped n+ regions, source (S) & drain (D) are diffused

→ Between source & drain, there is narrow region of substrate called channel.

→ channel is covered by SiO_2 called gate-oxide

→ over gate-oxide is polycrystalline silicon electrode called gate.

→ Threshold Voltage (V_t) is minimum voltage that is applied from gate-to-source to establish channel.

→ when $V_{gs} = 0$, it is similar to 2 diodes connected back-to-back between source & drain. So no current flows. Also depletion region forms at source-substrate and drain-substrate junctions.

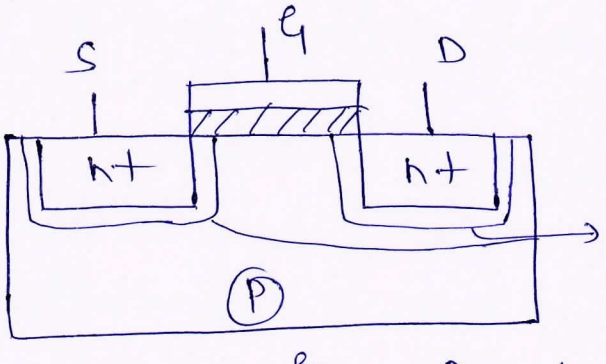
→ when $V_{gs} < V_t$, holes under gate are repelled to produce a depletion region and it becomes continous under gate from source-to-drain.

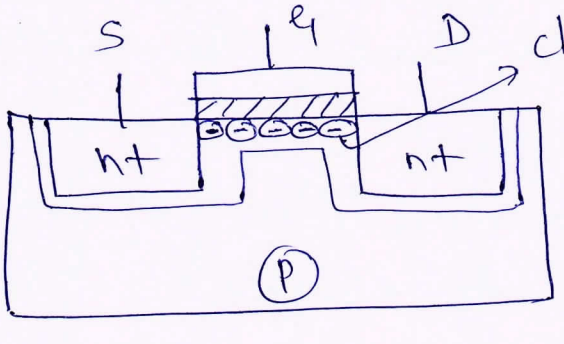
→ $V_{gs} < V_t$ & $V_{ds} = 0$ is termed as cut-off region

→ when $V_{gs} > V_t$, electrons in p-substrate cross depletion region and it reaches under gate. This process is called inversion.

→ After channel is created, V_{ds} becomes positive, drain-substrate junction gets reverse biased & depletion region widens as drain becomes more positive w.r.t source. Current flow starts. Current increases with increase in V_{ds}.

→ Further increase in V_{ds} causes channel to get pinched-off. However transistor remains ON, but current remains Constant





cut-off region

$V_{gs} < V_t$

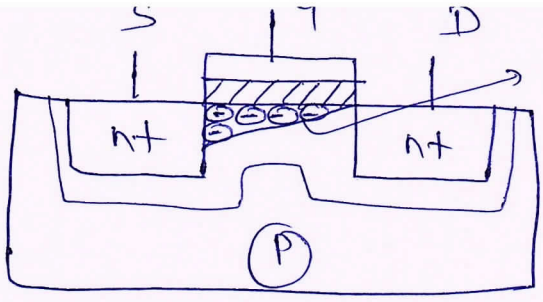
$V_{ds} = 0$

$I_{ds} = 0$

Linear Region

$V_{gs} > V_t$

$V_{ds} = 0$

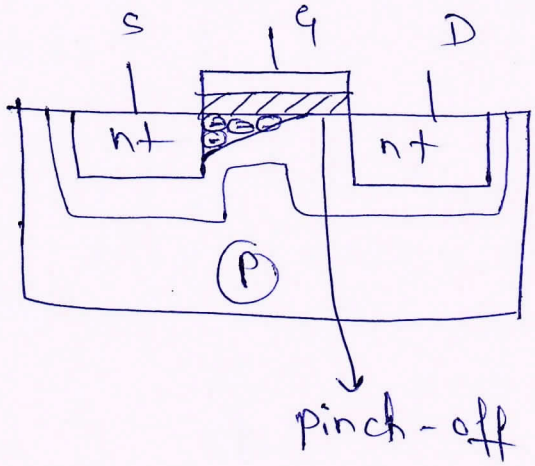


Linear Region

$V_{gs} > V_t$

$V_{ds} < V_{gs} - V_t$

$$I_{ds} = \beta\left[(V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$



Saturation Region

$V_{gs} > V_t$

$V_{ds} \geq V_{gs} - V_t$

$$I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2$$

2a Derive expression for drain current in linear and saturation for nmos transistor.

8 Marks

Solution

→ Mos transistor has 3 regions of operations
- * cut-off (or) subthreshold region
- * linear / non-saturation / Triode / Resistive region
- * saturation region

→ In cut-off region, there is zero current from drain - source, $I_{ds} = 0$.

→ In other regions, gate attracts carriers to form channel.

→ Electrons drift from source to drain at a rate proportional to Electric field between these regions.

→ Thus we can compute current if we know the amount of charge in channel and rate at which it moves.

→ we know that, charge on each plate of capacitor is $Q = CV$

$\therefore$ charge in channel $Q_{channel} = C_g (V_{gc} - V_t)$

where $C_g = \frac{\varepsilon_o W L}{t_{ox}}$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$\therefore C_g = C_{ox} W L$

where,
C_g = Capacitance of gate to channel
$(V_{gc} - V_t)$ → Voltage that attracts charge to channel
μ → Mobility
ε_o → permitivity
t_{ox} – oxide thickness
W – width
L – length
E – Electric field

Velocity of carrier is given by $V = \mu E$

$E = \frac{V_{ds}}{L}$

$\therefore I_{ds} = \frac{Q_{channel}}{time} = \frac{Q_{channel}}{L/V}$

$= \frac{C_g (V_{gc} - V_t)}{L/V}$

$I_{ds} = \frac{C_g V}{L} (V_{gc} - V_t)$

$= \frac{C_{ox} W L}{L} \cdot \mu E (V_{gc} - V_t)$

$= C_{ox} W \mu \frac{V_{ds}}{L} (V_{gc} - V_t)$

$\therefore V_{gc} = V_{gs} - \frac{V_{ds}}{2}$

$\beta = \mu C_{ox} \frac{W}{L}$

$I_{ds} = \mu C_{ox} \frac{W}{L} \left(V_{gs} - \frac{V_{ds}}{2} - V_t \right) V_{ds}$

$$\boxed{I_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]}$$ Linear Region

For Saturation Region

$V_{ds} \geq V_{gs} - V_t$

$\therefore I_{ds} = \beta \left[(V_{gs} - V_t)(V_{gs} - V_t) - \frac{(V_{gs} - V_t)^2}{2} \right]$

$$\therefore \boxed{I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2}$$

[2b] With neat sketches explain the CMOS P-well Process steps to fabricate CMOS inverter

8 marks

Solution

→ P-well acts as a substrate for n-device within parent n-type substrate

Mask-1 → Defines the area in which deep p-well diffusions are to take place.

Mask 2 → Defines thinox regions, namely those areas where thick-oxide is to be stripped and thin-oxide grown to accomodate p and n transistors

Mask-3 → used to pattern polysilicon layer.

Mask-4 → p+ mask is used to define areas where p-diffusion is to take place

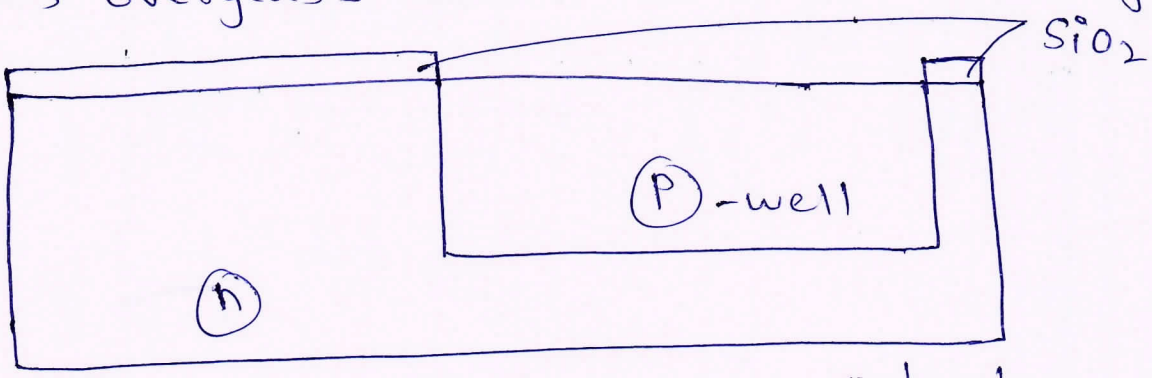
Mask-5 → negative p+ mask is used to define areas where n-diffusion is to take place

Mask-6 → Contact cuts are defined

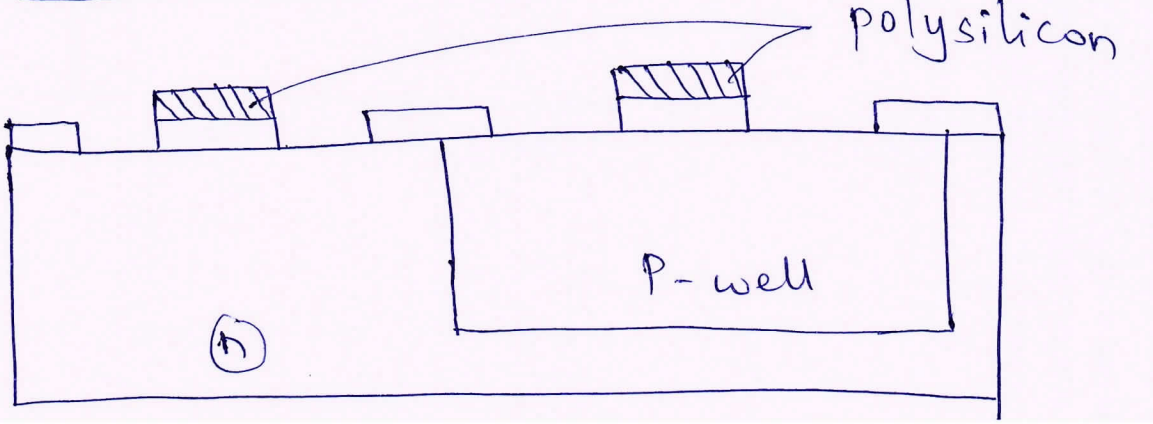
Mask-7 → Metal layer is defined

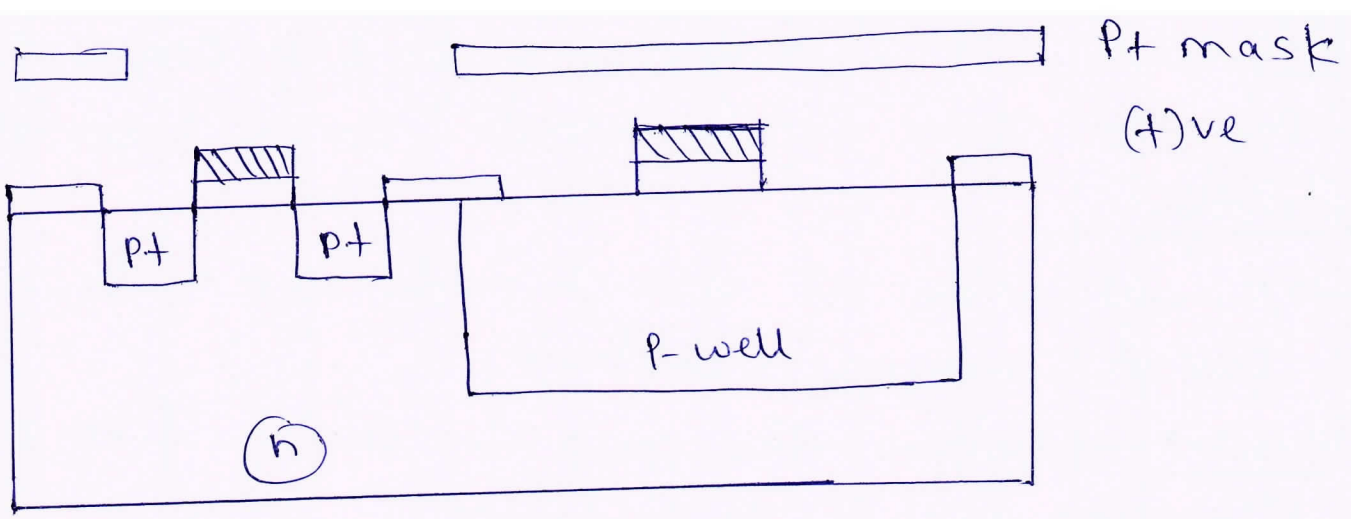
Mask-8 → overglass with cuts for bonding pads

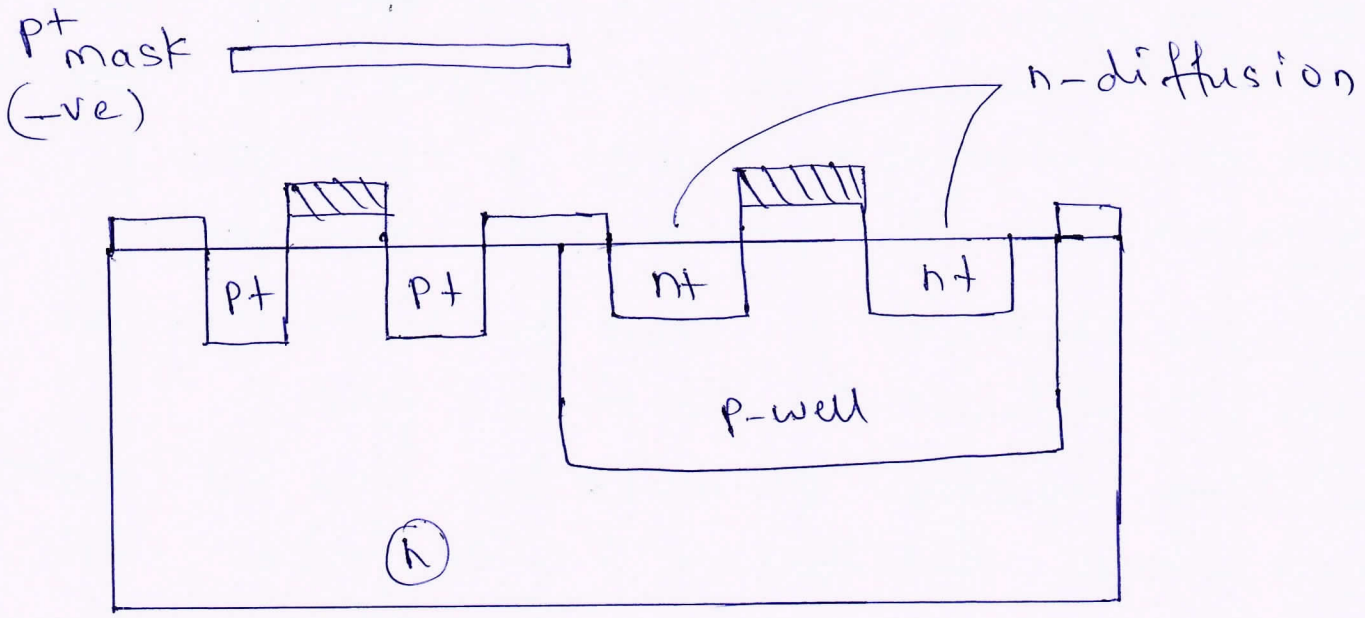
1.

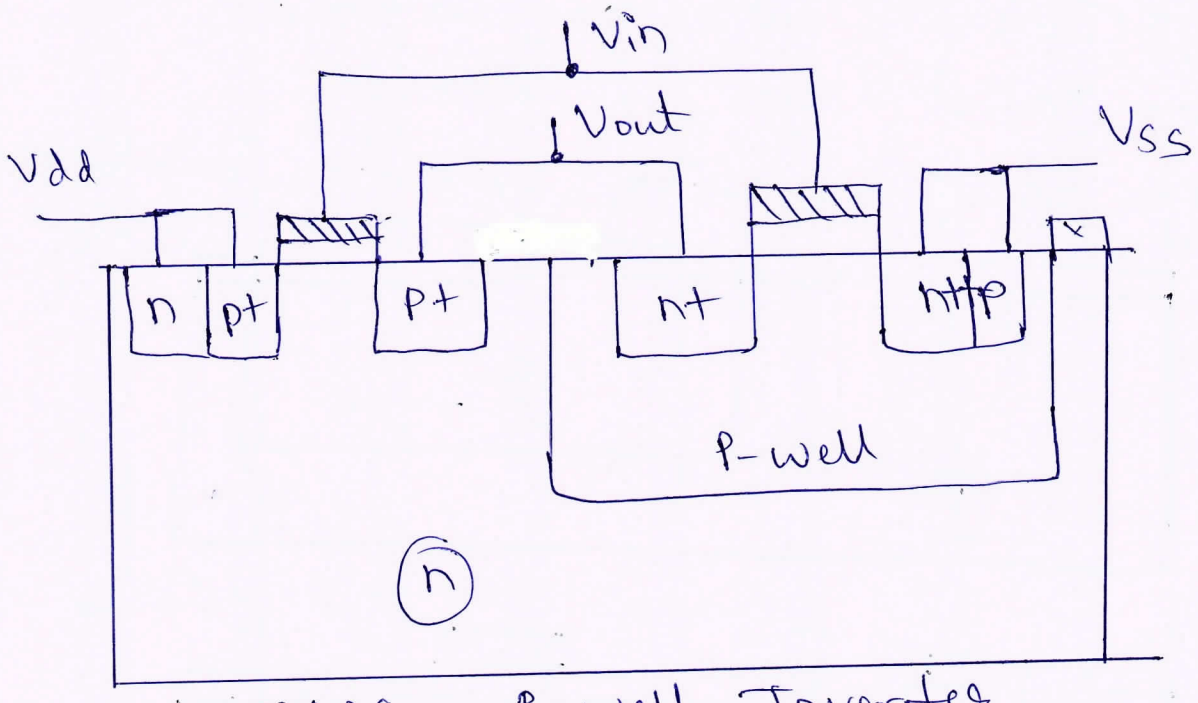


2.









CMOS P-well Inverter

[4a] Define sheet resistance (R_s), standard unit of Capacitance ($\square C_g$) and delay unit (τ) — 6 marks.

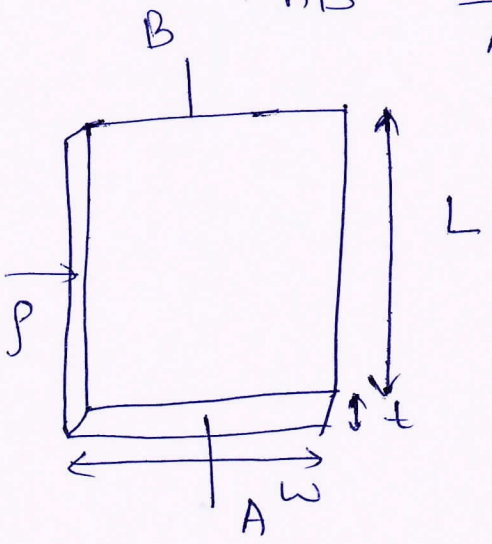
Solution

Sheet Resistance (R_s)

Consider uniform slab of conducting material of resistivity (ρ), width (w), thickness (t) and length (L)

$$R_{AB} = \frac{\rho L}{A}\ \Omega = \frac{\rho L}{tw}$$

A = Cross-section Area



Consider square of resistive materia in which $L = w$

$$\therefore R_{AB} = \frac{\rho}{t} = R_s$$

$$\therefore \boxed{R_s = \frac{\rho}{t}\ \Omega/\square}$$

{ R_s = sheet resistanc

$$\therefore \boxed{R_{AB} = \frac{R_s \cdot L}{w}\ \Omega}$$

nmos transistor sheet resistance $R_{sn} = 10k\Omega$

pmos transistor sheet resistance $R_{sp} = 25k\Omega$

Standard unit of Capacitance ($\square C_g$)

Gate-to-channel capacitance of MOS transistor having $w = L =$ feature size.

for 5μm $\square C_g$ Value is

Area/standard square $= 5\mu m \times 5\mu m = 25\mu m^2$

Capacitance value $= 4 \times 10^{-4}\ pF/\mu m^2$

$\therefore$ Standard Value $(\square C_g) = 4 \times 10^{-4}\ \frac{pF}{\mu m^2} \times 25\mu m^2$

for 2μm $\square C_g$ value is

$\square C_g = 0.01\ pF$

Area/standard square $= 2\mu m \times 2\mu m = 4\mu m^2$

Capacitance value $= 8 \times 10^{-4}\ pF/\mu m^2$

$\therefore$ standard value $(\square C_g) = 8 \times 10^{-4}\ \frac{pF}{\mu m^2} \times 4\mu m^2$

$\square C_g = 0.0032\ pF$

for 1.2μm

Area/standard square = 1.2μm × 1.2μm = 1.44μm²

Capacitance value = $16 \times 10^{-4} \frac{pF}{\mu m^2}$

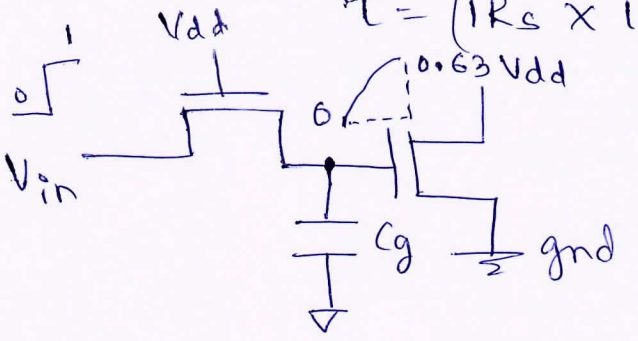
∴ Standard Value (□Cg) = $16 \times 10^{-4} \frac{pF}{\mu m^2} \times 1.44 \mu m^2$

$\square C_g = 0.0023\ pF$

Delay unit (τ)

standard gate area capacitance being charged through one feature size square of n-channel resistance.

$\tau = (1R_s \times 1 \square C_g)$ seconds.

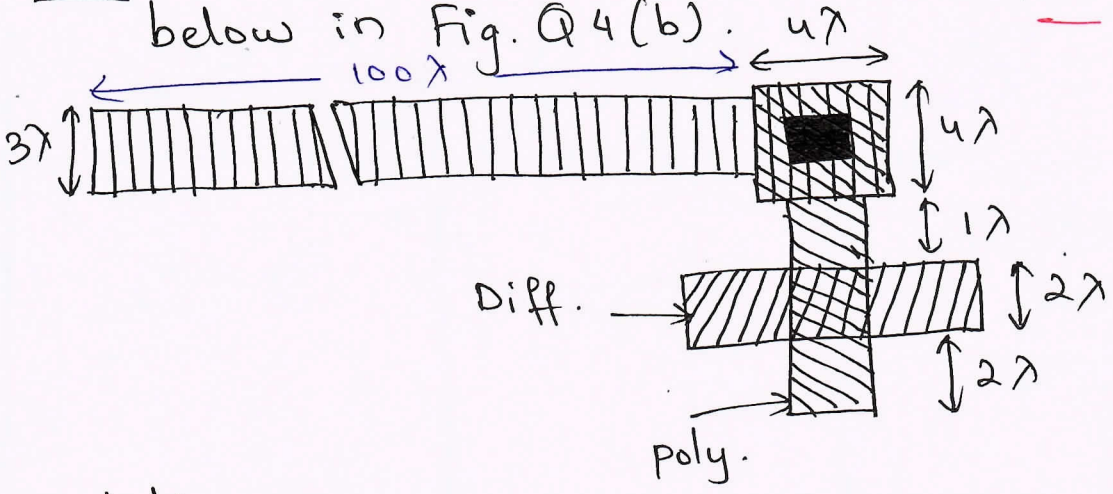


5μm $\tau = 10^4 \Omega \times 0.01 pF = 0.1 ns$

2μm $\tau = 2 \times 10^4 \Omega \times 0.0032 pF = 0.064 ns$

1.2μm $\tau = 2 \times 10^4 \Omega \times 0.0023 pF \doteq 0.046 ns$

4b Calculate the capacitance of structure given below in Fig. Q4(b). — 10 Marks



Solution

Metal capacitance (C_m) = Relative area × Relative 'c' value

$$= \frac{3\lambda \times 100\lambda}{2\lambda \times 2\lambda} \times 0.075 \square C_g$$

$$\boxed{C_m = 5.625 \square C_g}$$

Polysilicon Capacitance (C_p) $= \frac{(4\lambda \times 4\lambda) + (3\lambda \times 2\lambda)}{2\lambda \times 2\lambda} \times 0.10 C_g$

$$\boxed{C_p = 0.55 \square C_g}$$

Gate capacitance $C_g = 1 \square C_g$

$\therefore$ Total Capacitance $= C_m + C_p + C_g$

$= 5.625 \square C_g + 0.55 \square C_g + 1 C_g$

$= 7.20 \square C_g$

Module-3

5a Obtain the scaling factor for the following device parameters: — 08 Marks

(i) Gate capacitance (ii) gate area
(iii) Saturation Current (I_{ds}) (iv) channel Resistance (R_{on})
(v) Maximum Operating frequency (f_o)
(vi) Power Dissipation per gate (P_g)
(vii) Current Density (J)
(viii) Gate delay (T_d)

Solution

(i) Gate Capacitance

	Combined Voltage and dimension scaling Model	Constant Electric field scaling Model ($\beta = \alpha$)	Constant Voltage Scaling Model ($\beta = 1$)
(i)	**Gate Capacitance** $C_g = C_o L w$ $= \beta \cdot \frac{1}{\alpha} \cdot \frac{1}{\alpha}$ $\boxed{C_g = \frac{\beta}{\alpha^2}}$	$C_g = \frac{1}{\alpha}$	$C_g = \frac{1}{\alpha^2}$
(ii)	**Gate area** $A_g = L \times w = \frac{1}{\alpha} \cdot \frac{1}{\alpha}$ $\boxed{A_g = \frac{1}{\alpha^2}}$	$A_g = \frac{1}{\alpha^2}$	$A_g = \frac{1}{\alpha^2}$
(iii)	**Saturation Current (I_{ds})** $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$ $= \mu \frac{C_{ox} w}{L} (V_{gs} - V_t)^2$ $= \frac{\beta \cdot 1/\alpha}{1/\alpha} \cdot \frac{1}{\beta^2}$ $\boxed{I_{ds} = \frac{1}{\beta}}$	$I_{ds} = \frac{1}{\alpha}$	$I_{ds} = 1$
(iv)	**Channel Resistance (R_{on})** $R_{on} = \frac{L}{w} \cdot \frac{1}{Q_{on} \cdot \mu}$ $= \frac{1/\alpha}{1/\alpha} \cdot \frac{1}{1}$ $\therefore \boxed{R_{on} = 1}$	$R_{on} = 1$	$R_{on} = 1$
(v)	**Maximum Operating frequency (f_o)** $f_o = \frac{w}{L} \cdot \frac{\mu C_o V_{dd}}{C_g}$ $f_o = \frac{1}{T_d}$ $\boxed{f_o = \alpha^2/\beta}$	$f_o = \alpha$	$f_o = \alpha^2$

Combined Voltage & dimension Scaling Model	Constant Electric field Scaling Model ($\beta = \alpha$)	Constant Voltage Scaling Model ($\beta = 1$)
(vi) Power dissipation per gate (P_g) $P_g = P_{gs} + P_{gd}$ $P_{gs} = \frac{V_{dd}^2}{R_{on}} = \frac{1}{\beta^2}$ $\therefore P_{gs} = \frac{1}{\beta^2}$ P_{gd} = dynamic component $= \epsilon_g \cdot f_0$ $P_{gd} = \frac{1}{\beta^2}$ $\therefore \boxed{P_g = \frac{1}{\beta^2}}$	$P_g = \frac{1}{\alpha^2}$	$P_g = 1$
(vii) Current Density (J) $J = \frac{I_{ds}}{A} = \frac{Y\beta}{1/\alpha^2}$ $\boxed{J = \frac{\alpha^2}{\beta}}$	$J = \alpha$	$J = \alpha^2$
(viii) Gate Delay $T_d = R_{on} \cdot C_g$ $T_d = \frac{\beta}{\alpha^2}$	$T_d = \frac{1}{\alpha}$	$T_d = \frac{1}{\alpha^2}$

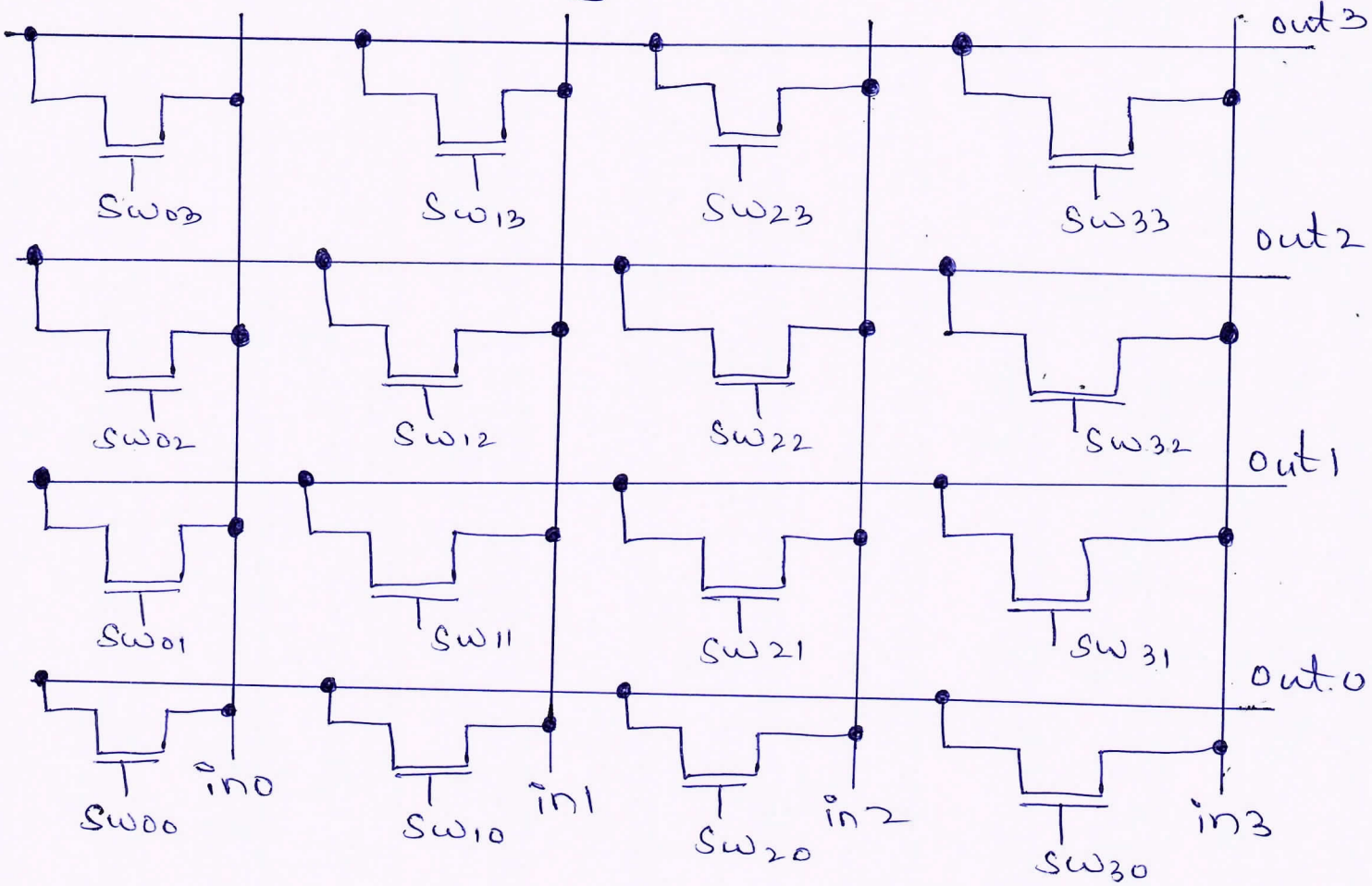
5b With a neat diagram explain 4x4 Barrel shifter — 8 Marks

Solution :

→ Any general purpose n-bit shifter should be able to shift incoming data by upto (n-1) places in right - shift or left - shift direction.

→ shifter must have :

* input from a four - line parallel data bus.
* four output lines for shifted data.
* means of transferring input data to output lines.



→ cross - Bar switch results in few limitations

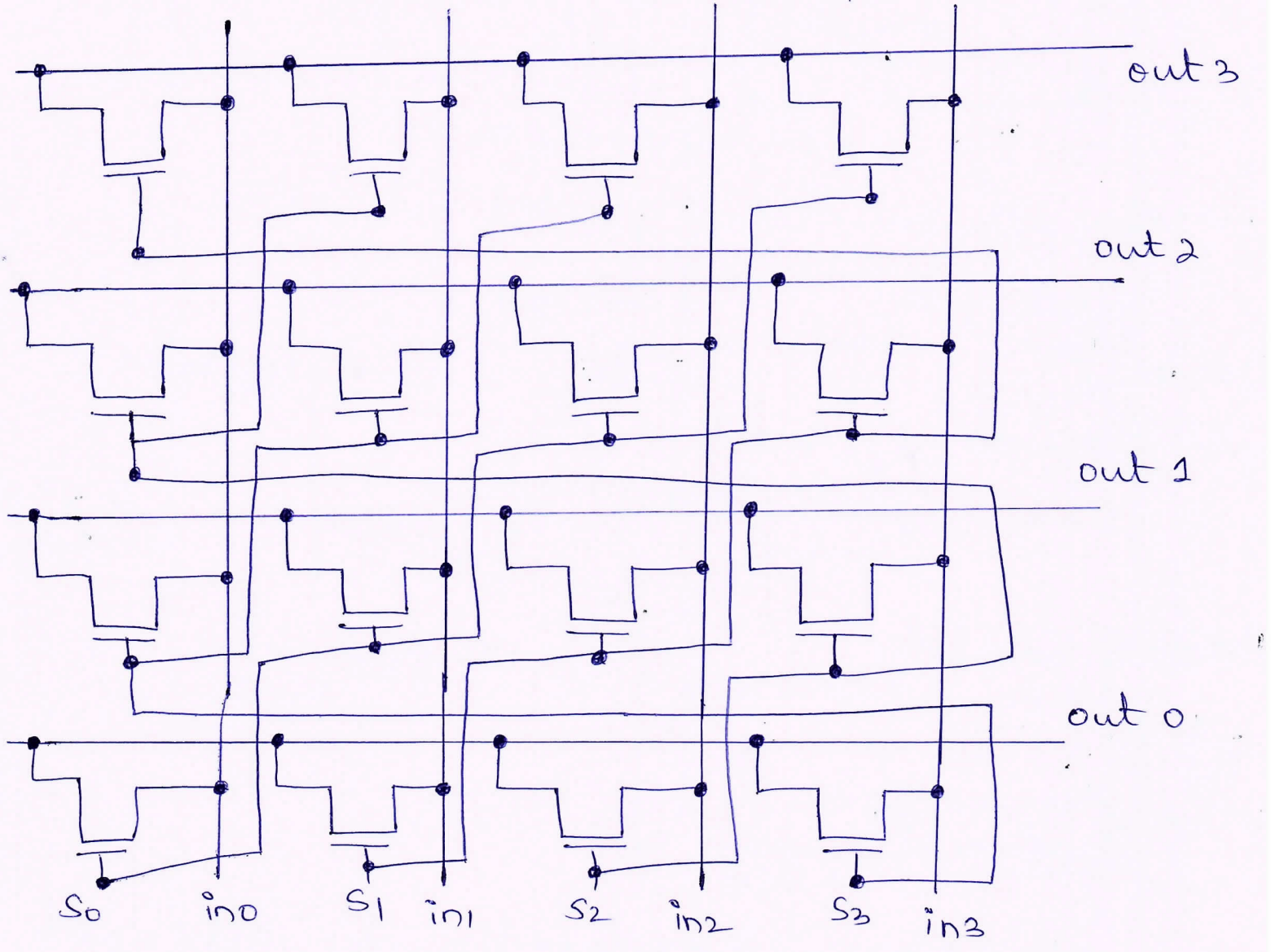
→ any input line can be connected to any or all output lines.

→ if all switches are closed, then all inputs are connected to all outputs in one short circuit.

→ 16 Control signals ($sw_{00} - sw_{15}$) are required for each transistor switch

→ Such Complexity is highly undesirable.

→ Hence barrel-shifter is more efficient which overcomes drawbacks of cross-bar switch



S_0	S_1	S_2	S_3	out0	out1	out2	out3	RL	RR
1	0	0	0	in0	in1	in2	in3	—	—
0	1	0	0	in1	in2	in3	in0	1	3
0	0	1	0	in2	in3	in0	in1	2	2
0	0	0	1	in3	in0	in1	in2	3	1

[6a] Explain the general arrangement of a 4-bit data path for processor — 8 Marks

Soln

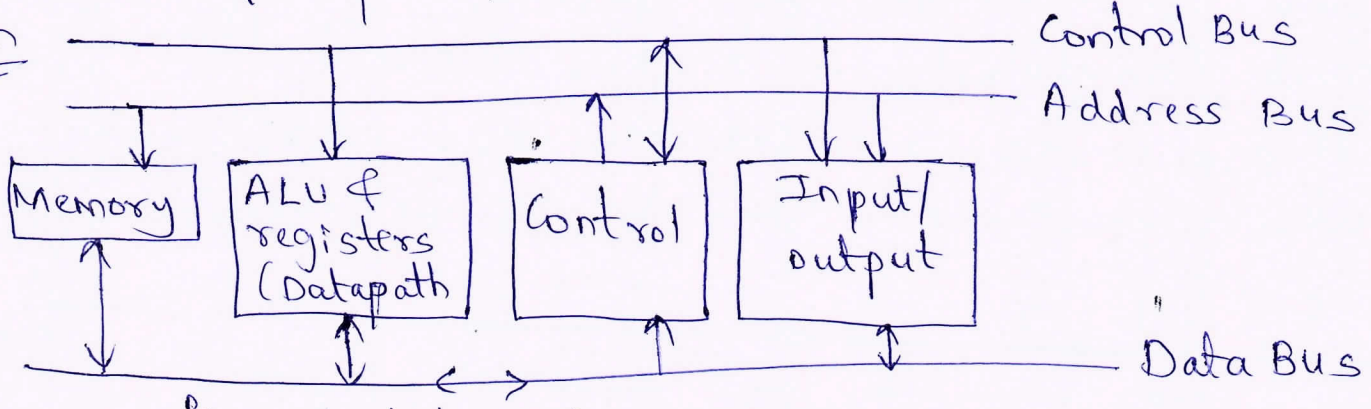
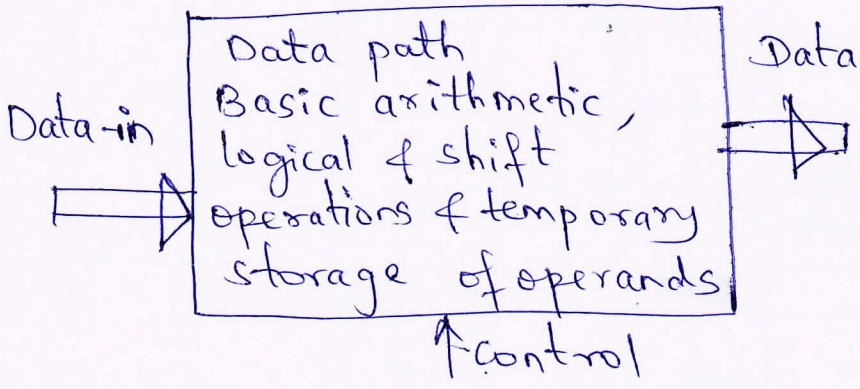
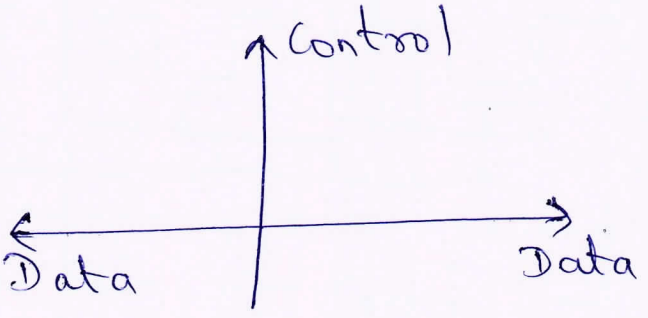


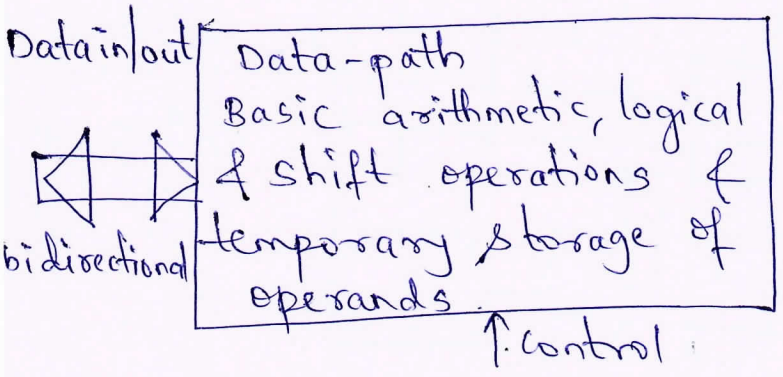
fig: 4-bit Microprocessor

→ Data-path has been separated out below

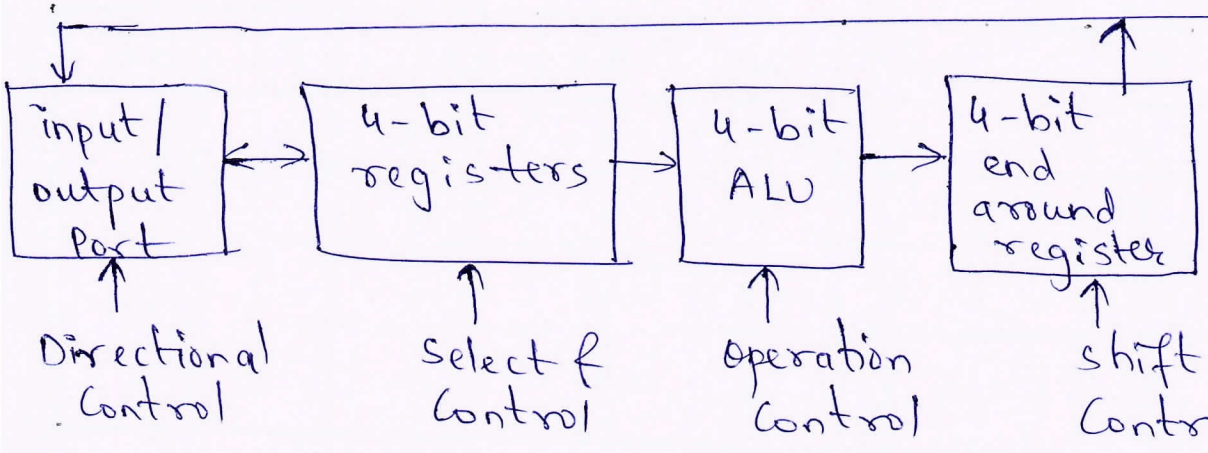




Interconnection Strategy



Sub-units & basic interconnection for data-path



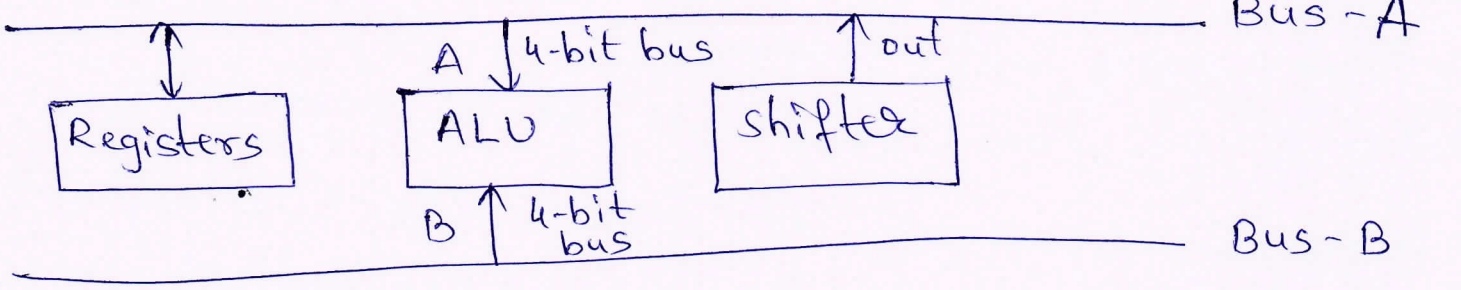
→ ALU & registers can be interfaced with 3 bus architectures as follows.

One-bus architecture

Sequence

- 1st operand from register to ALU, operand is stored there
- 2nd operand from register to ALU. operands are added & result is stored in ALU.
- Result is passed through shifter & stored in register.

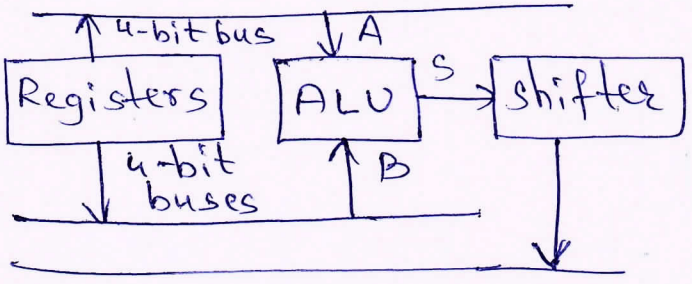
Two-bus architecture



Sequence

- 2 operands A & B are sent from register to ALU and are operated upon & result is stored in ALU.
- Result passed through shifter & stored in register

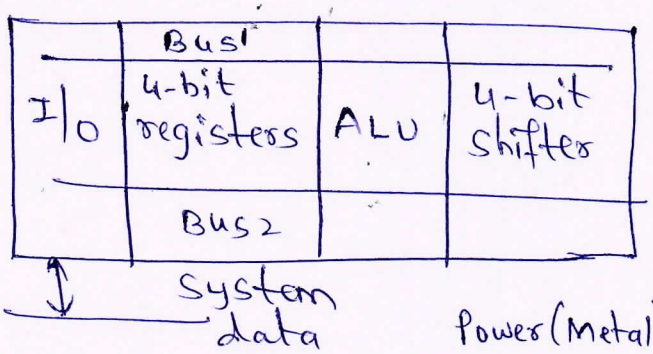
Three-bus architecture



Sequence

2 operands A & B sent from registers. Operated upon & shifted result returned to register.
All in same clock period

Floor-plan for 4-bit data-path



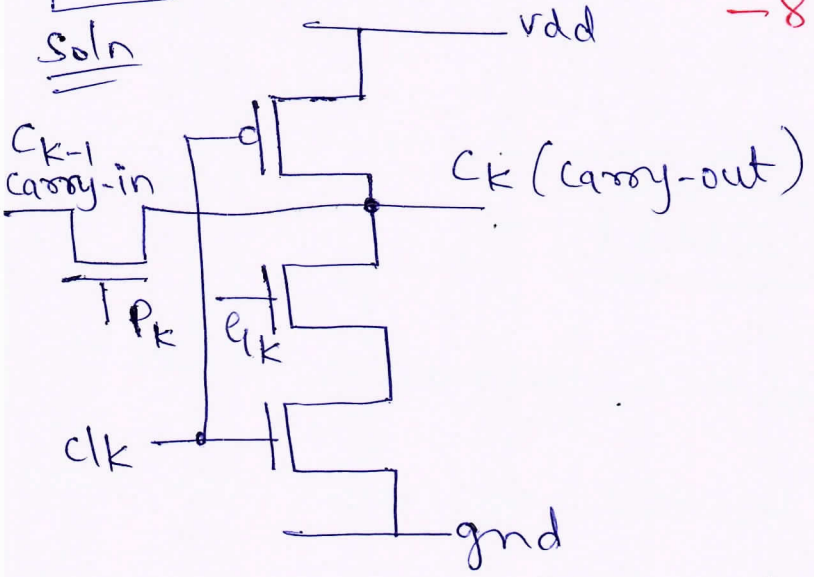
Power (Metal)

Strategy

Data

6b Describe Manchester Carry-chain Element — 8 Marks

Soln



$P_k = A_k \oplus B_k$

P_k = propagate

g_k = generate

$g_k = \overline{A_k} \cdot \overline{B_k}$

→ It is a fast-adder circuit

→ when clock is 0, output will be charged to logic high, because pmos will be ON state

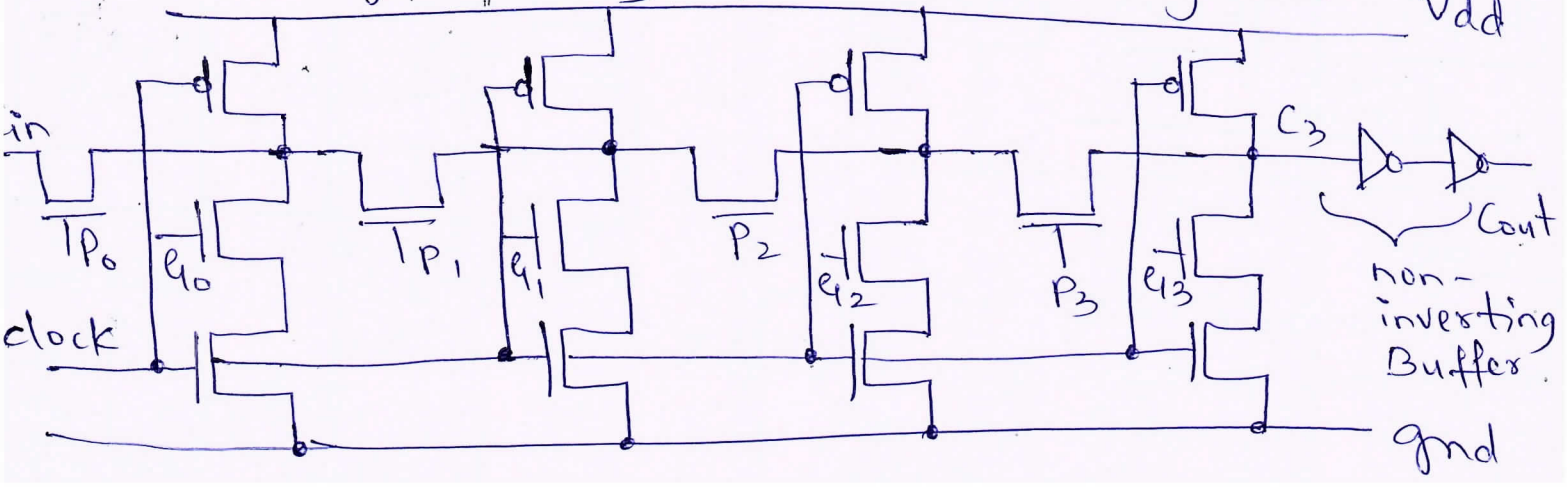
→ when clock is 1, pmos will be off. If $P_k = 1$ then carry will propagate

→ If $P_k = 0$, then C_{k-1} will not be propagated.

→ Depending on inputs at g_k ($A_k = B_k = 1$, carry will be generated) ($A_k = B_k = 0$ no carry generation)

→ Even though, manchester carry are faster, while cascading delay is observed. Cascading is done by connecting pass-transistors in series.

→ As n-pass transistors are cascaded, delay also increases as square of n. Thus to reduce delay, buffers are included after every 4-chain as shown below. Fig: Cascading of Manchester carry adder



Module-4

7a Discuss the architectural issues to be followed in the design of VLSI sub-system - 5 Marks

Soln

→ Design of VLSI system requires logical and systematic approach

→ Eg: Consider design of 500 transistor VLSI system requires 2 engineer-months. Then 500k transistor VLSI system requires 2000-engineer months.

→ Design time rises exponentially with increased complexity

→ Hence we must adopt design methods which allow handling of complexity in less time and less labourers

→ Guidelines are set out as follows.

- Define requirements
- partition overall architecture into subsystems.
- Consider communication paths carefully
- Floorplan: how the system is to map onto silicon.
- Aim for regular structures
- Draw stick or symbolic diagrams.
- Convert each cell to a layout.
- Carry out design rule check on each cell.
- Simulate performance of each subsystem

[7b] Explain in detail the generic structure of an FPGA fabric. – 6 Marks

Soln

→ FPGA consists of 3 major elements
- Combinational logic
- Interconnect
- I/O pins

→ Combinational logic is divided into small units which is known as logic element (LE) or Combinational logic blocks (CLB).

→ LE or CLB forms the functions of several logic gates.

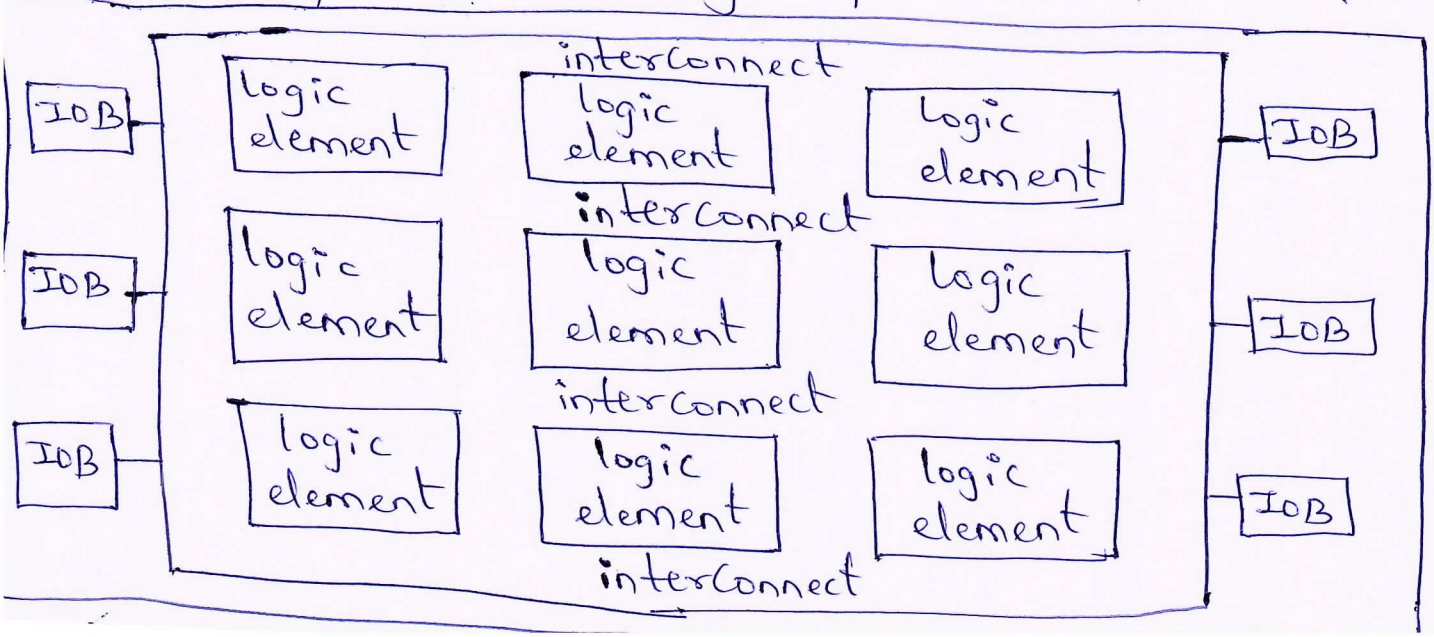
→ Interconnection between these logic elements are made using programmable interconnects

→ This interconnects are logically organized into channels or other units.

→ FPGA offers several interconnects depending on the distance between CLB's that are to be Connected.

→ clock signals are provided with their own inter-Connection networks.

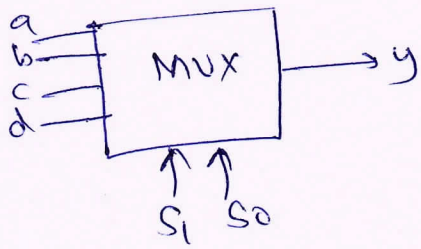
→ I/O pins are referred as I/o blocks (IOB) These are generally programmable for inputs or outputs and often provides other features such as low power or high speed connection.



7c Explain switch logic implementation of CMOS 5-way selector with neat-diagram. – 5 Marks

Soln

nmos	S_1	S_0	y	Pmos
$\bar{S}_1\bar{S}_0$	0	0	a	S_1S_0
$\bar{S}_1S_0$	0	1	b	$S_1\bar{S}_0$
$S_1\bar{S}_0$	1	0	c	$\bar{S}_1S_0$
S_1S_0	1	1	d	$\bar{S}_1\bar{S}_0$



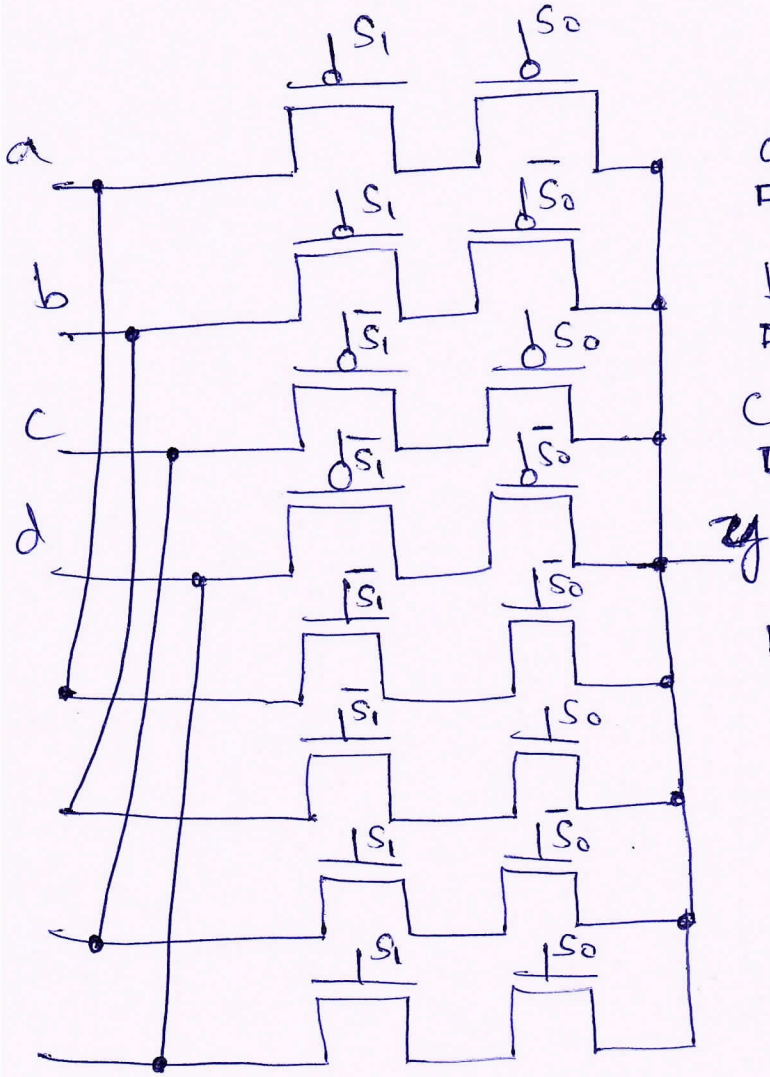


Fig: CMOS ckt. of 4-way selector

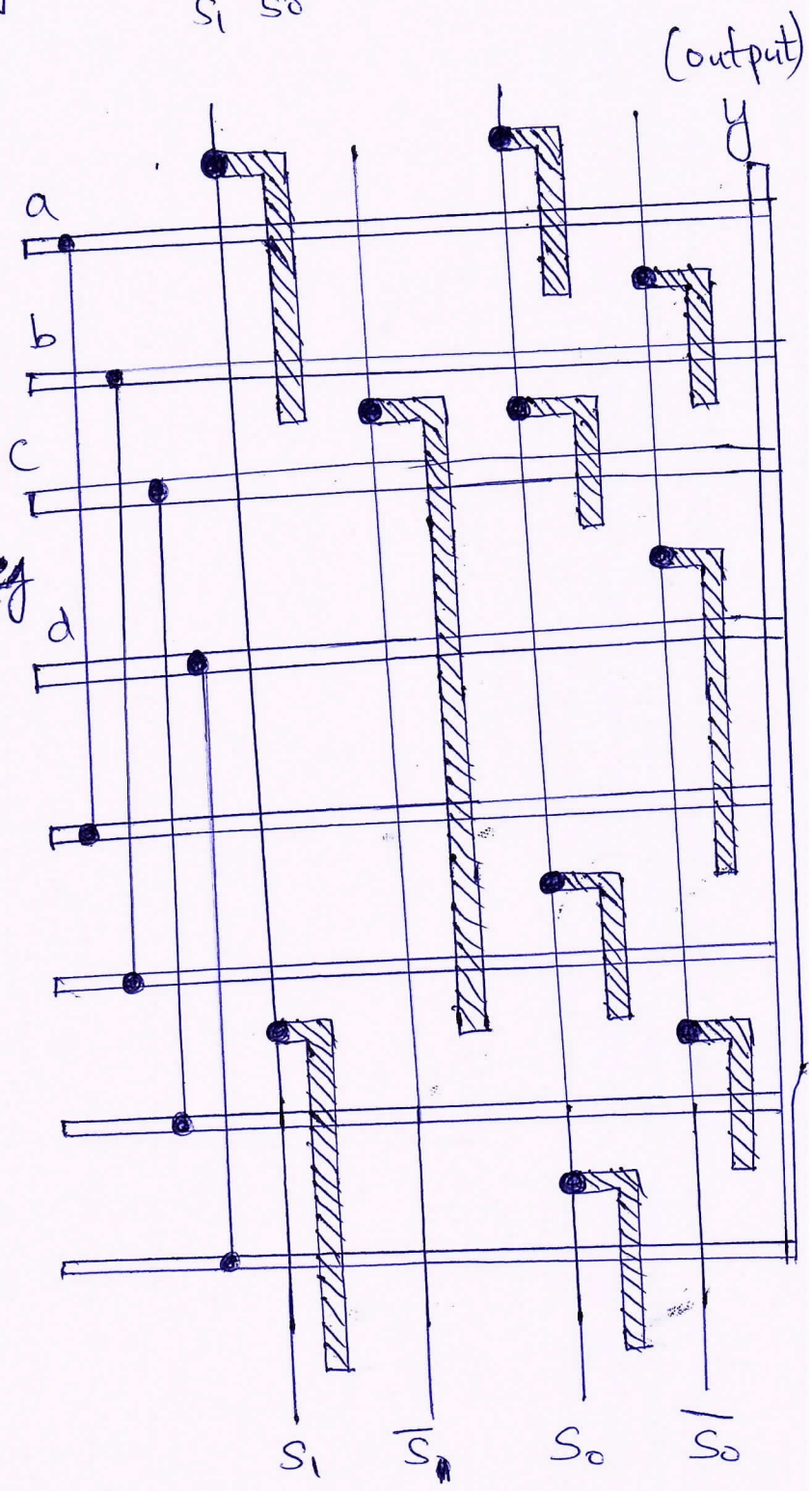


fig: stick-diagram of 4-way selector

8a Explain the structured-design approach for the implementation of a parity Generator - 8 Marks

Soln

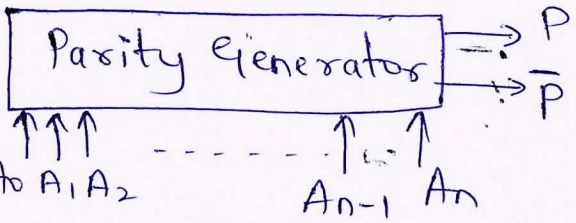


Fig: Basic block diagram

$$P = \begin{cases} 1 & \text{even number of 1s at input} \\ 0 & \text{odd number of 1s at input} \end{cases}$$

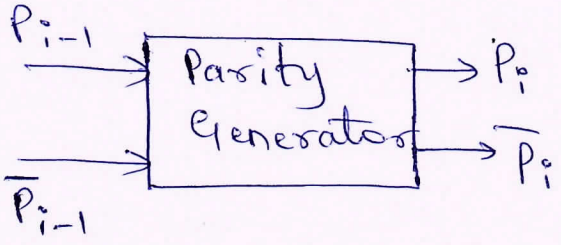
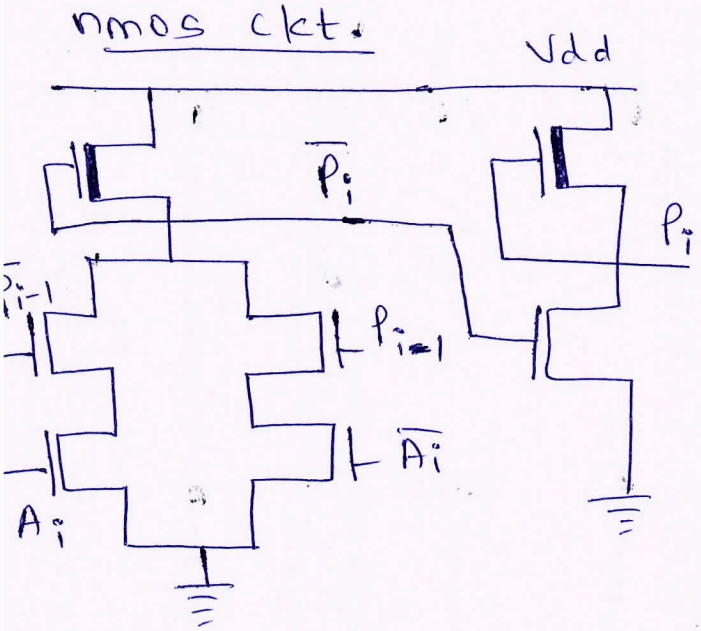


Fig: Parity-Generator basic 1-bit cell

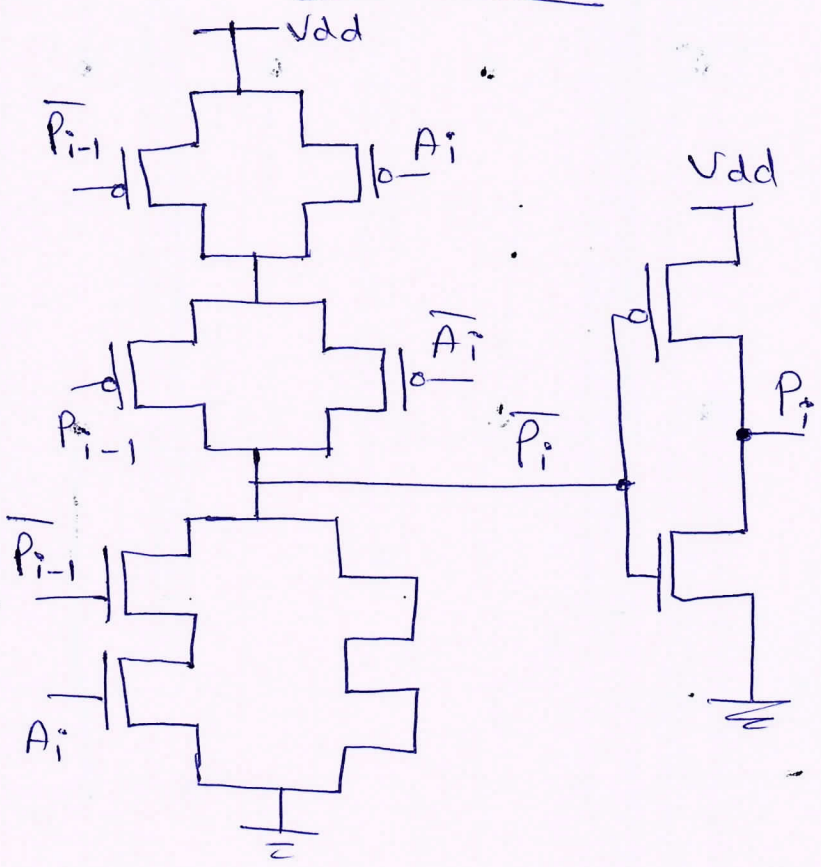
$$P_i = \bar{P}_{i-1} A_i + P_{i-1} \cdot \bar{A}_i$$

$$\bar{P}_i = \overline{\bar{P}_{i-1} A_i + P_{i-1} \bar{A}_i}$$

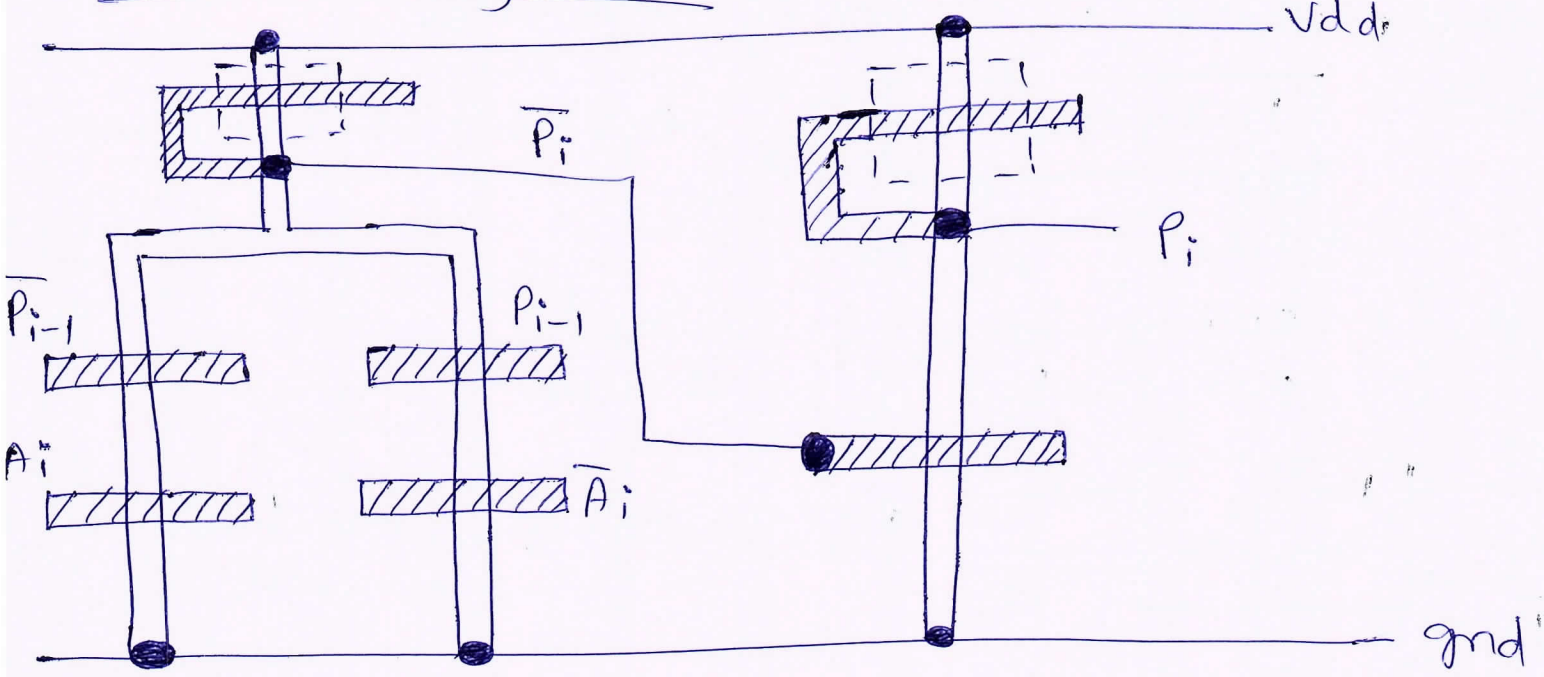
nmos ckt.



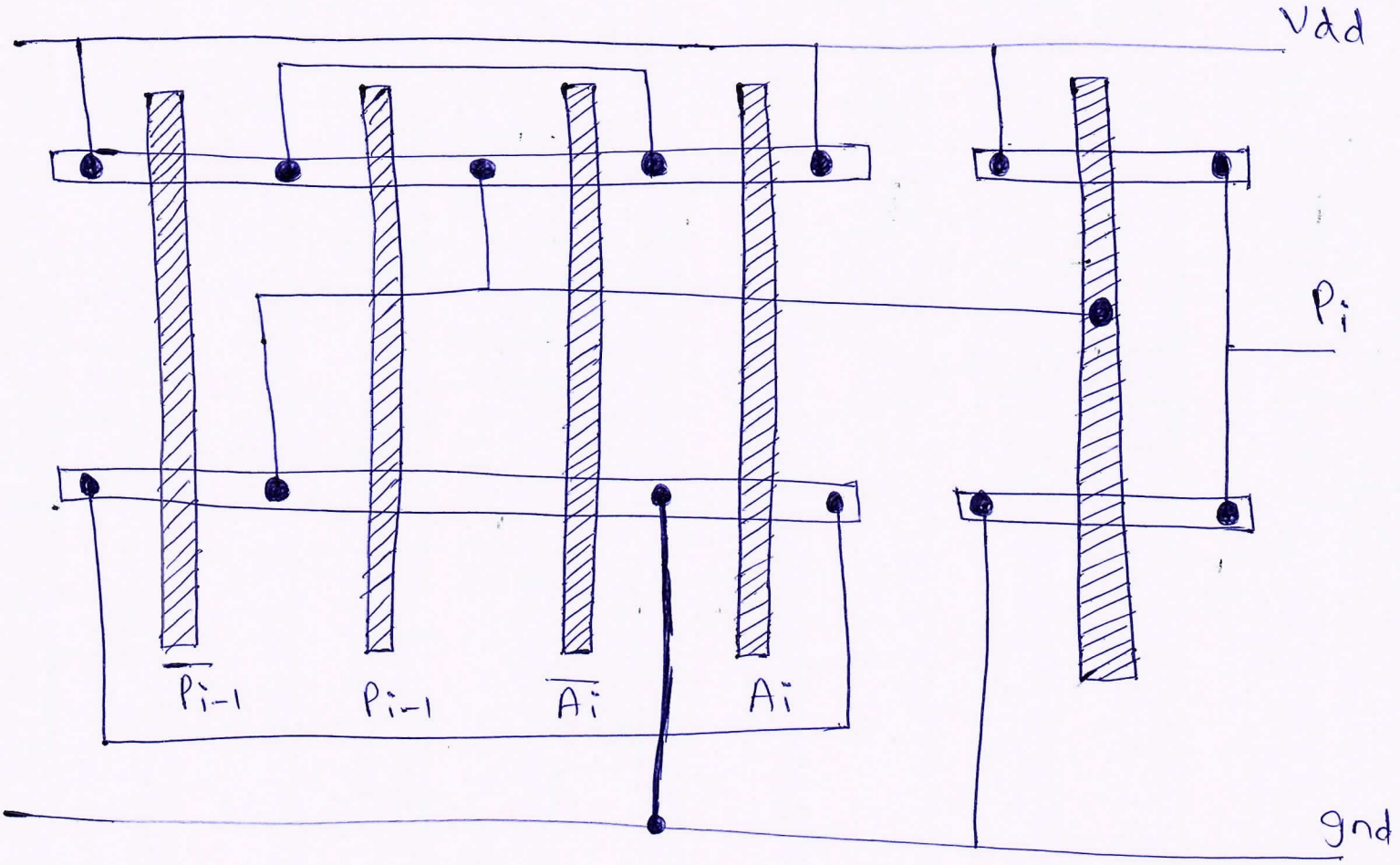
CMOS ckt.



nmos stick diagram

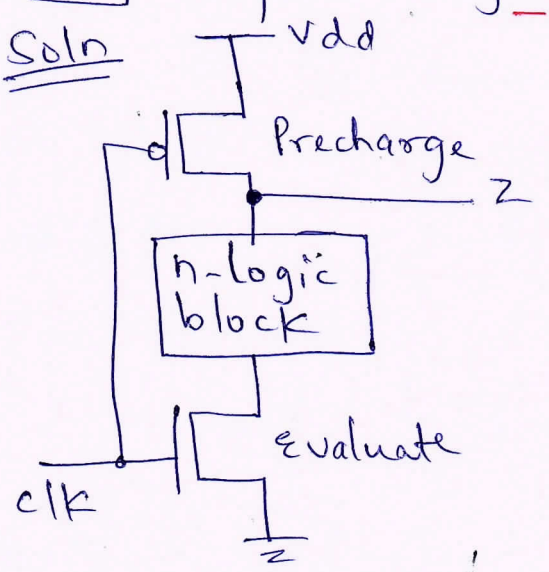


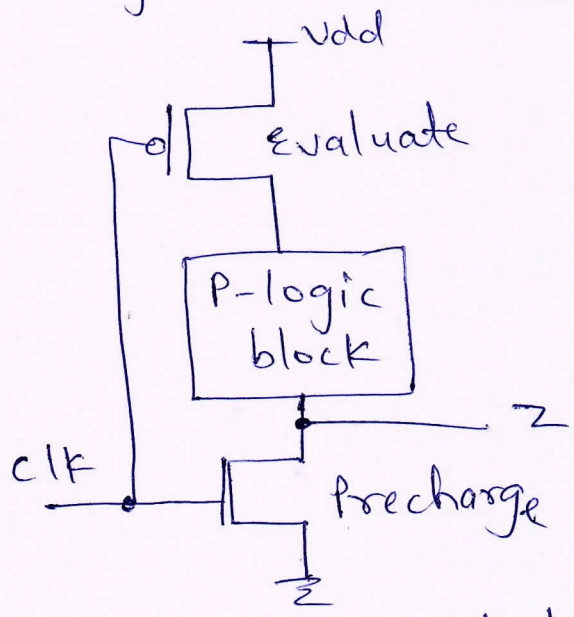
CMOS stick-diagram



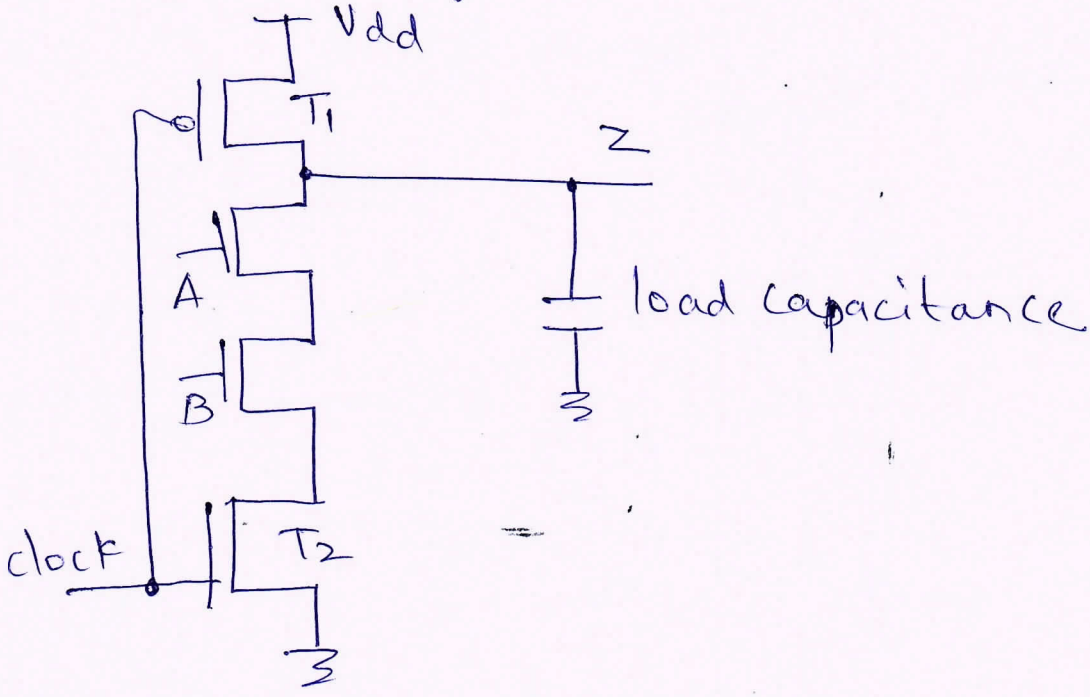
[8b] Explain dynamic CMOS logic with example – 8 Marks

Soln





→ Consider now a dynamic logic implementation of NAND gate.



→ The dynamic logic circuit requires 2 phases.

→ The first phase, when clock = 0, is called precharge phase.

→ second phase, when clock = 1, is called Evaluation phase.

→ when clock = 0, T_1 is ON, T_2 is off, the output node Z is precharged to Vdd, unconditionally (no matter the values of A & B)

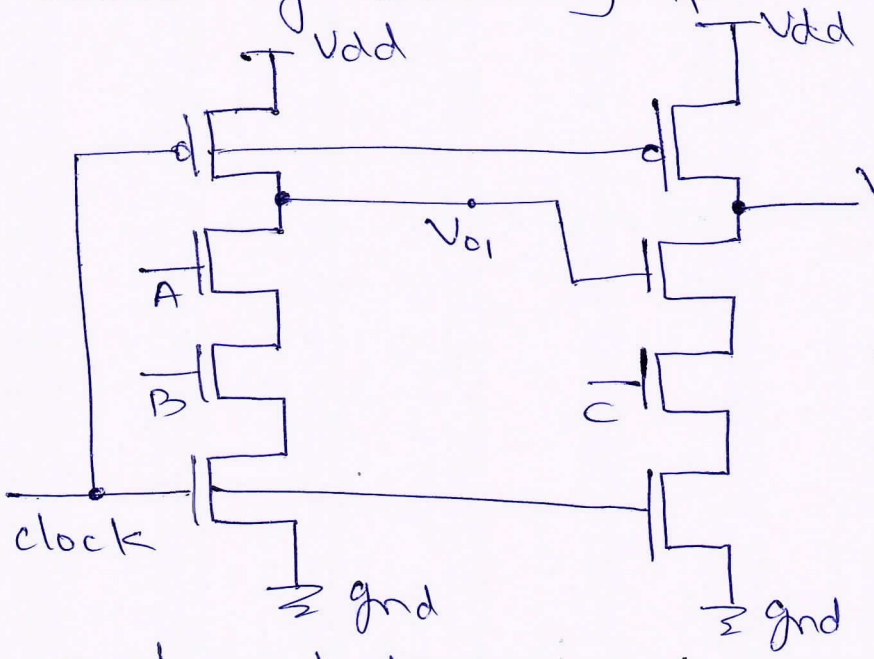
→ The load capacitor of this gate becomes charged because the transistor T_2 is turned off, it is impossible for the output to be connected to Vdd

→ During evaluation phase, clock = 1. If A & B are also high, the output will be pulled low ($z = 0$)

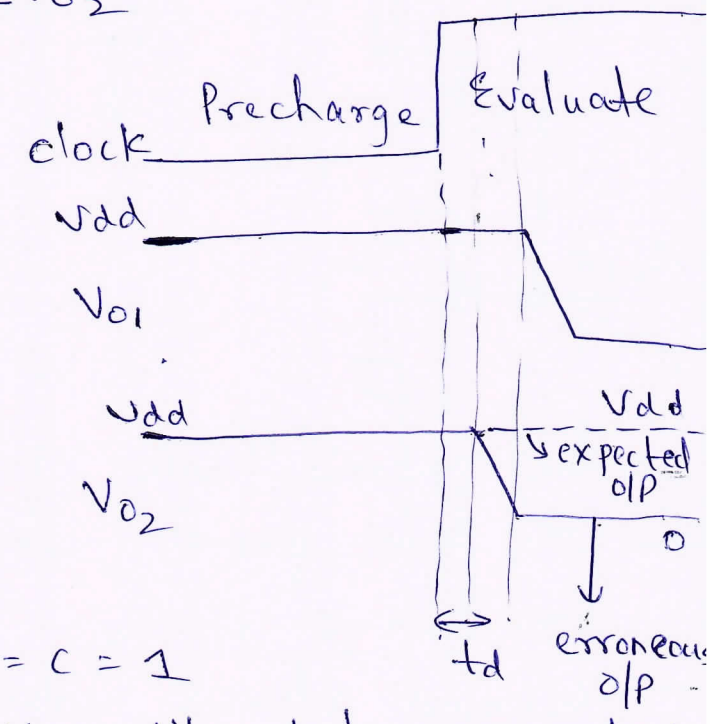
→ otherwise the output stays high due to load capacitance.

→ It requires (n+2) transistors. Has higher speed and lower area.

→ dynamic CMOS has a serious limitation, illustrated below by cascading of 2 NAND gates.



let A = B = C = 1



→ when clock = 0, V_{O_1} & V_{O_2} are precharged to Vdd.

→ when clock = 1, for A = B = C = 1

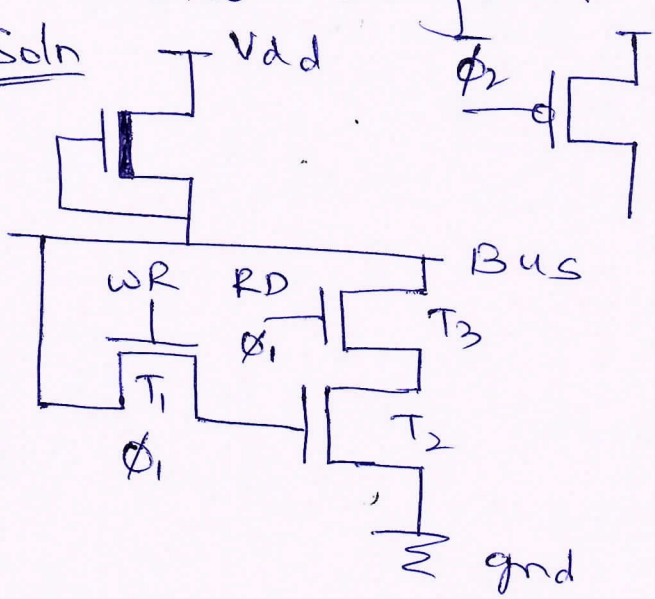
$\boxed{V_{O_1} = 0}$ & $\boxed{V_{O_2} = 1}$ But V_{O_2} will not be expected state

→ Reason is V_{O_1} will not go low, until its capacitance is completely discharged. Hence there will be propagation delay (td). But as C = 1, V_{O_2} will go low Thus we have erroneous o/p at V_{O_2}. Hence cascading is not possible with dynamic cmos

Module - 5

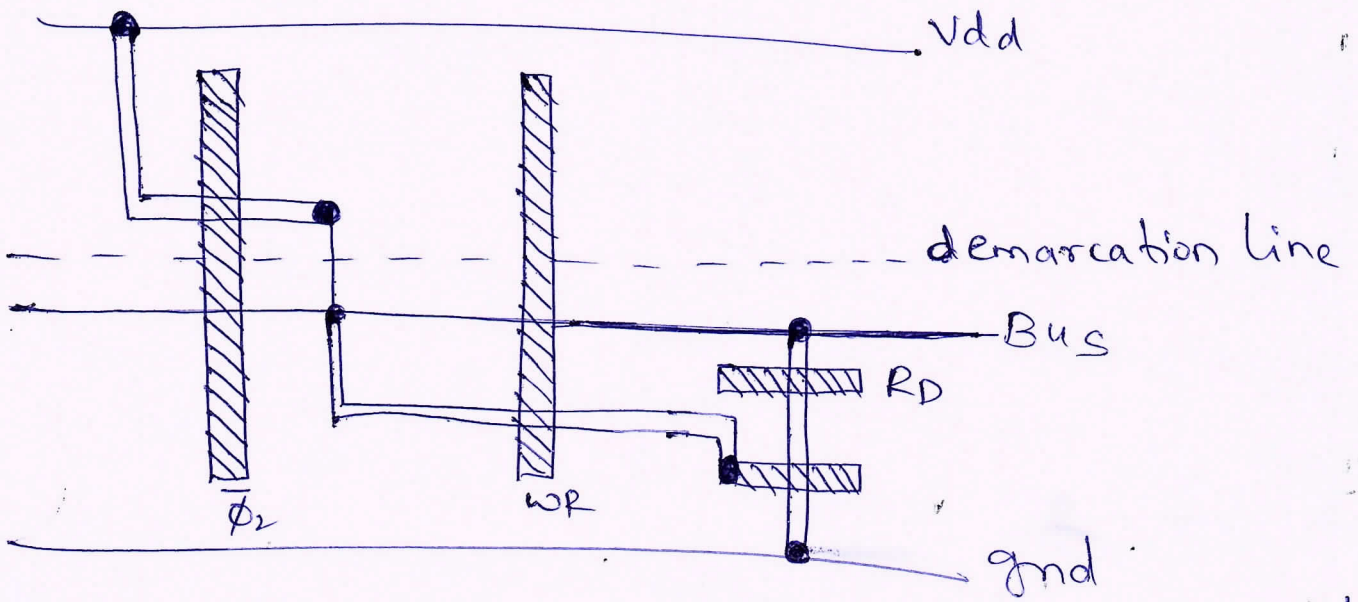
(9a) Explain 3 transistor dynamic RAM cell with schematic diagram. — 6 Marks

Soln



nMOS 3T DRAM cell

stick-diagram



→ with RD = 0, WR = 1, the logic level on bus is stored on gate capacitance of T_2. Then WR is made low again.

→ when both RD = WR = 0, bit valued is stored for sometime by C_g of T_2.

→ To read stored bit, make RD high and WR low & bus will be pulled to ground through T_3 & T_2 if a 1 was stored

→ otherwise T_2 will be non-conducting & bus will remain high due to pull-up circuit.

→ Complement of stored bit is read onto bus.

→ Cell is dynamic & will hold data as long as sufficient charge remains on C_g of T_2

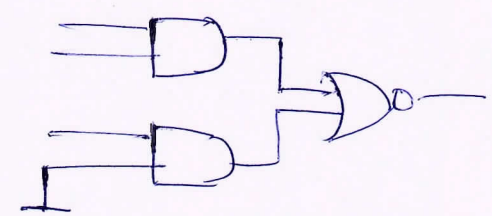
9b Explain any 2 fault-models in Combination Circuits — 6 Marks

Soln

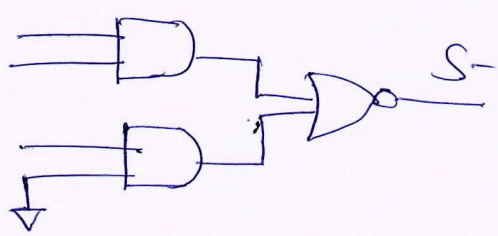
stuck-at-Faults

→ In stuck-at model, a faulty gate input is modeled as stuck-at zero (S-A-0) or stuck-at-one (S-A-1)

→ These faults occur due to gate-oxide shorts or metal-to-metal shorts.

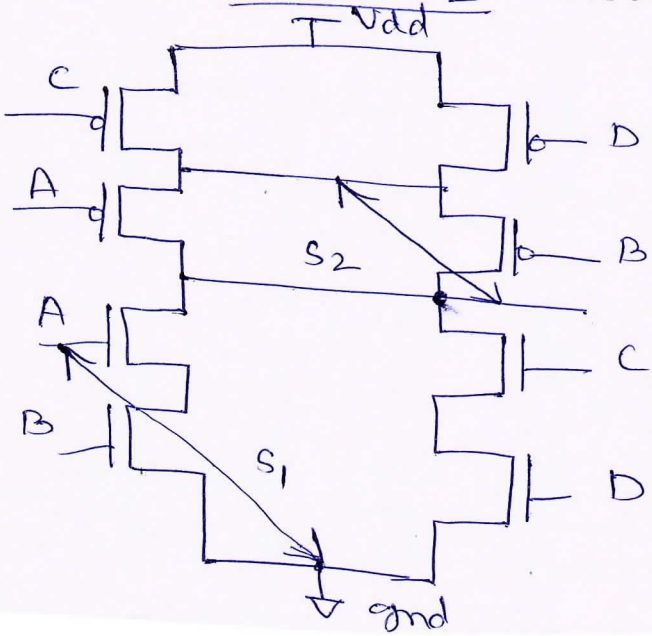


S-A-1 fault



short-Circuit and open-Circuit faults

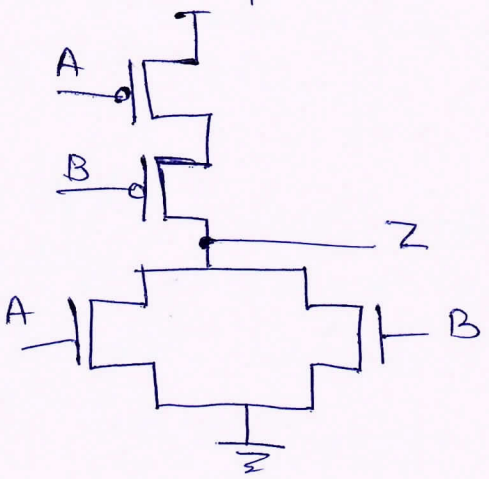
→ short S_1 results in S-A-0 fault at input A, while short S_2 modifies function of gate.



→ To ensure accurate modeling, faults should be modeled at transistor level because only at this level complete structure is known.

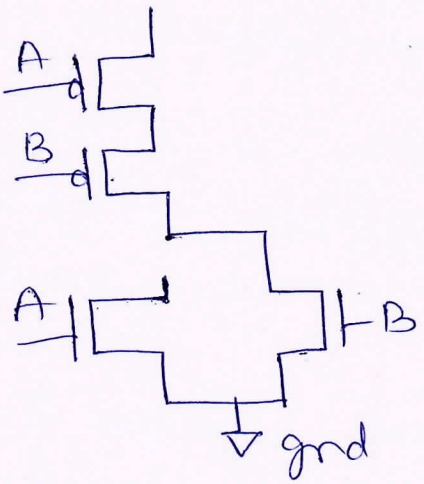
→ A problem that arises with CMOS is that it is possible for a fault to convert combinational circuit into sequential circuit.

Eg 2-input NOR gate



$$Z = \overline{A+B} = n(A|B)$$

→ If above circuit has open-circuit fault, the function will be



$$Z = n(A|B) \,|\, (nB \,\&\, Z')$$

where Z' is previous state of gate.

(9c) Write a note on automatic test pattern generation. — 4 Marks

Soln **Automatic Test pattern generation (ATPG).**

→ In IC industry, logic and circuit designers implemented the functions at RTL or schematic level, mask designers completed the layout and test engineers wrote the tests.

→ In many ways, the test engineers were the sherlock Holmes of the industry, reverse engineering circuits and devising tests that would test the circuits in an adequate manner

→ For the longest time, test engineers implored circuit designers to include extra circuitry to ease the burden of test generation

→ As processes have increased in density and chips have increased in complexity, the inclusion of test circuitry has become less of an overhead for both the designer and the manager worried about the cost of die.

→ As tools have improved, more of burden for generating tests has fallen on designers.

→ To deal with this burden, ATPG methods have been invented.

→ Commercial ATPG tools can achieve excellent fault coverage. However, they are computation-intensive and often must be run on servers or many parallel processors.

→ Adding scan & built-in self-test improves the observability of a system and reduces the number of test vectors required to achieve a desired fault-coverage.

Write short-notes on:
(i) Observability and Controllability
(ii) Built-in Self Test (BIST) — 8 Marks

Soln

Observability:

→ The observability of a particular circuit node is th degree to which you can observe that node at the outputs of an integrated circuit (i.e, pins)

→ This metric is relevant when you want to measure the output of a gate within a larger circuit to check that it operates correctly

→ Given the limited number of nodes that can be directly observed, it is the aim of good-chip designers to have easily observed gate outputs.

Controllability:

→ Controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

→ An easily controllable node would be directly settable via an input pad.

→ A node with little controllability requires thousands of cycles to get it to right state.

→ It is impossible to generate a test sequence to set a number of poorly controllable nodes into right state.

→ It should be aim of good-chip designers to make all nodes easily Controllable.

BIST (Built-in-Self Test)

→ The combination of signature analysis and the scan technique creates a structure known as **BIST**.

→ BIST is a scanable, resettable register that also can serve as a pattern generator and signature analyzer

→ C[1:0] specifies the mode of operation.

→ In reset mode (10), all the flip-flops are synchronously initialized to 0.

→ In normal mode (11), the flip-flops behave normally with their D input and Q-outputs.

→ In scan mode (00), the flip-flops are configured as a 3-bit shift register between SI and SO.

→ In test mode (01), the register behaves as pseudo-random sequence generator or signature analyzer

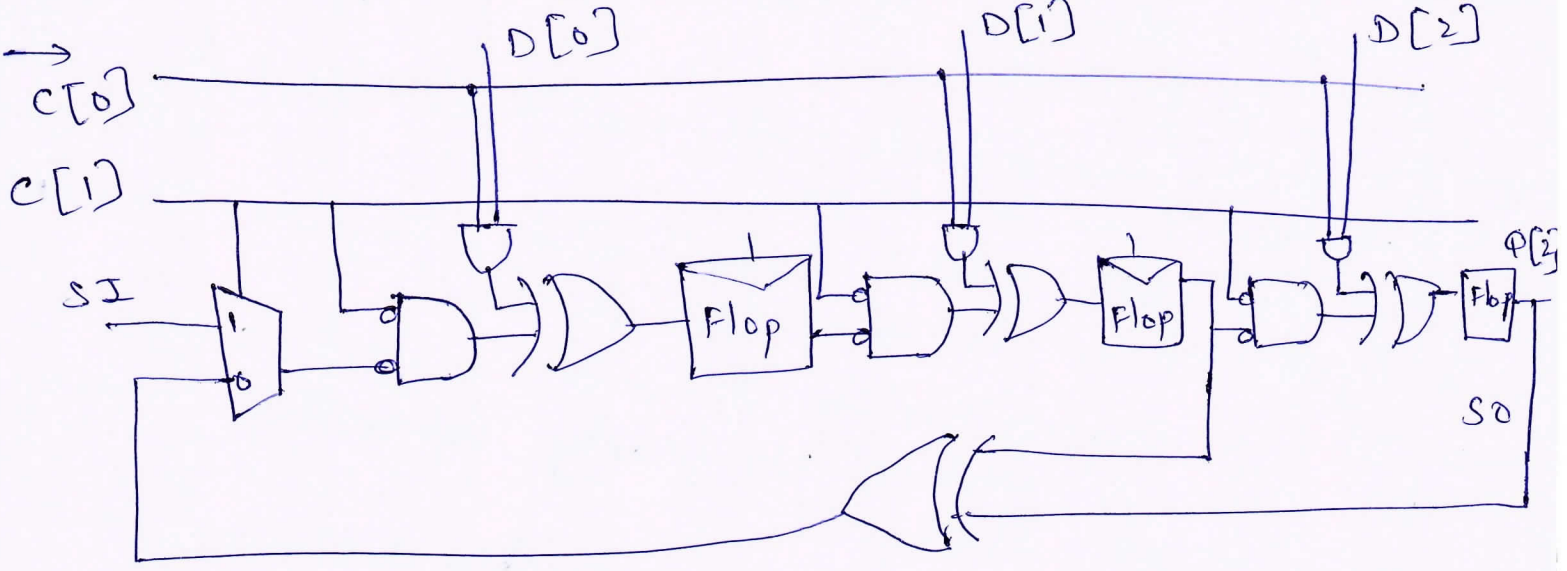


fig: BIST (3-bit register)

→ Bit is written on activating WR line, which occurs with ϕ_1 of clock.

→ Bit is stored on gate-capacitance (Cg) of inverter-1, which will produce complemented O/P at inverter-1 & true at o/p of inverter-2.

→ At every ϕ_2 stored bit is refreshed through gated feedback path.

→ To read stored bit, R_D is made high, which occurs with ϕ_1 of clock.

→ ϕ_2 is used for refreshing, hence no data to be read, if so charge-sharing effect occurs leading to destruction of stored bit

→ WR & RD must be mutually exclusive.

br

10b Explain nmos pseudo-static RAM cell with schematic diagram — 8 Marks

Soln

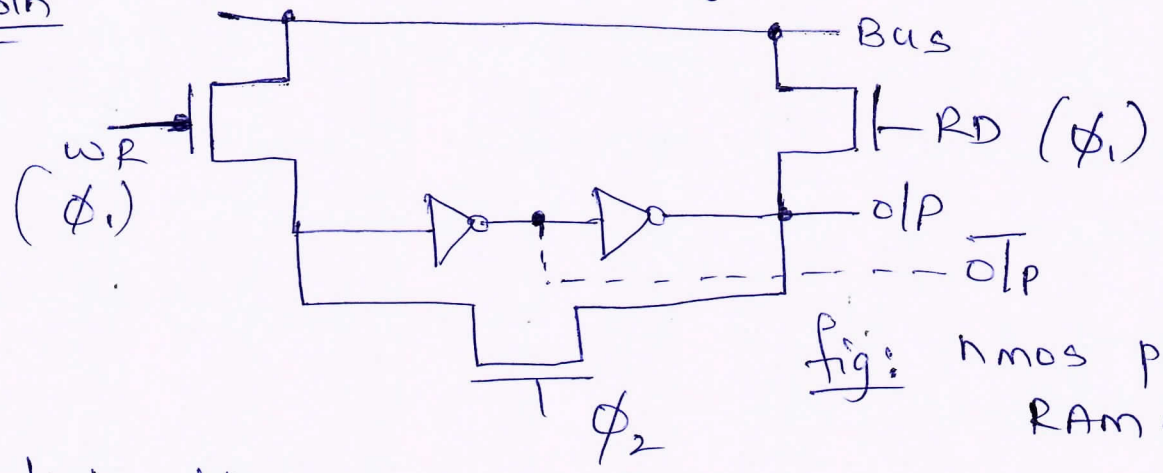
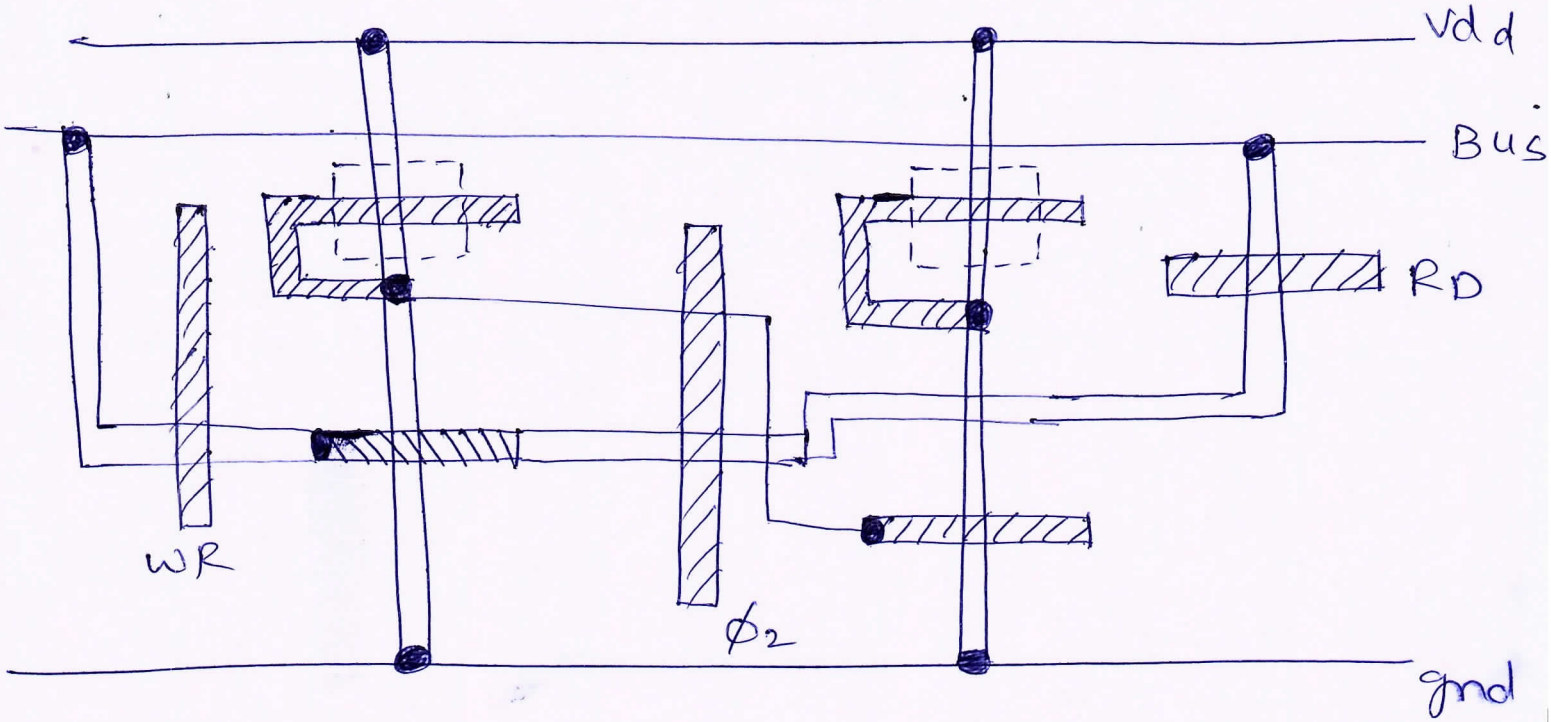


fig: nmos pseudo-static RAM cell

stick-diagram



→ DRAM needs to be refreshed periodically & hence not convenient.

→ Hence Pseudo-static RAM is designed which holds data indefinitely

→ 2 back-to-back inverters form a basic bistable element which is our memory

→ ϕ_2 is used to refresh the data every clock cycle.