Model Question Paper-1 with effect from 2019-20 (CBCS Scheme)

USN | | | | | | | | | | |

Fourth Semester B.E. Degree Examination

Subject Title: Analog Circuits

TIME: 03 Hours **Max. Marks: 100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	Explain the design constraints of a classical discrete-circuit biasing arrangement with circuit and relevant equations. How does R_E provide a negative feedback action to stabilize the bias current?	L2	8
	b	Considering the conceptual circuit of common emitter configuration, derive the expressions for g_m, r_Π, and r_e. Draw the hybrid –Π model of a transistor.	L1,L2	8
	c	A BJT having β=120 is biased at a DC collector current of 1 mA. Find the value of g_m, r_e , r_Π at the bias point .	L3	4
		OR		
Q.02	a	Design a fixed V_G bias circuit using Voltage divider arrangement to establish a DC drain current of 0.5mA. The MOSFET is specified to have V_t=1V, K_n'W/L=1mA/V^2 $\{\lambda = 0\}$. Use V_{DD} = 12V.Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another MOSFET having the same k_n'W/L but V_t = 1.5V.	L3	10
	b	Explain the MOSFET biasing technique using a large drain-to-gate feedback resistance R_G. Design the drain-to-gate feedback biasing circuit to operate at a DC drain current of 0.5mA. Assume V_{DD} =5V, k_n'W/L=1mA/V^2, λ=0.	L3	6
	c	Draw and explain the small signal model of the MOSFET assuming $\lambda \neq$ 0.	L1	4
		Module-2		
Q. 03	a	With a neat circuit diagram and ac equivalent circuit derive the expressions for R_{in}, A_{vo}, A_v and R_o for common source amplifier with an unbypassed source resistance.	L2	8
	b	Explain the internal capacitances of a MOSFET and hence draw the high frequency small signal model of MOSFET.	L1,L2	6
	c	For the n-channel MOSFET with t_{ox}=10nm, L=1µm, W=10µm, L_{OV}=0.05 µm, C_{sbo} = C_{dbo} = 10fF, V_O=0.6V, V_{SB}=1V and V_{DS}=2V. Calculate i)C_{OX} ii)C_{OV} iii)C_{gs} iv)C_{gd} v)C_{sb} vi)C_{db}	L3	6
		OR		
Q.04	a	Derive the expression for low frequency response of a common source amplifier.	L1,L2	8
	b	It is desired to design a phase-shift oscillator (Self biased JEFT amplifier) using a JEFT having g_m=5000µs, r_d =40kΩ, and feedback circuit resistance of R=10kΩ. Select the value of 'C' for oscillator operation at 1 kHz and R_D for a gain A=40 to ensure oscillator action.	L3	4

09.07.2021

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Scheme & Solution Prepared by

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	c	With a neat diagram explain working of a crystal oscillator. Explain series and parallel resonance action with equivalent circuits and relevant expressions. A crystal has L=0.334H, C=0.065pF, C_M=1pF and R=5.5kΩ. Calculate its series and parallel resonant frequency.	L3	8
		Module-3		
Q. 05	a	With a neat block diagram explain the working of a negative feedback amplifier. How is the overall gain affected in these amplifiers?	L1,L2	8
	b	Determine the voltage gain, input and output impedance with feedback for a voltage series feedback amplifier having A= -100, R_i=10k Ω, R_o=20kΩ for a feedback of i)β=1 and ii)β= -0.5	L3	8
	c	Draw the four basic negative-feedback topologies.	L1	4
		OR		
Q. 06	a	Define power amplifiers and list the types of power amplifiers based on the location of Q point, conduction angle, efficiency and applications.	L1,L2	8
	b	Prove that the maximum conversion efficiency of a transformer coupled Class A amplifier is 50%.	L2	6
	c	Calculate the efficiency of a transformer coupled Class B amplifier for a supply of 12V and peak output voltage of 6V.	L3	2
	d	Explain in brief the working of a Class C power amplifier.		4
		Module-4		
Q. 07	a	How does negative feedback affect the performances of an inverting amplifier using opamp? Derive the relevant expressions for Gain, input resistance and output resistance.	L2	8
	b	The opamp 714C is connected as an inverting amplifier with R_I=1kΩ and R_F=4.7kΩ. Compute the closed loop parameters: A_F, R_{IF}, R_{OF}, f_F. Given A=400000, R_i=33MΩ and R_O=60Ω; supply voltages are ± 13V; Max output voltage swing = ± 13V, Unity gain bandwidth = 0.6MHz .	L3	6
	c	With a neat circuit diagram explain the opamp based inverting scaling amplifier and averaging circuit with relevant expressions for the output.	L1,L2	6
		OR		
Q. 08	a	What is an instrumentation amplifier? What are its applications? With a neat circuit diagram explain an instrumentation amplifier using a transducer bridge.	L1,L2	10
	b	Draw the circuit and waveforms for an inverting Schmitt Trigger using opamp, with relevant expressions.	L1	4
	c	For an inverting Schmitt Trigger circuit R_1 = 15KΩ ; R_2 = 1KΩ and V_{in} = 10$V_{p\text{-}pp}$ sine wave. The saturation voltages are ± 14V and V_{ref}= 2 V. i) Determine the threshold voltages V_{ut} and V_{lt}. ii) Find the value of Hysteresis voltage V_{hy}.	L3	6
		Module-5		
Q. 09	a	Explain the working of a Successive Approximation type of ADC.	L2	8
	b	Explain with a neat circuit diagram, the working of a small signal half wave precision rectifier using an Opamp.	L2	4
	c	What is R-2R network type DAC? Explain with relevant expressions.	L1,L2	8
		OR		
Q. 10	a	Explain the working of a second order high pass Butterworth filter with a neat circuit diagram and frequency response. Write the relevant design equations.	L1,L2	6
	b	Explain the operation of 555 timer as a Monostable multivibrator with relevant expressions.	L1,L2	8

	c	In an astable multivibrator $R_A = 2.2\ K\Omega$; $R_B = 3.9\ K\Omega$ and $C = 0.1\mu F$. Determine the positive pulse width T_c and negative pulse th T_d and free running frequency 'f_o'.	L3	6

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

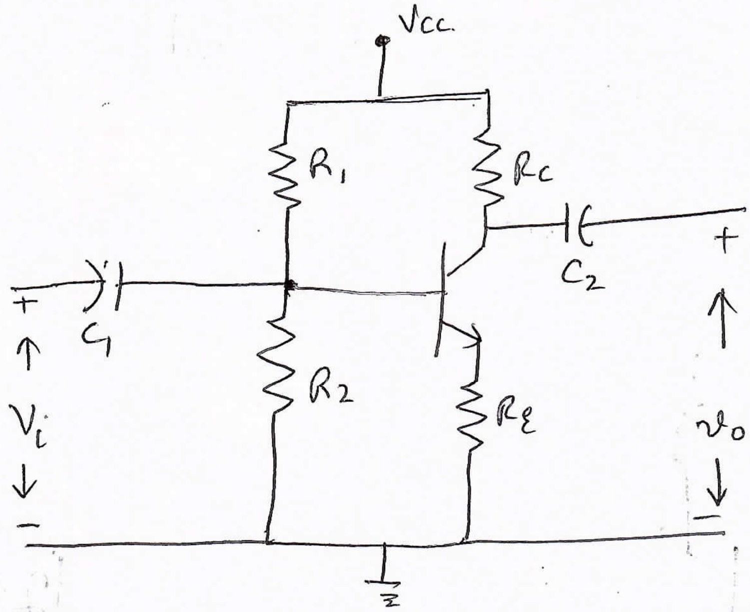
Model Question paper - 1

Subject Name :- A.C. **Subject. Code :- 18EC42.**

PART - A

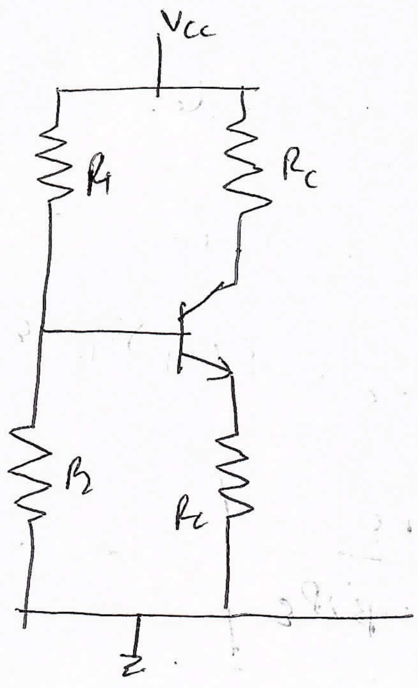
Total Marks (8M)

1a) Voltage divider bias Circuit

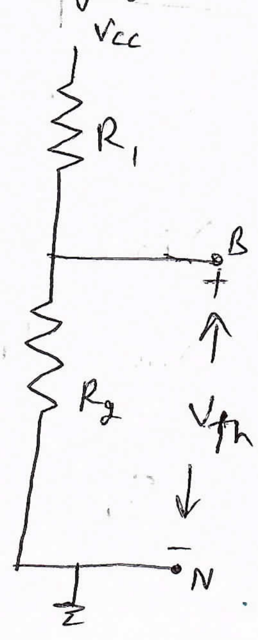


— (2M)

To obtain DC Equivalent Circuit



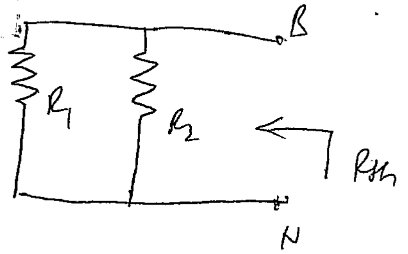
Applying thevenin Equivalent ckt



To find V_{th}

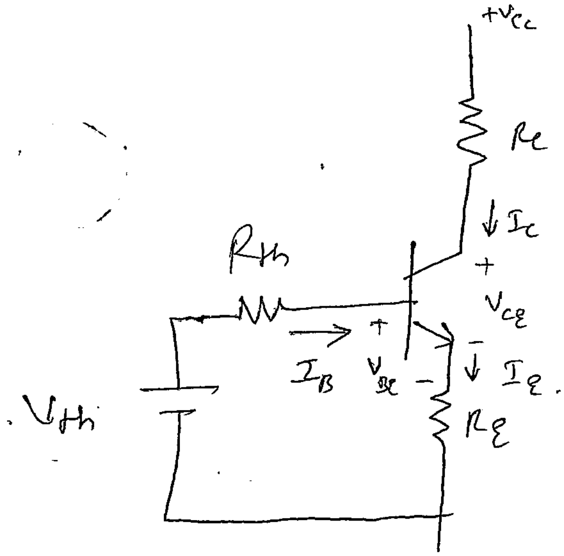
$$V_{th} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

To find R_{th}



$R_{th} = R_1 \| R_2$

Thevenin Equivalent Circuit



2m

Application of KVL at input side.

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E \longrightarrow (1)$$

$$V_{th} = I_B R_{th} + V_{BE} + (1+\beta) I_B R_E$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E} \longrightarrow (2)$$

$$I_C = \beta I_B$$

$$I_E = (1+\beta) I_B$$

$$= (1+\beta) \frac{(V_{th} - V_{BE})}{R_{th} + (1+\beta)R_E}$$

$$\boxed{I_E = \frac{V_{th} - V_{BE}}{R_{th} + \frac{R_E}{(1+\beta)}}} \rightarrow (3)$$

-(2M)

Applying KCL at o/p side

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E.$$

At o/p side. $I_C \approx I_E$.

$$\therefore \boxed{V_{CC} = I_C (R_C + R_E) + V_{CE}} \rightarrow (4)$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E \rightarrow (5)$$

from eqn (1)

$$V_{th} - V_{BE} = I_B R_T + I_E R_E.$$

Since $V_{th} - V_{BE}$ = Constant, when temp. increases

1) I_C increases $\rightarrow$ ($\because I_C = \beta I_B$)

2) $I_E R_E$ increases.

3) Since, $V_{th} - V_{BE}$ is constant, $I_B R_{th}$ should decrease (4)

4) Hence I_C decreases

5) Increase in I_C is reflected in increase in $I_E R_E$ which in-turn causes I_C to decrease.

Here R_E causes -ve feedback to maintain stability in circuit.

Design constraints.

1) $V_E = \frac{V_{CC}}{10}$ & $V_{CE} = \frac{V_{CC}}{2}$.

2) $R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C}$

3) $R_2 \leq \frac{\beta R_E}{10}$ → (2M)

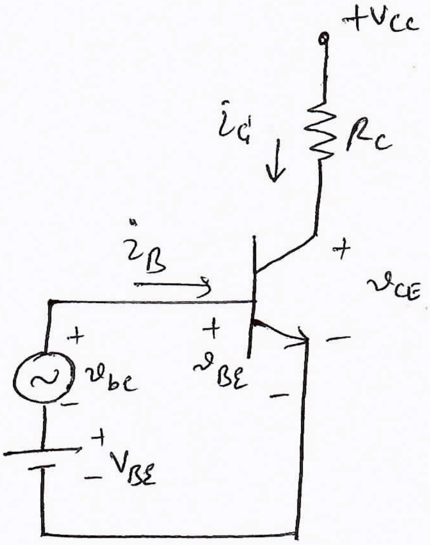
4) $V_B = V_{th} = \frac{V_{CC} \times R_2}{R_1 + R_2}$.

5) $R_C = \frac{V_{CC} - V_C}{I_C}$.

1b) Expression for gm.

(5) 19

Total Marks (8M)



→ (1M)

1) In the above figure we can see that base-Emitter junction is forward biased by V_{BE} & CB jn is ~~forward~~ Reverse biased by Vcc.

2) Small signal voltage v_{be} is applied to base of transistor, ∴ instantaneous value of BE voltage is given by

$$v_{BE} = V_{BE} + v_{be} \rightarrow (1)$$

WKT,

$$i_C = I_S e^{v_{BE}/V_T} \rightarrow (2)$$

Substituting (1) in (2)

$$i_C = I_S e^{(V_{BE} + v_{be})/V_T}$$

$$i_C = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$

$$i_C = I_C e^{v_{be}/V_T} \rightarrow (3)$$

Since $v_{be} << V_T$, we can write ③ as ⑥

20

$$i_C = I_C \left(1 + \frac{v_{be}}{V_T}\right)$$

$$\therefore \quad i_C = I_C + \frac{I_C \, v_{be}}{V_T} \rightarrow ④$$

$$i_C = i_c + I_C \rightarrow ⑤$$

WKT

Comparing ④ & ⑤

$$i_c = \frac{I_c}{V_T} v_{be} \rightarrow ⑥$$

$$i_c = g_m v_{be} \rightarrow 7$$

$$\therefore g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T} \rightarrow ⑧$$

2M.

2) r_π

WKT.,

$$i_B = \frac{i_C}{\beta} \rightarrow (9)$$

$$\therefore i_B = \frac{I_C}{\beta} + \frac{I_C}{\beta V_T} v_{be} \rightarrow (10)$$

Since

$$i_B = I_B + i_b \rightarrow (11)$$

Comparing (10) & (11)

$$I_B = \frac{I_C}{\beta} \rightarrow (12)$$

$$i_b = \frac{1}{\beta} \frac{I_C}{V_T} v_{be}. \rightarrow (13)$$

But $\frac{I_C}{V_T} = g_m$

2M

$$\therefore \boxed{i_b = \frac{g_m}{\beta} v_{be}} \rightarrow (14)$$

22

$$\therefore \boxed{r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m}} \rightarrow (15)$$

3) $$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} \rightarrow (16)$$

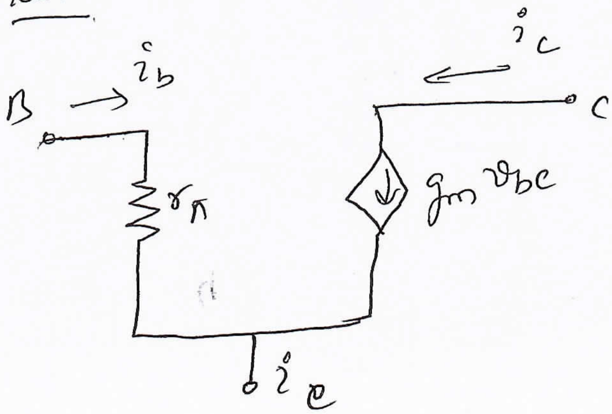
NKT $\quad i_E = I_E + i_e$

$$I_E = \frac{I_C}{\alpha}$$

$$i_e = \frac{i_c}{\alpha} = \frac{1}{\alpha}\frac{I_C}{V_T} v_{be} = \frac{I_E}{V_T} v_{be}$$

$$\therefore \boxed{r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E}} \rightarrow (17) \qquad \boxed{2M}$$

Hybrid π - model



$\boxed{1M}$

Total Marks (9)

(4M) 25

1c) Given. $\beta = 120$ $I_C = 1mA$.

1) $g_m = \frac{I_C}{V_T} = \frac{1mA}{25mV}$

$= 40 mA/V$.

↳ [2M]

2) $r_e = \frac{1}{g_m} = \frac{1}{40mA/V} = 25\Omega$

↳ [1M]

3) $r_\pi = (1+\beta) r_e$

$= (1+120) 25\Omega$.

$= 3K\Omega$ //

↳ [1M]

26

2a) Given:-

$I_D = 0.5\,mA$ $\quad K_n' W/L = 1\,mA/V^2$

$V_t = 1V$ $\quad V_{DD} = 12V$.

Total Marks [10] M

Soln:-

As a thumb rule we choose R_D & R_S to provide $1/3\ V_{CC}$ as drop across R_D

for $V_{DD} = 12V$, we get.

$V_D = +8V$, $V_S = +4V$.

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12-8}{0.5m} = 8K\Omega$$

$$R_S = \frac{V_S}{I_S} = 8K\Omega$$ — 2M

To find V_{GS},

$$I_D = \frac{1}{2} K_n'\left(\frac{W}{L}\right) V_{ov}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{ov}^2.$$

$V_{ov} = 1V.$

(11)

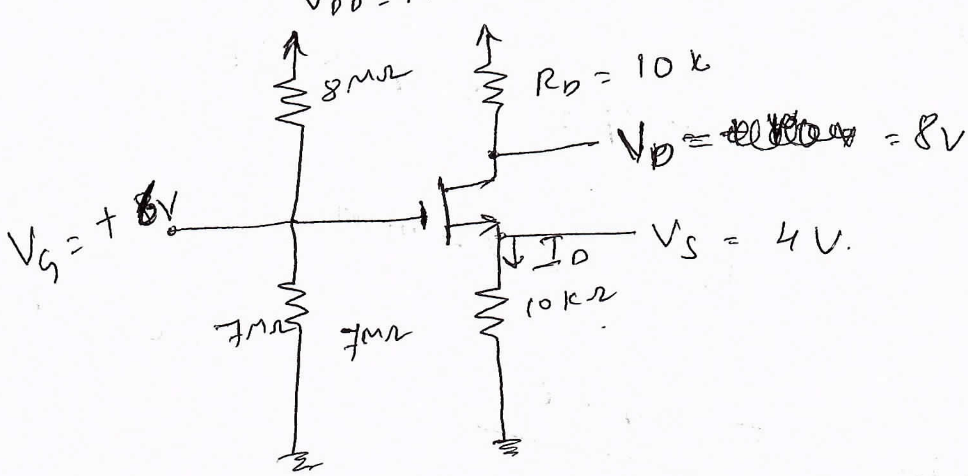
$\therefore \quad V_{GS} = V_t + V_{ov} = 1+1 = 2V \rightarrow$ [1M]

27

Since $V_S = +4V.$

$V_G = V_S + V_{GS} = 2+4 = 6V. \rightarrow$ [1M]

To establish this voltage we select $R_{G1} = 8M\Omega$, $R_{G2} = 7$.



$\rightarrow$ [2M]

ii) for $V_t = 1.5V$

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \rightarrow (1)$$

But

$$V_G = V_{GS} + I_D R_S$$

$$6 = V_{GS} + 8k\Omega \times I_D \rightarrow (2)$$

$\rightarrow$ ~~V_{GS}^2 ...~~

Substituting (1) in (2) we get (12)

$$6 = V_{GS} + 8\left(\frac{1}{2}(V_{GS} - 1.5)^2\right)$$

Solving we get

$$V_{GS} = 2.44V. \rightarrow (3) \quad \boxed{2M}$$

Substituting (3) in (2) we get

$$6 = 2.44 + 8k\Omega \times I_D$$

$$\therefore I_D = 0.44\,mA.$$

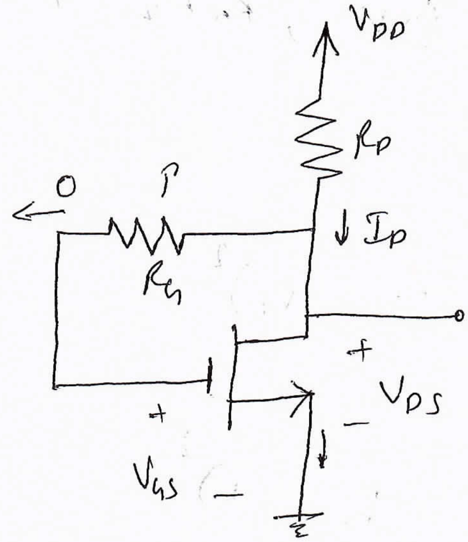
$$\therefore \Delta I_D = 0.44 - 0.5 = -0.06\,mA.$$

$$\therefore \%\ change = -\frac{0.06}{0.5} \times 100 = -12\%$$

$\hookrightarrow \boxed{2M}$

13)
2b) Biasing using drain to Gate feedback Resistor. (13)

Total Mark : 6M 33



1M

1) The above figure shows biasing using Drain to greate feedback

2) Here Large feedback resistance R_G forces the dc voltage at the gate to be equal to that of drain. ($\because I_G = 0$)

Hence
$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$\therefore V_{DD} = V_{GS} + I_D R_D$$ 1M

3) If I_D increases for some reason then V_{GS} should decrease. Hence decrease in V_{GS} inturn decreases I_D.

4) Thus -ve f/b or degeneration provided by R_G helps

to keep I_D as constant as possible

34

Given :- $I_D = 0.5mA$, $V_{DD} = 5V$, $k_n' W/L = 1mA/V^2$,

$V_t = 1V$ & $\lambda = 0$.

WKT $I_D = \frac{1}{2} \times k_n' \frac{W}{L} \times (V_{GS} - V_t)^2$

$0.5 = \frac{1}{2} \times (1) \times (V_{GS} - 1)^2$

$1 = (V_{GS} - 1)^2$

$\therefore V_{GS} = 2$ — 1M

To find R_D

$V_{DD} = V_{GS} + I_D R_D$

$5 = 2 + (0.5m) R_D$

$R_D = 6 k\Omega$

$\simeq 6.2 k\Omega$ (std) 1M

To find I_D for $R_D = 6.2k\Omega$

$V_{DD} = V_{GS} + I_D R_D$

$5 = 2 + I_D (6.2k\Omega)$

$I_D = 0.48mA$ — 1M

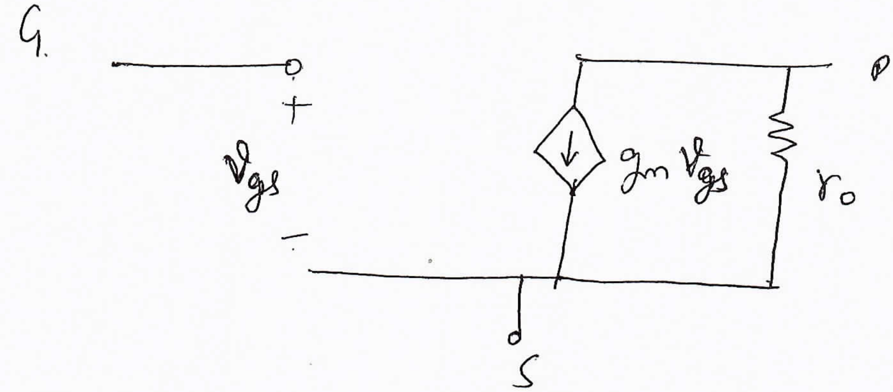
$\therefore V_D = V_{DS} = V_{DD} - R_D I_D$

$V_D = 1.96\,V$ — 1M

35

2c) <u>Small Signal Equivalent Circuit Model</u>

4M — Total Marks



— 1M

1) From signal point of view FET behaves like voltage controlled current source. It ~~provides~~ accepts signal v_{gs} & provides current $g_m v_{gs}$ at drain terminal.

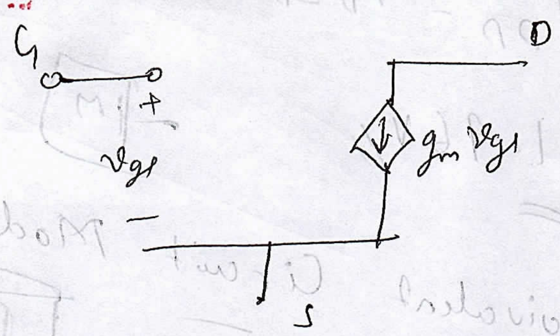
2) Since i/p resistance is very high. ~~∴~~ the input side i.e Gate & source side is replaced by open ckt.

→ 1M

3) $r_o = \dfrac{|V_A|}{I_D}$

But $V_A = 1/\lambda$ → 1M

If $\lambda = 0$ $V_A = \infty$ $\therefore r_o = 0$. we get



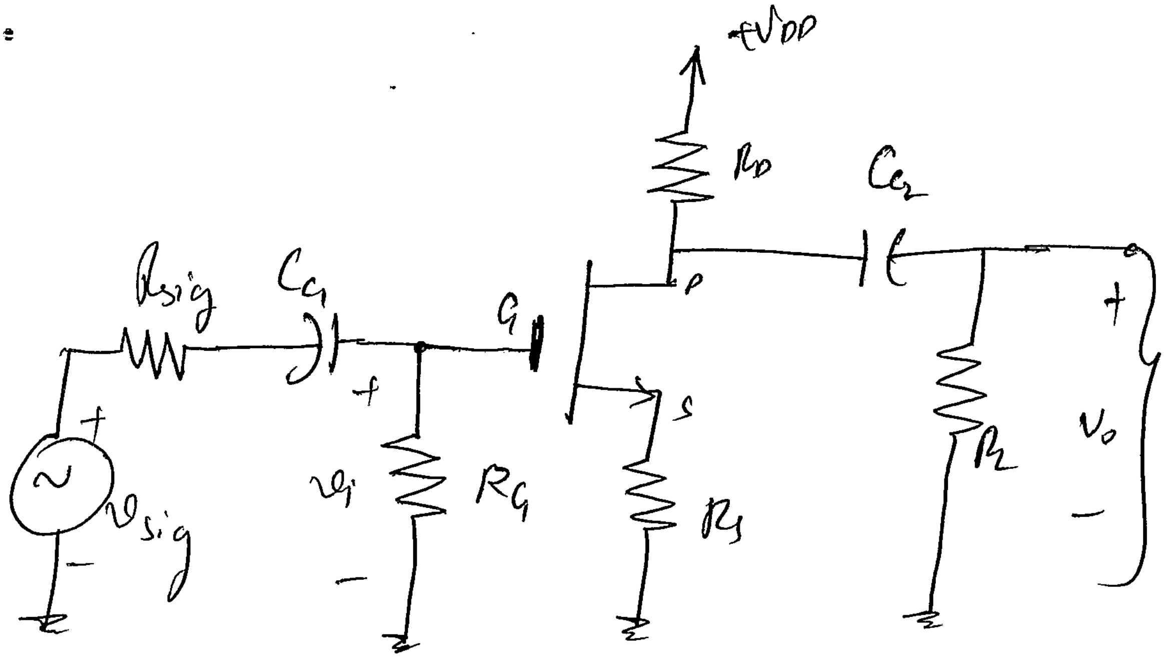
(1

— |M|

3a) C.S. Amplifier with unbypassed source Resistance

5-2

Total Marks 8M

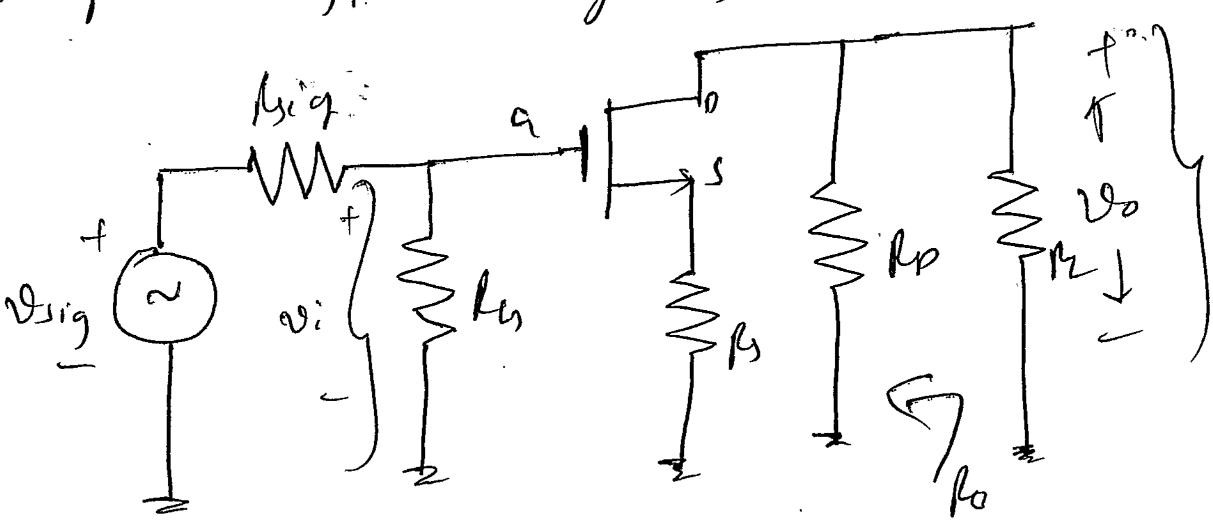


— (1M)

1) Figure shows common source amplr. with source resistance Rs.

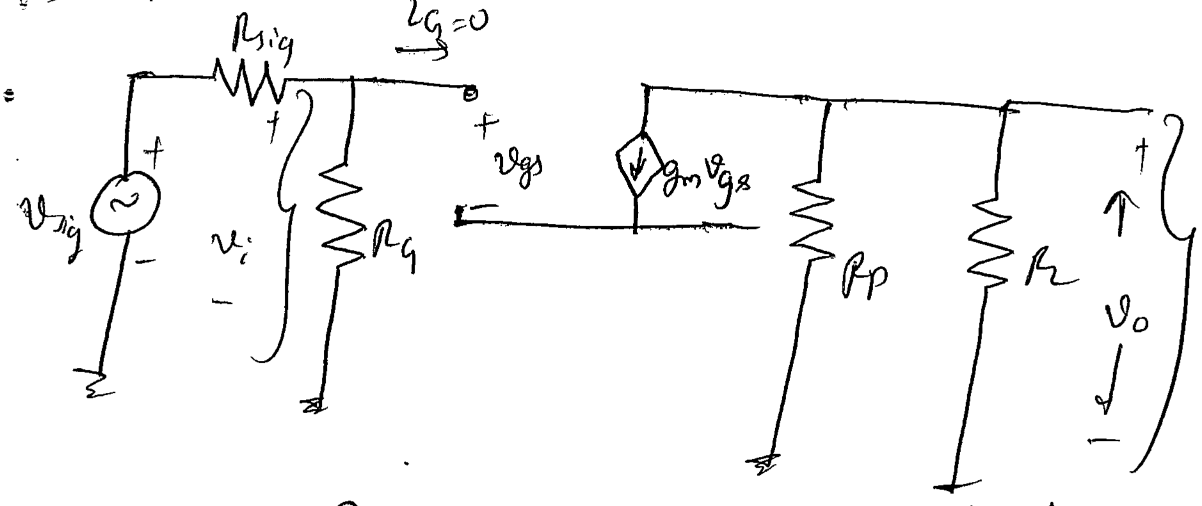
2) Here input signal is applied to gate via Rsig & o/p signal v_o is taken at drain.

3) Rs stabilizes the operating point of MOSFET under variation in MOSFET parameter such as temperature, current gain, transconductance etc



→ (1M)

(53)



(2M)

Small Signal Equivalent circuit.

6) Looking at i/p side $= i_g = 0$.

7) I/p resistance R_{in} is given by.

$$\boxed{R_{in} = R_G} \rightarrow (1)$$

Usually R_G will be (1MΩ - 10MΩ)

8) $$\boxed{v_i = \frac{v_{sig} \times R_G}{R_G + R_{sig}}} \rightarrow (2)$$

(1M)

But $R_G >> R_{sig}$ Hence

$$v_i = \frac{R_G}{R_G} \times v_{sig}$$

$$\boxed{v_i = v_{sig}} \rightarrow (3)$$

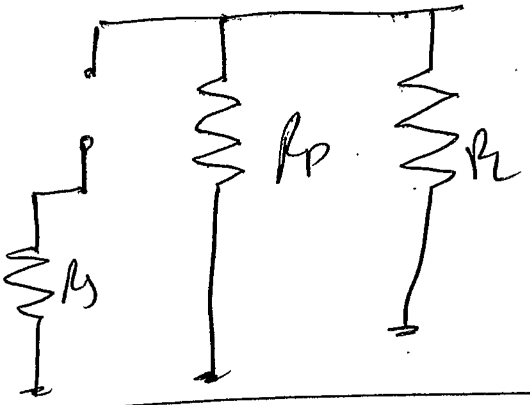
Applying KVL at input side

$$\boxed{v_i = v_{gs}(1 + g_m R_S)} \rightarrow (4)$$

10) Make $v_i = 0$ we get $v_{gs} = 0$

we get

(57)



$$R_o = R_D$$

11) $$v_o = -g_m v_{gs} (R_D \| R_L)$$ → (5)

12) $$A_v = \frac{v_o}{v_{in}} = \frac{-g_m v_{gs} (R_D \| R_L)}{v_{gs} (1 + g_m R_S)}$$

$$A_v = \frac{-g_m (R_D \| R_L)}{(1 + g_m R_S)}$$ → (6)

→ (2M)

13) To find A_{v_o} we make $R_L = \infty$

$$A_{v_o} = \frac{-g_m R_D}{(1 + g_m R_S)}$$ → (7)

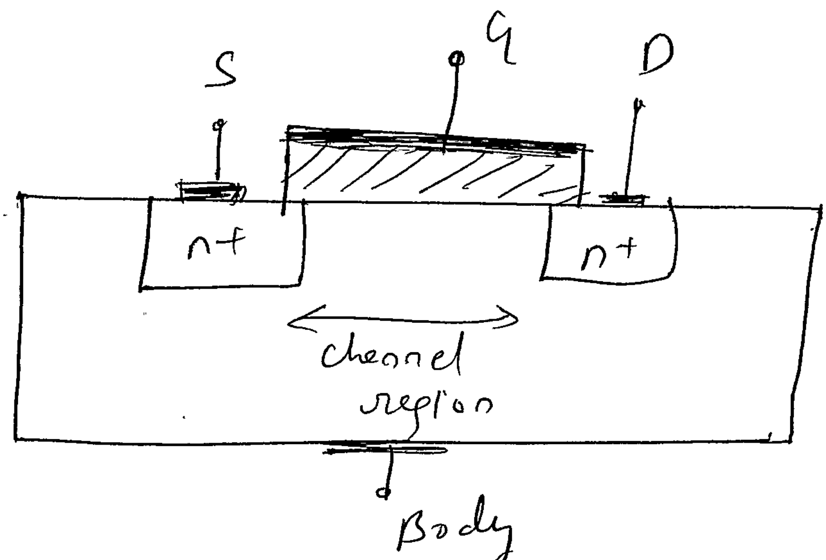
14) Since $v_i = v_{sig}$

$$G_v = A_v = \frac{v_o}{v_i} = \frac{-g_m (R_D \| R_L)}{(1 + g_m R_S)}$$ → (8)

→ (2M)

3b) MOSFET internal capacitance

(58)



Total mark
6M

There are basically 2 types of internal capacitance in MOSFET.

1) Gate Capacitive Effect :- Gate electrode along with channel forms parallel plate with SiO_2 acting as dielectric

2) The source & drain depletion layer Capacitor :-

When source & drain are reverse biased depletion region will be created b/w drain n+ & p-substrate & also b/w Source & substrate.

→ (1M)

1) The Gate capacitive effect.

It can be modelled by
C_{gs}, C_{gd}, C_{gb}.

1) When MOSFET is operating in triode region (5M)
Where V_{DS} will be small & channel will be uniform ; we have

$$C_{gs} = C_{gd} = \frac{1}{2} W L C_{ox} \rightarrow (1)$$

(1/2 M)

2) When MOSFET is operating in satn region, where V_{DS} will be large & channel at drain end is zero, we have

$$C_{gs} = \frac{2}{3} W L C_{ox} \rightarrow (2)$$

(1/2 M)

$$C_{gd} = 0.$$

3) When MOSFET is in cutoff region the channel disappears, then we have

$$C_{gs} = C_{gd} = 0$$

$$C_{gb} = W L C_{ox} \rightarrow (3)$$

(1/2 M)

4) $$C_{ov} = W L_{ov} C_{ox} \rightarrow (4)$$

(1/2 M)

2) Junction Capacitance

When source & drain are reverse biased, there will be capacitance formed b/w source (n+) & substrate (body) & also b/w drain (n+) & body.

This is given by

$$C_{SB} = \frac{C_{SB0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \rightarrow (5)$$

— (1M)

C_{SB0} = Capacitive value at zero reverse bias vol.

V_{SB} = Magnitude of reverse bias vol.

V_0 = Junction built in voltage. (0.6 to 0.8V)

$$C_{DB} = \frac{C_{DB0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} \rightarrow (6)$$

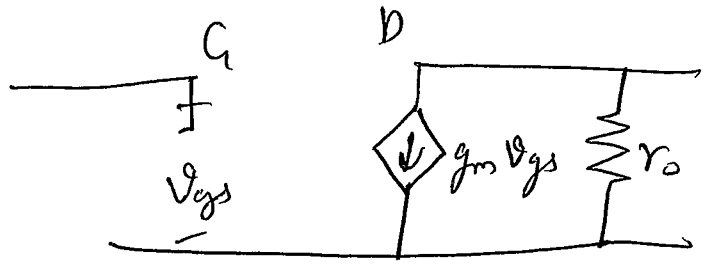
— (1M)

C_{db} = Capacitance at zero reverse bias vol.

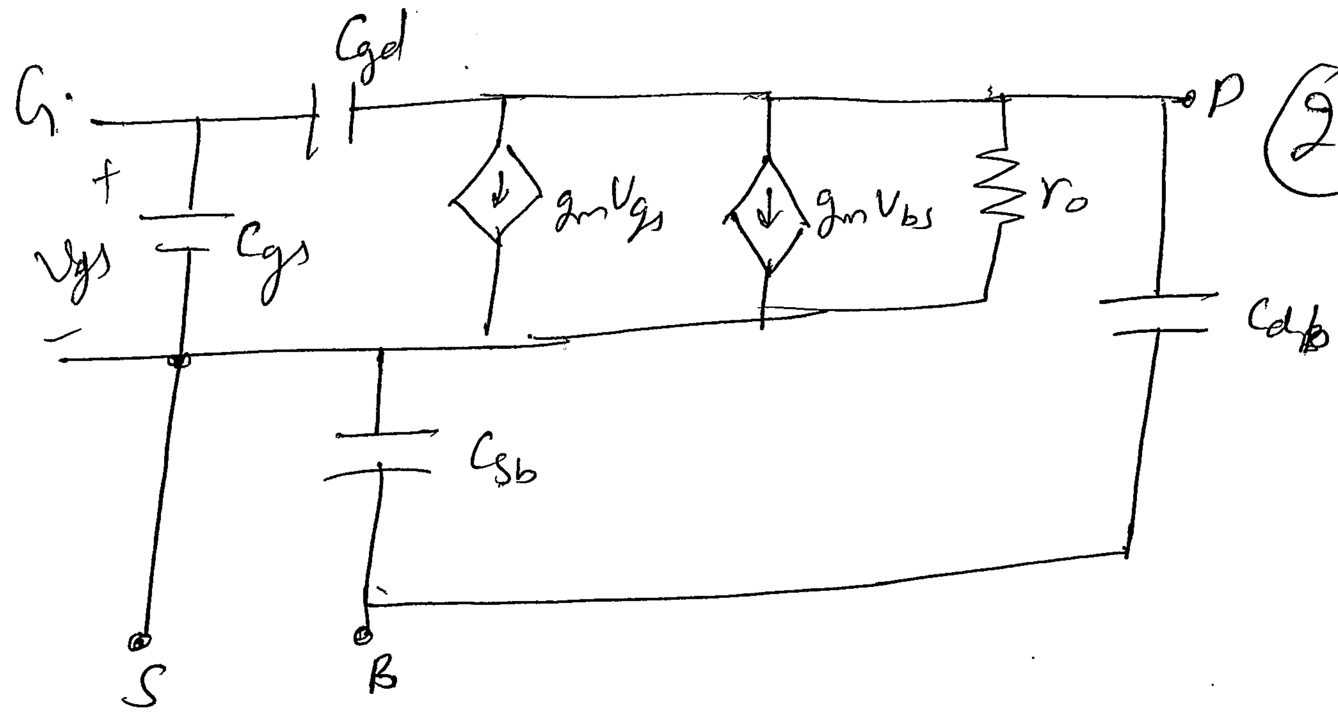
V_{dB} = Magnitude of " " "

V_0 = Junction built-in voltage (0.6 to 0.8V)

High frequency MOSFET model



(Small signal Equivalent Circuit)



2M

(High freq circuit of MOSFET)

Total Marks :- 6M

3c) $t_{ox} = 10nm$, $L = 1.0\mu m$, $W = 10\mu m$, $L_{ov} = 0.05\mu m$

$C_{sb0} = C_{db0} = 10fF$, $V_0 = 0.6V$, $V_{SB} = 1V$, $V_{DS} = 2V$.

1) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\,\varepsilon_0}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-12}}{10nm} = 3.45\ fF/\mu m^2$ → (1M)

2) $C_{ov} = W L_{ov} C_{ox} = 1.72\ fF$ → (1M)

3) $C_{gs} = \frac{2}{3} W L C_{ox} = 24.7\ fF$ → (1M)

(89)

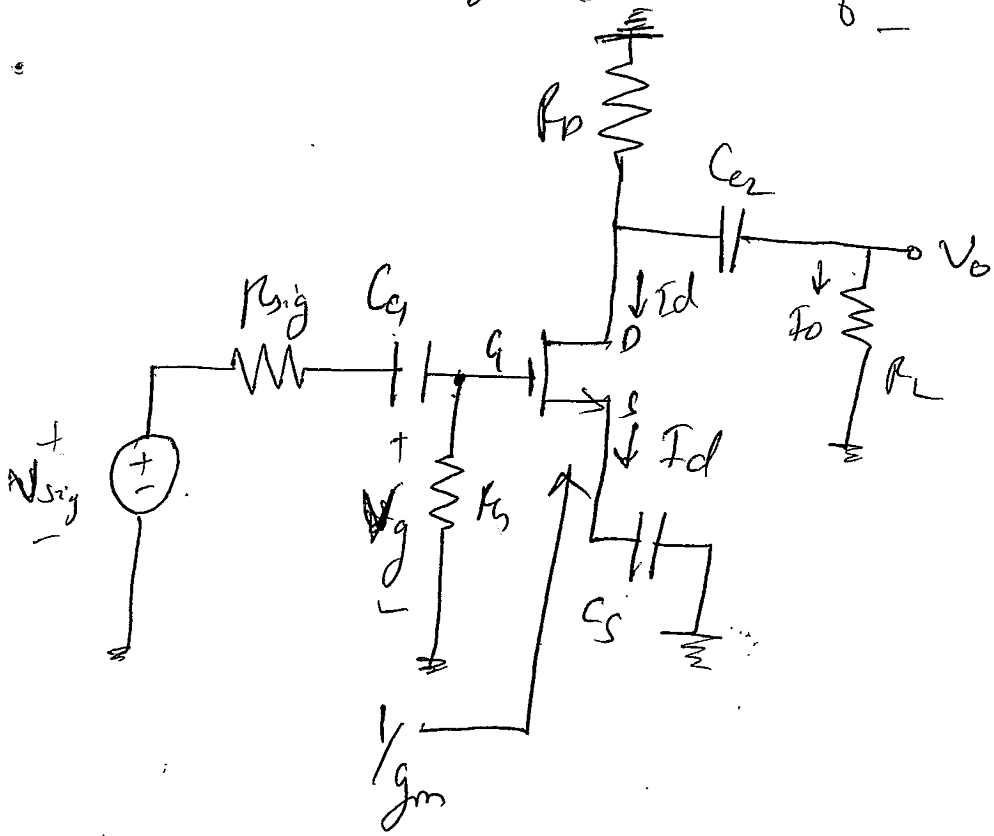
$$C_{gd} = \frac{1}{2} WL\,C_{ox} = 1.72\, fF$$ → (1m)

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} = 6.1\, fF$$ → (1m)

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} = 4.1\, fF$$ // → (1m)

Low Frequency Response of Common Source Amplifier. (6)

(Total Marks: 8M)



(1M)

To determine low frequency gain of the common source amplifier, ~~...~~

1) DC sources are eliminated
2) Ignoring resistance r_o.

The analysis begins at signal generator by finding the fraction of V_{sig} that appears at transistor gate

$$V_g = V_{sig} \times \frac{R_G}{R_G + \frac{1}{sC_{C_1}} + R_{sig}}$$

$$V_g = V_{sig} \times \frac{R_G}{R_G + R_{sig}} \times \frac{s}{s + \frac{1}{C_{C1}(R_G + R_{sig})}}$$ (1M)

Effect of coupling capacitor C_{C_1} with break frequency ω_{P_1} is given by

(61)

$$\omega_{P_1} = \omega_0 = \frac{1}{C_{C_1}(R_G + R_{sig})}$$ → (2M)

$$I_d = \frac{V_g}{\frac{1}{g_m} + \frac{1}{sC_s}}$$

$$I_d = g_m V_g \frac{s}{s + \frac{g_m}{C_s}}$$

Effect of C_s with break frequency ω_{P_2} is given by

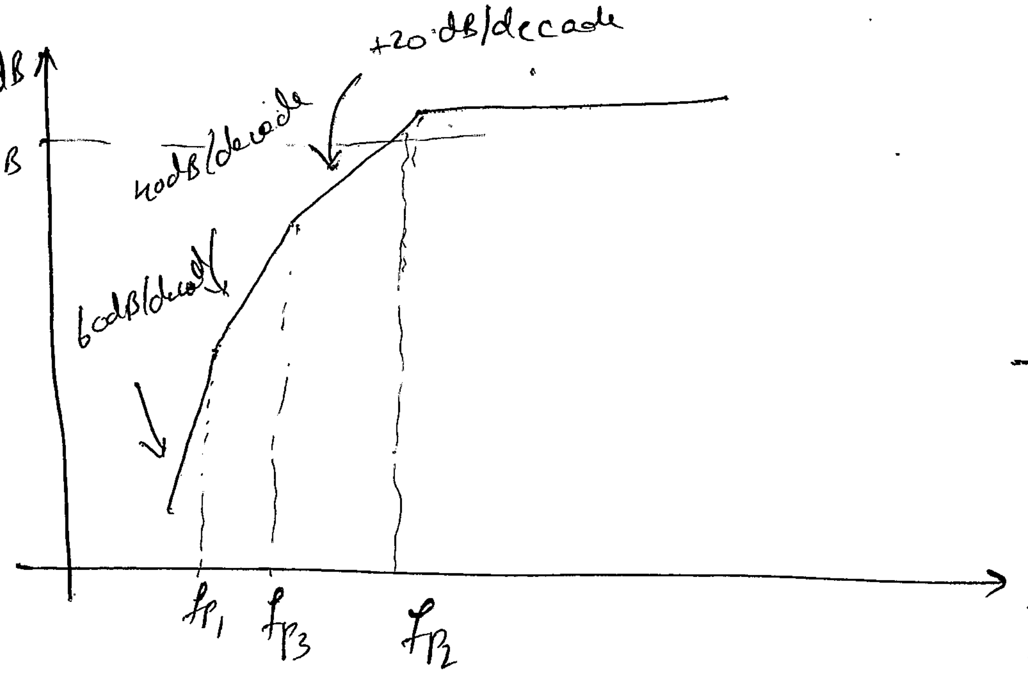
$$\omega_{P_2} = \frac{g_m}{C_s}$$

$$I_o = -I_d \frac{R_D}{R_D + \frac{1}{sC_{C_2}} + R_L}$$

$$\therefore V_o = I_o R_L = -I_d \frac{R_D R_L}{R_D + R_L} \frac{s}{s + \frac{1}{C_{C_2}(R_D + R_L)}}$$

→ (2M)

(62)



— (2M)

Total Marks :- 4M

4b) $g_m = 5000\,\mu S$, $r_d = 40k\Omega$, $R = 10k\Omega$.

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\therefore C = \frac{1}{2\pi f C\sqrt{6}} = 6.49\,nf.$$ → (2M)

$$|A| = g_m R_L$$

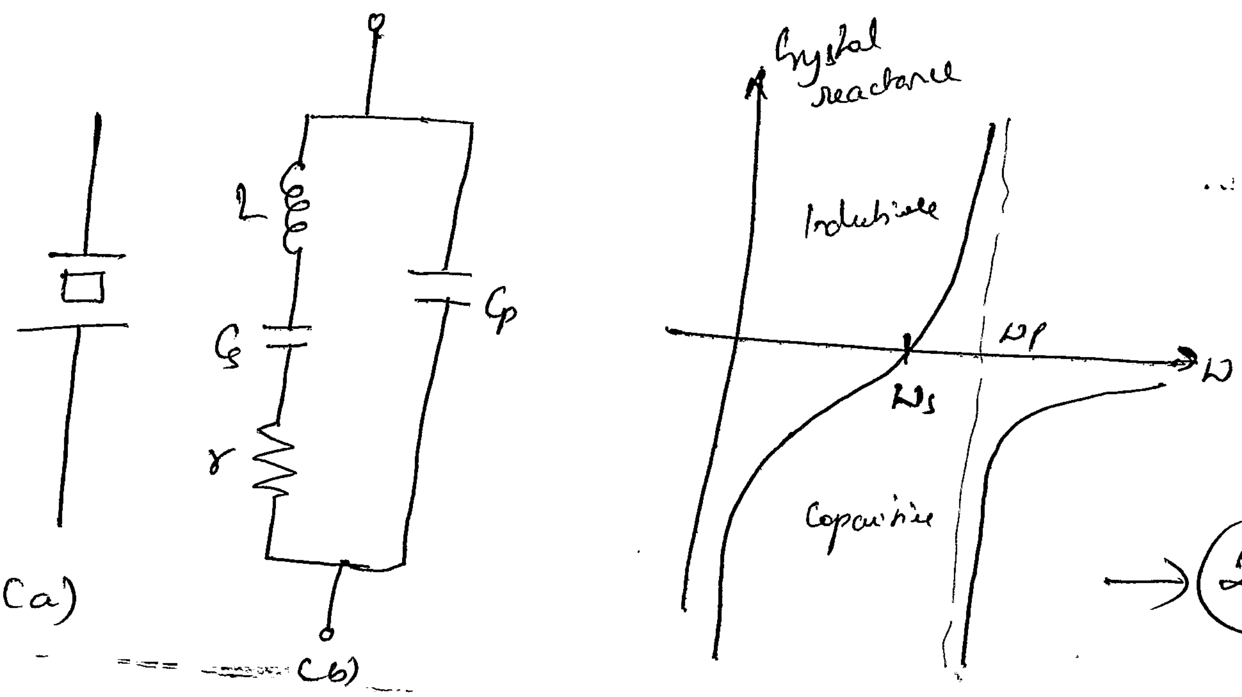
$$\therefore R_L = |A|/g_m = \frac{40}{5000\mu S} = 8k\Omega$$

→ (2M)

4c) Crystal Oscillator

[Total Marks :- 8M]

A piezoelectric crystal such as Quartz, exhibits electromechanical resonance characteristics that are stable



→ (2M)

Fig (a) shows symbol of crystal & fig (b) shows its electric equivalent circuit.

The resonance properties are characterised by large inductance L ; a very small series capacitance Cs, a series resistance r representing a Q factor ωoL/r that can be as high as few hundred thousand.

↳ Expln → (2M)

Since Q factor is very high, we neglect resistance r E_1.
Express impedance as

$$Z(s) = 1/\left[sC_p + \frac{1}{sL + 1/sC_s}\right] \rightarrow (1)$$

→ (1/2 M)

The crystal has 2 resonance frequencies,

Series resonance $\boxed{\omega_s = \frac{1}{\sqrt{LC_s}}}$ → (2)

→ (1/2 M)

parallel resonance $\boxed{\omega_p = \frac{1}{\sqrt{L\left(\frac{C_s C_p}{C_s + C_p}\right)}}}$ → (3)

→ (1/2 M)

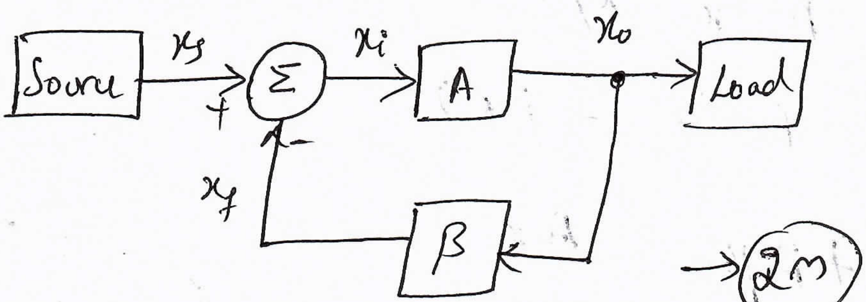
$$f_s = \frac{1}{2\pi\sqrt{LC}} = 1.08 \text{ KHz}$$ → (1M)

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = 1.11 \text{ KHz}$$ → (1M)

$$C_{eq} = \frac{C_M C}{C_M + C} = 61 \times 10^{-15} F$$ → (1/2 M)

5a) **Block diagram of negative feedback**

37 (17)



→ (2M)

Total Marks: 8 M.

i) The above figure shows basic structure of feedback amplifier

ii) Here 'x' represents either Voltage or Current.

A → Open loop gain of amplifier

β → Gain of feedback network

$$x_o = Ax_i \rightarrow (1)$$ → (1M)

The o/p x_o is fed to load as well as feedback N/W.

The o/p of F/b N/W 'x_f' is related to 'x_o' by

$$x_f = \beta x_o \rightarrow (2)$$

KVL KT,

$$x_i = x_s - x_f \rightarrow (3)$$ → (1M)

Since x_s is subtracted from x_f the feedback is said to be negative.

38-

WKT,

(18)

$$x_o = A x_i$$

$$x_o = A (x_s - x_f)$$

$$x_o = A (x_s - \beta x_o)$$

$$x_o (1 + A\beta) = A x_s$$

$$\therefore \boxed{A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta}} \rightarrow (4)$$

→ (2M)

where $A\beta$ = Loop Gain

A_f is smaller than open loop gain A by quantity $(1 + A\beta)$ ⟶ (1M)

$\therefore (1 + A\beta)$ ⟶ Amount of feedback.

usually $A\beta \gg 1$.

$$\therefore \boxed{A_f = 1/\beta} \rightarrow (5) \longrightarrow (1M)$$

Since feedback n/w usually made up of 'R' & 'C' The gain with feedback is also constant & stable

5b). To find :- A_v, R_{if}, R_{of}.

Total Marks :- 8M

(19)

39

Given :- $A = -100$, $R_i = 10k\Omega$, $R_o = 20k\Omega$.

for $\beta = 1$ & $\beta = 0.5$.

i) $A_f = \frac{A}{1+A\beta} = \frac{-100}{1+(-100)} = 1.01$. → (1m)

$R_{if} = R_i(1+A\beta) = 10k[1+(-100)\cdot(1)] = 990k\Omega$. → (1½ m)

$R_{of} = \frac{R_o}{(1+A\beta)} = \frac{20k}{(1+(-100)(1))} = 202\Omega$. → (0.5m)

ii) $\beta = 0.5$

$A_f = \frac{A}{1+A\beta} = \frac{-100}{1+(-100)(-0.5)} = -1.96$. → (1m)

$R_{if} = R_i(1+A\beta) = 10k[1+100(-0.5)] = 490k\Omega$ → (1½m)

$R_{of} = \frac{R_o}{(1+A\beta)} = 408.1 \Omega$ → (1½ M.)

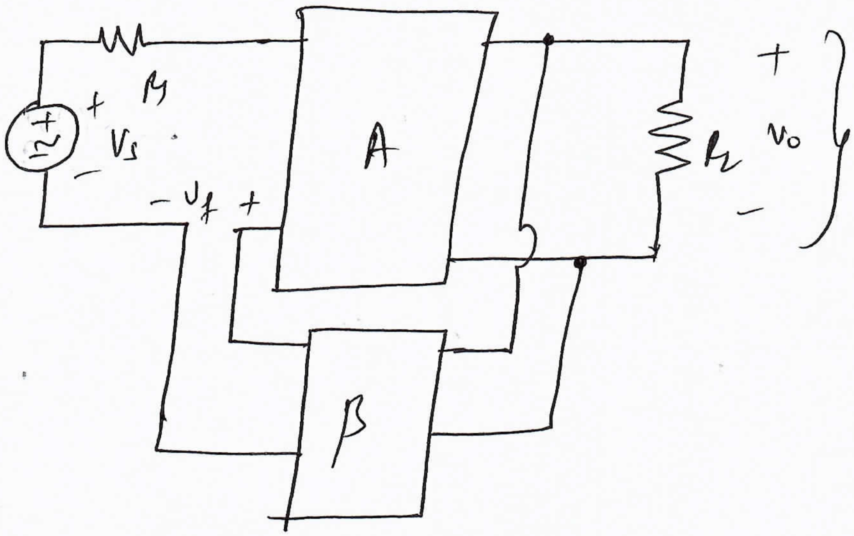
5(i) feedback Topologies

40

(20)

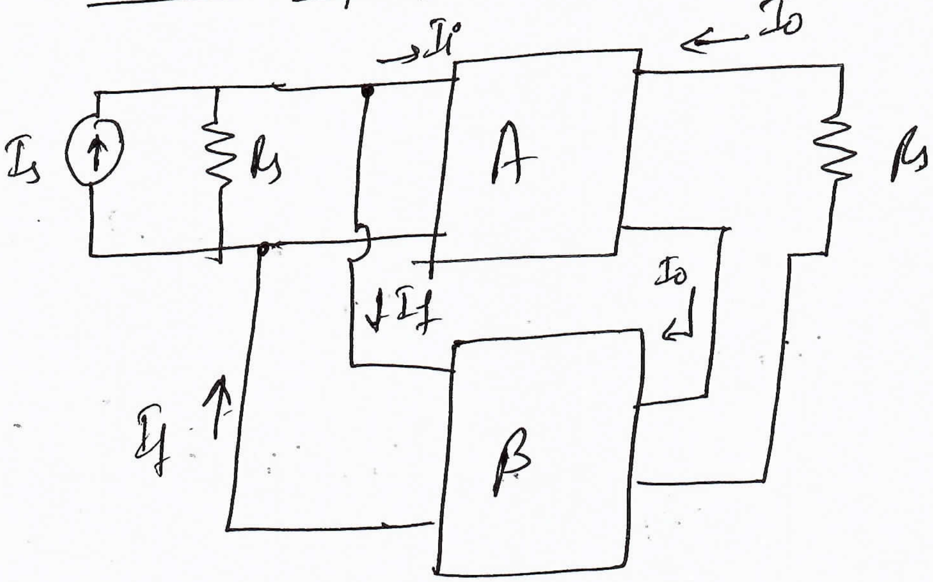
Total Marks
4M

1) Voltage Amplifier



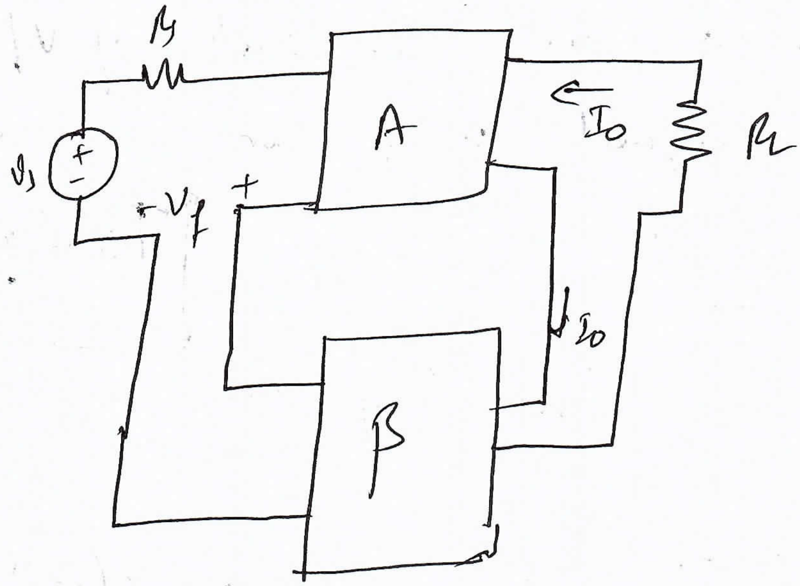
→ (1M)

2) Current Amplifier



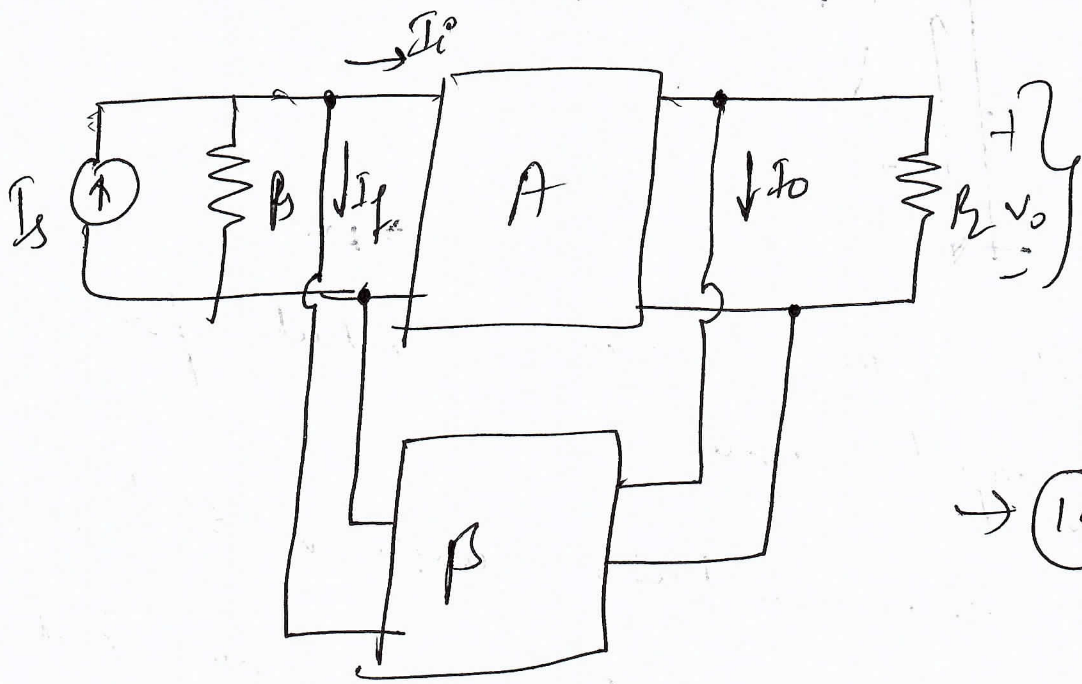
→ (1M)

3) Transconductance Amplifier



→ (1M)

4) Trans Resistance Amplifier



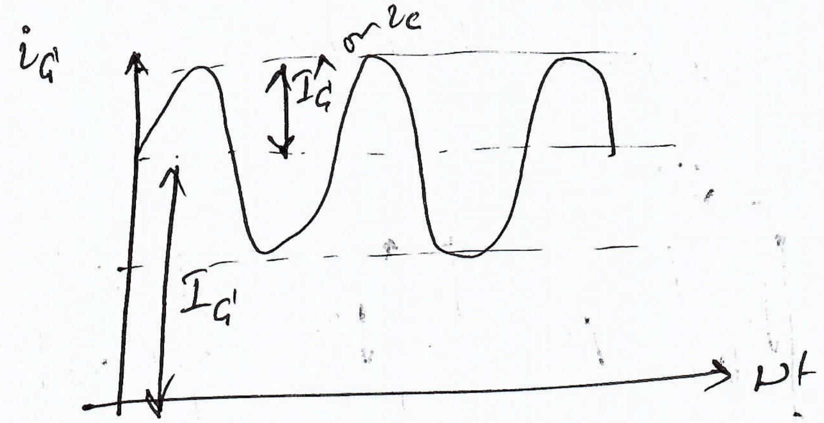
→ (1M)

22 6a) A power Amplifier is an electronic device. (22)
used to increase the magnitude of V/I/P
of an input signal using an external power
source. → (1M)

Total Marks: 8M

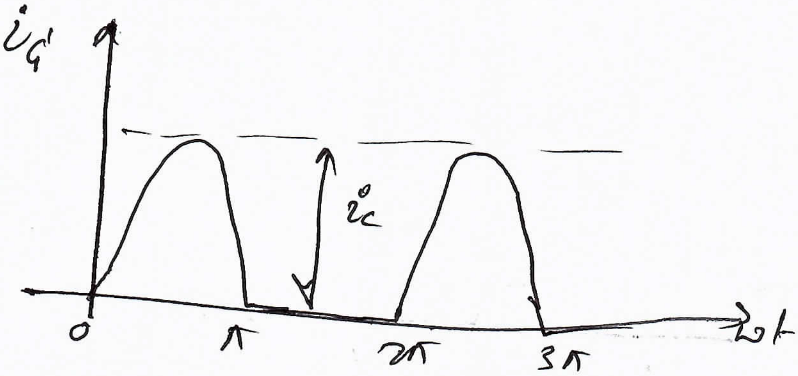
Classification of Power Amplifier

1) Class A power Amplifier → (2M)



*) Here the transistor conducts for entire cycle
of input signal
*) Here conduction angle is 360°.
*) It has high o/p power but poor
conversion efficiency.
*) Here Q-pt is located at centre of DC
load line
*) $\eta < 50\%$

2) Class B O/P stage → (2 m) (23) 23



*) Here transistor conducts for only one half cycle of input signal.

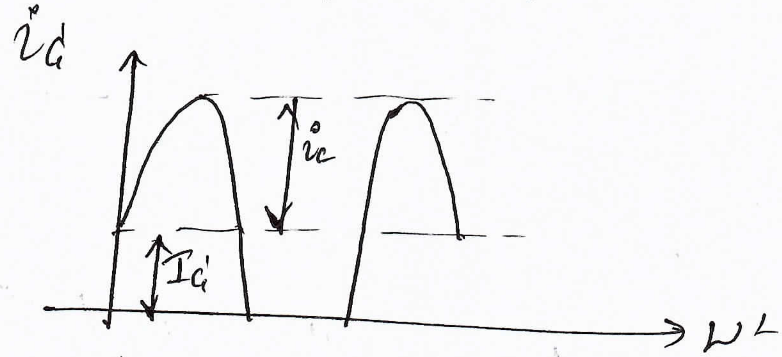
*) Conduction angle = 180°.

*) Here I_C is zero.

*) Here Q-point is located in cutoff region

*) $\eta > 50\%$ But $\eta \leq 78.5\%$

3) Class AB O/P stage. → (2 m)



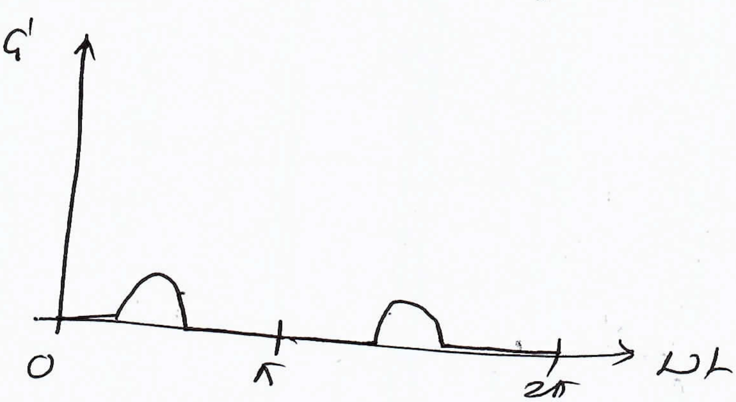
*) Here transistor conduction lies between that of Class A & B Amplifier

*) Here conduction angle is $> 180°$. but $< 360°$

*) Here $I_C < i_C$.

*) Here Q-point is located above

24 4) Class 'C' output stage — (1M) (24)



*) Here transistor conducts less than half.
*) Here conduction angle is $< 180°$.
*) Here $\eta \geq 90\%$.
*) It is used for RF power Amplification

6b) Power Conversion Efficiency

Total Marks:- 6M

$$\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% \rightarrow (1) \rightarrow (1m)$$

It is the ratio of ac o/p power to dc input power.

$$P_{i(dc)} = V_{ce} I_{cq} \rightarrow (2)$$

$$P_{o(ac)} = V_{rms} I_{rms} \rightarrow (3)$$

} → (1m)

WKT, $V_{rms} = \frac{V_{CE(p)}}{\sqrt{2}}$ $I_{rms} = \frac{I_{C(p)}}{\sqrt{2}}$ (20) 5

$$P_{o(ac)} = \frac{V_{CE(p)} I_{C(p)}}{2} \rightarrow (4) \rightarrow (1M)$$

$$V_{CE(p)} = V_{CEQ} = V_{CC} \rightarrow (5)$$

$$\rightarrow (6)$$

} → (1M) le

$$I_{C(p)} = I_{CQ}$$

$$\therefore P_{o(ac)} = \frac{V_{CC} \times I_{CQ}}{2} \rightarrow (1M)$$

$$\therefore \eta = \frac{\frac{V_{CC} I_{CQ}}{2}}{V_{CC} \times I_{CQ}} \times 100\%$$

$$\therefore \eta = 50\% \quad //$$

} → (1M)

26

6c) Given :- $V_{cc} = 12V$ $V_{o(ac)} = 6V$

Total Marks ~~2~~M ②

$$\eta = \frac{V_{cc}^2 / R_L}{V_{o(ac)}^2 / 2R_L} \times 100$$

$P_{o(ac)} = \frac{V_{o(ac)}^2}{2} \times R_L$

$= 0.25 \times 2$

$=$ ~~[illegible]~~ $= 50\%$ → (2M)

6d) Class C power Amplifier.

Total Marks :- 4M

1) In class C power amplifier Q - point is located below cutoff region. ([illegible])

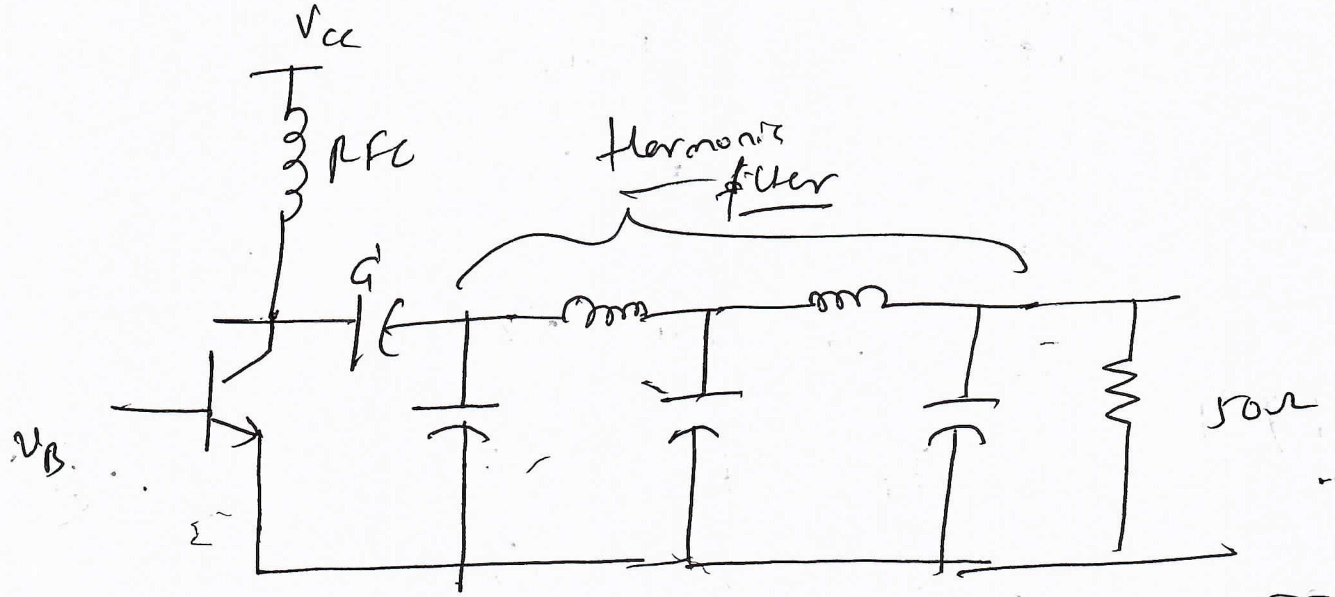
2) When input signal is off, the transistor is off. When input signal is applied the transistor operates in satn region.

3) When transistor is off the current flowing through transistor is less, Hence power dissipation is negligible.

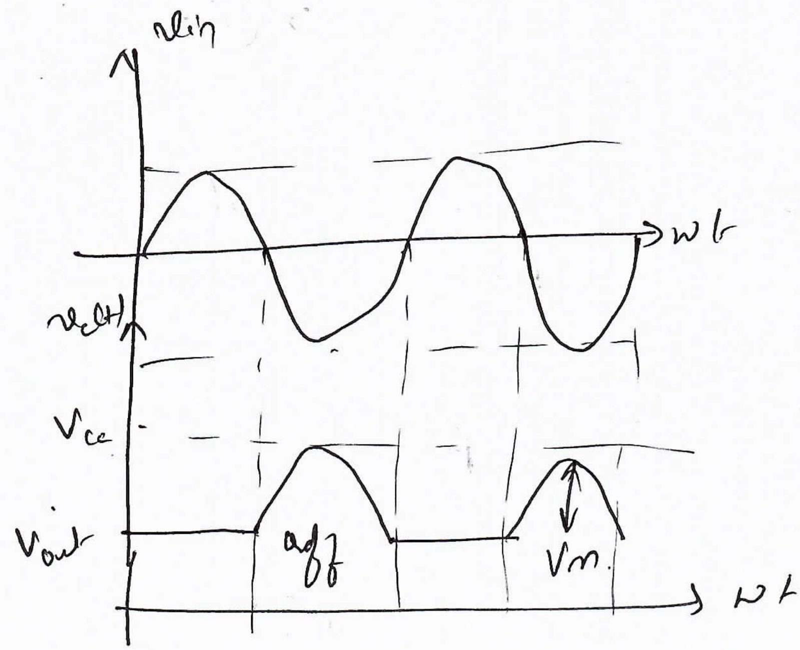
· When transistor is ON, voltage drop across transistor is less. ⓩ27

4) Disadvantage:- Class C amplifier is highly non-Linear & produces distorted o/p.

5) The drawback is overcome by connecting LPF at the o/p. (Expln → 2M)



C → (1M)

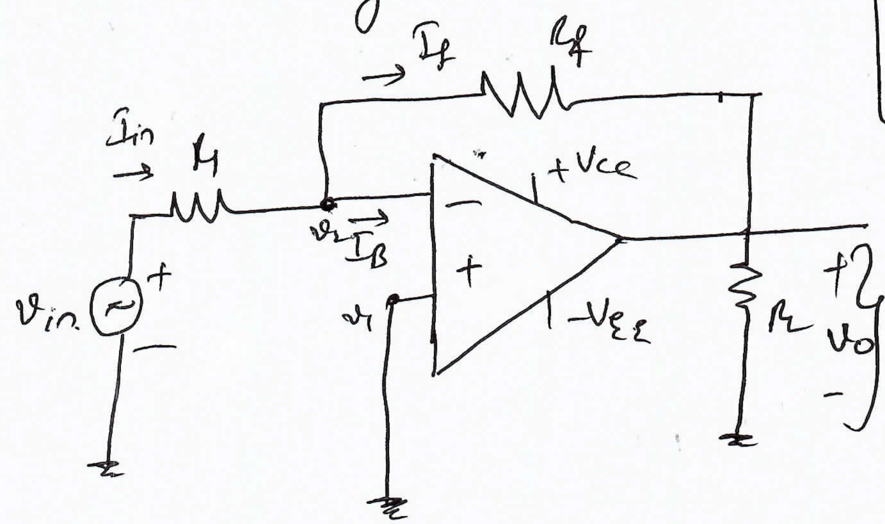


→ (1M)

28 When input voltage is positive above V_{BE} transistor ON is ON & operates in sat^n. Hence $V_o = V_{CE\,sat}$

7a) Inverting Amplifier

Total Marks :- 8M



Applying KCL at node v_2

$$I_{in} = I_B + I_f. \longrightarrow (1)$$

Since ($R_i \doteq 2M\Omega$ for 741)

$$I_{in} \simeq I_f. \longrightarrow (2)$$

$$\frac{v_{in} - v_2}{R_1} = \frac{v_2 - v_o}{R_f}. \longrightarrow (3)$$

$$v_{id} = v_1 - v_2 = \frac{v_o}{A}$$

Since $v_1 = 0$

$$v_2 = -\frac{v_o}{A}. \longrightarrow (4)$$

→ 2M

Substituting (4) in (3)

$$\frac{v_{in} + v_o/A}{R_1} = \frac{-(v_o/A) - v_o}{R_f}$$

$$\frac{v_{in}}{R_1} + \frac{v_o}{AR_1} = -\frac{v_o}{AR_f} - \frac{v_o}{R_f}$$

$$v_o\left(\frac{1}{AR_1} + \frac{(A+1)}{R_f A}\right) = \frac{-v_{in}}{R_1}$$

$$\therefore \frac{v_o}{v_{in}} = -\frac{A(R_1 R_f)}{(R_1+R_f+AR_1)\,R_1}$$

→ (1M)

$$\therefore \boxed{A_f = -\frac{AR_f}{(R_1+R_f+AR_1)}} \rightarrow (5)$$

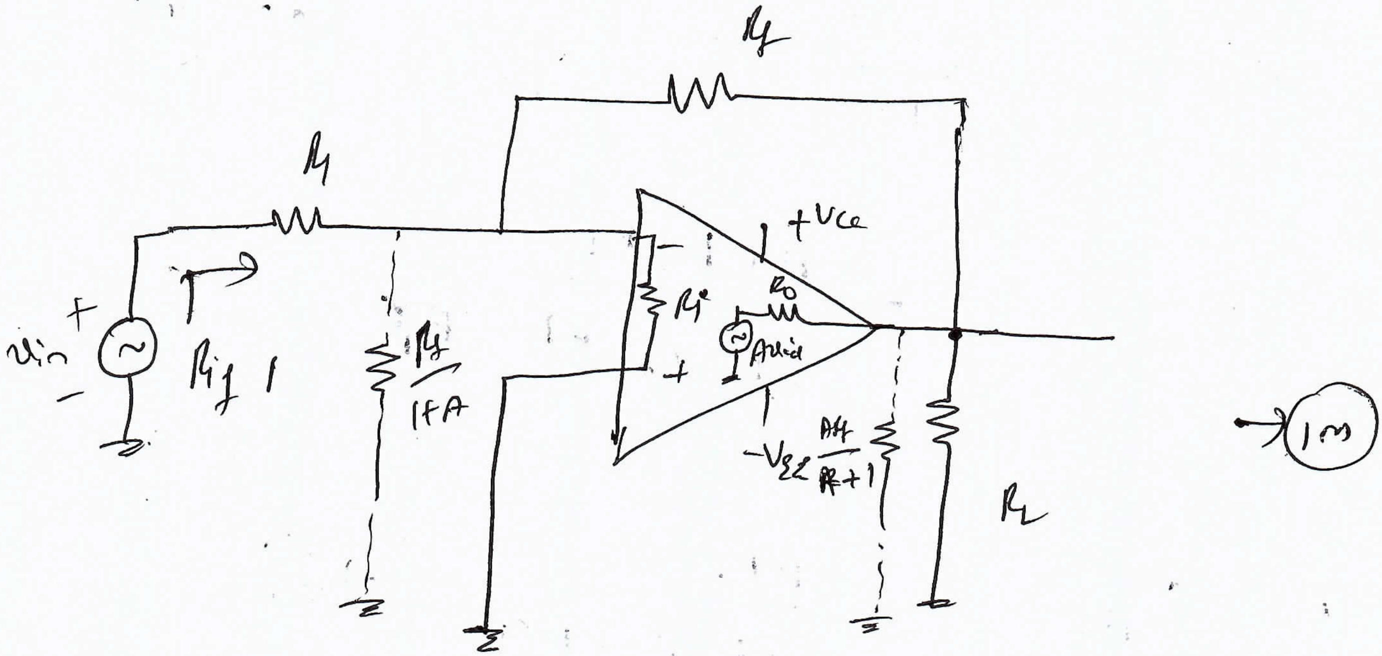
Since $AR_1 >> (R_1+R_f)$

$$A_f = -\frac{AR_f}{AR_1} = -R_f/R_1$$

$$\boxed{A_f = -R_f/R_1} \rightarrow (6)$$

from eqn (6) we can see that with negative feedback the gain of the opamp is reduced and even gain can be is constant since gain depends only on R_1 & R_f.

Input Resistance with f/b :-



Applying miller effect at input & o/p side the feedback resistance R_f can be split as

$R_f/(1+A)$ at i/p side & $\frac{AR_f}{(1+A)}$ at o/p side

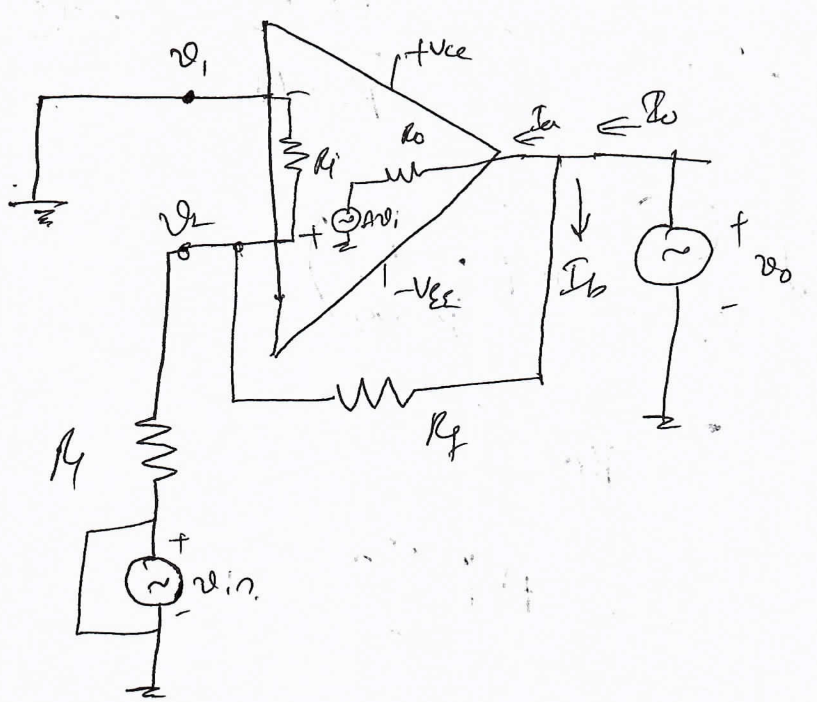
$$R_{if} = R_1 + \left(R_i \| \frac{R_f}{(1+A)}\right) \quad \rightarrow (7)$$

Here $R_i >> \left(\frac{R_f}{1+A}\right)$

$\therefore$ $R_{if} = R_1 + \frac{R_f}{(1+A)}$ → (1M)

we get $\boxed{R_{if} = R_1}$

Output Resistance with feedback.



→ (1M)

Applying KCL at o/p side

$I_o = I_a + I_b$ → (1)

Since $[(R_i \| R_1) + R_f] \geq R_o$

$I_a >> I_b$

$\therefore \quad I_o \simeq I_a.$

Applying KVL to o/p loop.

$-v_o + I_o R_o + A v_{id} = 0$

$$I_o = \frac{v_o - A v_{id}}{R_o} \rightarrow (2)$$

$$v_{id} = v_1 - v_2 = 0 - \frac{v_o R_1}{R_1 + R_f} \rightarrow (3)$$

Substituting (3) in (2)

$$I_o = \frac{v_o + A\left(\frac{v_o R_1}{R_1 + R_f}\right)}{R_o}$$

$$I_o = \frac{v_o + A\beta v_o}{R_o}$$

$$I_o = \frac{v_o (1 + A\beta)}{R_o}$$

$$R_{of} = \frac{R_o}{1 + A\beta} \rightarrow (4)$$

→ 4M

+b) Given $R_1 = 1\,K\Omega$. $R_f = 4.7\,K\Omega$.

(33)

$A = 400000$, $R_i = 33\,M\Omega$, $R_o = 60\,\Omega$, $\pm 13V$

$UGB = 0.6\,MHz = f_o$

Total Marks 6M

To find : A_f, R_{if}, R_{of}, f_f.

$A_f = -\frac{R_f}{R_1} = -\frac{4.7\,K\Omega}{1\,K\Omega} = -4.7$

$R_{if} = R_i(1 + A\beta) = 33\,M\Omega(1 + 400000 \times \beta) = 2.31 \times 10^{12}\,\Omega$ → (1M)

$\beta = \frac{R_1}{R_1 + R_f} = 0.175$ → (1M)

$R_{of} = R_o/(1 + A\beta) = \frac{60}{(1 + 400000 \times 0.175)} = 8.57 \times 10^{-4}\,\Omega$ → (2M)

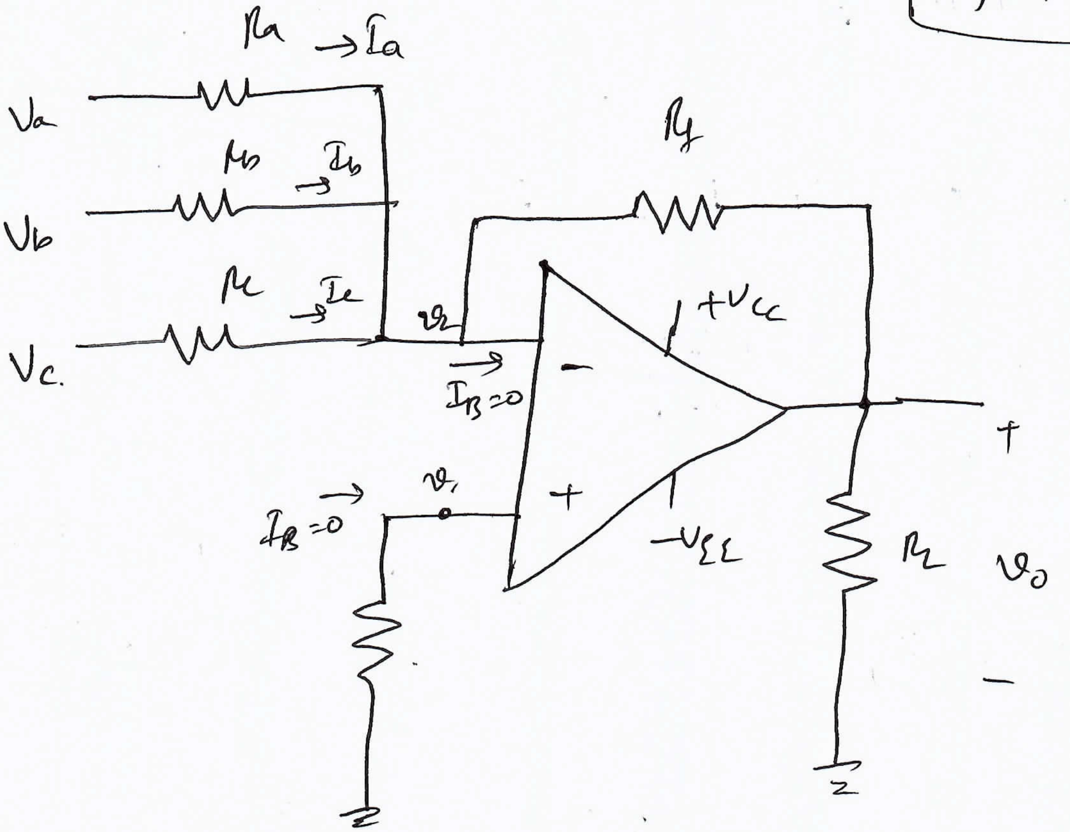
$f_F = f_o(1 + A\beta)$

$= 0.6\,M(1 + 400000 \times 0.175)$

$= 4.2 \times 10^{10}\,Hz$ → (2M)

7c) Inverting Scaling Amplifier & Averaging circuit:

Total Marks :- 6M



→ (2M)

1) The above fig shows inverting summing ampl. with 3 i/p va, vb, vc.

2) Applying KCL at i/p side.

$$I_a + I_b + I_c = I_f + I_B \rightarrow (1)$$

Since Ri is very large. we get $I_B \approx 0$.

$$\therefore \quad I_a + I_b + I_c = I_f \rightarrow (2)$$

(1M)

$$\frac{v_a - v_2}{R_a} + \frac{v_b - v_2}{R_b} + \frac{v_c - v_2}{R_c} = \frac{v_2 - v_0}{R_f}$$

By concept of virtual Ground.

$$v_1 = v_2 = 0$$

$$\frac{v_a}{R_a} + \frac{v_b}{R_b} + \frac{v_c}{R_c} = -\frac{v_0}{R_f}$$

$$v_0 = -R_f\left[\frac{v_a}{R_a} + \frac{v_b}{R_b} + \frac{v_c}{R_c}\right] \rightarrow (3)$$

(1M)

Scaling Amplifier

If each input voltage is amplified by different factor. it is called scaling or weighted amplr

$$v_0 = -\left(\frac{R_f}{R_a} v_a + \frac{R_f}{R_b} v_b + \frac{R_f}{R_c} v_c\right) \rightarrow (4)$$

where $R_f/R_a \neq R_f/R_b \neq \frac{R_f}{R_c}$.

→ (1M)

Averaging Amplifier

If $R_a = R_b = R_c = R$. & $R_f/R = \frac{1}{n}$.

where n = no. of i/p.

$$v_o = -\frac{(v_a + v_b + v_c)}{3}$$ → (1M)

→ (4)

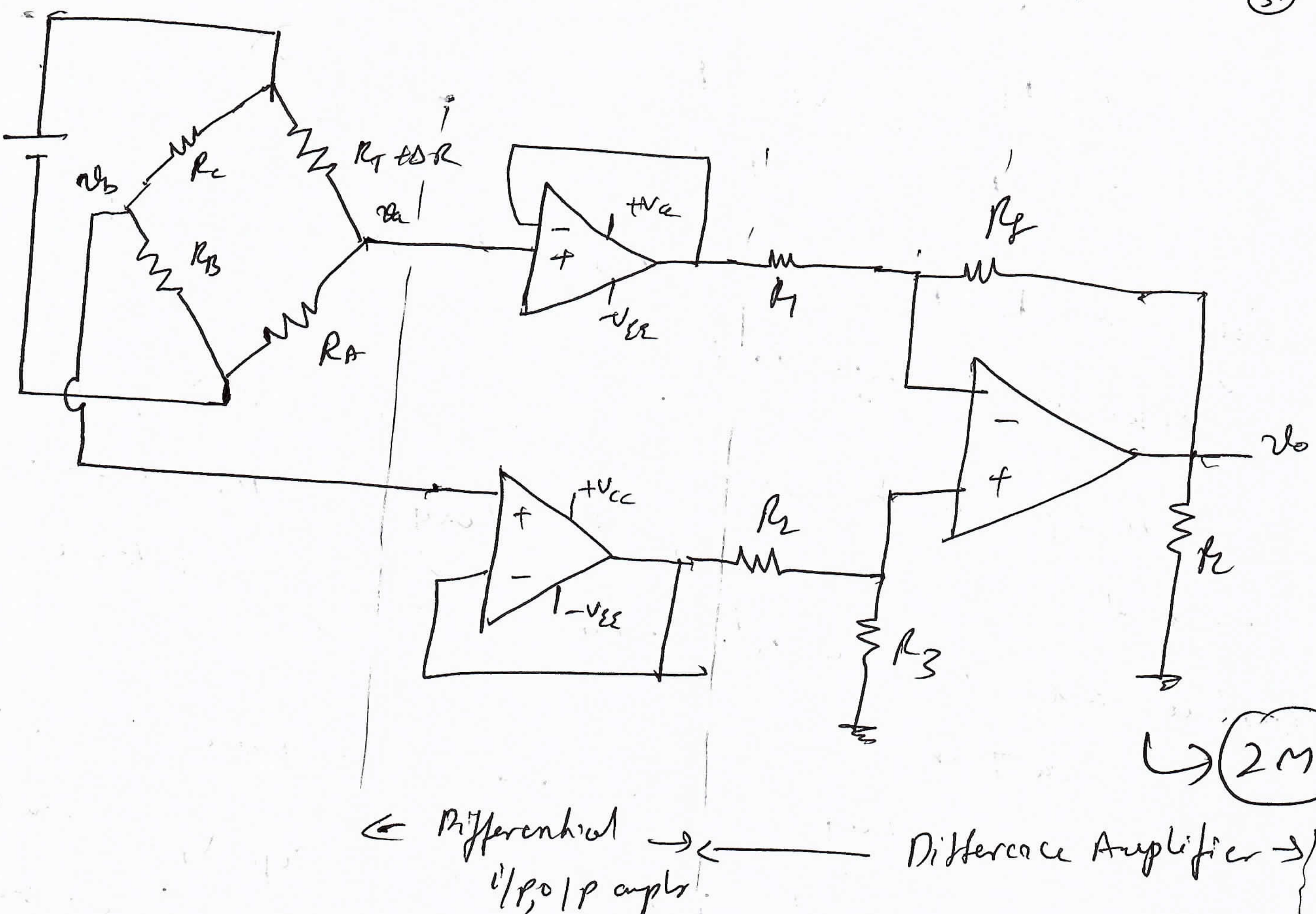
8a) Instrumentation Amplifier [Total Marks :- 10M]

An instrumentation Amplr is a type of differential Amplifier with buffer amplifier. at i/p side, which eliminates need for impedence matching, & make amplifier stable for use in measurement & test equipment → (1M)

Applications:-

1) To enhance the S/N ratio in audio applications.
2) Video data acquisition in high speed signal.

→ (1M)



→ (2M)

1) The above figure shows instrumentation amplifier using transducer bride.

2) Here a resistive transducer (straingauge) is used whose resistance changes as function of physical energy applied

3) It is denoted by $R_T + \Delta R$, where R_T is resistance of transducer & ΔR is change in resistance of R_T.

4). At bridge balance.

Expln → (1M)

$$v_a = v_b$$

$$\frac{V_{dc} \times R_B}{R_c + R_B} = \frac{V_{DC} \times R_A}{R_A + R_T} \quad \longrightarrow (2M)$$

5) Generally R_a, R_b, R_c & R_T chosen to be same at some reference temperature.

6) The bridge is balanced at reference condn., as the physical qty to be measured changes, the resistance of transducer also be changed., causing bridge imbalance $V_a \neq V_b$

7) Let ΔR be change in resistance of transducer, since R_B & R_C are fixed resistor, the voltage V_b is constant. However V_a varies as the function of transducer resistor

$$V_a = \frac{V_{dc} \times R_A}{R_A + (R_T + \Delta R)} \rightarrow (2)$$

$$V_b = \frac{V_{dc} \times R_B}{R_c + R_B} \rightarrow (3)$$

$$V_{ab} = V_a - V_b$$

$$= \frac{V_{dc} \times R_A}{R_A + (R_T + \Delta R)} - \frac{V_{dc} \times R_B}{R_c + R_B}$$

(2M)

$$V_{ab} = \frac{-V_{dc} \times \Delta R}{2(2R+\Delta R)} \rightarrow (5)$$

Here -ve sign indicates V_a is less than V_b.

The o/p voltage V_{ab} is applied to differential i/p, o/p amplifier consisting of 3 opamp.

$$\therefore V_o = \frac{R_f}{R_1}\left(\frac{V_{dc} \times \Delta R}{2(2R+\Delta R)}\right) \rightarrow (6)$$

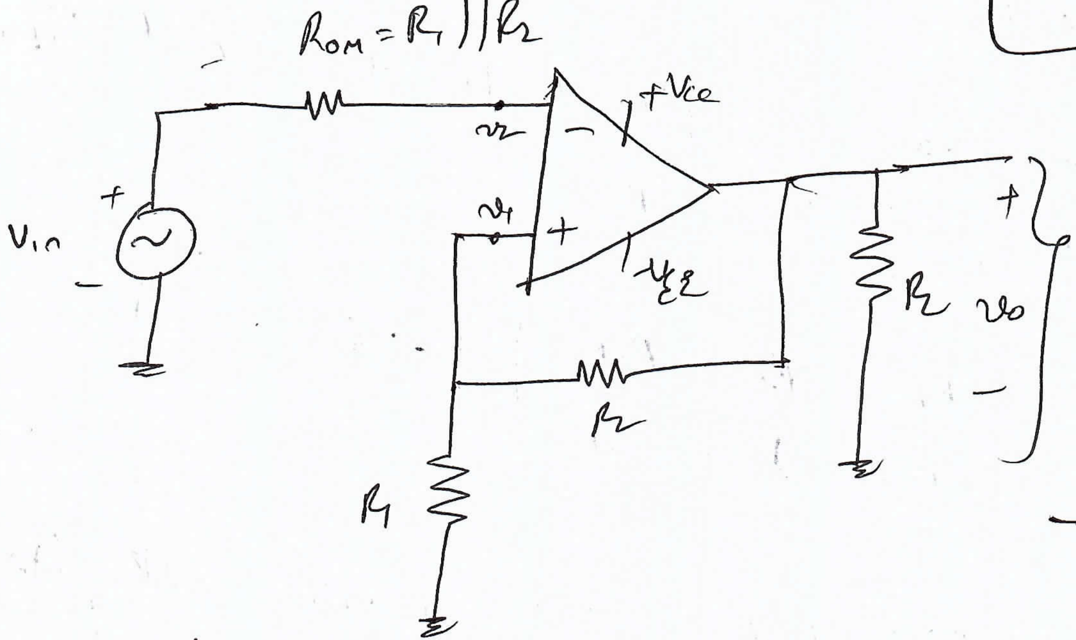
Since $2R >> \Delta R \Rightarrow 2R+\Delta R \approx 2R$ (1M)

$$V_o = \frac{R_f}{R_1}\frac{\Delta R}{4R} V_{dc}$$

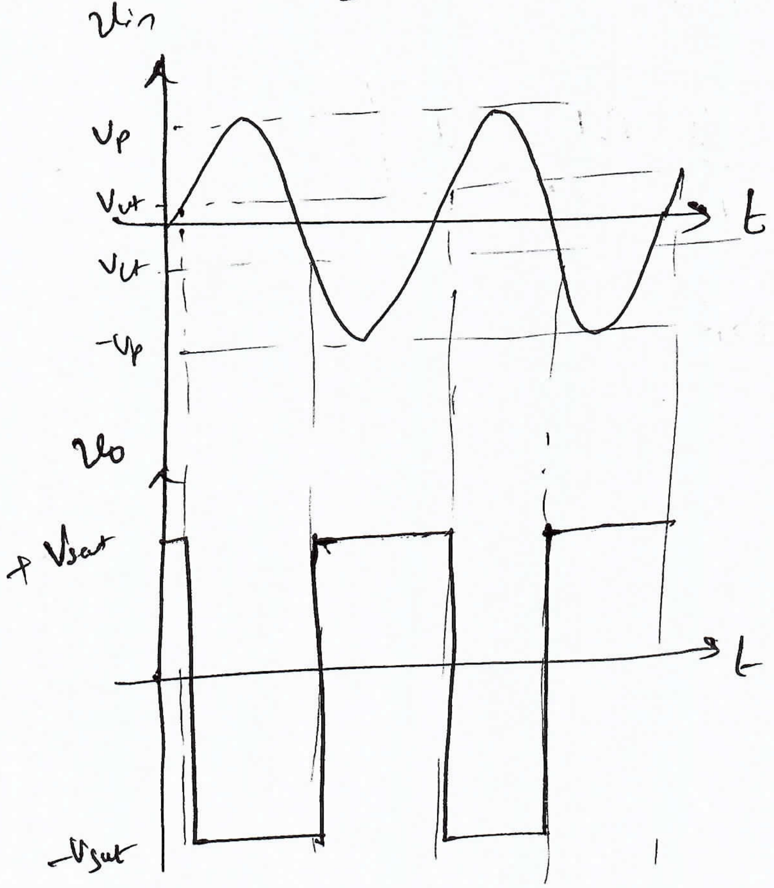
$V_o \propto \Delta R$

8b) 40 Inverting Schmitt trigger

Total Marks 4M



→ 1M



→ 1/2 M

* As long as $V_{in} < V_{ut}$, $V_o = +V_{sat}$.

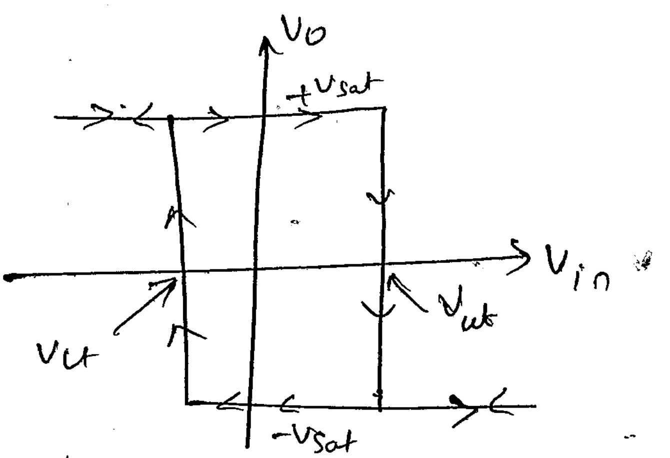
$$V_{ut} = (+V_{sat}) \frac{R_1}{(R_1+R_2)} \rightarrow (1) \qquad \rightarrow \frac{1}{2}M$$

When $V_o = -V_{sat}$ the voltage a/c R_1 refers as Lower T voltage V_{LT}. When V_{in} becomes more -ve that V_{LT},

$$V_{LT} = (-V_{sat}) \left(\frac{R_1}{R_1+R_2}\right) \rightarrow (2)$$

$$V_{hy} = V_{ut} - V_{LT} \rightarrow (3) \qquad \rightarrow 1M$$

$$V_{hy} = \frac{R_1}{R_1+R_2} \left[+V_{sat} - (-V_{sat})\right] \rightarrow (4)$$



→ 1M

8 c) $R_1 = 15K\Omega$, $R_2 = 1K\Omega$. $V_{in} = 10V_{p-p}$.

$\pm V_{sat} = \pm 14V$, $V_{ref} = 2V$.

Total Marks 6M

To find :- V_{ut}, V_{LT}, V_{hy}

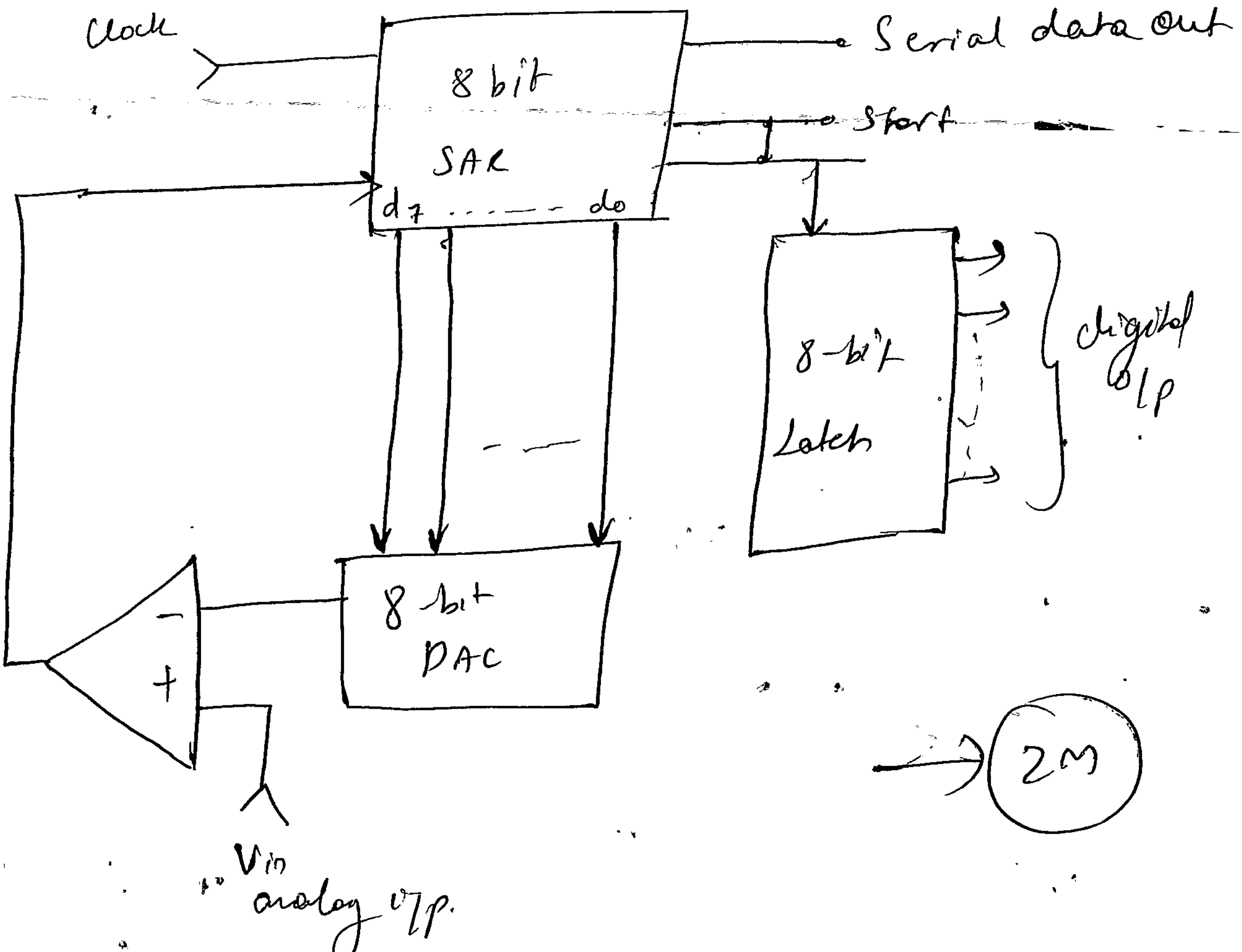
$$V_{ut} = +V_{sat}\left(\frac{R_1}{R_1+R_2}\right) = 14\left(\frac{15k\Omega}{16k\Omega}\right) = 13V \rightarrow 2M$$

$$V_{lt} = -V_{sat}\left(\frac{R_1}{R_1+R_2}\right) = -14\left(\frac{15k\Omega}{16k\Omega}\right) = -13V \rightarrow 2M$$

$$V_{hy} = V_{ut} - V_{lt} = 26V \rightarrow 2M$$

9a) Successive Approximation type ADC

Total Marks 8M



→ 2M

V_{in} — SAR (O/P) — Comparator O/P (M3)

V_{in}	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	Comparator O/P
4.156	1	0	0	0	0	0	0	0	1
(212)	1	1	0	0	0	0	0	0	1
	1	1	1	0	0	0	0	0	0
	1	1	0	1	0	0	0	0	1
	1	1	0	1	1	0	0	0	0
	1	1	0	1	0	1	0	0	1
	1	1	0	1	0	1	1	0	0
	1	1	0	1	0	1	0	1	0
	1	1	0	1	0	1	0	0	0

→ (2M)

1) The heart of circuit is 8 bit SAR.
2) The O/P of SAR is given to 8-bit DAC
3) The O/P of 8-bit DAC is compared with analog i/p Vin
4) Initially Start = 1 & SAR is reset
On first clock pulse, MSB is set & all other bits are reset

Expln — 2M.

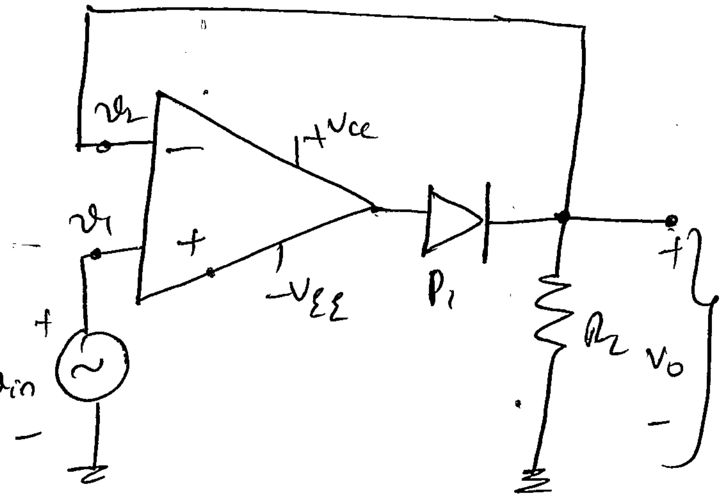
i) If Vin < Va O/P of comparator is zero
SAR resets current bit & sets next bit. (2M)

ii) If Vin > Va O/P of comparator is 1
SAR retains current bit & sets next bit.

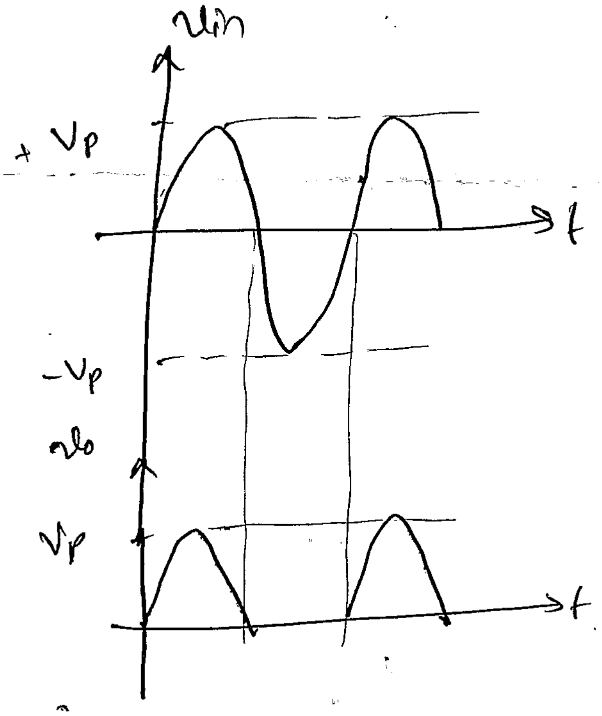
5) After 8th clock pulse conversion pin is high. & data is latched at o/p.

9b) Small Signal Half wave Rectifier.

Total Marks 4M



→ 1M



→ 2M

1) Thee above figure shows the small sigal HWR.

2) The circuit can rectify signals having peak value in mV.

3) Because of high open loop gain of op Amp. the forward bias voltage drop of diode is 0.

• The diode acts like ideal diode

(45)

4) During the +ve half cycle as v_{in} increases V_o' increases diode D_1 is forward biased & circuit acts as voltage follower & we get $v_o = v_{in}$.

5) During -ve half cycle V_o' is -ve & diode is reverse biased. open circuiting the feedback path we get $v_o = 0V$ & $V_o' = -V_{sat}$.

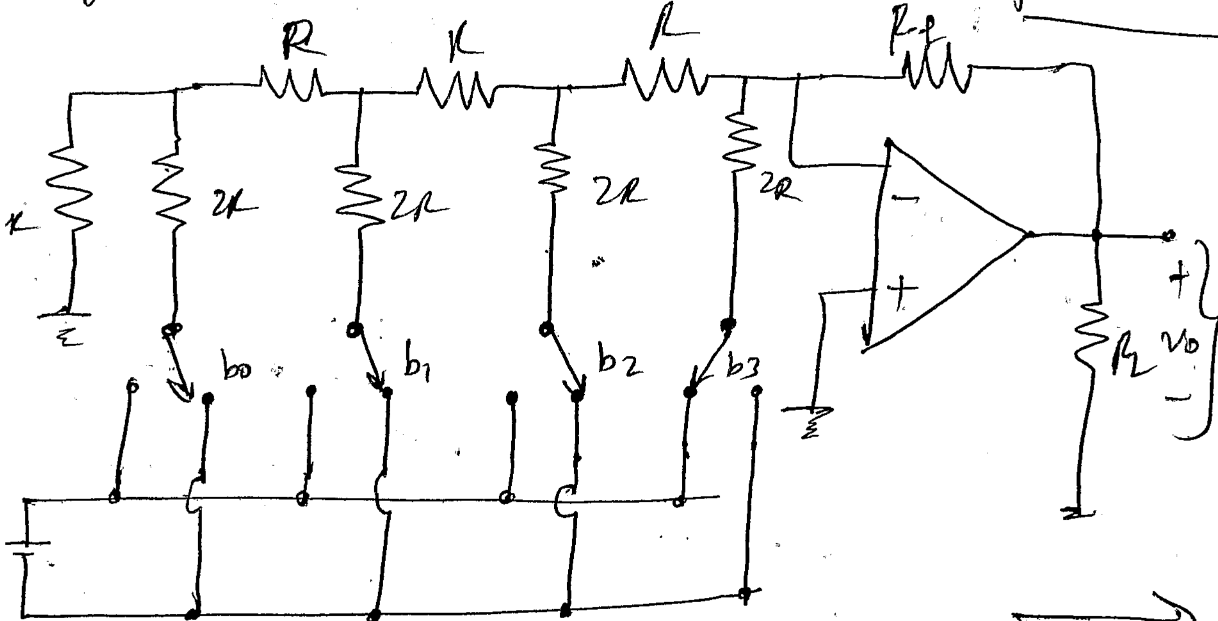
6) Op Amp takes some time to come out of saturation Hence high speed op Amp like HA2500 should be used.

Explaination - 2M.

8c) R-2R DAC:-

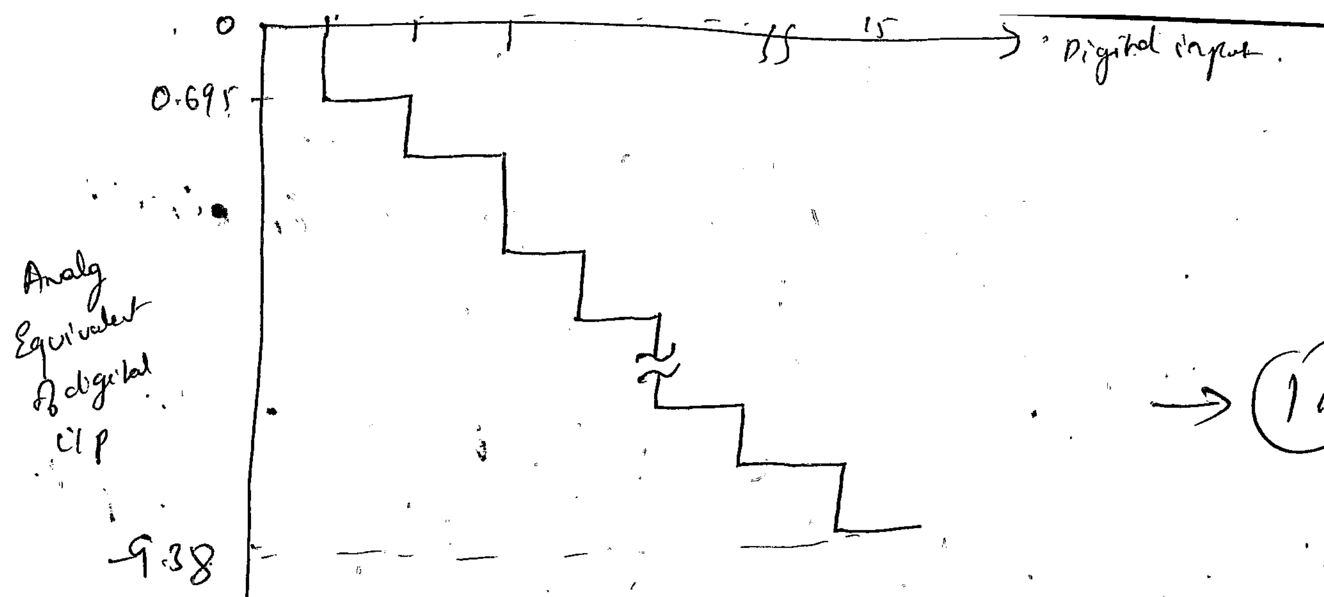
It is a digital to analog converter built using only two types of resistor R & 2R.

Total Marks :- 8M.



→ (2M)

fig (a)

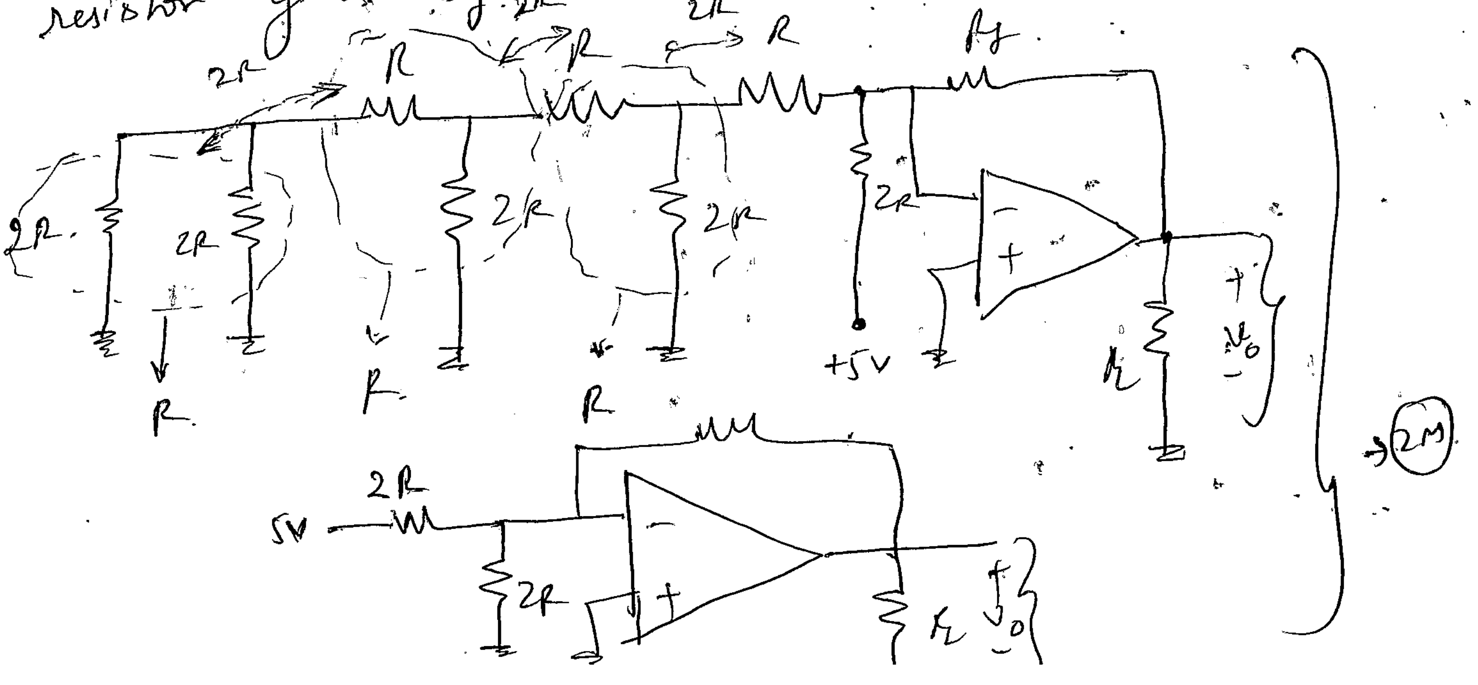


→ (1M)

fig (b)

1) ~~That above~~ figure (a) shows DAC with R-2R resist
2) The binary input are given via switches b_0 to b_3.
3) The o/p voltage is directly proportional to binary i/p
4) The problem with binary weighted DAC is overcome ~~by using R-2R DAC~~, since it uses only 2 presized resistors R-2R. [Expl2 - 1M]

5) If MSB bit b_3 is connected to 5V & other switches are connected to ground, we get thevenin equivalent resistor given by



$$R_{th} = \left[R \left[(2R \| 2R) + R \right] \| 2R \; \} + R \right] \| 2R$$ (47)

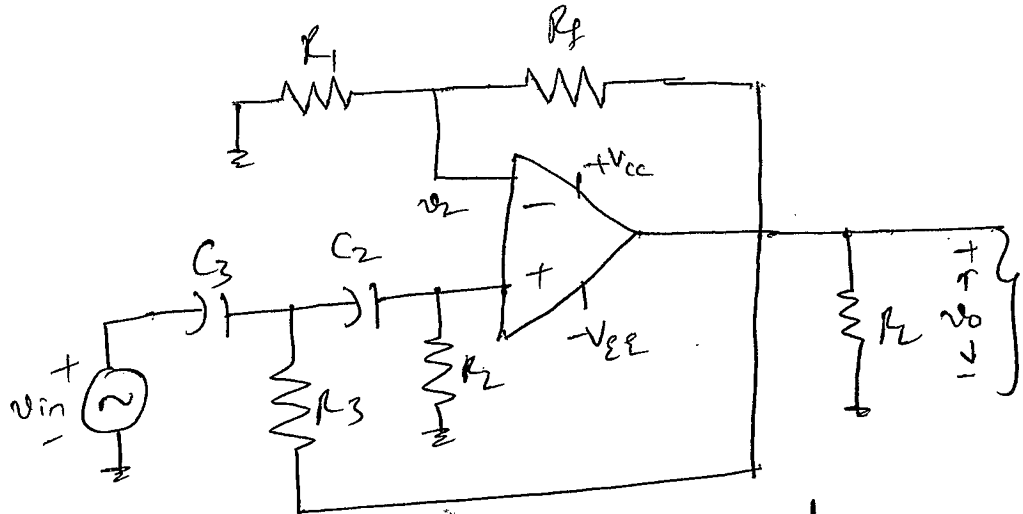
$R_{th} = 2R$.

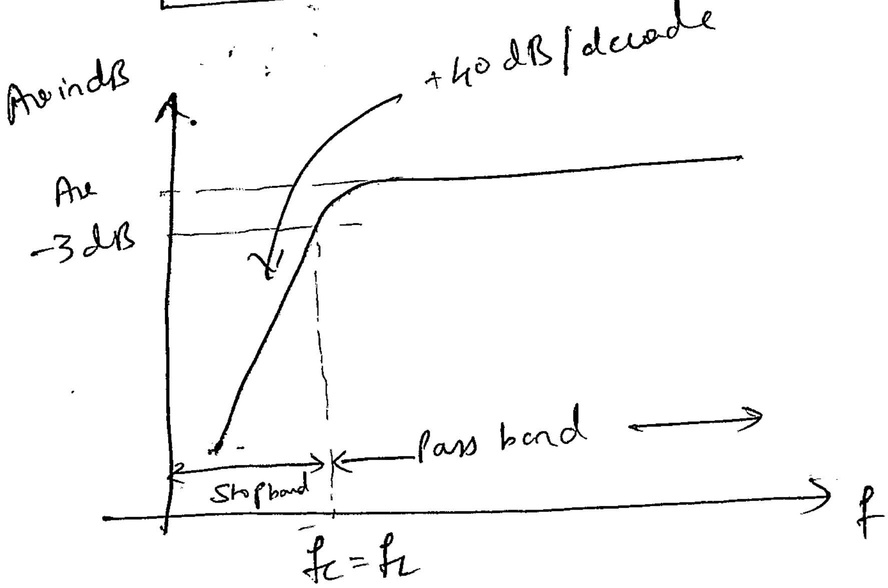
The equation of o/p voltage is given by.

$$\therefore \; v_o = -R_f \left(\frac{b_0}{2R} + \frac{b_1}{4R} + \frac{b_2}{8R} + \frac{b_3}{16R} \right)$$ → (2M)

10 a) Second order Butterworth HPF

Total Marks 6M





→ (2M)

1> The figure shows second order Butterworth HPF.
2> In first order Butterworth HPF the gain falls at rate of -20 dB/decade at lower frequencies.

3) In order to increase the rate of gain fall we go for 2nd order HPF.

4) Here gain falls at rate of −40dB/decade at lo[w] frequencies.

5) 1st order HPF can be converted into 2nd order HPF using RC N/W.

6) At high frequency the reactance of capacitance C_2 & C_3 is very low & capacitor acts like short ckt & entire input signal is fed as input to op-Amp

Explaination:- 2M

7) As frequency goes on decreasing the ~~gain~~ reactance of capacitor goes on increasing.

8) At low freq. the reactance of capacitor C_2 & C_3 is very large. Hence capacitor acts as O/C & no input is fed to opAmp. & we get $v_o = 0V$.

9) R_2 & C_2 will give roll of rate of 20dB/decade

10) Phase lead introduced by R_2 & C_2 & Phase lag introduced by R_3 along with junction of C_3 & R_2 will provide additional roll-off of 20dB/decade

∴ total roll of rate = −40dB/decade

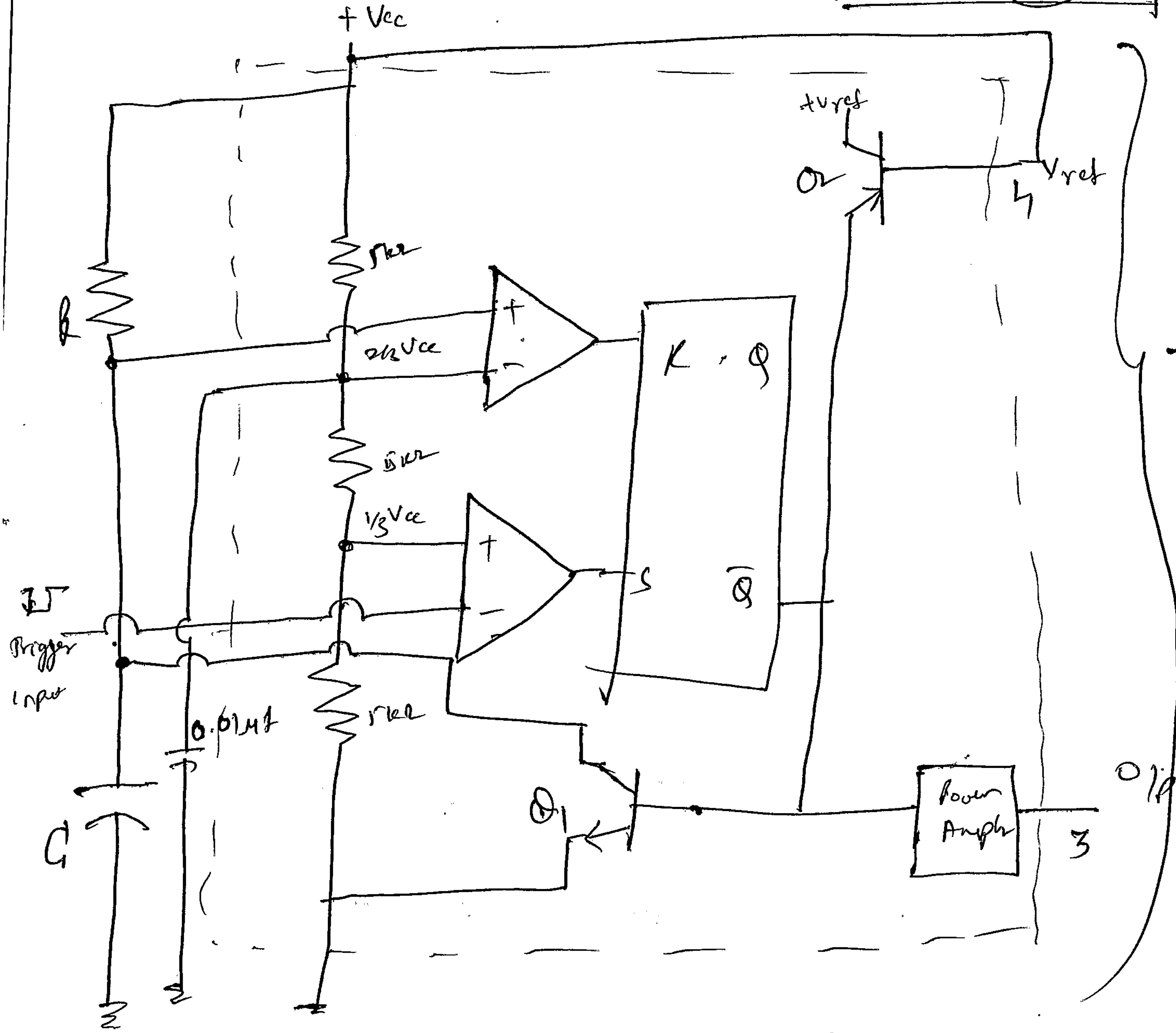
11) The lower cutoff freq. is given by

$$f_L = \frac{1}{2\pi\sqrt{R_2 C_2 R_3 C_3}}$$ (1M)

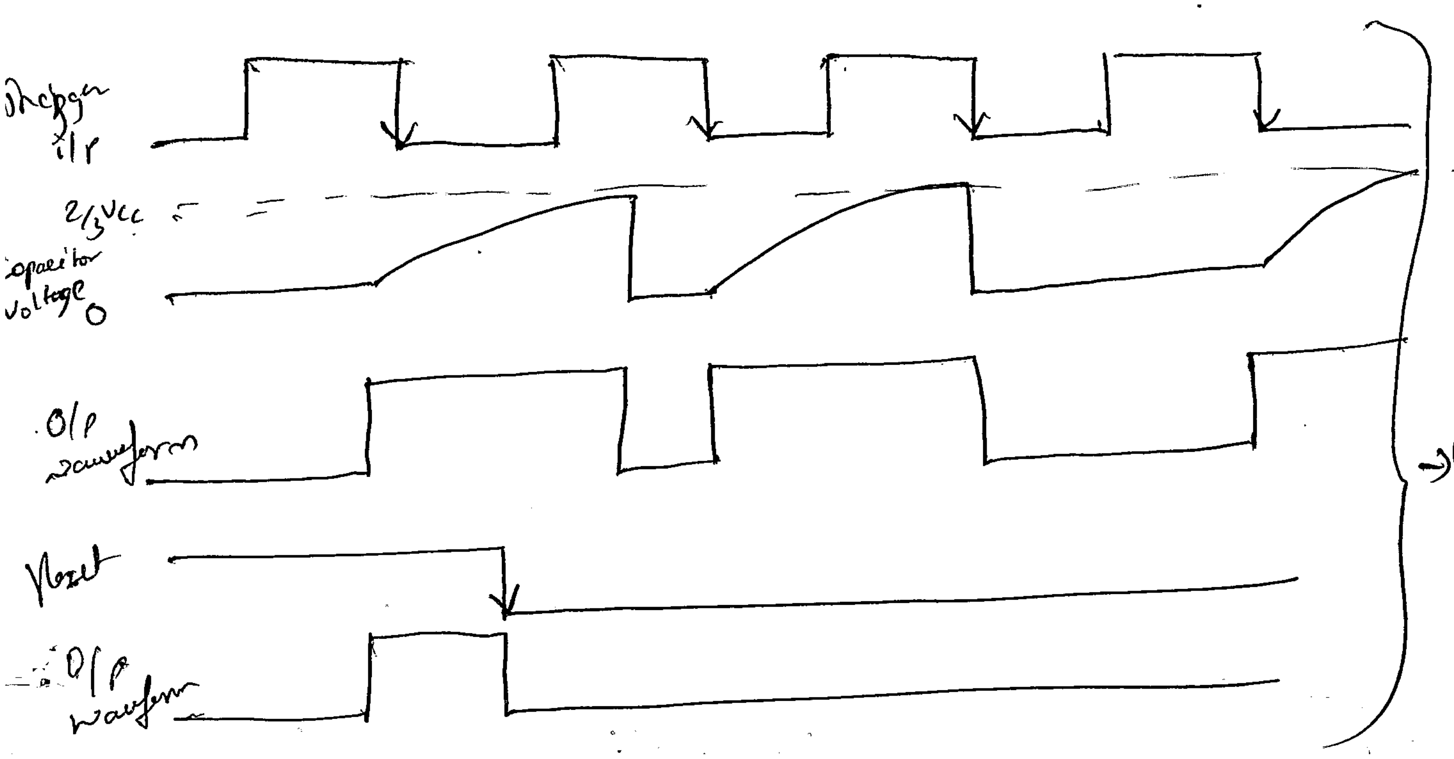
12) voltage gain $= \left|\frac{v_o}{V_{in}}\right| = \frac{A_f\,(f/f_L)}{\sqrt{1+(f/f_L)^4}}$ (1M)

Q.10 b) Monostable Multivibrator

Total Marks 5M



→ 3M



→ 2M

1) In standby state $\bar{Q}$ o/p of SR flipflop = 1. (80)

2) Hence o/p of 555 timer = 0, discharge transistor Q_1 is ON, clamping capacitor to ground.

3) When trigger voltage is applied & Trigger vol. goes below $\frac{1}{3}V_{cc}$, the o/p of L.C. is S=1, Q=1. ∴ $\bar{Q}$ = 0. The o/p of timer is (high).

4) The discharge transistor Q_1 is off, Now capacitor starts charging towards V_{cc} via R.

5) The capacitor continues to charge until voltage of capacitor exceeds $2/3 V_{cc}$, When vol. across capacitor goes above $2/3 V_{cc}$, R=1, $\bar{Q}$=1. & o/p of 555 timer goes low.

6) The discharge transistor Q_1 is ON, clamping external timing capacitor C to gnd.

7) from the waveform we can see that once triggered the o/p remain in high state until time T_p

8) When reset goes low, o/p is forced to Zero. Since ~~discharge~~ reset transistor is turned ON.

Explaination → 2M

$$v_C = V_{CC}(1 - e^{-t/RC})$$

At time $t = T$

$$\tfrac{2}{3}V_{CC} = V_{CC}(1 - e^{-T/RC})$$

$$e^{-T/RC} = \tfrac{1}{3}$$

$$-T/RC = \ln(1/3)$$ → 1M

$$\boxed{T = 1.1\,RC}$$

Total Marks :- 6M

10c) $R_A = 2.2\,k\Omega$, $R_B = 3.9\,k\Omega$, $C = 0.1\mu F$.

$$T_C = 0.693\,(R_A + R_B)\,C = 0.42\,ms.$$ → 2M

$$T_d = 0.693\,(R_B)\,C = 0.27\,ms$$ → 2M

$$f_0 = \frac{1.45}{(R_A + 2R_B)\,C} = 1.45\,kHz$$ → 2M