Basic Electronics - Dr. Vikas Balikai

CBCS SCHEME

USN | | | | | | | | | | |

18ELN14/24

First/Second Semester B.E. Degree Examination, Dec.2019/Jan.2020
Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the working of PN junction diode under forward and reverse biased conditions. **(06 Marks)**

b. Explain the working of Photodiode. **(05 Marks)**

c. Explain with neat circuit diagram and waveforms, the working of full wave bridge rectifier. Show that the efficiency of full wave bridge rectifier is 81%. **(09 Marks)**

OR

2 a. Explain the operation of Half wave rectifier with capacitor filter with neat circuit diagram and waveforms. **(06 Marks)**

b. A full wave rectifier uses 2 diodes having internal resistance of 10 Ω each. The transformer RMS secondary voltage from center to each end is 200V. Find I_m, I_{dc}, I_{rms} and V_{dc} if the load is 800 Ω. **(06 Marks)**

c. Explain how zener diode helps in voltage regulation with neat circuit diagram. Give detail mathematical analysis. **(08 Marks)**

Module-2

3 a. Explain the construction, working and characteristics of n-channel JFET. **(09 Marks)**

b. With a neat circuit diagram, explain the working of CMOS Inverter. **(06 Marks)**

c. For a n-channel JFET if I_{DSS} = 9 mA and V_p = –6V. Calculate I_D at V_{gs} = – 4V and V_{gs} at I_D = 3 mA. **(05 Marks)**

OR

4 a. Explain the construction, working and characteristics of enhancement type MOSFET. **(09 Marks)**

b. Explain the working of Silicon Controlled Rectifier [SCR] using two transistor model. **(06 Marks)**

c. For an EMOSFET, determine the value of I_D if $I_{D(on)}$ = 4 mA, $V_{gs(on)}$= 6V, V_T = 4V and V_{gs} = 8V. **(05 Marks)**

Module-3

5 a. What is an OP-AMP? List the characteristics of an ideal OP-AMP. **(06 Marks)**

b. Explain the operation of an OP-AMP as inverting amplifier with neat diagram and waveforms. **(06 Marks)**

c. Explain how OP-AMP can be used as (i) Integrator (ii) Voltage follower. **(08 Marks)**

OR

6 a. Explain the different input modes of an OP-AMP. **(06 Marks)**

b. Design an adder circuit using OP-AMP to obtain an output voltage, $V_o = -[2V_1 + 3V_2 + 5V_3]$. Assume R_f = 10 kΩ. **(06 Marks)**

Scheme & Solution Prepared by

Prof Vikas Balikai

Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T., HALIYAL (U.K.)

c. Explain the following terms with respect to OP-AMP:
(i) CMRR (ii) Slew rate (iii) Input bias current (iv) Supply Voltage Rejection ratio. (08 Marks)

Module-4

7 a. With a neat circuit diagram, explain how transistor is used as an amplifier. Derive an equation for A_v. (08 Marks)
b. Explain RC phase shift oscillator with circuit diagram and necessary equations. (08 Marks)
c. Explain the voltage series feedback circuit and derive an equation for voltage gain, A_{vf} with feedback. (04 Marks)

OR

8 a. With a neat circuit diagram, explain the working of Wein-bridge oscillator. (08 Marks)
b. Explain the operation of IC555 as an Astable oscillator with neat circuit diagram and necessary equations. (08 Marks)
c. The Transistor in CE configuration is shown in Fig.Q8(c) with $R_C = 1\ k\Omega$ and $\beta_{DC} = 125$. Determine
(i) V_{CE} at $V_{in} = 0$ V.
(ii) $I_{B(min)}$ to saturate the collector current
(iii) $R_{B(max)}$ when $V_{in} = 8$ V
$V_{CE(sat)}$ can be neglected.

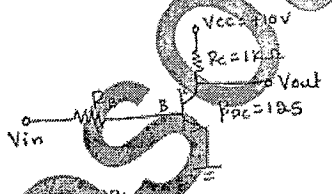

Fig.Q8(c) (04 Marks)

Module-5

9 a. Design Full adder circuit and implement it using basic gates. (08 Marks)
b. Find (i) $(1101\ 0111\ 0110.1010)_2 = (\ ?\ )_{16}$
(ii) $(EB986)_{16} = (\ ?\ )_2$
(iii) $(925.75)_{10} = (\ ?\ )_8$ (06 Marks)
c. Explain the basic elements of communication system with block diagram. (06 Marks)

OR

10 a. State and prove De-Morgan's theorem. (06 Marks)
b. With a block diagram explain the working of a 3-bit ripple counter. (06 Marks)
c. What is a flip-flop? Explain the operation of master-slave JK flip-flop. (08 Marks)

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Subject - Basic Electronics - Dec 2019/Jan 2020
Subject code: 18ELN14/24
CBCS Scheme
Faculty - Dr. Vikas Balikai

Module 01

1.a

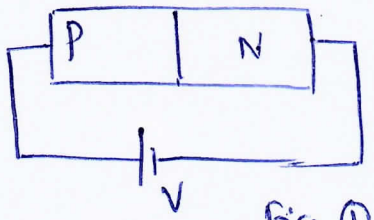


Fig ①

Fig ②

6 Marks

Forward bias

- The diode is said to be in forward bias when P side of the diode is at highest potential & N side of diode is at lowest potential.
- When P is connected to positive side of battery the depletion region reduces & the current through the diode increases slowly as shown below in fig ④

- Reverse bias

When P side of diode is connected to N side of battery & N side of diode is connected to P side of battery then diode is said to be in reverse bias.

During reverse bias the depletion region increases & very small or no current flows through the diode as shown in fig ④.

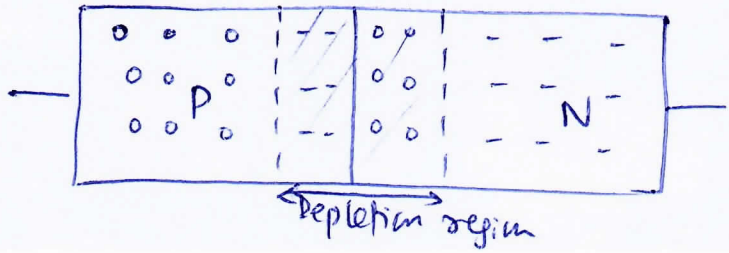


Fig ③

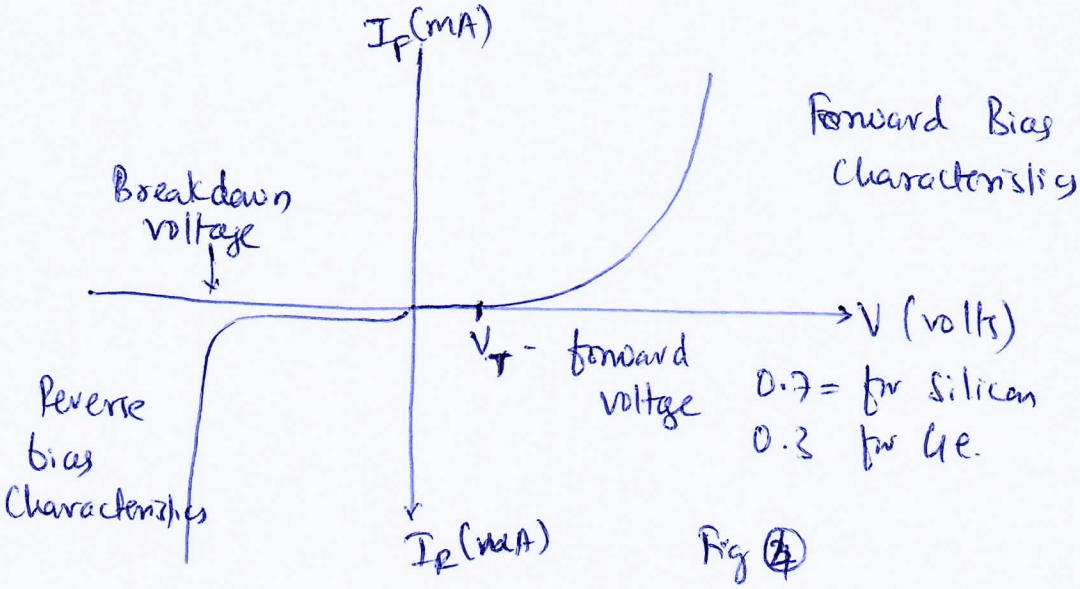


Fig (4)

1.b Working & Photo diode

A photo diode is a semiconductor device that converts light into electric current. It is also called photo detector, photosensor or light detector.

It is a PN junction operated in reverse bias region as shown in Fig 5 (a) (b).

5 marks

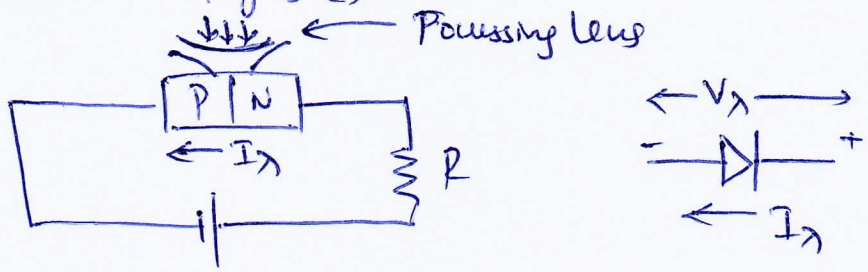


Photo diode in reverse bias Fig 5(a) Symbol Fig 5(b)

In photo diode the reverse saturation current I_λ is limited by the availability & thermally generated minority carriers. A light is made to impinge on the junction, the light photons impart energy to the valence electrons causing more e⁻ hole pairs to be released. As a result the concentration & minority carriers increases & so does the current I_λ.

The symbol & photo diode is shown in Fig 5(b)

The IV characteristics for various ~~light~~ values of light intensity (f_c) are drawn in fig. (6)

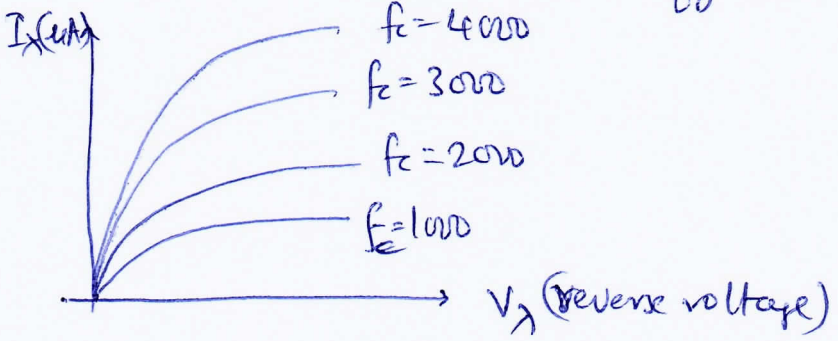


Fig. 6 V-I characteristics

1c Full wave rectifier (Bridge)

Fig 7 shows the ckt diagram of a full wave bridge rectifier ckt.

9 marks

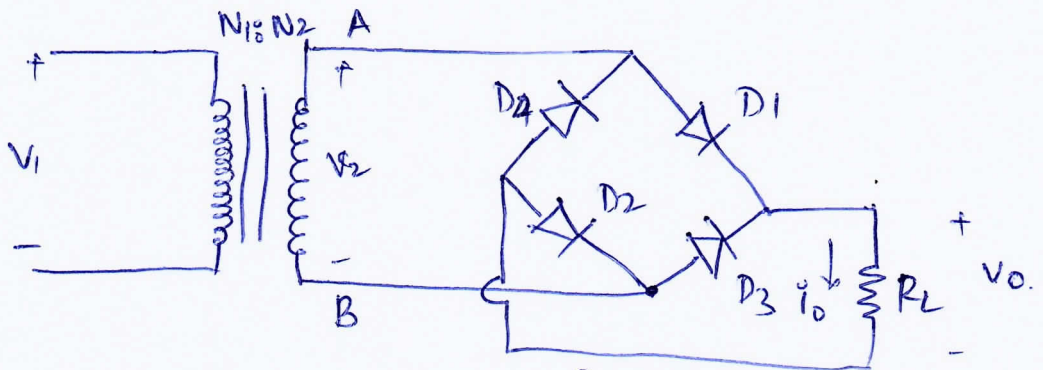


Fig 7- Full wave bridge rectifier ckt

Operation

During +ve half cycle of ac i/p signal, end A becomes +ve with respect end B. This makes diodes D_1 & D_2 forward biased while Diode D_3 & D_4 are reverse biased. Therefore only diodes D_1 & D_2 conducts. The current flows through diode D1 load resistance R_L & D2 to reach end B.

current direction (A) → (D1) → (R_L) → (D_2) → (B)

Diodes on → D1, D2

Diodes off → D_3, D_4

This can be seen in Fig 8

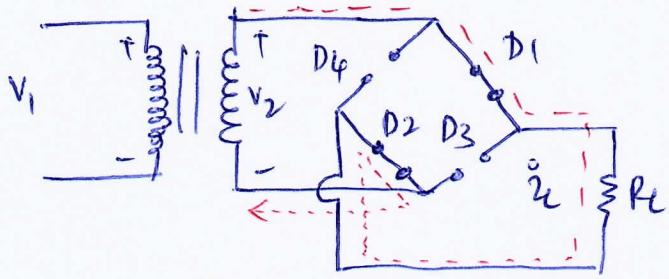


Fig 8 - Working of B.W.R under positive i/p cycle

During -ve half of the ac i/p cycle, end A becomes -ve w.r.t end B. This makes diode D3 & D4 forward biased while D1 & D2 are reverse biased.
Therefore only diodes D3 & D4 conducts. The current flows from end A through diodes D3 & D4 through RL as shown in Fig 9

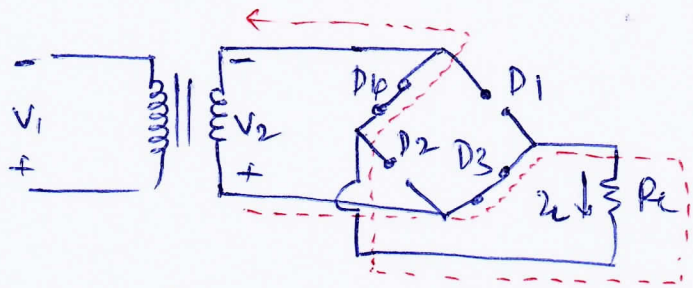


Fig 9 - Working of BWR under -ve i/p cycle.

Input output Waveforms

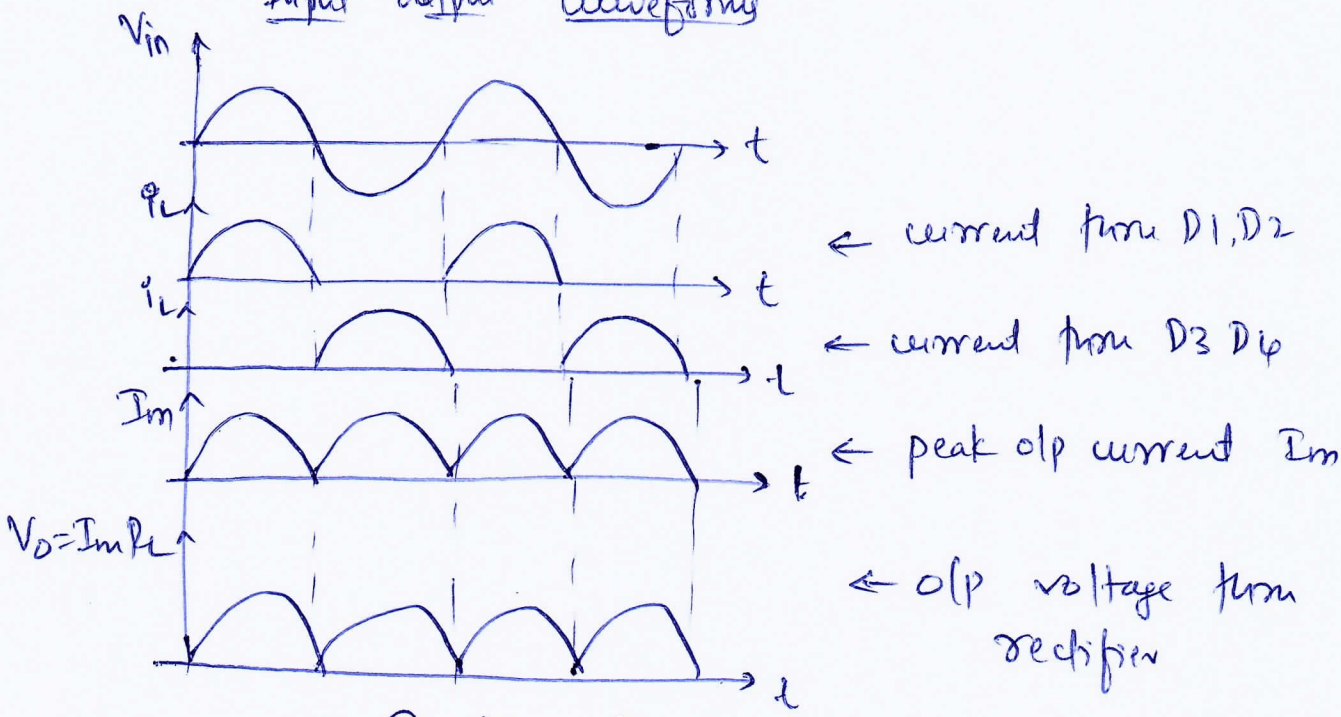


Fig 10 - Waveforms for BWR

Efficiency

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$= \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$P_{dc} = \frac{4}{\pi^2} I_m^2 R_L \quad -(1)$$

$$P_{ac} = I_{rms}^2 R_L$$

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 \cdot R_L$$

$$P_{ac} = \frac{I_m^2}{2} \cdot R_L \quad -(2)$$

Using (1) & (2)

$$\eta = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2}{2} \cdot R_L}$$

$$\eta = 0.81$$

$$\text{or } \eta = 81\%$$

2.a Half wave rectifier with capacitor filter.

Fig 10 shows the ckt of HWR with capacitive filter

6 marks

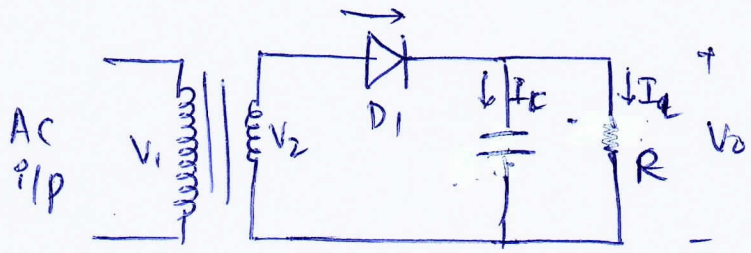
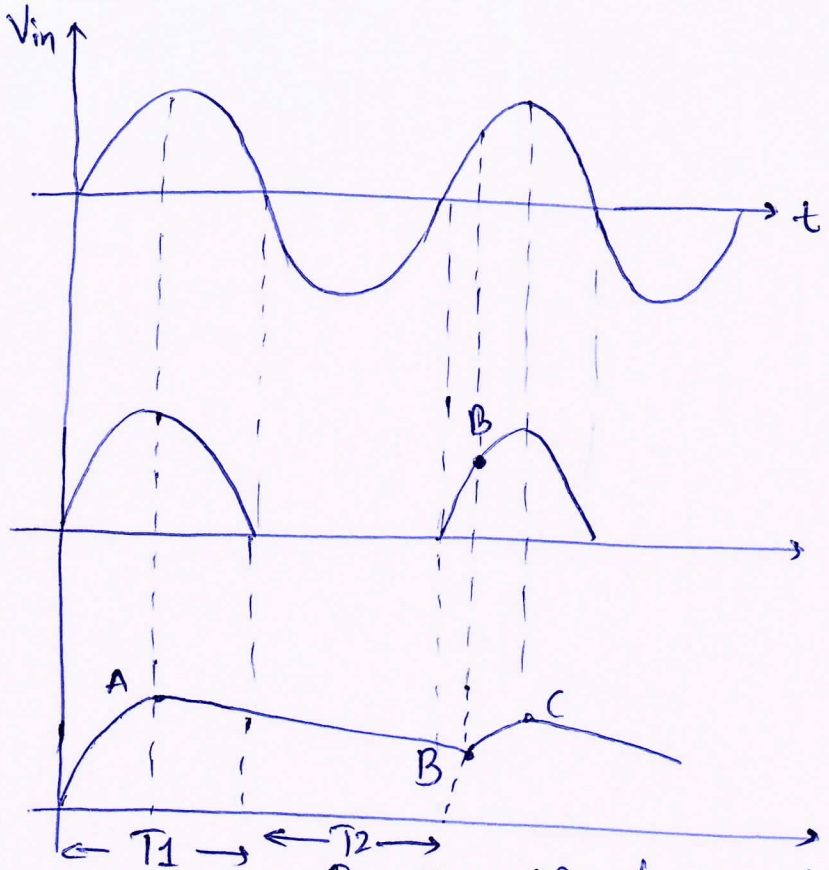


Fig 10 HWR with C-filter.

In order to minimize the ripple content in the o/p the capacitor 'C' is used in H.W.R.

- During the positive half cycle of the i/p voltge the
- Diode D1 is forward biased & the capacitor charges to its maximum value. Vm.
- The initial charging happens once when D1 is on.
- When i/p starts decreasing & falls below Vm the diode stops conducting because the diode is getting reverse biased.
- Under such scenario the capacitor starts to discharge.
- The discharging of capacitor continues until the capacitor starts to charge which happens only in next +ve cycle.
- The discharging of capacitor is decided by $R_L C$ time constant which is large & hence capacitor discharges very little from Vm.
- The waveforms in Fig 11 depicts the same



$T_1 + T_2$ = Total time.

Fig 11 - Waveforms of HWR with C-filter

The capacitor starts charging at point B where i/p exceeds the capacitor voltage.
From B onwards cap starts charging again & gets charged till V_m. This process continues to give the o/p as seen in Fig 11.

2.b Given $R_f = 10\Omega$ $R_L = 800\Omega$ $V_2 = 200V$

$V_m = \sqrt{2} V_2 = \sqrt{2} \cdot 200 = 282.8V$ 6 marks

$I_{dc} = \frac{2I_m}{\pi} \Rightarrow \boxed{222.3mA = I_{dc}}$

$\therefore I_m = \frac{V_m}{R_f + R_L} = \frac{282.8}{810} \Rightarrow \boxed{I_m = 349\ mA}$

$I_{rms} = \frac{I_m}{\sqrt{2}} = \boxed{246.7mA}$

$V_{dc} = I_{dc}(R_f + R_L)$

$\boxed{V_{dc} = 180V}$

or

$V_{dc} = 2V_m/\pi = 180V$ //

2.c Zener diode as voltage regulator

8 marks

Zener diode as regulator with R_L

Zener diode accepts unregulated DC supply as input & provides a constant DC o/p irrespective of changes in the load current & line voltage.

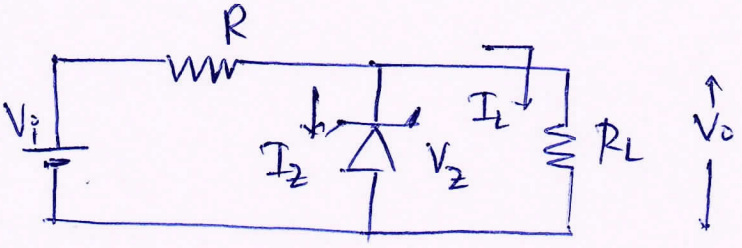


Fig 12 - Zener diode as regulator with load

- Zener diode operates in reverse breakdown region & has constant voltage V_Z across its terminals.
- For zener diode to operate in the breakdown the dc i/p V_i must be greater than the zener breakdown voltage V_Z
  i.e $V_i > V_Z$

Analysis

Since R_L and zener diode are in parallel voltage across R_L == voltage across zener diode. i.e

$V_o = V_Z$ —①

& V_o will be constant because V_Z is constant

∴ V_o remains constant even if there is any fluctuations in V_i until $V_i > V_Z$ condition is maintained

From Fig 12 we get

$I = I_Z + I_L$ —②

$I_Z = I - I_L$ —③

but $I = \frac{V_i - V_o}{R}$ —④

using ④ in ③

$I_Z = \left[\frac{V_i - V_o}{R}\right] - I_L$ —⑤

⑤ represents current through zener diode

Considering V_i variations betn $V_{i\,min}$ & $V_{i\,max}$ & I_L varies betn $I_{L\,min}$ & $I_{L\,max}$ & I_Z betn $I_{Z\,min}$ & $I_{Z\,max}$

$\therefore$ we write $I_{Z\,min} < I_Z < I_{Z\,max}$ — (6)

Now $I_{Z\,max}$ → max zener current flows when $V_i = V_{i\,max}$

& w.k.t $I = I_Z + I_L$

Constant = incr + decr

— if I_Z is maximum, then I_L will be minimum such that I is constant.

— $I_{Z\,max}$ flows when $V_i = V_{i\,max}$

& if I_Z is maximum then I_L will be minimum

So from (6) & (5)

$$I_Z < I_{Z\,max}$$

$$\left[\frac{V_{i\,max} - V_0}{R}\right] - I_{L\,min} < I_{Z\,max} \quad - (7)$$

Similarly for $I_Z > I_{Z\,min}$

$$\left[\frac{V_{i\,min} - V_0}{R}\right] - I_{L\,max} > I_{Z\,min} \quad - (8)$$

Thus zener diode regulates the current through it using conditions (7) & (8)

MODULE 02

3.a Construction & Working of n-JFET

9 marks

Construction

Figure 13 below shows the construction of N-channel JFET

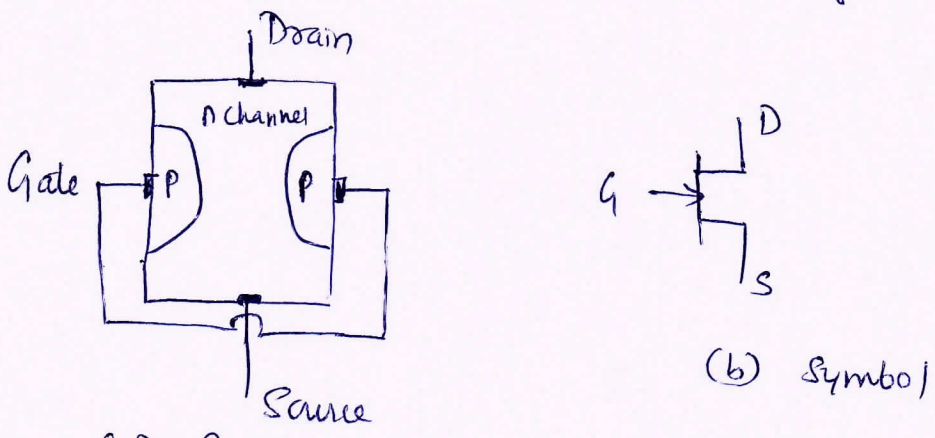


Fig 13 (a) Basic Structure (b) Symbol

Fig 13(a) shows the basic structure of a N-channel JFET Wire leads are connected to each end of the N-channel the drain is at upper end & the Source is at lower end. Two P type regions are diffused in the n-type material to form a channel & both p-type regions are Connected to the gate lead.

The symbol of n-JFET is shown in Fig 13 (b)

Operation

To illustrate the Operation of a JFET Fig 14 shows dc voltages applied to N-channel JFET.

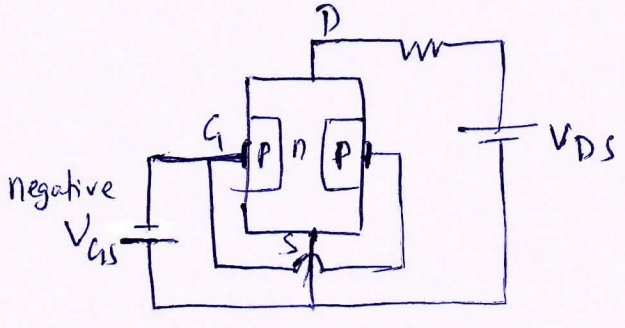


Fig 14

V_{DS} provides Drain to Source voltage & supplies current from drain to Source

V_{GS} sets the reverse bias bet^n gate & Source.
By default all JFET are depletion type.

When V_{GS} = negative the P-N junction formed inside the JFET will be reverse biased & as a result the reverse biased P-N jn increases the depletion width.
Due to this the channel narrows down & the current flow is affected.

- V_{GS} - helps in adjusting the width of the channel.
- Once V_{GS} is fixed, then V_{DS} is applied.

V_{DS} determines how much current (drain current) flows bet^n drain & Source.

In n-channel JFET V_{GS} is negative & V_{DS} is positive

Characteristics

Drain characteristics

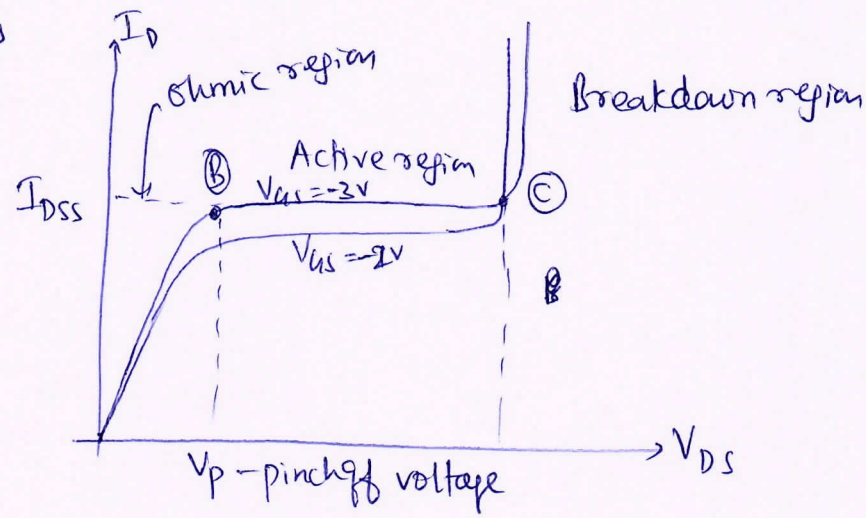


Fig 15 Drain Char of N-JFET

Ohmic region - Drain current increases linearly
Pinchoff voltage (V_p) - Point at which JFET enters Saturation & I_D doesn't depend on V_{DS}
Saturation region - I_D remains constant
Breakdown region - I_D increases rapidly due to breakdown of gate to Source jn due to avalanche

3.6 Working of CMOS inverter

6 marks

Figure 16 shows the structure of CMOS inverter. It consists of one P-channel MOSFET & one N-channel MOSFET.

P-channel mosfet is connected towards V_{DD} & N-channel MOSFET is connected towards ground.

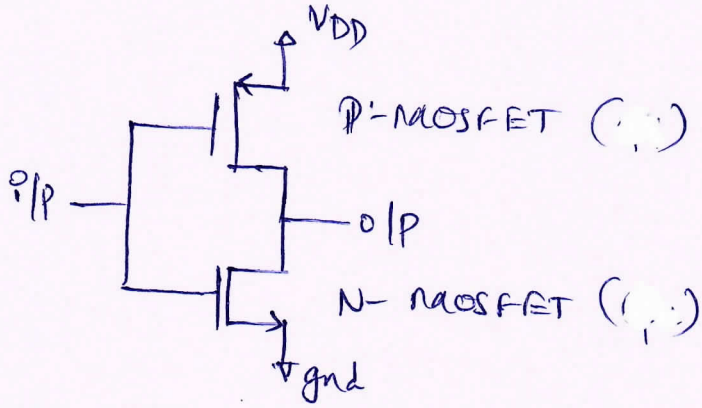


Fig. 16(a) CMOS inverter.

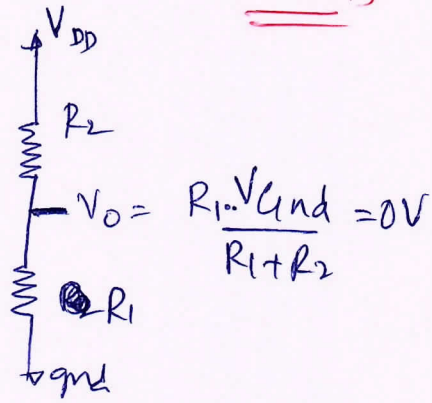


Fig 16 (b) Equivalent ckt for $V_{in} = 5V$ (logic 1)

Case (i)

When $V_{in} = 5V$ or logic 1 State

When i/p is +ve the P-channel MOSFET does not create the channel & hence PMOS does not conduct the current, which means PMOS is in its off state for $V_{in} = 5V$

~~So, when $V_{in} = 5V$~~

But for $V_{in} = 5V$ (+ve), the n-channel MOSFET conducts the current by creating the channel, which means NMOS is in its ON state for $V_{in} = 5V$.

∴ For i/p ⇒ logic 1 (5V) PMOS OFF, NMOS ON } $V_o = (0V)$ logic 0

∴ Considering the equivalent ckt from Fig 16 (b) we can calculate o/p voltage as $V_o = \frac{R_1 \cdot V_{Gnd}}{R_1+R_2} = 0V$

∴ $V_o = 0V$ //

Case (2)

When $V_{in} = 0V$ or logic 0 state

When i/p is 0V or logic 0 or -ve value then the P-channel MOSFET conducts by creating the channel & as a result PMOS will be in its ON state.

On the other hand for the i/p $V_{in} = 0$ the N-channel MOSFET (NMOS) does not conduct because there will be no channel. Hence for $V_{in} = 0$ the NMOS will be in its OFF state

∴ For i/p ⇒ logic 0 (0V) PMOS ON, NMOS OFF } $V_o = (5V)$ logic 1

From the equivalent ckt we can find the o/p as

$$V_o = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \Rightarrow 5V //$$

3.c Given $I_{DSS} = 9mA$ $V_p = -6V$ $V_{GS} = -4V$ $I_D = 3mA$

a) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$ 5 marks

$= 9m\left[1 - \frac{(-4)}{(-6)}\right]^2 = I_D = 1mA //$

b) $V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right] \Rightarrow -6m\left[1 - \sqrt{\frac{3}{9}}\right] \Rightarrow \boxed{V_{GS} = -2.53\ mV}$

4.a Enhancement MOSFET – Considering N-channel E-MOSFET

Construction

9 marks

The basic structure of N-channel enhancement type MOSFET can be seen in fig 17.

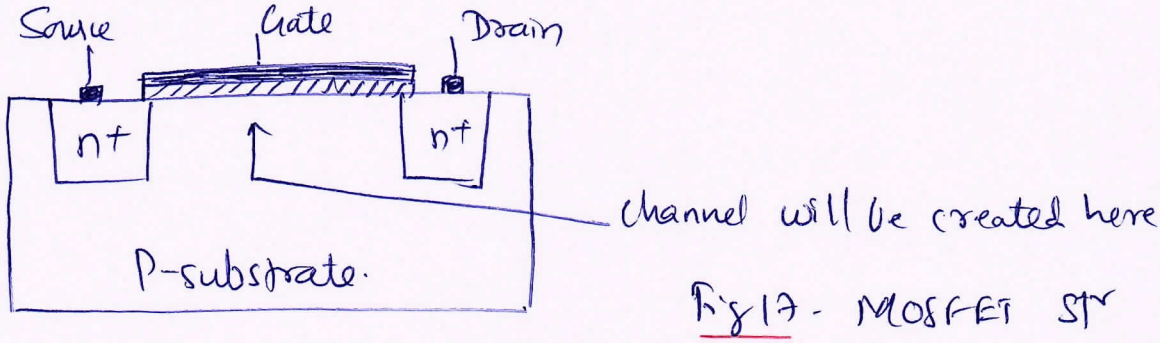


Fig 17 - MOSFET Str

The N-channel mosfet has 3 terminals Source, Gate, Drain. Two n^+ diffusions are made at Source & Drain Side.

A p-type substrate is the basic structure upon which n-type regions are diffused to obtain Source & Drain. An oxide layer is placed exactly at the centre between Source & Drain. Metallic layer is placed above the oxide layer. The gate contact is taken from the middle of the metallic layer. The gate is electrically insulated from both n-type & p-type ~~regions~~ substrate.

Regardless of the polarity of applied voltage, no e^- can flow from Source to drain because the n-type Source, p-type substrate & n-type drain ~~to~~ behave as two p-n jn connected back-to-back & one of them is always reverse biased

Operation

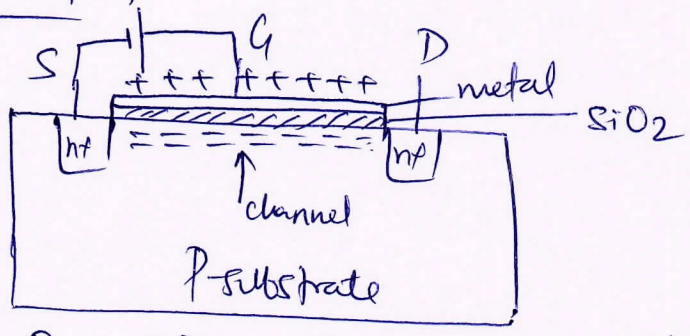


Fig 18(a) operation

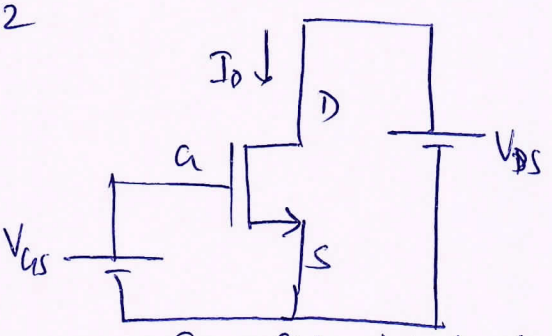


Fig 18(b) ckt level opn

(i) With no gate voltage

With no gate voltage there is no gate current conduction from drain to Sour as no channel is formed.

(ii) Creating a channel

With V_{GS} = +ve. & ~~No~~ $V_{DS} = 0$

When V_{GS} & +ve voltage is applied the +ve charges from V_{GS} attracts the -ve charges & these -ve charges are accumulated beneath the oxide layer forming a layer known as channel.

~~Here a V_{GS} & V_{GS} &~~

The process & creation & channel continues until ample e^- are made to sit beneath the oxide ~~so that~~ such that it assists in the flow & current.

The ~~point~~ ~~at~~ voltage at which ample & amount & e^- are attracted to form a proper channel is known as threshold voltage. Once channel is formed V_{GS} is ~~fixed~~ & will not be increased.

Fig. 18(a) depicts the same.

With V_{GS} = fixed value V_{DS} = Some +ve voltage.

under this Condn the e⁻ from the V_{DS} battery are pushed into Source & they move from Source to Drain through the channel.

Under this scenario we say that the mosfet has started to conduct the current.

Characteristics

I_D v/s V_{GS} (Transfer Characteristics)

Fig 19(a)

I_D v/s V_{DS}

Drain Characteristics

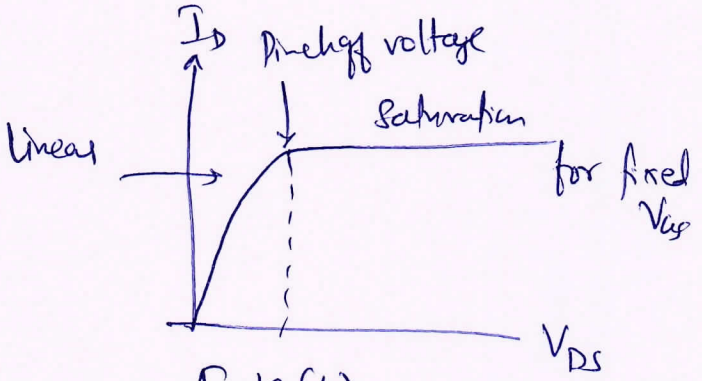


Fig 19 (b)

Fig 19(a) & 19(b) depicts the transfer & drain char of n-MOS. From the graphs we can see various modes of operation.

The point at which the current remains Constant is known as pinchoff point & the region after pinchoff voltage is - saturation region.

4.b Working of Silicon Controlled Rectifier (16)

SCR is a switching device widely used in power control applications. The basic operation of ~~an~~ SCR can be best explained by splitting the 4-layer PNPN structure into two - three layer structure as shown in Fig 20.

6 marks

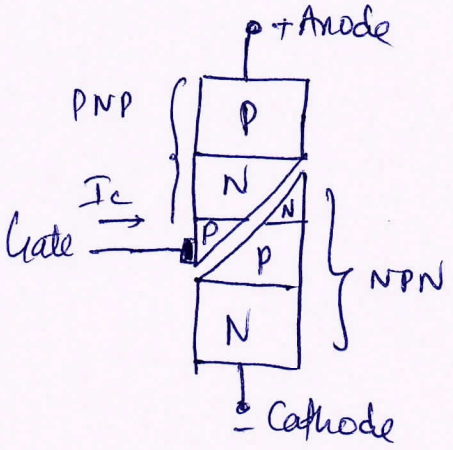


Fig 20(a) Cross sectional view

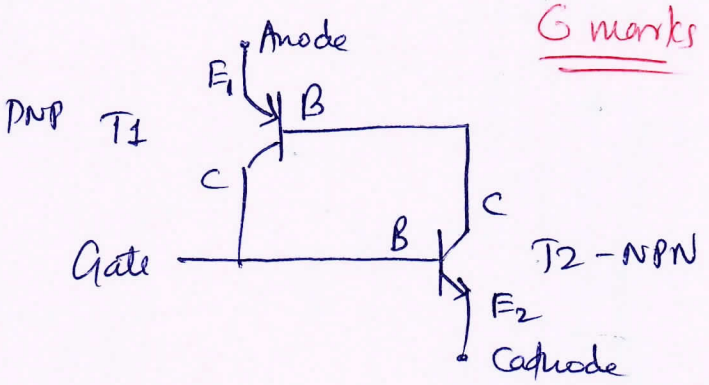


Fig 20(b) Equivalent ckt

Thus the equivalent ckt of SCR is composed of pnp transistor & npn transistor as seen in Fig 20.

Switching action (operation)

Let a positive voltage V be applied to the anode (E1) & let the cathode (E2) & gate (G) be both grounded as shown in fig 20.

As $V_G = V_{BE2} = 0$ the transistor T2 is in off state. It means that the C-B j^n of T2 through E-B j^n of T1 is R/B. Therefore $I_{B1} =$ very low or no base current hence the anode current $I_A = I_{B1} = 0$. Thus making SCR to off.

Now let $V_G > 0$ be applied at gate. As $V_{BE2} = V_G$ when V_G is sufficiently large I_{B2} will cause T2 to turn ON & I_{C2} becomes large. As $I_{B1} = I_{C2}$, T1 turns on causing I_{C1} to flow. this in turn increases I_{B2} causing a regenerative action. As a result SCR turns ON

The collector current of T1 is base current of T2. This action being very cumulative since an incr of current in one transistor causes incr of current in another. As a result both tx are in saturation & heavy current flows

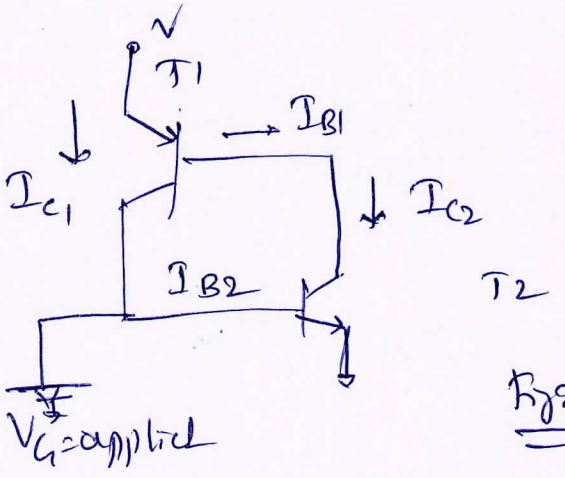


Fig 21 with V_G applied

4.c

5 marks

$$K = \frac{I_{Don}}{(V_{GSon} - V_T)^2} = \frac{4 \times 10^{-3}}{(6-4)^2} = 1\,mA/V^2$$

$$I_D = K(V_{GS} - V_t)^2 = 1\,mA/V^2 (8-4)^2 \Rightarrow 16\,mA \;//$$

MODULE 3

5.a Opamp is a direct coupled multistage voltage amplifier with extremely high gain.

6 marks

Characteristics

1) Infinite voltage gain $A = \infty$
2) Infinite input impedence $Z_{in} = \infty$ or $R_{in} = \infty$
3) Zero o/p impedence $Z_{out} = 0$
4) Zero offset voltage
5) Infinite B/W
6) Infinite slew rate
7) Infinite CMRR

5.b

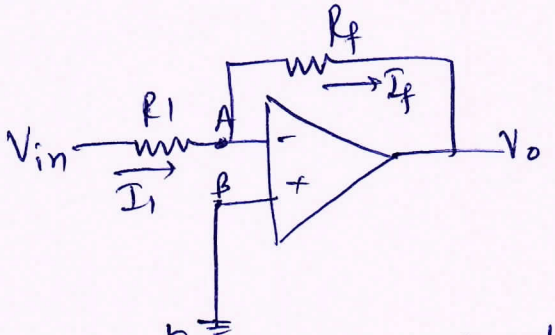


Fig-22 opamp inverting configuration

6 marks

$$I_1 = \frac{V_{in} - V_A}{R_1} \quad - (1)$$

$$I_f = \frac{V_A - V_o}{R_f} \quad - (2)$$

From the concept of virtual gnd

$V_A = V_B \quad \therefore V_A = 0$

Also no current can enter opamp due to high R_{in} $\therefore I_1 = I_f$

$$\therefore \frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{R_f} \Rightarrow V_o = -V_{in}\left(\frac{R_f}{R_1}\right) \;//$$

5.c Opamp integrator

8 marks

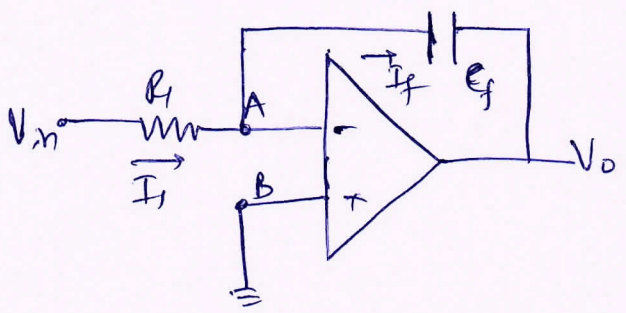


Fig 23 (a) Opamp integrator.

From the concept of virtual gnd

$V_A = V_B = 0$.

Also due to high i/p resistance No current can enter opamp.

$\therefore \quad I_1 = I_f \Rightarrow \quad I_1 = \frac{V_{in} - V_A}{R_1} \quad -(1) \qquad I_f = C_f \frac{d(V_A - V_o)}{dt} \quad -(2)$

$$\frac{V_{in} - V_A}{R_1} = C_f \frac{d(V_A - V_o)}{dt} \Rightarrow \text{(substitute } V_A = 0\text{)}$$

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt}$$

integrating on both sides

$$\int_0^t \frac{V_{in}}{R_1} = -C_f V_o \Rightarrow \boxed{V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in}}$$ //

Opamp voltage follower

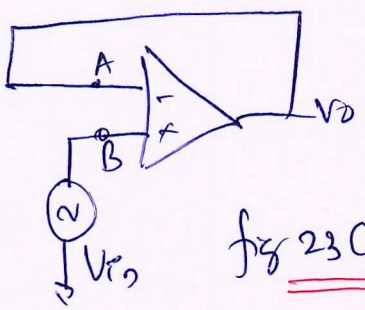


Fig 23 (b) voltage follower

Since B is at V_{in} $\therefore V_A = V_{in}$

& since V_A is directly connected to o/p we have

$V_o = V_A = V_{in}$

$\therefore \boxed{V_o = V_{in}}$ //

6.a Different input modes of opamp

6 marks

There are two modes in which opamp can operate

1) Common mode
2) Differential mode

Common mode -

- Two voltages are applied which are equal in all aspects i.e $V_1 = V_2$.
- Under such scenario the gain is known as common mode gain given by $A_C = \frac{V_o}{V_c}$

$$V_C = \frac{V_1 + V_2}{2} \quad -(1)$$

- When we apply common signal, then ideally the o/p voltage must be zero, but the o/p voltage of the practical opamp also depend on avg common level of i/p which is denoted by (1)

The gain is A_C.

Differential mode

- For any two different i/p the o/p of opamp is given as $V_o = A_d (V_1 - V_2)$ — (2)

A_d – differential gain -

The opamp amplifies the difference between 2 i/p signals

- The voltage $V_1 - V_2 \rightarrow$ difference voltage V_d

$$V_o = A_d V_d \quad \text{or} \quad A_d = \frac{V_o}{V_d}$$

For ideal opamp A_d must be ∞ while A_c must be 0

6.b Given $V_o = -[2V_1 + 3V_2 + 5V_3]$ $R_f = 10k\Omega$

W.K.T $V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$ 6 marks

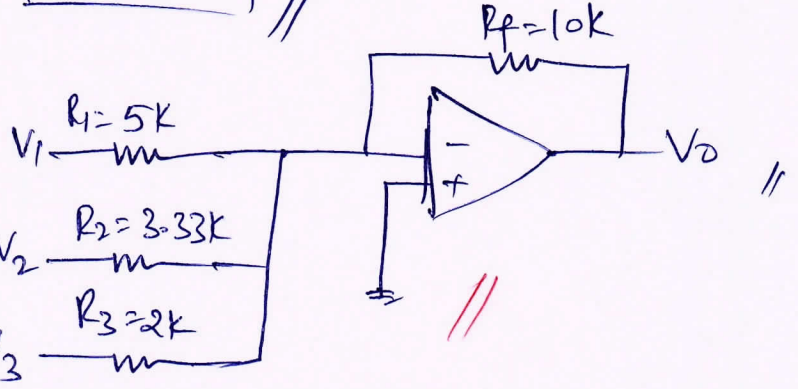
Comparing the given eqn with standard eqn we get

$\frac{R_f}{R_1} = 2 \quad \frac{R_f}{R_2} = 3 \quad \frac{R_f}{R_3} = 5$

$\therefore \frac{10k}{R_1} = 2 \Rightarrow \boxed{R_1 = 5k\Omega} \quad \frac{10K}{R_2} = 3 \Rightarrow \boxed{R_2 = 3.33k\Omega}$

$\frac{10k}{R_3} = 5 \Rightarrow \boxed{R_3 = 2k\Omega}$ //

Designed ckt ⇒



//

6.c CMRR – Ratio of differential voltage gain (A_d) to common mode voltage gain (A_c) $CMRR = \frac{A_d}{A_c}$ 8 marks

- CMRR – expressed in dB
- ideally CMRR = ∞ practically very high.
- Higher the CMRR, better is the ability of opamp to reject the common mode signal

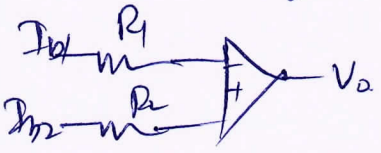
Slew rate – Defined as max rate of change of o/p voltage with time $S = \left.\frac{dV_o}{dt}\right|_{max}$ V/μsec

- due to slew rate, for a particular i/p freq o/p gets distorted.

- i/p bias current

avg value of dc current flowing into opamp

$I_b = \frac{I_{b1} + I_{b2}}{2}$



Supply voltage rejection ratio SVRR or PSRR

SVRR is defined as ratio of the change in i/p offset voltage due to the change in supply voltage producing it, keeping other power supply constant.

$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{\text{Constant } V_{EE}}$ //

Module 04

7. a

BJT amplifies current because the collector current is equal to the base current multiplied by the current gain β. The base current in a transistor is very small compared to the collector & emitter current. Because of this the collector current is approximately equal to emitter current.

Fig. 30 shows the basic transistor amplifier ckt with ac source voltage V_s is superimposed on the dc bias voltage V_{BB}. By capacitive coupling. The dc bias voltage V_{BB} is connected to base through base resistor R_B & dc bias voltage V_{cc} is connected to collector through collector resistor R_c.

The B-E jn has very low resistance to ac signal. This internal resistance is denoted by r_e' & appears in series with R_B. The ac base voltage is

$$V_b = I_e r_e' \quad - (1)$$

8 marks

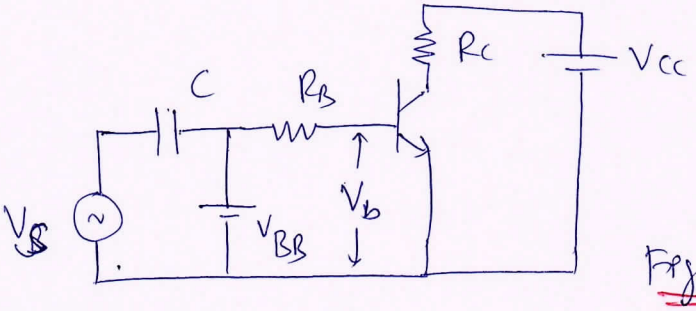


Fig. 30 – BJT as amplifier.

Since $I_c \approx I_e$

$$V_c = I_e R_c \quad - (2)$$

$$V_b = V_s - I_b R_B \quad - (3)$$

$$A_v = \frac{V_c}{V_b} \approx \frac{I_e R_c}{I_e r_e'} \quad \therefore \boxed{A_v = \frac{R_c}{r_e'}} \; //$$

7.b RC phase shift Oscillator.

8 marks

The phase shift is achieved by RC network. Because of the loading effect, three RC stages are needed as shown in Fig. 29.(a)

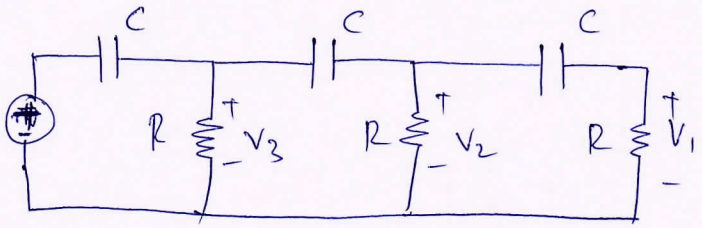


Fig 29(a) RC phase shifting nlw.

$$\bar{\beta} = \frac{\bar{V}_1(j\omega)}{\bar{V}_0(j\omega)}$$

By equating the j part of it in the denominator, we find the freq at which β is -ve (180° phase shift)

The results we get are,

freq of oscillation $\omega_0 = \frac{1}{RC\sqrt{6}}$ - ①

& $\beta(\omega_0) = \frac{-1}{29}$; 180° phase shift - ②

For oscillations to occur

$$|\bar{\beta}| > \frac{1}{29}$$

freq of oscillation $\omega_0 = \frac{1}{RC\sqrt{6}}$

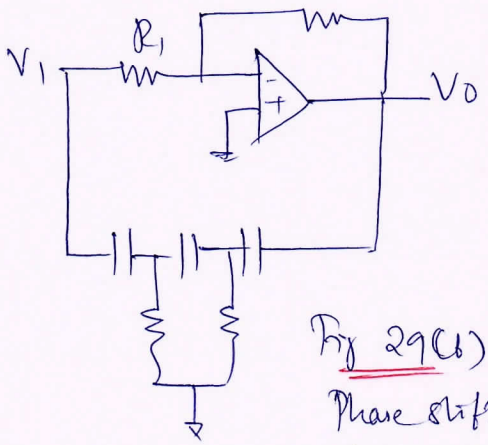


Fig 29(b)
Phase shift Oscillator using Opamp

$$A = \frac{-R_f}{R}$$

$$A\bar{\beta} = \frac{-1}{29}\left(\frac{-R_f}{R}\right)$$

$$= \frac{R_f}{29R} > 1 \text{ by about 5\%.}$$

$R_f > 29R$

7.c

4 marks

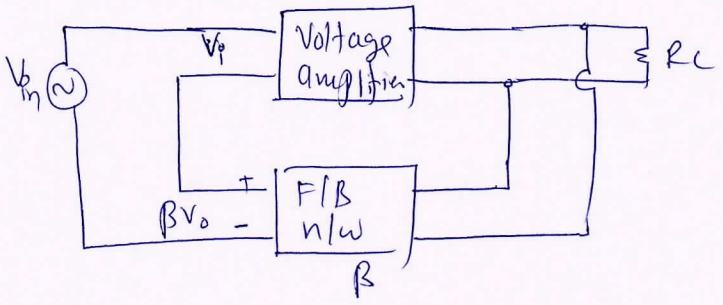


Fig 31 - Voltage series f/b amplifier

Let V_i - i/p that enters voltage amplifier

V_o - o/p of voltage amplifier

After feedback the i/p voltage V_i becomes

$$V_i = V_{in} - \beta V_o \quad - (1)$$

W.K.T $V_o = A V_i \quad - (2)$

Substitute (1) in (2)

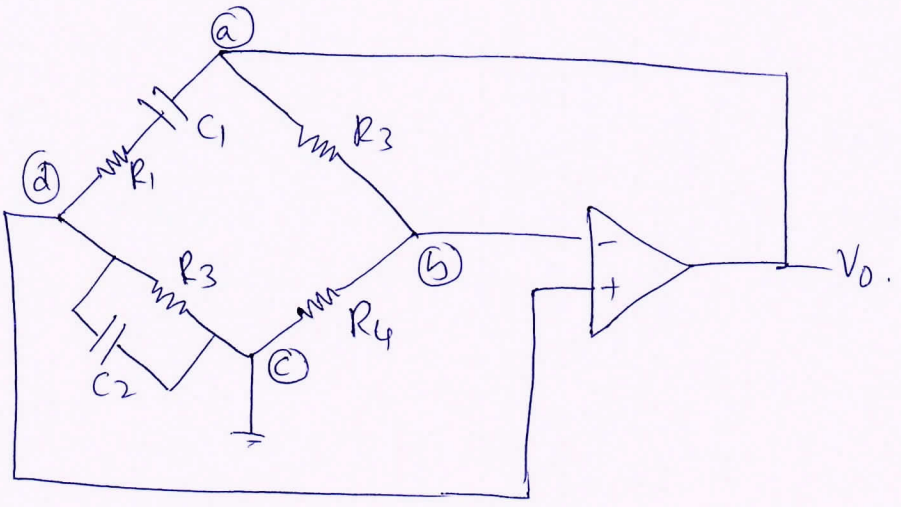
$$V_o = A(V_{in} - \beta V_o) \Rightarrow V_o = A V_{in} - A\beta V_o$$

$$V_o + A\beta V_o = A V_{in}$$

$$V_o(1 + A\beta) = A V_{in} \Rightarrow \boxed{\frac{V_o}{V_{in}} = \frac{A}{1 + A\beta}} \quad - (3)$$

(3) represents voltage gain for voltage-series f/b ampl^r.

8.a



8 marks

Fig. 31 Wein bridge Oscillator

- Fig 31 depicts the Wein bridge oscillator.
- The forward path uses an opamp used in non-inv mode. Thus it does not introduce any phase shift
- The f/b n/w uses a bridge ~~n/w~~ called Wein bridge
- The two arms of the bridge namely R_1 C_1 in series & R_2 C_2 in parallel are called freq sensitive arms.
- This is because the components of these two arms decide the freq of oscillator. Such a f/b n/w is called lead lag n/w
- This is because at very low frequencies it acts like a lead while at very high freq it acts as lag network
- The o/p is bet a & c
- i/p is bet b & d

gain of amplifier is decided by R_3 & R_4

$$A = 1 + \frac{R_3}{R_4}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \text{ Hz.}$$

$$f_0 = \frac{1}{2\pi RC} \text{ Hz.}$$

The components are selected such that

$R_1 = R_2 = R$ & $C_1 = C_2 = C$

- With $R_1 = R_2 = R$ & $C_1 = C_2 = C$ the β of network gain $\beta = \frac{1}{3}$ & to satisfy Barkhausen Criteria $A\beta > 1$ $A \geq 3$ for the amplifier

8.b

555 timer as astable multivibrator

8 marks

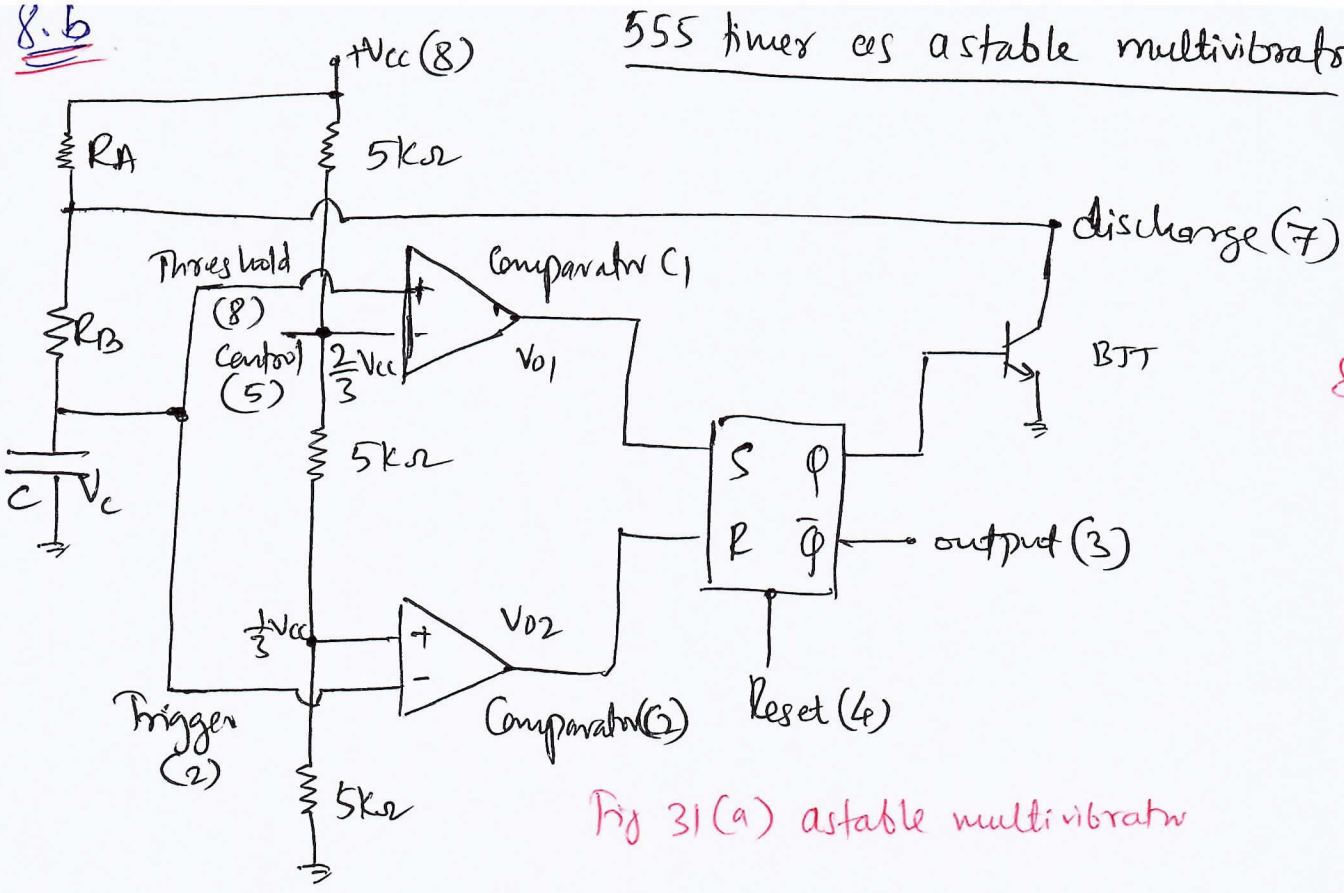


Fig 31 (a) astable multivibrator

- Here trigger & threshold are tied together.
- Initially we assume capacitor C = 0. (no charge)

  When C=0, for comparator C2 -ve terminal at 0V
  +ve terminal at $\frac{1}{3}$ Vcc

  Hence V_{o2} = +Vcc = logic 1. ∴ R = 1

  This makes o/p of S-R flip flop Q = 0 or $\bar{Q}$ = 1
- Once Q = 0, the BJT is off. & it behaves as open switch.
- Because the capacitor is initially empty, now it starts to charge through RA & RB from Vcc.
- The capacitor charges till $\frac{2}{3}$ Vcc, & as soon as the capacitor charge goes above $\frac{2}{3}$ Vcc, the comparator 1 will do the comparison.

now for comparator C1, +ve terminal at more than $\frac{2}{3}V_{cc}$
-ve terminal at $\frac{2}{3}V_{cc}$

∴ +ve terminal at highest potential..
-ve " lowest potential

∴ o/p of Comparator C1 = $+V_{cc}$ or logic 1.

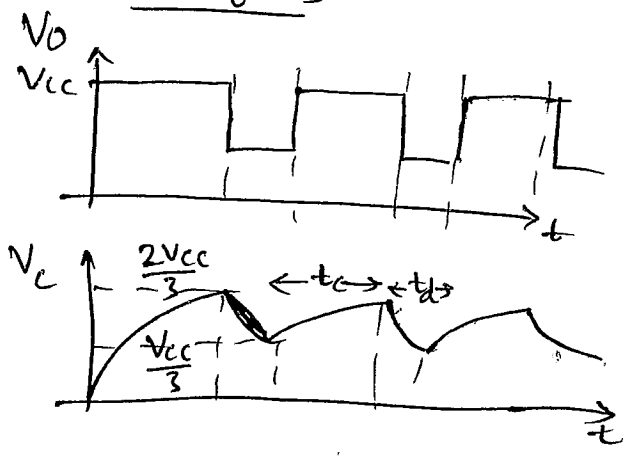
∴ S = 1. This makes o/p of S-R flip flop $\varphi = 1$ $\overline{\varphi} = 0$

- The moment $\varphi = 1$ the BJT is ON. & acts as short circuit.
- As a result of this the capacitor discharges & its value starts to decrease.
- As soon as the capacitor charge reaches just below $\frac{1}{3}V_{cc}$ the Comparator 2 will again throw the result as '1' because +ve terminal of Comparator 2 is at $\frac{1}{3}V_{cc}$ &
-ve " " " at less than $\frac{1}{3}V_{cc}$

& this process continues & as a result of which for every charging & discharging action the o/p will be either '1' or '0'. Hence a square waveform is generated.

st charging 0 to $\frac{2}{3}V_{cc}$
st discharging $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$
d charging $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$
d discharging $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$

Waveforms



For astable multivibrator. the capacitor voltage can be said ~~§~~ to consisting ~~§~~ charging time constant (t_c) & discharging time constant. (t_d)

$$t_c = 0.69(R_A + R_B)C.$$

$$t_d = 0.69 R_B . C$$

$$T = t_c + t_d \Rightarrow 0.69(R_A + 2R_B)C$$

Free running frequency or. frequency ~~§~~ Oscillation is

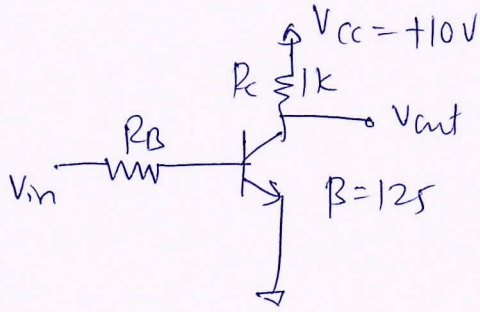
$$f_0 = \frac{1}{T} = \frac{1.45}{(R_A + R_B)} \quad \frac{1.45}{(R_A + 2R_B)C}$$

$$\% \text{ duty cycle} = \frac{t_c}{T} \times 100$$

$$\%. \text{ duty cycle} = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} \Rightarrow \frac{R_A + R_B}{R_A + 2R_B} \times 100 \rightarrow (1) \quad //$$

to ~~need~~ generate a Square wave, the duty cycle must be 50 %, which is made possible by making $R_A = 0$ in eqn (1) $\therefore$ %. duty cycle (Square wave) $= \frac{0 + R_B}{0 + 2R_B} \times 100 = 50\%$ //

8.c



4 marks

a) V_{CE} at $V_{in} = 0$ the transistor is in cutoff ∴

$$V_{CE} = V_{CC} = 10V \;//$$

b) $$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

but $$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10V}{1k} \Rightarrow 10mA$$

$$\therefore I_{B(min)} = \frac{10m}{125} \Rightarrow I_{B(min)} = 80\mu A \;//$$

c) $$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}}$$

but $$V_{R_B} = V_{in} - V_{BE} = 8 - 0.7 = 7.3V$$

$$\therefore R_{B\,max} = \frac{7.3}{80\mu} = 91.25\,k\Omega \;//$$

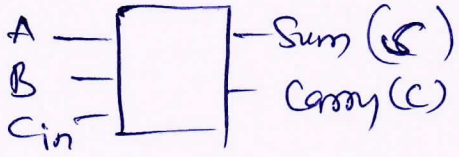
//

MODULE 05

9.a **Full adder using basic gates**

- Here 3 bits can be added at a time. The 3rd bit is a carry from previous lower significant bit.
- Thus full adder is a combinational ckt that performs arithmetic sum of 3 i/p bits.
- Let 3 i/p be A B & Cin & two o/p Sum, Carry
  - The third i/p Cin represents the carry from the previous lower significant bit.

8 marks



Truth table

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = \bar{A}\bar{B}Cin + \bar{A}B\bar{Cin} + A\bar{B}\bar{Cin} + ABCin$

$Sum = \bar{Cin}[\bar{A}B + A\bar{B}] + Cin[\bar{A}\bar{B} + AB]$

$= \bar{Cin}(A \oplus B) + Cin(\overline{A \oplus B})$

$=$ Cin Let $x = A \oplus B$, $y = \overline{A \oplus B}$

$\therefore Sum = \bar{Cin}\,x + Cin\,\bar{x}$

$Sum = Cin \oplus x$

$\boxed{Sum \Rightarrow Cin \oplus A \oplus B}$

$Carry = \bar{A}BCin + A\bar{B}Cin + AB\bar{Cin} + ABCin$

$BCin[A + \bar{A}]$

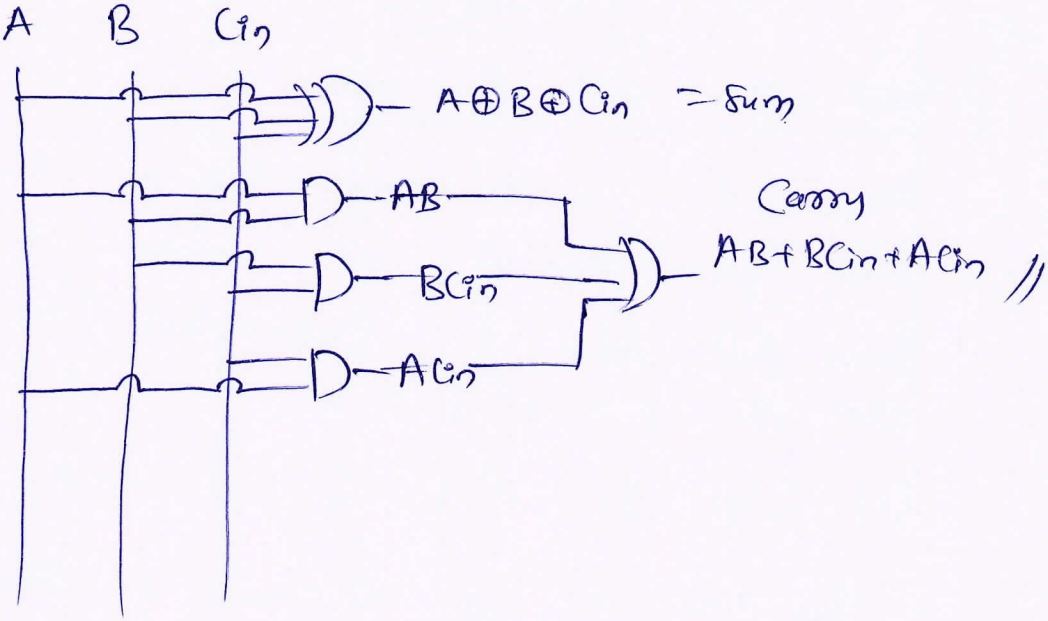
use identity $A + \bar{A} = A$

$Carry = \bar{A}BCin + A\bar{B}Cin + AB\bar{Cin} + ABCin + ABCin$

$BCin(A + \bar{A}) + A\bar{B}Cin + AB\bar{Cin} + ABCin + ABCin$

$BCin + ACin(\bar{B} + B) + AB(\bar{Cin} + Cin) \Rightarrow \boxed{Carry = BCin + ACin + AB}$ //

Fig 24



9.b (i) $(1101\ 0111\ 0110\ 1010)_2 = (D76A)_{16}$

(ii) $(EB986)_{16} = (1110\ 1011\ 1001\ 1000\ 0110)_2$

(iii) $(925.75)_{10} = (1635.6)_8$ //

6 marks

8	925	$0.75 \times 8 = 6$
8	115 – 5	
8	14 – 3	
	1 – 6 ↑	

9.c Communication System

Communication is the process of transferring information from one point to the other.

6 marks

The block diagram is as shown in fig 25

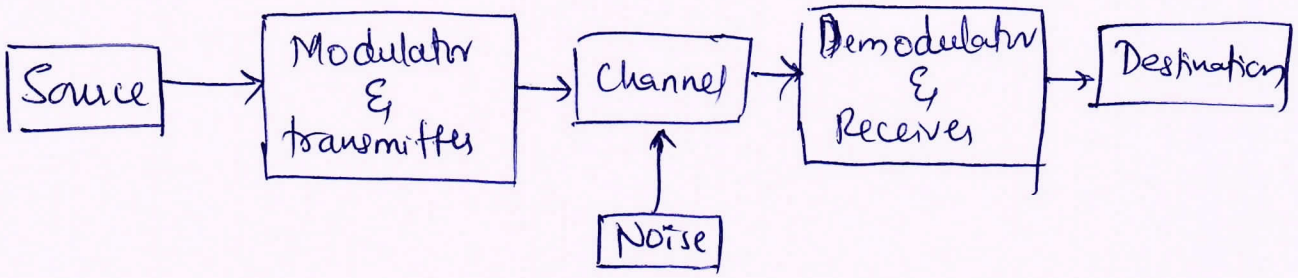


fig 25 Communication system

Source – The aim of a communication system is to convey a message & this message originates from a source.

Modulator & transmitter :- It processes the message from source & makes it suitable for transmission over the channel. The transmitter consists of encoders, decoders, transducers, ampl^r. etc

A signal in its original form is called baseband signal & transfer of these signals directly over the channel is called as broadband communication.

However baseband signals cannot travel longer distance & they get attenuated as well. Hence modulator is used

9.c Continued ... (30)

Channel - It is the physical medium that connects transmitter & receiver. Communication channels can be pair of conductors, optical fibre or just free space (wireless communication)

Noise - Noise is any unwanted random signal that gets added to the message during communication

Demodulator & Receiver - It performs the reverse process of modulation & transmission. The receiver processes the signal & gets back the actual msg. that was transmitted. Demodulator extracts the msg from the carrier wave.

10.a De-morgans theorem

Theorem 1 - The compliment of the product of two variables is equal to the sum of the compliment of each variable.

$\overline{A B} = \bar{A} + \bar{B}$ Theorem 1

6 marks

A	B	$\bar{A}$	$\bar{B}$	AB	$\overline{AB}$	$\bar{A}+\bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

↑ = ↑

Theorem 2 - The compliment of the sum of two variables is equal to the product of the compliment of each variable

$\overline{A+B} = \bar{A}\bar{B}$

A	B	$\bar{A}$	$\bar{B}$	$\bar{A}\bar{B}$	$A+B$	$\overline{A+B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

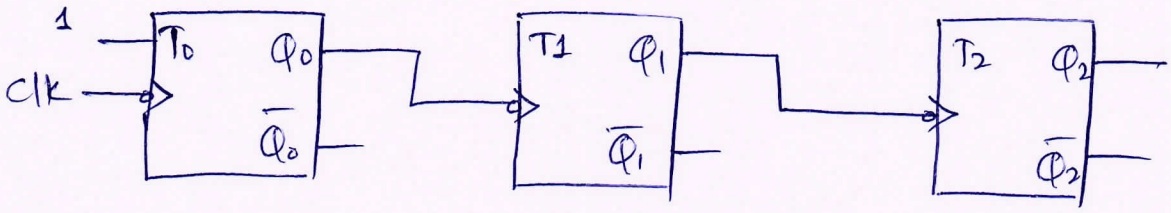
↑ = ↑

Hence proved //

10.b 3 bit ripple Counter

A Counter is a sequential ckt that Counts the no. of i/p pulses.

Fig 26(a) 3-bit Counter — 6 marks



The flip flops are -ve edge triggered. All the T inputs are kept High (1) for toggling State. The clk is given to the first T flf & other two receive the clock pulses from the o/p of preceding flip flops. The clock pulses ripples from through the flf & hence the name.

The Counter is initially reset to $Q_0 Q_1 Q_2 = 000$. When the first clock pulse is applied the values in each flip flop will be $Q_0 Q_1 Q_2 = 100$. The state of Counter after 2nd clk will be $Q_0 Q_1 Q_2 = 010$. This process continues. At the 8th ~~clock~~ clock pulse the Counter resets to 000. Thus Counter counts from 000 to 111. Hence it's also known as mod-8 counter.

clk	Q_2	Q_1	Q_0	i/p
Initial	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	1	1	0	6
↓	1	1	1	7
↓	0	0	0	8

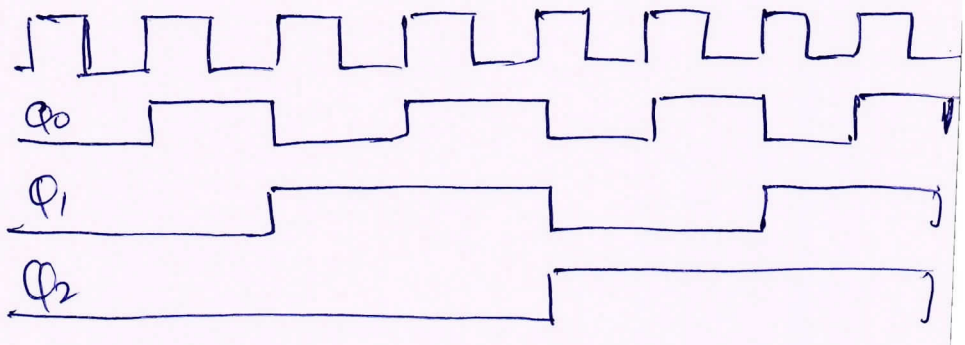
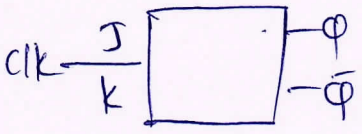


Fig-26(b) timing waveform for 3 bit Counter

//

10.c Flip flop is a bistable memory element which has two states 0 or 1.

8 marks



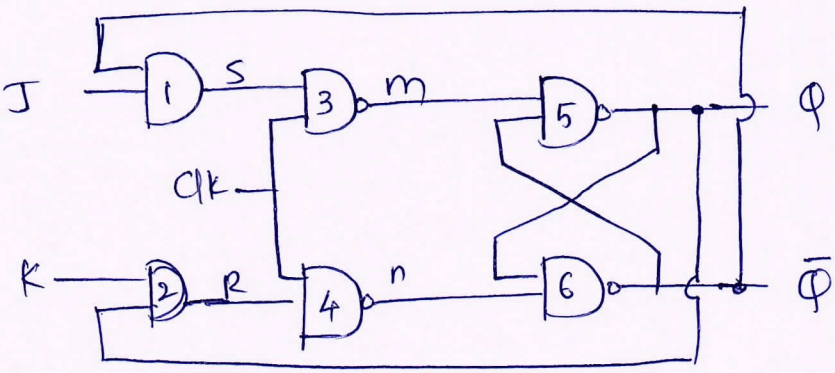


Fig 27 J-K flip flop

Truth table

J	K	Q	$\bar{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	toggle.	

Case(i) Let J=0 K=1 Q=0 $\bar{Q}$=1

① ⇒ $\bar{Q}$=1 S=0 J=0 ③ S=0 m=1 clk=1 ⑤ m=1 Q=0 $\bar{Q}$=1

② ⇒ K=1 Q=0 R=0 ④ clk=1 n=1 R=0 ⑥ Q=0 $\bar{Q}$=1 n=1

∴ For J=0 K=1 Q=0 $\bar{Q}$=1

Case(ii) let J=0 K=0 & Q=0 $\bar{Q}$=1

① ⇒ $\bar{Q}$=1 S=0 J=0 ③ S=0 m=1 clk=1 ⑤ m=1 Q=0 $\bar{Q}$=1

② ⇒ K=0 Q=0 R=0 ④ clk=1 n=1 R=0 ⑥ Q=0 $\bar{Q}$=1 n=1

∴ For J=0 K=0 flip flop still remains in its original state

Case(iii) for J=1 K=1 Q=0 $\bar{Q}$=1

① $\bar{Q}$=1 S=1 J=1 ③ S=1 m=0 clk=1 ⑤ m=0 Q=1 $\bar{Q}$=1

② K=1 Q=0 R=0 ④ clk=1 n=1 R=0 ⑥ Q=1 $\bar{Q}$=1 n=1

Under this state o/p will be in toggling state

10.c Continued...

Master slave flip flop

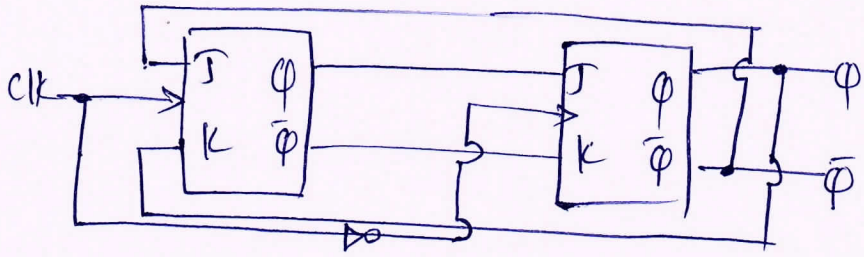


Fig 28(a)

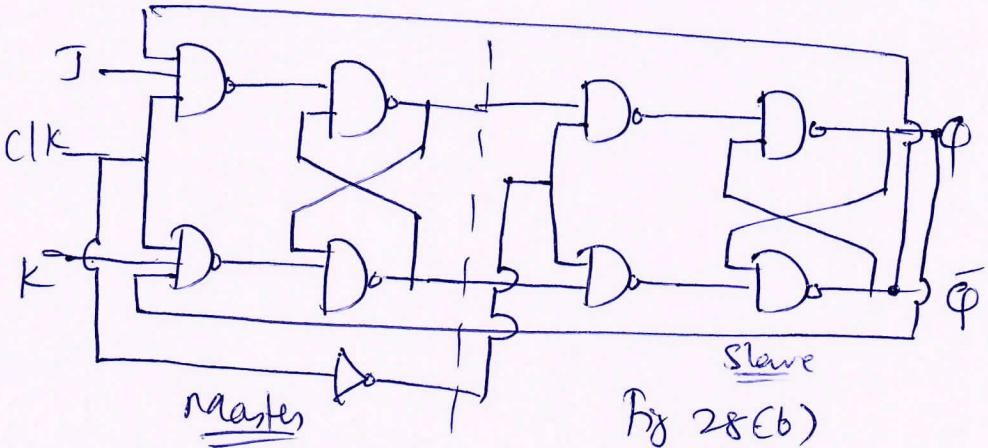


Fig 28(b)

Master slave - J-K flip flop

The main reason for going into master slave J-K flip flop is to avoid toggle state.

Master flip flop works on clock slave works on -ve clk. When master is on slave is off & vice versa. //