1

CBCS SCHEME

USN | | | | | | | | | | |

18EC32

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Network Theory

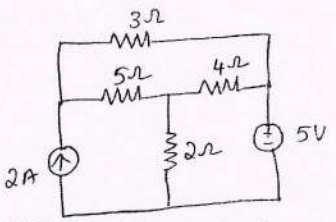
Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

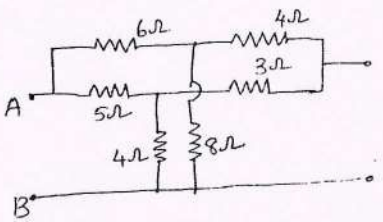
1 a. Using source transformation and source shifting techniques, find voltage across 2Ω resistor as shown in Fig.Q.1(a). **(07 Marks)**

Fig.Q.1(a)



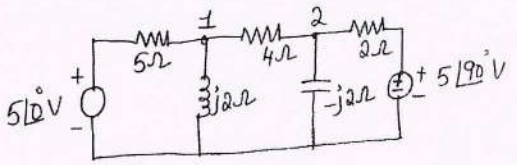
b. For the network shown in Fig.Q.1(b), find the equivalent resistance between A and B using Star-Delta transformation. **(05 Marks)**

Fig.Q.1(b)



c. Determine the node voltages V_1 and V_2 by nodal analysis for the network in Fig.Q.1(c). **(08 Marks)**

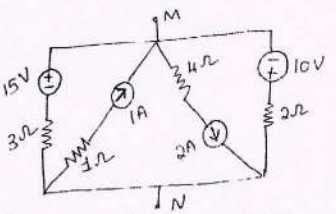
Fig.Q.1(c)



OR

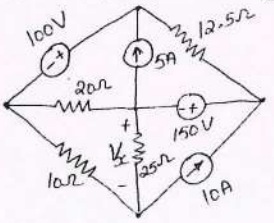
2 a. Find the potential difference between M and N using source transformation, for the network shown in Fig.Q.2(a). **(05 Marks)**

Fig.Q.2(a)



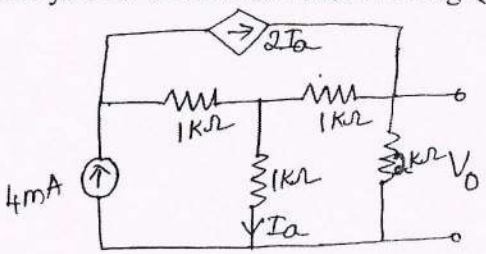
b. Find V_x using nodal analysis for the network shown in Fig.Q.2(b). **(08 Marks)**

Fig.Q.2(b)



c. Determine V_0 using mesh analysis for the network shown in Fig.Q.2(c). **(07 Marks)**

Fig.Q.2(c)

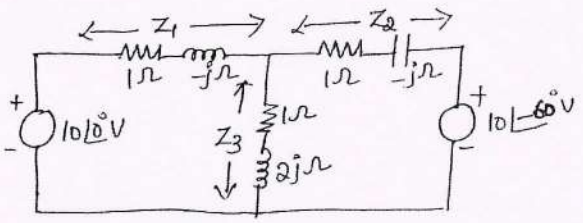


Module-2

3 a. State and prove Millman's theorem. **(06 Marks)**

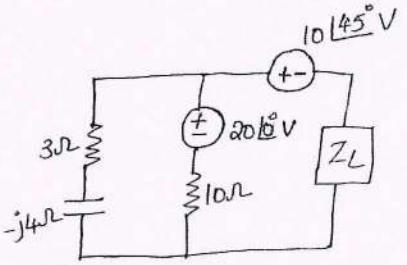
b. Find the current through Z_3 using superposition theorem for the network shown in Fig.Q.3(b). **(10 Marks)**

Fig.Q.3(b)



c. Find the value of Z_L for which maximum power transfer occurs in the network shown in Fig.Q.3(c). **(04 Marks)**

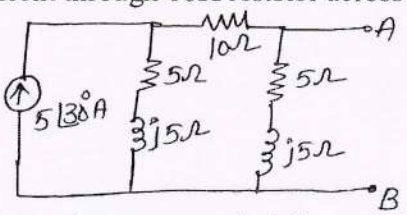
Fig.Q.3(c)



OR

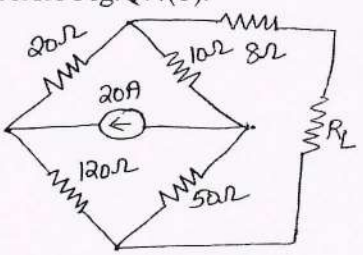
4 a. Obtain Thevenin's and Norton's equivalent circuit at terminals AB for the network shown in Fig.Q.4(a). Hence, find the current through 10Ω resistor across AB. **(12 Marks)**

Fig.Q.4(a)



b. Find the value of R_L for which maximum power is delivered. Also find the maximum power that is delivered to the load R_L. Refer Fig.Q.4(b). **(08 Marks)**

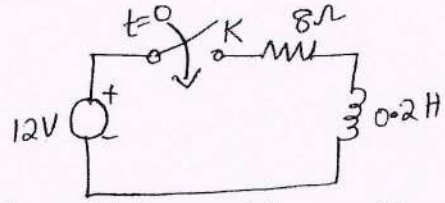
Fig.Q.4(b)



Module-3

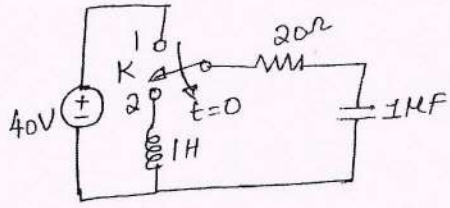
5 a. In the given network Fig.Q.5(a), K is closed at t = 0, with zero current in the inductor. Find the values of i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$. **(05 Marks)**

Fig.Q.5(a)



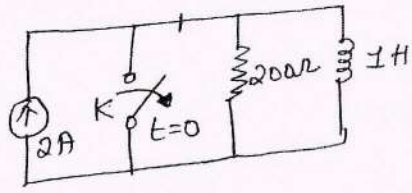
b. In the network Fig.Q.5(b), the switch is moved from position 1 to position 2 at t = 0. The steady-state has been reached before switching. Calculate i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$. **(07 Marks)**

Fig.Q.5(b)



c. In the network Fig.Q.5(c), the switch K is opened at t = 0. At $t = 0^+$, solve for v, $\frac{dv}{dt}$ and $\frac{d^2v}{dt^2}$. **(08 Marks)**

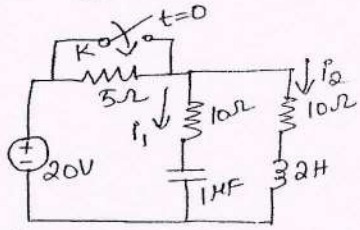
Fig.Q.5(c)



OR

6 a. For the circuit shown in Fig.Q.6(a), steady state is reached with switch K open. The switch is closed at t = 0. Find i_1, i_2, $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$ at $t = 0^+$. **(10 Marks)**

Fig.Q.6(a)



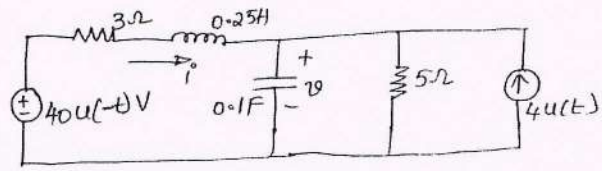
b. For the circuit in Fig.Q.6(b). Find:

i) $v(0^+)$ and $i(0^+)$

ii) $\frac{dv(0^+)}{dt}$ and $\frac{di(0^+)}{dt}$

iii) $v(\infty)$ and $i(\infty)$. **(10 Marks)**

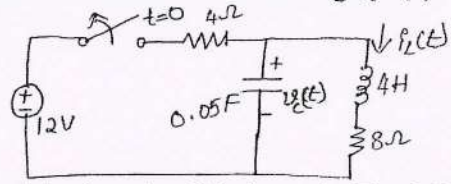
Fig.Q.6(b)



Module-4

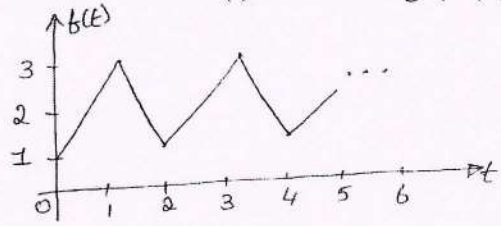
7 a. Determine the current $i_L(t)$ for $t \geq 0$ for the circuit in Fig.Q.7(a). **(10 Marks)**

Fig.Q.7(a)



b. Find the Laplace transform of the function f(t) shown in Fig.Q.7(b). **(10 Marks)**

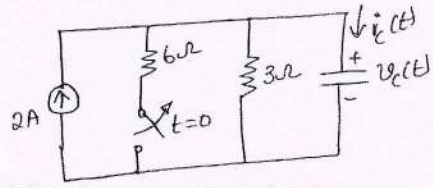
Fig.Q.7(b)



OR

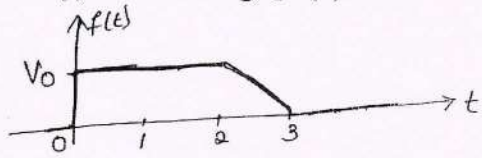
8 a. Determine the voltage $v_c(t)$ and the current $i_c(t)$ for $t \geq 0$ for the circuit shown in Fig.Q.8(a). **(10 Marks)**

Fig.Q.8(a)



b. Find the Laplace transform of f(t) shown in Fig.Q.8(b). **(10 Marks)**

Fig.Q.8(b)

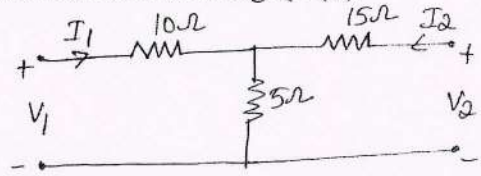


Module-5

9 a. Express Y parameters in terms of h-parameters. **(06 Marks)**

b. Find Z-parameters for the network shown in Fig.Q.9(b). **(06 Marks)**

Fig.Q.9(b)



c. The Z-parameters of a two port network are $z_{11} = 20\Omega$, $z_{22} = 30\Omega$, $z_{12} = z_{21} = 10\Omega$. Find Y and ABCD parameters of the network. **(08 Marks)**

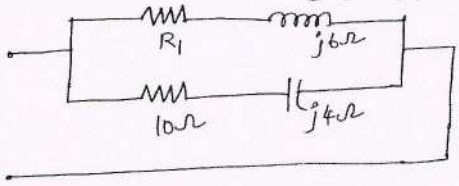
OR

10 a. Prove that the resonant frequency is the geometric mean of the two half power frequencies. **(06 Marks)**

b. A series RLC circuit has $R = 10\Omega$, $L = 0.01H$ and $C = 0.01\mu F$ and it is connected across 10mv supply. Calculate: i) f_0 ii) Q_0 iii) bandwidth iv) f_1 and f_2 v) I_0. **(06 Marks)**

c. Find the value of R_1 such that the circuit shown in Fig.Q.10(c) is resonant. **(08 Marks)**

Fig.Q.10(c)



* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the figures of the resulting orbitals when isolated atoms brought together and explain the characteristics. **(10 Marks)**

b. Obtain the relationship between mobility and hall coefficient in a p-type bar placed in a magnetic field in the Z-direction. **(10 Marks)**

OR

2 a. Derive the equation which relates current density and mobility in a semiconductor in an applied electric field. **(10 Marks)**

b. A silicon bar 2μm long and 200μm^2 in cross sectional area is doped with 1.5×10^{17}/cm^3 phosphorus. Find the current at 300K with 30V applied voltage. How long does it take an average electron to drift 2μm in pure silicon at an electric field of 80V/cm? Also calculate the time required at 10^5V/cm. Assume mobility of electrons is 0.1350m^2/Vsec. Also assume that saturation of electron drift velocity for silicon is 10^7 cm/s for the electric field above 10^5 V/cm. **(10 Marks)**

Module-2

3 a. Show the effect of bias at a pn junction on transition region width, electric field, electrostatic potential, energy band diagram partic flow and current direction under the following conditions:
i) Equilibrium ii) Forward bias iii) Reverse bias. **(10 Marks)**

b. Illustrate the care and issues to be considered in the design of solar cells. **(10 Marks)**

OR

4 a. Explain Avalanche break down and obtain equation for the electron multiplication factor. **(10 Marks)**

b. Derive the relationship between the open circuit voltage and optic generation rate starting from the expression for the optically generated illuminated pn junction. **(10 Marks)**

Module-3

5 a. Show the hole and electron flow in a pnp transistor with proper biasing. **(08 Marks)**

b. For the circuit shown in Fig.Q.5(b) calculate β, I_B and I_C. Given that τ_p =18μs, and τ_t = 0.2μs. What happens to the output current when I_B increases and β increases?

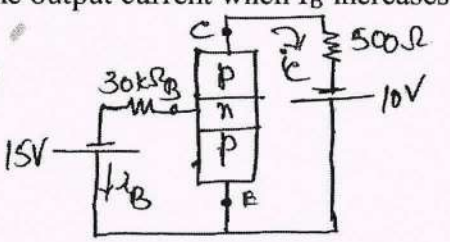


Fig.Q.5(b)

(06 Marks)

c. Explain the concept of base narrowing in a $p^+ - n - p^+$ transistor. **(06 Marks)**

OR

6 a. Obtain the Ebers-Moll equations and represent the same in the model form. **(12 Marks)**

b. Describe the switching effects in a CE transistor circuit. **(08 Marks)**

Module-4

7 a. Analyze the effect on gate-to-channel-space charge region and IV characteristics for the following conditions in a JFET:

i) Zero gate voltage of a small drain voltage

ii) Zero gate voltage of a large drain voltage

iii) Small V_{DS} value and small reverse-biased gate voltage. **(10 Marks)**

b. Draw the energy band diagram in an MOS capacitor structure for the following cases:

i) p-type substrate for a positive gate bias

ii) p-type substrate for a large positive gate bias

iii) n-type substrate for a positive gate bias. **(10 Marks)**

OR

8 a. Write the small signal equivalent circuit of a JFET, ideal low frequency small signal equivalent circuit and ideal equivalent circuit including r_s. **(10 Marks)**

b. Show the channel formation in the MOS structure and I_D versus V_{DS} curve for the following cases:

i) $V_{gs} > V_t$ and small V_{DS} value

ii) $V_{gs} > V_t$ and large V_{DS} value

iii) $V_{gs} > V_t$ and $V_{DS} = V_{DS}$ (sat) **(10 Marks)**

Module-5

9 a. What are the fabrication steps used in the fabrication of pn junctions? **(10 Marks)**

b. With figures, describe the complementary MOS structure. **(10 Marks)**

OR

10 a. Illustrate the evolution of integrated circuits. **(10 Marks)**

b. Explain the formation of resistors in integrated circuits. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Design a logic circuit that has 4 inputs, the output will be high, when the majority of the inputs are high. Use K-map to simplify. **(07 Marks)**

b. Express the following functions into canonical form:
(i) $f_1 = ab' + ab' + bc$ (ii) $f_2 = (a + b')(b' + c)$ **(06 Marks)**

c. Identify all the prime implicants and essential prime implicants of the following using K-map.
i) $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + dc(1, 4, 5, 11, 15)$
ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 9, 10) + dc(0, 14, 15)$
iii) $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ **(07 Marks)**

OR

2 a. Simplify the following using tabulation methods:
$Y = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$ **(07 Marks)**

b. Simplify the following expression using K-map. Implement the simplified expression using NAND gates only. $F = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$. **(07 Marks)**

c. Explain briefly K-map, incompletely specified functions, essential prime implicants and gray codes. **(06 Marks)**

Module-2

3 a. Design a two bit magnitude comparator. **(10 Marks)**

b. Realize the following functions expressed in maxterm canonical form in two possible ways using 3:8 decodes. $f_1(a, b, c) = \pi M(1, 2, 6, 7)$ and $f_2(a, b, c) = \pi M(1, 3, 6, 7)$ **(10 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$, using;
(i) 8:1 mux with a, b, c, as select lines (ii) 4:1 mux with a, b as select lines. **(08 Marks)**

b. Explain 4-bit carry look-ahead adder with necessary diagram and relevant expressions. **(04 Marks)**

c. Draw a PLA circuit to implement the logic function A′BC + AB′C + AC′ and A′B′C′ + BC. **(08 Marks)**

Module-3

5 a. Explain with timing diagrams the workings of SR latch as a switch debouncer. **(08 Marks)**

b. What is race around condition? Explain JK Master Slave flipflop with a diagram, function table and timing diagram. **(07 Marks)**

c. List the difference between combinational and sequential circuits. **(05 Marks)**

OR

6 a. Explain the operation of clocked SR flipflop using NAND gates. **(07 Marks)**

b. What is the significance of Edge Triggering? Explain the working of positive edge triggered D-FF with their function table. **(07 Marks)**

c. Explain the working of 4-bit twisted ring counter using necessary diagram and logic table. **(06 Marks)**

Module-4

7 a. Using positive edge triggering SR flipflops design a counter which counts in the following sequence: 000, 111, 110, 101, 100, 011, 010, 001, 000 … **(10 Marks)**

b. Design a synchronous mod-6 counter using D-flipflop to generate the sequence (0, 2, 3, 6, 5, 1, 0) **(10 Marks)**

OR

8 a. Write the difference between Mealy and Moore model with necessary diagrams. **(10 Marks)**

b. Explain state machine notations with an example. **(10 Marks)**

Module-5

9 a. Construct Mealy state diagram that will detect input sequence 10110, when input pattern is detected, Z is asserted high. Give state diagram for each state. **(10 Marks)**

b. With necessary diagram, explain the concept of serial adder with accumulators. **(10 Marks)**

OR

10 a. Design a sequential circuit to convert BCD to excess 3 code. **(10 Marks)**

b. Explain the design of sequential circuit using CPLD's and give CPLD implementation of a shift register and parallel adder with accumulator. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Power Electronics and Instrumentation

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Discuss various power converter circuits with necessary sketches and applications of each. **(07 Marks)**

b. With necessary sketches, explain the static V-I characteristics of SCR and its operation. **(08 Marks)**

c. List different turn-on methods, explain all in brief. **(05 Marks)**

OR

2 a. Explain turn-ON/turn-OFF dynamic characteristics of SCR with neat diagram. **(07 Marks)**

b. With suitable diagram and waveform, explain the working of RC full wave firing circuit. **(08 Marks)**

c. Describe the operation of UJT with neat sketches. **(05 Marks)**

Module-2

3 a. Explain the working of 1ϕ full wave center tapped controlled rectifier for resistive load with necessary sketches and also develop mathematical model to evaluate performance parameter of same (V_{dc}, V_{rms}, Efficiency). **(10 Marks)**

b. Evaluate performance parameter of 1ϕ half controlled rectifier with resistive load, has a transformer secondary voltage of 230V, 50Hz with R = 10Ω and firing angle α = 60°. Determine:

i) Average voltage and current
ii) Rms value of voltage and current
iii) Efficiency
iv) Ripple factor
v) Form factor. **(10 Marks)**

OR

4 a. Input to the step-up chopper is 200V the output required is 600V, if the conduction time of thyristor is 200μsec. Compute:

i) Chopping frequency
ii) If the pulse width is halved for constant frequency operation, find the new output voltage. **(07 Marks)**

b. Explain the operation step-up chopper with neat diagram and derive an expression for output voltage. **(08 Marks)**

c. Elaborate on the control techniques used in choppers and also give detailed classification of choppers. **(05 Marks)**

Module-3

5 a. With neat circuit diagram and waveforms. Explain the operation of 1ϕ full bridge inverter for RL load. **(07 Marks)**

b. Design a multi range ammeter with range 0-1A, 0-5A and 0-10A employing individual shunt in each a D'Arsonval movement with an internal resistance of 500Ω and full scale deflection of 10mA is available. **(08 Marks)**

c. What are the errors encountered in measurement process? Explain all with suitable example. **(05 Marks)**

OR

6 a. Design modified multirange voltmeter with basic D'Arsonval movement with an internal resistance of 50Ω and full scale deflection of 2mA, with voltage ranges of 0-10V, 0-50V, 0-100V and 0-250V. Draw the schematic diagram and show all values after design. **(07 Marks)**

b. Explain the various static characteristics of measuring instruments. **(08 Marks)**

c. With neat diagram, explain the operation of isolated flyback converter. **(05 Marks)**

Module-4

7 a. With neat block diagram, explain the operation of Ramp type Digital voltmeter. **(07 Marks)**

b. Explain the operation of Time measurement with neat block diagram. **(08 Marks)**

c. Draw the schematic diagram of Wheatstone's bridge and derive an expression for calculating unknown resistance and explain. **(05 Marks)**

OR

8 a. Explain the operation inductance comparision bridge with necessary equations. **(07 Marks)**

b. Discuss the operation of successive approximation type DVM with necessary diagram. **(08 Marks)**

c. An unbalanced Wheatstone bridge shown in Fig.Q.8(c), calculate the current through the galvanometer. **(05 Marks)**

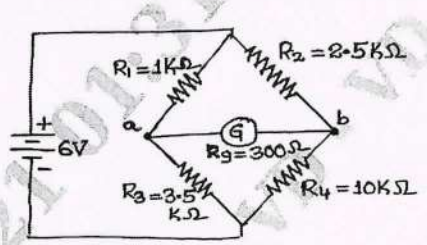


Fig.Q.8(c)

Module-5

9 a. Draw the schematic diagram to measure displacement using resistive transducer and explain. **(07 Marks)**

b. Explain the operation of PLC with neat block diagram. **(05 Marks)**

c. Explain the operation of Instrumentation amplifier using transducer bridge and derive equation for output voltage. **(08 Marks)**

OR

10 a. Explain the construction and working principle of LVDT with characteristic curve. **(07 Marks)**

b. What are factors to be considered for selecting the transducer? **(08 Marks)**

c. Illustrate working of analog weight scale. **(05 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is BJT transistor modeling? Obtain the expression for voltage gain, Z_{in} and Z_o of CB configuration using AC equivalent circuit with re model. **(05 Marks)**

b. Derive the expression for A_i, A_v, Z_i and Z_o for a voltage divider bias circuit of BJT, with unbypassed RE, using re equivalent model of BJT. Show the phase relationship between input and output wave form. **(10 Marks)**

c. State the characteristic features of Darlington connection. Calculate the DC bias voltages and currents in the circuit.

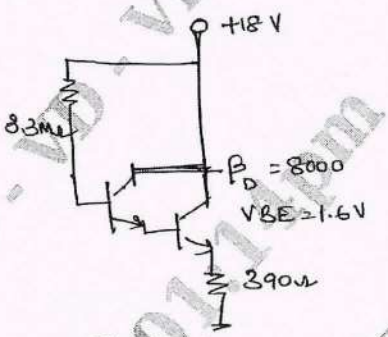


Fig.Q1(c) **(05 Marks)**

OR

2 a. Give the relation between re parameters and h parameters. What are the advantages of h parameters? **(05 Marks)**

b. Derive the expressions for current gain, voltage gain, input impedance and output impedance for an emitter follower circuit using approximate hybrid equivalent circuit. (Without the effect of r_o). **(10 Marks)**

c. For the network shown in Fig.Q2(c), determine re, Z_i, Z_o, A_v (with $r_o = \infty\Omega$) and A_v (with r_o = 50 KΩ)

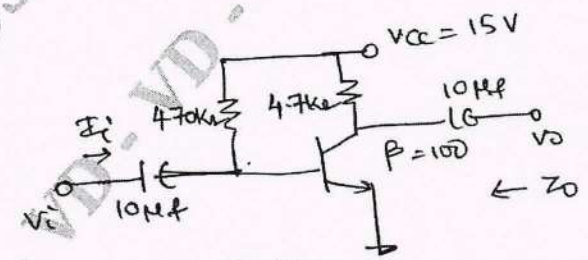


Fig.Q2(c) **(05 Marks)**

Module-2

3 a. Explain the construction of N channel JFET. Also explain the drain and transfer characteristics of the JFET. **(06 Marks)**

b. With equivalent circuit obtain the expression for Z_o and A_v for JFET self bias configuration. **(08 Marks)**

c. The fixed bias configuration shown in Fig.Q3(c) has $V_{GSQ} = -2V$, $I_{DQ} = 5.625$ mA with $I_{DSS} = 10$ mA, $V_P = -8V$ and $Y_{OS} = 40$ μS. Determine g_m, r_d, Z_o and A_v.

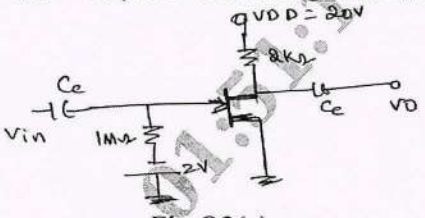


Fig.Q3(c) **(06 Marks)**

OR

4 a. Differentiate between enhancement and depletion MOSFET. **(05 Marks)**

b. With necessary equivalent circuit, obtain the expression for A_v for a JFET source follower configuration. **(05 Marks)**

c. Calculate the DC bias, voltage gain, input impedance and output impedance and resulting output voltage for the cascade amplifier shown in Fig.Q4(c). Calculate the load voltage if a 10 KΩ load is connected across the output.

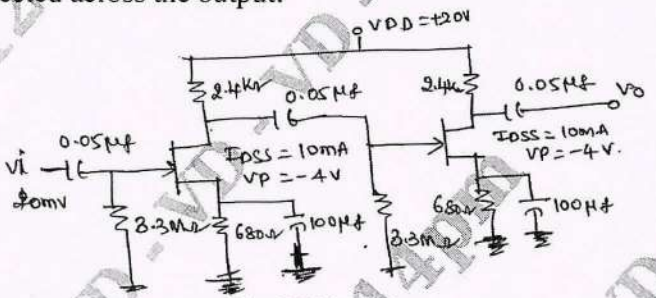


Fig.Q4(c) **(10 Marks)**

Module-3

5 a. Determine the lower cutoff frequency f_{LS} for the voltage divider bias network using the following parameters:
$C_S = 10$ μf, $C_E = 20$ μf, $C_C = 1$ μf, $R_S = 1$ KΩ, $R_1 = 40$ KΩ, $R_2 = 10$ KΩ, $R_E = 2$ KΩ, $R_C = 4$ KΩ, $R_L = 2.2$ KΩ, $\beta = 100$, $r_o = \infty\Omega$, $V_{CC} = 20$ V, re = 15.76 Ω. **(04 Marks)**

b. Explain the following: (i) Logarithm (ii) Decibel. With respect to transistor amplifier calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(06 Marks)**

c. Discuss the low frequency response of BJT amplifier and give expression for lower cut off frequency due to C_C, C_E and C_S. **(10 Marks)**

OR

6 a. Draw the Hybrid π model for the transistor in CE configuration and explain the significance of each component. **(06 Marks)**

b. Describe the Miller effect and derive an equation for Miller input capacitance. **(06 Marks)**

c. Determine the high cutoff frequencies for the network shown in Fig.Q6(c).

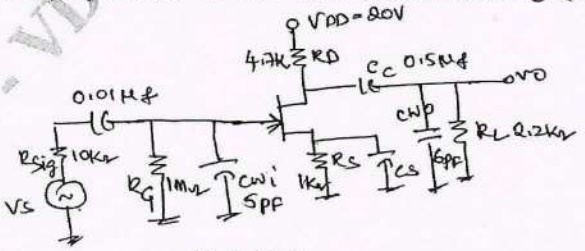


Fig.Q6(c) **(08 Marks)**

Module-4

7 a. With a block diagram, explain the concept of feedback amplifier and derive the expression for $A_f = \frac{A}{1+A\beta}$. **(06 Marks)**

b. Derive the expression for Z_{if} and Z_{of} for current series feedback amplifier. **(08 Marks)**

c. Explain a practical voltage series feedback circuit. **(06 Marks)**

OR

8 a. What is an oscillator? Discuss the concept of generating oscillations with the help of Barkhausen criteria. **(05 Marks)**

b. With a neat circuit diagram and necessary expressions, explain the Wein bridge oscillator. **(10 Marks)**

c. Design a unijuction transistor for a operation at 1 kHz and 150 kHz assuming $\eta = 0.58$. **(05 Marks)**

Module-5

9 a. Give the definition of power amplifiers and list the types of power amplifiers based on the location of Q point. **(05 Marks)**

b. Explain the working of class B complementary symmetry class B push pull amplifier. Obtain an expression for maximum conversion efficiency of this amplifier. **(10 Marks)**

c. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V and also calculate the total harmonic distortion for the amplitude components given above. **(05 Marks)**

OR

10 a. With necessary circuit diagram and characteristic curve, explain the class-A transformer coupled amplifier. Show that the maximum efficiency can be expressed as 50%. **(10 Marks)**

b. Describe the block diagram of series and shunt type voltage regulators. **(05 Marks)**

c. Calculate the output voltage and Zener current un the regulator circuit of Fig.Q10(c) for $R_L = 5\ K\Omega$.

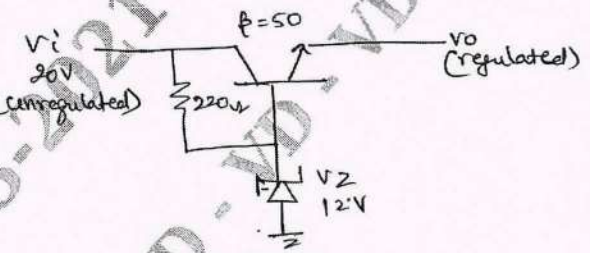


Fig.Q10(c) **(05 Marks)**

* * * * *

USN | | | | | | | | | | | 17EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Electronics

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define the following:
   i) Combinational circuit
   ii) Sequential circuit
   iii) Canonical SOP
   iv) Canonical POS
   v) Prime Implicant
   vi) Essential prime implicant. **(08 Marks)**

b. Express the following equations into decimal notations:
   i) $H = f(A, B, C) = A'BC + A'BC + ABC$
   ii) $T = f(a, b, c) = (a + b' + c)(a + b' + c')(a' + b' + c)$ **(08 Marks)**

c. Write mirror image version 5-variable K-map. **(04 Marks)**

OR

2 a. Obtain minimal expression using k-map for the following incompletely specified function $F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw circuit diagram using gates. **(10 Marks)**

b. Simplify the following using Quine-Mcclusky method
   $s = f(w, x, y, z) = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ **(10 Marks)**

Module-2

3 a. Explain the analysis and design procedure for combinational circuit with example. **(10 Marks)**

b. Implement full substractor using 3:8 decoder and write truth table. **(10 Marks)**

OR

4 a. Design full adder using i) 8:1 MUX ii) 4:1 MUX. **(10 Marks)**

b. Design 4 to 16 decoder using 3 to 8 decoder. **(05 Marks)**

c. Explain look ahead carry adder and give its advantages and disadvantages. **(05 Marks)**

Module-3

5 a. What is flipflop? Discuss working principle of SR flipflop with its TT and write characteristics equations. **(10 Marks)**

b. Sketch timing diagram for JK flipflop and D-flipflop. **(05 Marks)**

c. Explain the operation of a switch debouncer built using SR-latch with the help of waveforms. **(05 Marks)**

OR

6 a. Explain the working of a master-slave JK flip-flop with timing diagram. Show how race around condition is eliminated. **(10 Marks)**

b. Explain setup time, hold time and propagation delay for timing considerations. **(05 Marks)**

c. Write characteristics equation for D and T flip-flop. **(05 Marks)**

Module-4

7 a. Explain with diagram, operation and waveforms Serial In Serial Out (SISO) shift left mode register. **(10 Marks)**

b. Design BCD ripple counter using JK flip-flop. **(10 Marks)**

OR

8 a. Design an synchronous mod 5 counter using JK flip-flop and draw its timing diagram. **(10 Marks)**

b. Explain ring counter with timing sequence. **(05 Marks)**

c. Write a note on Johnson counter. **(05 Marks)**

Module-5

9 a. Draw and explain the block diagram of Moore and Mealy model with example and also compare both. **(10 Marks)**

b. Define, present state, next state, state diagram state table and state assignment. **(05 Marks)**

c. Draw and explain Moore JK-flipflop state diagram. **(05 Marks)**

OR

10 a. Analyze the synchronous sequential circuit show below in Fig.Q.10(a).

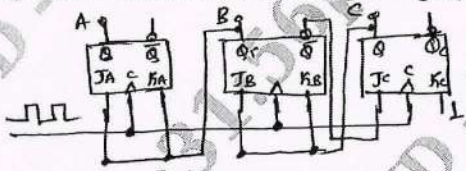


Fig.Q.10(a)

(12 Marks)

b. Design a synchronous counter using JK flipflops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define controlled source and mention its types. Also, mention its applications. **(05 Marks)**

b. Using source shift and source transformations, determine the voltage across the current source in Fig Q1(b).

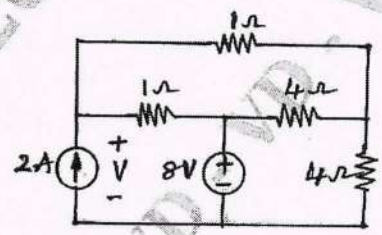


Fig Q1(b) **(05 Marks)**

c. For the circuit of Fig Q1(c), use nodal analysis to determine the voltage labeled V_x

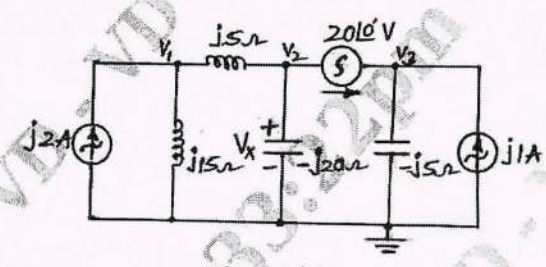


Fig Q1(c) **(10 Marks)**

OR

2 a. Define and explain supermesh. **(04 Marks)**

b. Use Star-Delta transformations to find the equivalent resistance at AB in Fig Q2(b).

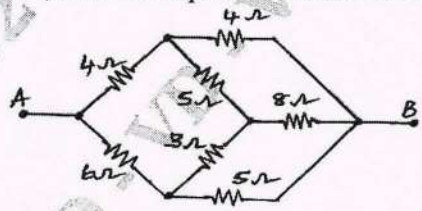


Fig Q2(b) **(06 Marks)**

c. Use Mesh analysis to determine V_1 and the power being supplied by the dependent current source in the circuit shown in Fig Q2(c).

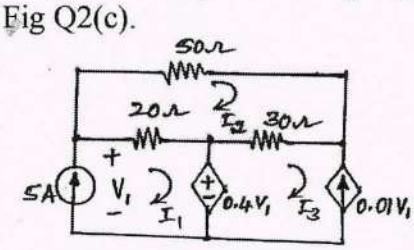


Fig Q2(c) **(10 Marks)**

Module-2

3 a. State and explain Millman's theorem for AC circuit. **(05 Marks)**

b. Use superposition on the circuit shown in Fig Q3(b) to find the current i_x.

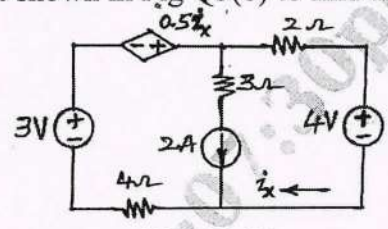


Fig Q3(b) **(05 Marks)**

c. Use Norton's theorem for the circuit of Fig Q3(c) to determine the power absorbed by the 20Ω resistor.

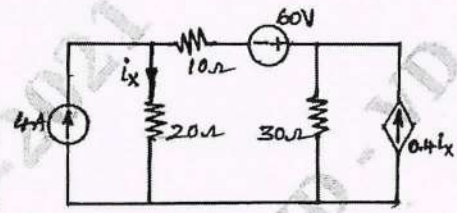


Fig Q3(c) **(10 Marks)**

OR

4 a. State and prove maximum power transfer theorem for AC voltage source with internal impedance connected to variable impedance. **(06 Marks)**

b. Verify reciprocity theorem for the circuit of Fig Q4(b).

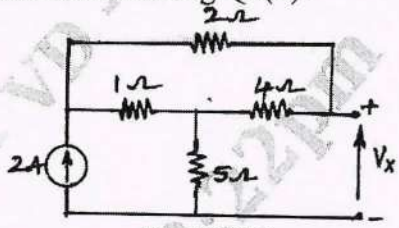


Fig Q4(b) **(04 Marks)**

c. For the circuit of Fig Q4(c), what value of R_L will absorb a maximum average power, and what is the value of this power?

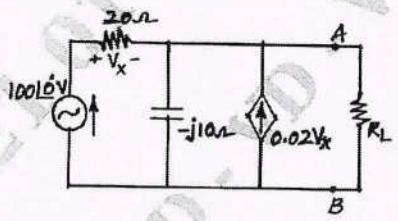


Fig Q4(c) **(10 Marks)**

Module-3

5 a. Explain the behavior of R, L and C elements for transients. Mention their representation at $t = 0^+$ **(06 Marks)**

b. In the network of the Fig Q5(b), is in the steady state with the switch K closed. At t = 0, the switch is opened. Find the values of v_1, v_2, $\frac{dv_1}{dt}$ and $\frac{dv_2}{dt}$ at $t = 0^+$.

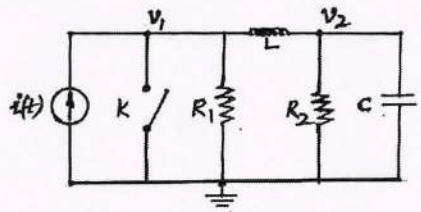


Fig Q5(b) **(08 Marks)**

c. Find the Laplace transform of the waveform shown in Fig Q5(c)

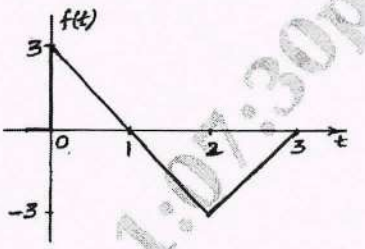


Fig Q5(c) **(06 Marks)**

OR

6 a. In the network of the Fig Q6(a), a steady state is reached with the switch K open. AT time $t = 0$, the switch is closed. Find the values of i_1, i_2, $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$ at $t = 0^+$.

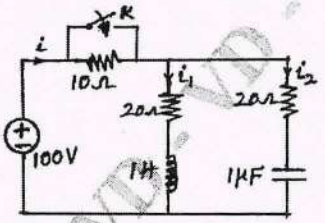


Fig Q6(a) **(10 Marks)**

b. In the network of the Fig Q6(b), the switch K is closed at t = 0 a steady state having previously excited. Draw the transform network and find the current i(t), using the Laplace transformation method.

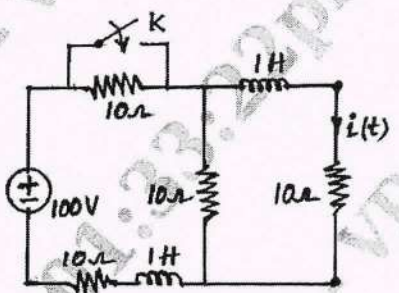


Fig Q6(b) **(10 Marks)**

Module-4

7 a. In a series resonant circuit, show that resonant frequency is equal to the geometric mean of half-power frequencies. **(06 Marks)**

b. An R-L-C series circuit of 8Ω resistance should be designed to have a bandwidth of 50Hz. Determine the values of L and C, so that the system resonates at 250Hz. Also determine the half power frequencies. **(06 Marks)**

c. For the network shown in Fig Q7(c), determine the value of C at which it resonates when f = 100Hz. Also find the values of R_L and R_C at which the circuit resonates at all frequencies.

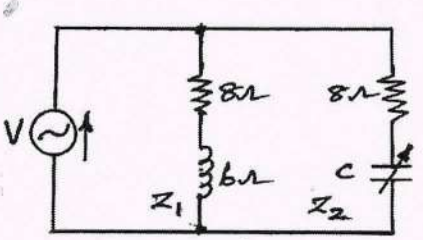


Fig Q7(c) **(08 Marks)**

OR

8 a. Define the following terms pertaining to a series R-L-C circuit, i) Resonance ii) Quality factor iii) Bandwidth iv) Selectivity. **(04 Marks)**

b. A series R-L-C circuit with an input voltage $5\angle 0°$ V resonates at a frequency of 8400Hz. The peak value of current is 500mA at resonance and the bandwidth is 120Hz. Determine the values of R, L, C and cut-off frequencies. **(06 Marks)**

c. For the network shown in Fig Q8(c), determine: i) Resonance frequency ii) Input admittance iii) Quality factor iv) Bandwidth and v) half power frequencies.

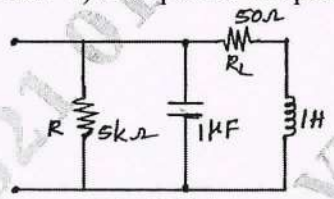


Fig Q8(c) **(10 Marks)**

Module-5

9 a. Obtain Y-parameters in terms of z-parameters. **(06 Marks)**

b. Find hybrid parameters for the two part shown in Fig Q9(b). What value of K in the two-part of figure shown will produce reciprocal network.

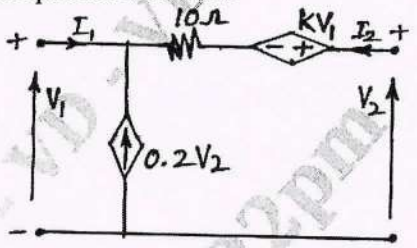


Fig Q9(b) **(06 Marks)**

c. Determine the ABCD parameters for the network of Fig Q9(c).

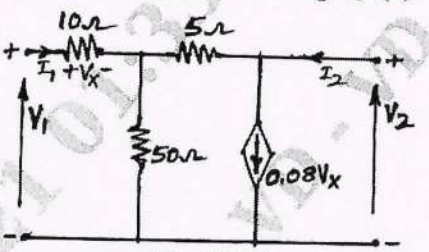


Fig Q9(c) **(08 Marks)**

OR

10 a. Explain h-parameters with equivalent circuit. Also obtain t-parameters in terms of h-parameters and hence show that AD – BC = 1. **(10 Marks)**

b. Find the Z-parameters and the Y-parameters for the network of Fig Q10(b)

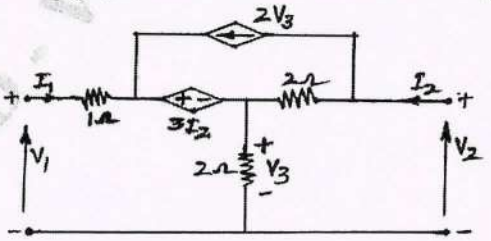


Fig Q10(b) **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Engineering Electromagnetics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. State and explain Coulomb's Law in vector form. **(04 Marks)**

b. Derive the expression for electric field intensity due to infinite line charge. **(08 Marks)**

c. Let a point charge $Q_1 = 25nc$ be located at A(4, –2, 7) and a charge $Q_2 = 60nc$ be at B(–3, 4, –2). Find $\vec{E}$ at C(1, 2, 3). Also find the direction of the electric field. Given $\in_0 = 8.854 \times 10^{-12} F/M$. **(08 Marks**

OR

2 a. Define electric field intensity and flux density also derive an expression for electric field intensity $\vec{E}$ at a point due to many charges. **(07 Marks)**

b. Point charges of 50nc each are located at A(1, 0, 0), B(–1, 0, 0), C(0, 1, 0) and D(0, –1, 0)m find the total force on the charge at A and also find $\vec{E}$ at A. **(08 Marks)**

c. A uniform line charge of infinite length with $P_L = 40nc/m$, lies along the Z-axis. Find $\vec{E}$ at (–2, 2, 8) in air. **(05 Marks)**

Module-2

3 a. State and prove Gauss Law for point charge. **(06 Marks)**

b. Define potential difference and absolute potential. **(04 Marks)**

c. In the given relation $D = 4xy\hat{a}_x + 2(x^2 + y^2)\hat{a}_y + 4yz\hat{a}_z \, c/m^2$. Evaluate both sides of the divergence theorem and find the charge enclosed within the rectangular parallelpiped $(0 \le x \le 2)$, $(0 \le y \le 3)$ and $(0 \le z \le 5)$m. **(10 Marks)**

OR

4 a. State and prove divergence theorem. **(04 Marks)**

b. Derive point form of continuity equation for current. **(08 Marks)**

c. A point charge of 6nc is located at origin in free space, find potential of point P, if P is located at (0.2, –0.4, 0.4) and

i) V = 0 at infinity

ii) V = 0 at (1, 0, 0)

iii) V = 20V at (–0.5, 1, –1). **(08 Marks)**

Module-3

5 a. State and prove uniqueness theorem. **(08 Marks)**

b. By applying Laplace equation find the expression for capacitance between the two concentric spheres. Make suitable assumptions. **(12 Marks)**

OR

6 a. Derive the expressions for Poisson's and Laplace's equation. **(04 Marks)**

b. State and explain Biot – Savart Law. **(06 Marks)**

c. Given the potential field $V = [Ar^4 + Br^{-4}]\sin 4\phi$:

i) Show that $\nabla^2 V = 0$

ii) Find A and B such that V = 10V and $\vec{E}$ = 500V/m at P(r = 1, ϕ = 22.5°, z = 2). **(10 Marks)**

Module-4

7 a. Derive an expression for magnetic forces on :

i) Moving point charge and

ii) Differential current element. **(10 Marks)**

b. Two differential current elements,

$I_1 \Delta \vec{L}_1 = 10^{-5}\,\hat{a}_2$ A.M at $P_1(1, 0, 0)$ and

$I_2 \Delta \vec{L}_2 = 10^{-5}(0.6\hat{a}_x - 2\hat{a}_y + 3\hat{a}_2)$ A.M at $P_2(-1, 0, 0)$

are located in free space. Find vector force exerted on $I_2 \Delta \vec{L}_2 = I_1 \Delta \vec{L}_1$. **(10 Marks)**

OR

8 a. Drive the magnetic boundary conditions at the interface between the two different magnetic materials. Discuss the conditions. **(10 Marks)**

b. A sq. loop carrying 2mA current is placed in the field of an infinite filament carrying current of 15Amp as shown in Fig.Q8(b). Find the force exerted on the sq loop.

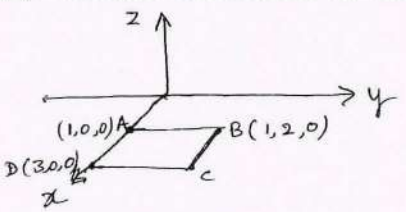


Fig.Q8(b). **(10 Marks)**

Module-5

9 a. Write a Maxwell's equations in point form and integral form. **(06 Marks)**

b. A uniform plane wave with an intensity of electric field equal to 1volt/m is travelling in free space. Find the magnitude of the associated magnetic field. **(04 Marks)**

c. State and explain pointing theorem. **(10 Marks**

OR

10 a. State and explain Faraday's Law of electromagnetic induction. **(04 Marks)**

b. Starting from Maxwell's equation obtain the general wave equations in electric magnetic fields. **(08 Marks)**

c. A UPW with 10MHz frequency has average pointing vector $1 W/m^2$ if the medium is perfect dielectric with $\mu_r = 2$, and $\epsilon_r = 3$, $\mu_0 = 4\pi \times 10^{-7}$H/m, $\epsilon_0 = 8.854 \times 10^{-12}$F/m ;

Find :

i) Velocity

ii) Wavelength

iii) Intrinsic impedance

iv) rms value of electric field. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC45

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define the following terms with respect to op-amp and mention their typical values
(i) CMRR (ii) PSRR (iii) Slew Rate (iv) I/P Offset voltages (v) Input bias current **(10 Marks)**

b. Sketch the circuit of an op-amp difference amplifier. Discuss the working common mode nulling capability with necessary circuit modifications and equations. **(10 Marks)**

OR

2 a. With a neat circuit diagram, explain the basic operational amplifier circuit. **(06 Marks)**

b. A non-inverting amplifier is to amplify a 100 mV signal to a level 5V. Using 741 op-amp design a suitable circuit. Also calculate the input and output impedances. **(08 Marks)**

c. With a neat circuit diagram, explain inverting summing amplifier and derive for output voltage and show how it can be converted into averaging circuit. **(06 Marks)**

Module-2

3 a. Sketch the circuit of a High Z_{in} capacitor Coupled Non-inverting amplifier and explain its working with necessary design steps. Show that the input impedance is very high compared to capacitor coupled Non-Inverting amplifier. **(10 Marks)**

b. Design a capacitor coupled Inverting amplifier using op-amp 741 to have a voltage gain of 50 and an output voltage of 2.5 V. The input signal frequency ranges from 10 Hz to 1 kHz with a load resistance of 250 Ω. **(06 Marks)**

c. What are the advantages of precision rectifiers over ordinary rectifiers? **(04 Marks)**

OR

4 a. Draw the circuit of an instrumentation amplifier and explain. Also show the method of nulling common mode outputs and how dc output voltage can be level shifted and list the features of instrumentation amplifier. **(10 Marks)**

b. With a neat sketch, explain the working of a precision voltage source with zener diode and op-amp. **(05 Marks)**

c. Explain how upper cutoff frequency can be set in Non-Inverting and Inverting capacitor coupled circuits. **(05 Marks)**

Module-3

5 a. Draw and explain an op-amp sample and hold circuit with necessary waveforms. **(08 Marks)**

b. Explain the working of Weinbridge oscillator using op-amp with a neat sketch of circuit, waveforms and equations. Design the same to get output frequency of 15 kHz with +/– 12 power supply using IC 741. **(08 Marks)**

c. With a neat circuit diagram, explain a multiplier using op-amp. **(04 Marks)**

OR

6 a. With a neat sketch, explain Inverting Schmitt trigger circuit with necessary waveforms and equations. Also design the same using IC741 op-amp to have UTP = 0V and LTP =– 2V with +/– 12V power supply. **(10 Marks)**

b. Sketch the circuit of fundamental log amplifier. Explain its working and derive for output voltage. What is the drawback of fundamental log amplifier and how it can be eliminated in temperature compensated log amplifier. **(10 Marks)**

Module-4

7 a. Sketch the circuit of second order active high pass filter using bipolor op-amp and explain its working. Design the same for a cutoff frequency of 7 kHz. **(08 Marks)**

b. Show how a bandpass filter can be constructed by the use of lowpass and high pass filters. Draw the circuit of a single stage band pass filter and explain the operation with necessary design equations. **(08 Marks)**

c. List the advantages of active filters over passive filters. **(04 Marks)**

OR

8 a. With a neat diagram, explain the operation of IC 723 as high voltage regulator. Design the same to have $V_0 = 12V$ and $I_0 = 2A$. **(08 Marks)**

b. Discuss the performance parameters of a three terminal IC regulator can be used as a current source. **(08 Marks)**

c. List the important characteristics of a three terminal IC regulator. **(04 Marks)**

Module-5

9 a. With a neat circuit diagram, explain the working of IC 566 voltage controlled oscillator with necessary waveforms. Also derive for output frequency. **(08 Marks)**

b. With a neat circuit diagram and waveforms explain the working of R-2R network D-A converter and derive the expression for output voltage. **(08 Marks)**

c. What is the output voltage produced by a DAC with output range of 0V to 10V for the given binary input number is (i) 0110 (for 4 bit DAC) (ii) 10111011 (for 8 bit DAC). **(04 Marks)**

OR

10 a. Draw the internal schematic of IC 555, configure it for astable operation and explain with necessary equations and waveforms. **(10 Marks)**

b. Explain the working of successive approximation Analog to Digital Converter (ADC). **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC46

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Microprocessors

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw and explain the internal architecture of 8086 microprocessor. **(10 Marks)**

b. Explain the concept of segmented memory. What are its advantages? **(06 Marks)**

c. If (CS) = 2000H, (DS) = 1234H, (SS) = 5678H, (BP) = 09ABH, calculate the physical address generated by the microprocessor when the following instruction is executed: MOV AL, [BP + 55H]. **(04 Marks)**

OR

2 a. With one example for each, describe any five addressing modes of 8086, used to access the data present in memory. **(10 Marks)**

b. List out any six conditional branch instruction that work based on the condition of any one flag. Mention the flag corresponding to each instruction. **(06 Marks)**

c. With numerical examples, illustrate the use of CBW and CWD instructions. **(04 Marks)**

Module-2

3 a. List out the five string manipulation instructions of 8086 and explain the operation of each. **(10 Marks)**

b. Write an Assembly Language Program (ALP) to add the data word located at address 2000H : 0500H to another data word available at offset 0600H in the same segment, and store the result and carry starting at 0700H in the same segment. **(06 Marks)**

c. With numerical examples, bring out the difference between SAR and SHR instructions. **(04 Marks)**

OR

4 a. Write an ALP using assembler directives to convert a 4-digit packed BCD number into equivalent 16-bit binary number, and store the result in memory. Write comments in your program. **(10 Marks)**

b. Explain the following instructions with one example each: RCR, XOR, SAHF. **(06 Marks)**

c. State the difference between the following two instructions: AND, TEST. What is the use of these instructions? **(04 Marks)**

Module-3

5 a. Explain the structure of stack in 8086 microprocessor. What is the role of stack during CALL and RET instructions? Illustrate with example. **(10 Marks)**

b. Explain any three methods of passing the parameters to and from a procedure. **(06 Marks)**

c. What is a macro? Give any two differences between macro and procedure. **(04 Marks)**

OR

6 a. Draw the interrupt vector table of 8086 and explain how an interrupt request is serviced, taking the example of type N interrupt. **(10 Marks)**

b. Write an ALP to generate a time delay of 10 seconds using an 8086 system that runs on 10MHz frequency. **(06 Marks)**

c. Bring out any four differences between maskable and non-maskable interrupts. **(04 Marks)**

Module-4

7 a. With a neat diagram, explain the maximum mode 8086 system. **(10 Marks)**

b. Write the functions of the following signals of 8086 : i) ALE ii) $\overline{DEN}$ iii) $\overline{BHE}$. **(06 Marks)**

c. Draw the minimum mode read cycle timing diagram, and explain briefly. **(04 Marks)**

OR

8 a. Design an interface between 8086 and two ICs of 32KB RAM and two ICs of 16KB EPROM. The RAM address must start at 00000H, and the EPROM address must end at FFFFFH. **(10 Marks)**

b. Draw the internal architecture of 8255 PIO and explain in brief. **(06 Marks)**

c. Explain Mode-1 and BSR modes of 8255. **(04 Marks)**

Module-5

9 a. Interface ADC 0808 with 8086 CPU using 8255 ports. Use port A for transferring digital data of ADC to CPU, and port C for control signals. Assume that analog input is present at input-3 of ADC. Draw the schematic and write the required ALP. **(10 Marks)**

b. Interface DAC0800 with 8086 CPU using port B of 8255. Write an ALP to generate a triangular waveform of frequency 400Hz. Assume that the system operates at 8MHz and the amplitude of the wave is 5V. **(10 Marks)**

OR

10 a. Write an ALP to read a 2-digit hexadecimal number from keyboard, and display its 4-digit square value on the computer screen, using appropriate DOS function calls. Use assembler directives and comments in your program. **(12 Marks)**

b. Write short notes on Von-Neumann architecture and Harvard architecture of computers with neat block diagrams. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. State the assumptions made.

Module-1

1 a. Define the following parameters with respect to op-amp.
i) Input offset current
ii) Input offset voltage
iii) CMRR
iv) PSRR **(08 Marks)**

b. Sketch an illustration to show the effect of op-amp slew rate and explain. **(04 Marks)**

c. If a Non-inverting amplifier is designed for a gain of 50, using op-amp with 90dB CMRR, calculate common mode output (V_{ocm}) for a common mode input (V_{icm}) of 100mV. **(04 Marks)**

OR

2 a. Design a direct-coupled non-inverting amplifier and explain its design steps. **(08 Marks)**

b. Two signals each ranging from 0.1V to 1V are to be summed. Using 741 op-amp design a suitable inverting summing circuit. **(04 Marks)**

c. Design a inverting amplifier using 741 op-amp with voltage gain of 50. The output voltage amplitude is 2.5V. **(04 Marks)**

Module-2

3 a. Draw the circuit to set the upper cut-off frequency using inverting amplifier and explain. **(08 Marks)**

b. A capacitor coupled non-inverting op-amp is to have gain of $A_v = 66$ and $V_i = 15mV$ with $R_L = 2.2K\Omega$ and $f_l = 120Hz$. Design the circuit. **(08 Marks)**

OR

4 a. Explain with a neat circuit design, precision full wave rectifier and also its design steps. **(08 Marks)**

b. Design a precision voltage source, with $V_o = 9V$ and supply voltage is $\pm 12V$. Allow 10% tolerance in zener diode [Assume 1N749 with $V_z = 4.3V$]. **(08 Marks)**

Module-3

5 a. Design a precision clipper to clip both ends, using dead zone circuit with relevant waveforms, explain the same. **(08 Marks)**

b. Design capacitor coupled zero-crossing detector with $f_l = 1kHz$ square wave input and $V_{o(p-p)} = 6V$. Use 741 op-amp with $\pm 12V$ supply [Assume $\Delta V = 1V$, $V_B = 0.1V$] **(08 Marks)**

OR

6 a. Define Barhausen's criteria. Explain with design, phase shift oscillator and with relevant waveforms. **(08 Marks)**

b. Show the realization of logarithmic amplifier using an op-amp. Obtain the expression for the output voltage. **(08 Marks)**

Module-4

7 a. Write a brief note on the following op-amp applications:
   i) First order low pass filter
   ii) Second order high pass filter. **(08 Marks)**

b. Design a single stage bandpass filter with frequency of $f_1 = 300Hz$ and $f_2 = 30kHz$. Also state whether the design is narrow band or wide band. Use 741 op-amp for designing. [Assume $c_2 = 1000pF$]. **(08 Marks)**

OR

8 a. Explain the working of a series regulator using op-amp. **(06 Marks)**

b. With a neat internal diagram of IC723. Explain the functions of each block. Mention the advantages. **(10 Marks)**

Module-5

9 a. Explain D to A converter using R-2R network. **(08 Marks)**

b. With a neat block diagram, explain the blocks of PLL. **(08 Marks)**

OR

10 a. Explain 555 timer as Monostable muiltivibrator with waveforms. **(08 Marks)**

b. Explain the working of A to D converter using successive approximation method. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC32

Third Semester B.E. Degree Examination, Jan./Feb.2021
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With necessary equivalent diagram obtain the expression for Z_{in}, A_V, Z_0 for Darlington Emitter follower. **(10 Marks)**

b. For an Emitter bias circuit (capacitor bypassed), determine r_e, Z_i, Z_O and A_V. Given $R_B = 470\ K\Omega$, $R_C = 2.2\ K\Omega$, $V_{CC} = 20\ V$, $R_E = 0.56\ K\Omega$, $C_E = 10\ \mu F$, $\beta = 120$, $r_0 = 40\ K\Omega$, $C_C = 10\ \mu F$. **(06 Marks)**

OR

2 a. Derive the expression for A_V, A_i, Z_i and Z_0 for C_E fixed bias configuration using complete hybrid equivalent model. **(10 Marks)**

b. Consider a single stage CE amplifier with $R_S = 1\ K$ and $R_L = 1.2\ K\Omega$. Calculate A_i, R_i, A_V, A_{is}, if $h_{ie} = 1.1\ K$, $h_{re} = 2.5\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\ \mu A/V$. **(06 Marks)**

Module-2

3 a. Derive the expression for transconductance g_m for FET. **(06 Marks)**

b. For the circuit shown in the Fig. Q3 (b), calculate (a) V_{GS} (b) I_{DQ} (c) V_{DSQ} (d) V_D. **(10 Marks)**

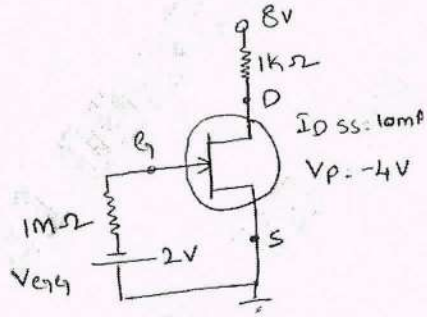


Fig. Q3 (b)

OR

4 a. With necessary equivalent circuit obtain the expression for A_V, Z_{in}, Z_O for a fixed biased JFET amplifier. **(08 Marks)**

b. Derive the expression for Z_i, Z_0, A_V considering common drain amplifier circuit. **(08 Marks)**

Module-3

5 a. Derive the expression for lower cut-of frequencies due to various RC networks in CE amplifiers. **(10 Marks)**

b. Determine the lower cut-off frequency for the emitter follower using BJT amplifier with $C_S = 0.1\ \mu F$, $R_S = 1\ K\Omega$, $R_1 = 12\ K\Omega$, $R_2 = 4\ K\Omega$, $R_E = 1.5\ K\Omega$, $C_C = 0.1\ \mu F$, $\beta = 100$, $r_0 = \infty$, $V_{CC} = 15\ V$, $V_{BE} = 0.7\ V$. **(06 Marks)**

OR

6 a. Describe Miller effect and derive an equation for Miller input and output capacitance. **(08 Marks)**

b. Calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

Module-4

7 a. Derive the expression for input resistance for a voltage of series and current series feedback. **(08 Marks)**

b. With a neat circuit diagram, explain FET based phase shift oscillator. **(08 Marks)**

OR

8 a. With the help of neat circuit diagram. Explain the operation of Colpitts and Hartley oscillator. Write the expression for the frequency of oscillation. **(12 Marks)**

b. In a transistor Colpitts oscillator $C_1 = 1$ nF, $C_2 = 100$ nF. Find the value of L for a frequency of 100 kHz. **(04 Marks)**

Module-5

9 a. Show that the transformer coupled class A power amplifier has maximum efficiency of 50%. **(08 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as,

$B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA

(i) Determine the percentage total harmonic distortion.

(ii) Assume a second identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion. **(08 Marks)**

OR

10 a. Explain with the block diagram, the basic types of voltage regulation circuit. **(08 Marks)**

b. Explain the operation of complementary symmetry class B amplifier. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC34

Third Semester B.E. Degree Examination, Jan./Feb.2021
Network Analysis

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define the terms with an example,
(i) Linear and non linear elements.
(ii) Lumped and distributed elements.
(iii) Unilateral and Bilateral elements.
(iv) Active and Passive elements. **(08 Marks)**

b. Find the current in 28 Ω resistor using mesh analysis in Fig. Q1 (b). **(08 Marks)**

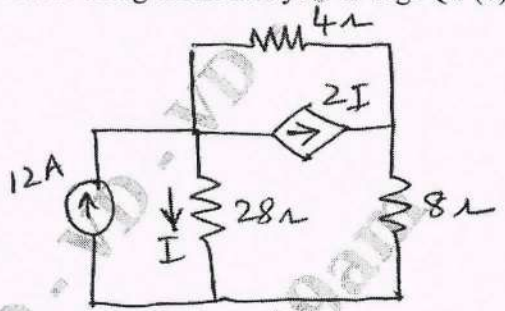


Fig. Q1 (b)

OR

2 a. Reduce the network in Fig. Q2 (a) to a single voltage source in series with a resistance using source shift and source transformation.

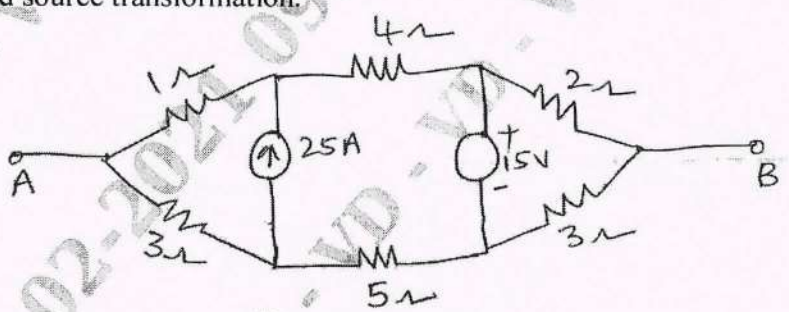


Fig. Q2 (a)

(08 Marks)

b. The node voltage equations of a network are,

$$\left[\frac{1}{5}+\frac{1}{j2}+\frac{1}{4}\right]V_1-\frac{1}{4}V_2=\frac{50\angle 0^0}{5}$$

and

$$-\frac{1}{4}V_1+\left[\frac{1}{4}+\frac{1}{-2j}+\frac{1}{2}\right]V_2=\frac{50\angle 90^0}{2}.$$

Derive the network. **(08 Marks)**

Module-2

3 a. State and prove superposition theorem. **(08 Marks)**

b. For the circuit shown in fig. Q3 (b), find the current through R_L using Thevenins theorem. **(08 Marks)**

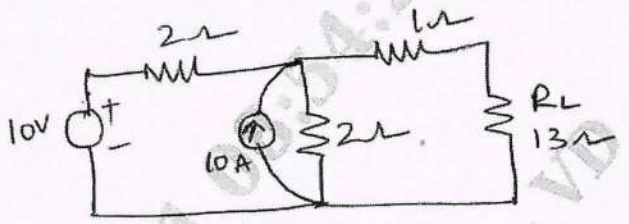


Fig. Q3 (b)

OR

4 a. State and prove Millers theorem. **(08 Marks)**

b. Find the value of Z_L for which power transferred to the load is maximum and also determine the maximum power for the circuit shown in Fig. Q4 (b). **(08 Marks)**

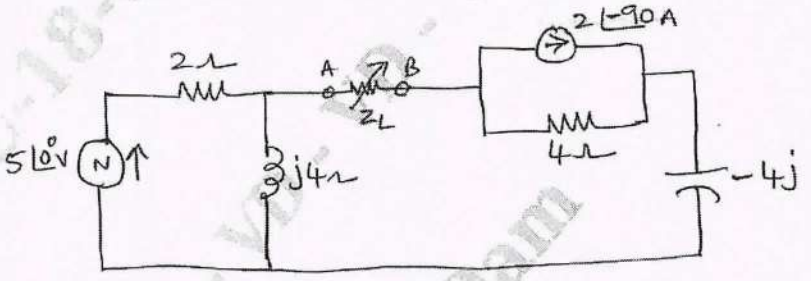


Fig. Q4 (b)

Module-3

5 a. In the circuit of Fig. Q5 (a). Switch K is opened at t = 0. Find the value of V, $\frac{dV}{dt}$ and $\frac{d^2V}{dt^2}$ at $t = 0^+$. **(08 Marks)**

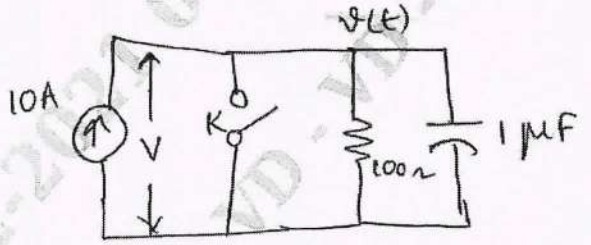


Fig. Q5 (a)

b. Obtain the Laplace transform of the square wave shown in Fig. Q5 (b). **(08 Marks)**

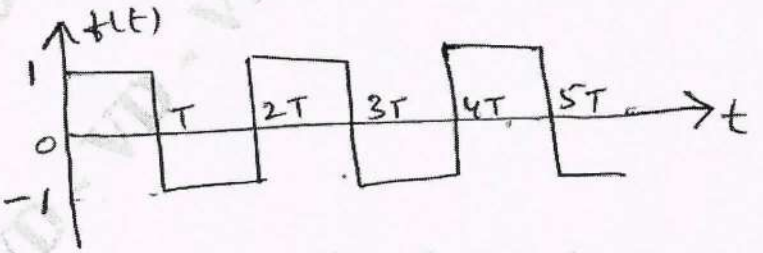


Fig. Q5 (b)

OR

6 a. State and prove initial value and final value theorem. **(08 Marks)**

b. For the network shown in Fig. Q6 (b) the switch is moved from position 1 to position 2 at $t = 0$ the steady state has been reached before switching. Calculate $i, \frac{di}{dt}, \frac{d^2i}{dt^2}$ at $t = 0^+$. **(08 Marks)**

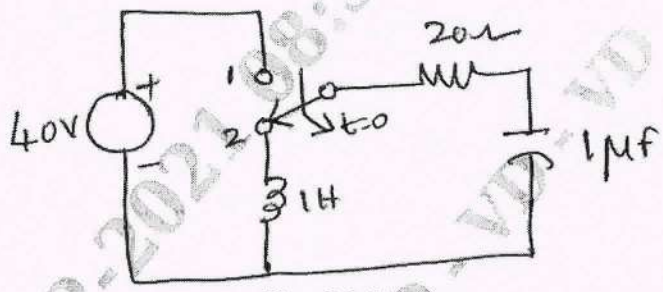


Fig. Q6 (b)

Module-4

7 a. Define the following terms :
(i) Resonance
(ii) Q-factor
(iii) Bandwidth
(iv) Selectivity. **(04 Marks)**

b. Derive an expression for frequency of resonance of a parallel resonant circuit containing resistance in both the branches. **(06 Marks)**

c. It is required that a series RLC circuit should resonate at 500 kHz. Determine the values of R, L and C if the bandwidth of the circuit is 10 kHz and its impedence is 100 Ω at resonance. Also find the voltages across L and C at resonance if the applied voltage is 75 volts. **(06 Marks)**

OR

8 a. Show that a two branch parallel resonant circuit is resonant at all the frequencies if $R_L = R_C = \sqrt{\frac{L}{C}}$ where R_L = Resistance in the inductor branch, R_C = Resistance in the capacitor branch. **(06 Marks)**

b. Give the comparison between series and parallel resonance. **(04 Marks)**

c. Find the value of R_1 such that the circuit given in Fig. Q8 (c) is resonant. **(06 Marks)**

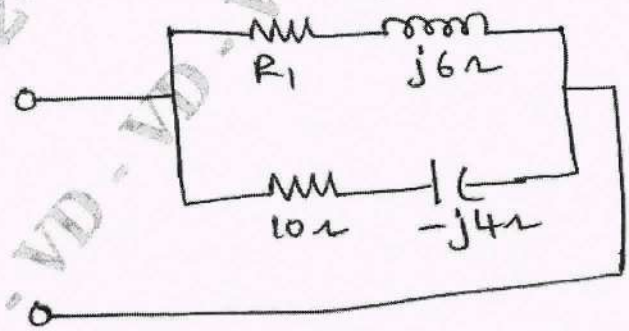


Fig. Q8 (c)

Module-5

9 a. Express Y parameters in terms of Z and T parameters. **(08 Marks)**

b. Find the transmission parameters for the network shown in Fig. Q9 (b). **(08 Marks)**

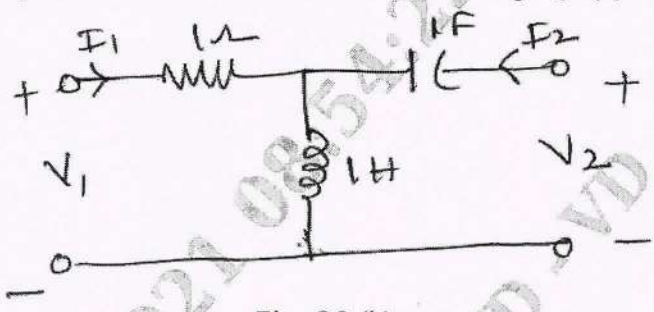


Fig. Q9 (b)

OR

10 a. Express ABCD parameters in terms of Y and h parameters. **(08 Marks)**

b. Find the h parameters of the network shown in Fig. Q10 (b). **(08 Marks)**

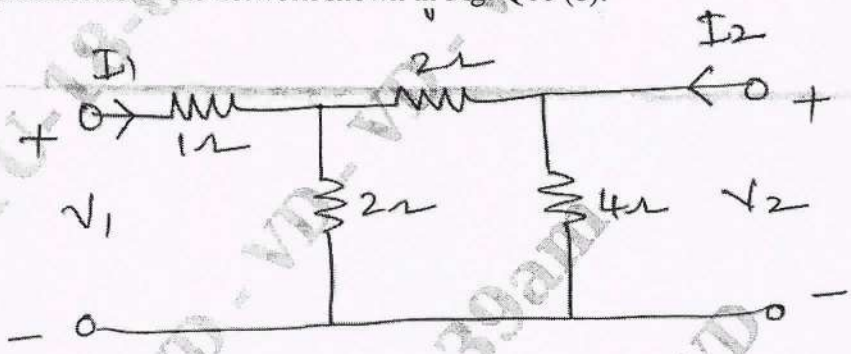


Fig. Q10 (b)

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Engineering Electromagnetics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. A charge $Q_A = -20\ \mu C$ is located at A(−6, 4, 7) and a charge $Q_B = 50\ \mu C$ is located at B(5, 8, −2) in free space. If distances are given in meters, find the vector force exerted on Q_A by Q_B. **(06 Marks)**

b. A charge of −0.3 μC is located at A(25, −30, 15) (in cm) and a second charge of 0.5 μC is located at B(−10, 8, 12) cm. Find Electric field intensity (E) at
(i) the origin (ii) P(15, 20, 50,)cm. **(08 Marks)**

c. Define electric flux density. **(02 Marks)**

OR

2 a. Calculate the total charge within the universe of $\rho_v = \frac{e^{-2r}}{r^2}$. **(04 Marks)**

b. Infinite uniform line charges of 5 nC/m lie along the (positive and negative) x and y axes in free space. Find Electric field intensity (E) at $P_A(0, 0, 4)$ **(04 Marks)**

c. Calculate Electric flux Density (D) in rectangular coordinates at point P(2, −3, 6) produced by
(i) a point charge QA = 55 mC at Q(−2, 3, −6);
(ii) a uniform line charge $\rho_{LB} = 20$ mC/m on the x-axis. **(08 Marks)**

Module-2

3 a. State and explain Gauss law in electrostatics. **(04 Marks)**

b. Derive the expression for electric field intensity due to an infinite line charge using Gauss law. **(04 Marks)**

c. In the region of free space that includes the volume $2 < x, y, z < 3$, $D = \frac{2}{z^2}(yza_x + xza_y - 2xya_z)\ c/m^2$.
(i) Evaluate the volume integral side of the divergence theorem for the volume defines here.
(ii) Evaluate surface integral side for the corresponding closed surface. **(08 Marks)**

OR

4 a. Derive an expression for continuity equation in point form. **(04 Marks)**

b. If $\hat{E} = 120\ a_\rho$ V/m, find the incremental amount of work done in moving a 50 μC charge a distance of 2 mm from (i) P(1, 2, 3) toward Q(2, 1, 4) (ii) Q(2, 1, 4) toward P(1, 2, 3). **(05 Marks)**

c. Current density is given in cylindrical coordinates as $J = -10^6\ z^{1.5}a^z\ A/m^2$ in the region $0 \le \rho \le 20\ \mu m$; for $\rho \ge 20\ \mu m$ J = 0.
(i) Find the total current crossing the surface z = 0.1 m in the a_z direction.
(ii) If the charge velocity is 2×10^6 m/s at z = 0.1m, find ρ_v (volume charge density). **(07 Marks)**

Module-3

5 a. Starting from Gauss law, derive Poisson's and Laplace's equation. **(04 Marks)**

b. Calculate numerical value for potential V and volume charge density ρ_v at $P\left(3,\frac{\pi}{3},2\right)$ if $V = 5\rho^2 \cos 2\phi$. **(06 Marks)**

c. Given the spherically symmetric potential field in free space, $V = V_0 e^{-r/a}$, find:
(i) ρ_v at r = a (ii) the electric field at r = a (iii) total charge. **(06 Marks)**

OR

6 a. State and explain Ampere's law. **(04 Marks)**

b. Evaluate both sides of Stoke's theorem for the field $H = 10 \sin\theta\, a_\phi$ and the surface r = 3, $0 \le \theta \le 90°$, $0 \le \phi \le 90°$. Let the surface have the a_r direction. **(06 Marks)**

c. Using the concept of vector magnetic potential, find the magnetic flux density at a point due to long straight filamentary conductor carrying current 'I' in the a_z direction. **(06 Marks)**

Module-4

7 a. Derive an expression for the force on a differential current element placed in a magnetic field. **(04 Marks)**

b. A point charge for which $Q = 2 \times 10^{-16}$ C and $m = 5 \times 10^{-26}$ kg is moving in the combined fields $E = 100\, a_x - 200\, a_y + 300\, a_z$ V/m and $B = -3a_x + 2a_y - a_z$ mT. If the charge velocity at t = 0 is V(0). $V(0) = (2a_x - 3a_y - 4a_z)10^5$ m/s.
(i) Give the unit vector showing the direction in which the charge is accelerating at t = 0.
(ii) Find the kinetic energy of the charge at t = 0. **(06 Marks)**

c. A rectangular loop of wire in free space joins points A(1, 0, 1) to B(3, 0, 1) to C(3, 0, 4) to D(1, 0, 4) to A. The wire carries a current of 6 mA, flowing in the a_z direction from B to C. A filamentary current of 15A flows along entire z axis in the a_z direction.
(i) Find 'F' on side BC (ii) Find 'F' on side AB (iii) Find F_{total} on the loop. **(06 Marks)**

OR

8 a. Given a material for which $x_m = 3.1$ and within which $B = 0.4ya_zT$, find:
(i) H (ii) μ (iii) μ_r (iv) M (v) J **(04 Marks)**

b. Let $\mu_{r_1} = 2$ in region 1 defined by $2x + 3y - 4z > 1$ while $\mu_{r_2} = 5$ in region 2 where $2x + 3y - 4z < 1$. In region 1, $H_1 = 50a_x - 30a_y + 20a_z$ A/m. Find:
(i) H_{N_1} (ii) H_{t_1} (iii) H_{t_2} (iv) H_{N_2} (v) θ_1 the angle between H_1 and a_{N21} **(08 Marks)**

c. Obtain an expression for the total energy stored in a steady magnetic filed in which 'B' is linearly related to 'H'. **(04 Marks)**

Module-5

9 a. Write Maxwell's equations in integral and point forms. **(06 Marks)**

b. Using Faraday's law, deduce Maxwell's equation, to relate time varying electric and magnetic fields. **(06 Marks)**

c. Explain the displacement current and displacement current density. **(04 Marks)**

OR

10 a. Derive wave equations for uniform plane wave in free space. **(06 Marks)**

b. Derive an expression for propagation constant intrinsic impedance and phase velocity for a uniform plane wave propagating in a conducting media. **(06 Marks)**

c. In free space $E(x,t) = 50\cos(\omega t - \beta x)a_y$ V/m. find the average power crossing a circular area of radius 5m in the plane x = constant. **(04 Marks)**

Module-3

5 a. The LTI systems are connected as shown in Fig.Q.5(a). If $h_1(n) = u(n-2)$, $h_2(n) = nu(n)$ and $h_3(n) = \delta(n-2)$. Find the overall response. **(10 Marks)**

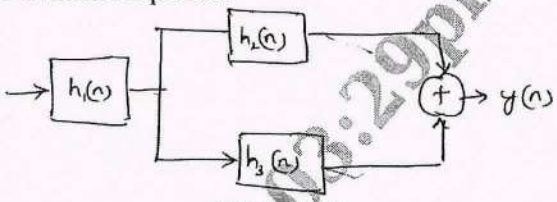


Fig.Q.5(a)

b. Evaluate the DTFS representation for the signal

$$x(n) = \sin\left(\frac{4\pi}{21}n\right) + \cos\left(\frac{10\pi}{21}n\right) + 1$$

Sketch the magnitude and phase spectra. **(10 Marks)**

OR

6 a. State and explain following continuous time Fourier series properties:
i) Time shift ii) Convolution iii) Parseval's Theorem. **(06 Marks)**

b. Check whether the system whose impulse response is
i) $h(n) = (1/2)^n u(-n)$ ii) $h(t) = e^{2t} u(t-1)$ stable, causal and memory less. **(09 Marks)**

c. Evaluate the step response for the LTI system represented by the following impulse response. $h(t) = t^2 u(t)$. **(05 Marks)**

Module-4

7 a. State the following properties of DTFT: i) Linearity ii) Frequency shift iii) Frequency differentiation iv) Modulation v) Convolution. **(10 Marks)**

b. Obtain the FT of the signal $x(t) = e^{-at} u(t)$; $a > 0$. **(10 Marks)**

OR

8 a. Find DTFT of the signal $x(n) = \{1, 3, \underset{\uparrow}{5}, 3, 1\}$ and evaluate $X(e^{j\Omega})$ at $\Omega = 0$ **(06 Marks)**

b. With neat diagrams, state and explain sampling theorem. **(08 Marks)**

c. Determine the Nyquist sampling rate and Nyquist sampling interval for
i) $x_1(t) = \text{Cos}(5\pi t) + 0.5\cos(10\pi t)$ ii) $x_2(t) = \text{Sinc}^2(200t)$ **(06 Marks)**

Module-5

9 a. Define Z-transform. Mention the properties of Region of Convergence (ROC). **(06 Marks)**

b. Determine the Z transform of these signals

i) $x_1(n) = n\left(\frac{5}{8}\right)^n u(n)$ ii) $x_2(n) = (0.9)^n u(n) * (0.6)^n u(n)$ **(08 Marks)**

c. Find Inverse Z transform, if $X(z) = \dfrac{\left(1/4\right)z^{-1}}{\left(1 - 1/2\, z^{-1}\right)\left(1 - 1/4\, z^{-1}\right)}$ for all possible ROCs. **(06 Marks)**

OR

10 a. Prove the following properties of Z-transform: i) Linearity ii) Time Reversal. **(08 Marks)**

b. A system has impulse response $h(n) = \left(1/2\right)^n u(n)$. Determine the input to the system if the output is given by $y(n) = \frac{1}{3}u(n) + \frac{2}{3}\left(-\frac{1}{2}\right)^n u(n)$. **(12 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC42

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Signals and Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define a signal. List the elementary signals. Differentiate between even and odd signals, energy and power signals. **(08 Marks)**

b. Sketch the signal $x(t) = r(t+1) - r(t) + r(t-1)$. **(04 Marks)**

c. Check whether the following signals are periodic or not. If periodic, determine the fundamental period:

i) $x(n) = \cos\left(\frac{\pi n}{2}\right) + \sin\left(\frac{\pi n}{4}\right)$ ii) $x(t) = \cos(2\pi t)\ \sin\ 4\pi t$ **(08 Marks)**

OR

2 a. Determine and sketch the even and odd components of the signal x(t) shown in Fig.Q.2(a). **(08 Marks)**

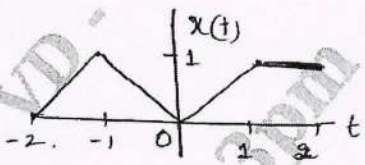


Fig.Q.2(a)

b. Find and sketch the derivatives of the following signals: $x(t) = u(t) - u(t-a)$, $a > 0$. **(04 Marks)**

c. Check whether the following system is
i) Static or dynamic
ii) Linear or nonlinear
iii) Time invariant or time variant
iv) Causal or non causal
v) Stable or unstable
vi) Invertible or non invertible. $y(n) = \log[x(n)]$. **(08 Marks)**

Module-2

3 a. Derive the expression for convolution integral. **(07 Marks)**

b. Prove the following: i) $x(n) * \delta(n) = x(n)$ ii) $x(n) * u(n) = \sum_{k=-\infty}^{n} x(k)$ **(06 Marks)**

c. Consider a LTI system with unit impulse response $h(t) = e^{-t}u(t)$. If the input applied to this system is $x(t) = e^{-3t}(u(t) - u(t-2))$. Find the output y(t) of the system. **(07 Marks)**

OR

4 a. State and prove commutative and distributive properties of convolution integral. **(08 Marks)**

b. The impulse response of LTI system is $h(n) = \{1, \underset{\uparrow}{2}\}$. Determine the response of the system to input signal $x(n) = \{1, \underset{\uparrow}{3}, 1\}$ using graphical method. **(06 Marks)**

c. Find the discrete time convolution sum given below:
$y(n) = \beta^n u(n) * \alpha^n u(n),\ |B| < 1,\ |\alpha| < 1$ **(06 Marks)**

CBCS SCHEME

USN | | | | | | | | | | |

17EC43

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Control Systems

Time: 3 hrs. Max. Marks: 100

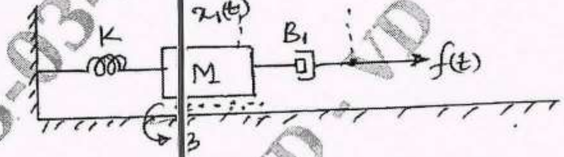
Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Differentiate between Open loop control system and Closed loop control system. **(06 Marks)**

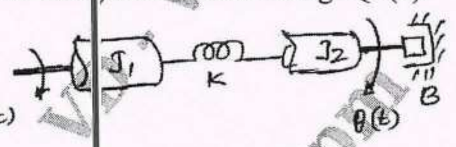
b. For the mechanical system, shown in fig. Q1(b), write the i) Mechanical network ; ii) Differential equations of performance. **(06 Marks)**

Fig.Q1(b)



c. Obtain the transfer function of the system shown in fig. Q1(c).

Fig.Q1(c)



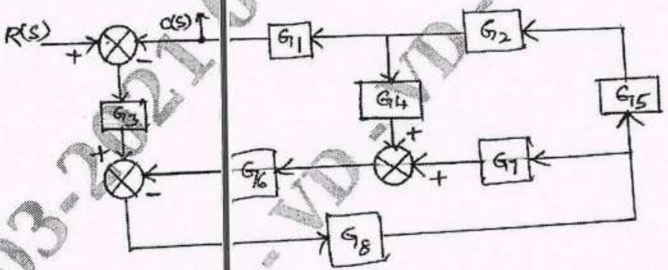
(08 Marks)

OR

2 a. Explain the block diagram rule regarding : i) Combining blocks in cascade ii) Moving a take off point beyond a block. **(04 Marks)**

b. Determine the transfer function C(s)/R(s) for the block diagram shown in fig. Q2(b), using block diagram reduction techniques.

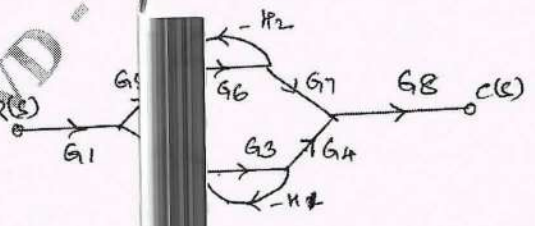
Fig.Q2(b)



(08 Marks)

c. Find $\frac{C(s)}{R(s)}$ for the following signal flow graph of fig. Q2(c).

Fig.Q2(c)



(08 Marks)

Module-2

3 a. With usual notation, derive an expression for the Peak time (t_p) and Rise time (t_r) of a response of second order system to a unit step input. **(06 Marks)**

b. Explain PI and PID controllers of a control system. **(06 Marks)**

c. A second order control system is represented by a transfer function given below :

$\frac{Q(s)}{T(s)} = \frac{1}{Js^2 + Bs + K}$, where Q(s) is the proportional output and T(s) is the input torque. A step unit of 10N-mt is applied to the system and test results are given below :

i) Maximum overshoot is 6% ii) Peak time is 1 sec iii) Steady static value of the output is 0.5 radian. Determine the values of J , F and K. **(08 Marks)**

OR

4 a. Define Steady state error and Static error coefficients with respect to step input, velocity input and acceleration inputs. **(06 Marks)**

b. For a unity feedback system $G(s) = \frac{s(s+1)}{s^2(s+3)(s+10)}$. Determine the type of system, error coefficients and steady state error for input $r(t) = 1 + 3t$. **(06 Marks)**

c. A signal is represented by the equation $\frac{d^2\theta}{dt^2} + 10.\frac{d\theta}{dt} = 150.e$. Where $e = (r-\theta)$ is the actuating signal. Calculate the value of damping ratio, undamped and damped frequency of oscillation. Also determine Open loop transfer function. **(08 Marks)**

Module-3

5 a. State R – H criterion and discuss its limitation. **(06 Marks)**

b. State the different rules for the construction Root locus. **(06 Marks)**

c. The open loop transfer function of a unity feedback system is given by

$G(s) = \frac{K}{s(s+3)(s^2+s+1)}$. Determine the value of K that will cause sustained oscillations in the closed loop system. Also find the frequency of sustained oscillations. **(08 Marks)**

OR

6 a. A unity feedback control system has $G(s) = \frac{K}{\quad}$ Sketch the root locus and show

OR

8 a. Explain Lag – lead compensating networks. **(06 Marks)**

b. Given $G(s)H(s) = \frac{12}{s[s+1][s+2]}$. Draw the Polar plot and hence determine if system is stable? **(06 Marks)**

c. The open loop transfer function of a control system is $G(s)H(s) = \frac{1}{s^2(s+2)}$. Sketch the Nyquist plot, Path and asertain the stability. **(08 Marks)**

Module-5

9 a. What is Signal Reconstruction? Explain it with SAMPLE and HOLD circuit. **(06 Marks)**

b. Find the State – transition Matrix for $A = \begin{bmatrix} 0 & -1 \\ +2 & -3 \end{bmatrix}$. **(06 Marks)**

c. Consider the system given by $\dddot{y} + 9\ddot{y} + 26\dot{y} + 24y = 6U$. Obtain its state model. **(08 Marks)**

OR

10 a. List the properties of State transition matrix. **(06 Marks)**

b. Explain Spectrum analysis of Sampling process. **(06 Marks)**

c. Obtain the transition matrix Q(t) of the following system

$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$. Also obtain the inverse of the transition matrix $\phi^i(t)$. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC44

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Illustrate the amplitude modulation process. What is envelope distortion? **(10 Marks)**

b. With the aid of neat block diagram, describe coherent detection of DSB-SC modulated wave. What is quadrature null effect? **(07 Marks)**

c. A single of 5KHz frequency signal is modulated on a carrier wave of a frequency 2 MHz. What are the frequencies of the resultant signal? **(03 Marks)**

OR

2 a. Describe ring modulator. Why the ring modulator is referred as a double balanced modulator? **(10 Marks)**

b. Describe quadrature carrier multiplexing. **(06 Marks)**

c. What are the factors influencing the choice of VSB modulation for the transmission of analog TV signals? **(04 Marks)**

Module-2

3 a. Derive an expression for FM signal. **(08 Marks)**

b. With the aid of neat block diagram, explain AM super heterodyne receiver. **(08 Marks)**

c. The resulting FM signal is 10 $\cos[(2\pi\ 10^5 t) + 15 \sin(2\pi\ 100t)]$. Find the approximate bandwidth of the FM signal. **(04 Marks)**

OR

4 a. Describe the PLL working. **(08 Marks)**

b. With the aid of neat circuit diagram balanced frequency discriminator. **(08 Marks)**

c. What are the RF frequency range and intermediate frequency for AM and FM ratio? **(04 Marks)**

Module-3

5 a. Define Mean, correlation and covariance Functions of a random process x(t). **(08 Marks)**

b. Discuss Gaussian process and its properties. **(08 Marks)**

c. Draw the characteristics of white noise. **(04 Marks)**

OR

6 a. Write the important properties of autocorrelation function. **(08 Marks)**

b. Discuss shot noise, and thermal noise. **(08 Marks)**

c. Define noise equivalent bandwidth. **(04 Marks)**

Module-4

7 a. Discuss noise in DSB-SC. Show that figure of merit for DSB-SC receiver is one. **(10 Marks)**

b. Discuss pre-emphasis and de-emphasis in FM. **(10 Marks)**

OR

8 a. Derive the expression for figure of merit for FM. **(14 Marks)**

b. Show that figure of merit for single tone AM modulation is equal to 1/3 for 100% modulation. **(06 Marks)**

Module-5

9 a. With the aid of block diagram, describe PPM Generation and detection. **(10 Marks)**

b. Design a PCM multiplexing system using 256 levels signal quantizer for the transmission of 3 signals: m_1 m_2 and m_3 band limited to 5KHz, 10KHz and 5KHz respectively. Assuming that each signal is sampled at its Nyquist rate and 8 bits are transmitted simultaneously. Compute :

i) Maximum bit duration

ii) Channel Bandwidth required to pass PCM signal

iii) The commutator speed in RPM. **(10 Marks)**

OR

10 a. Describe the basic elements of a PCM system. **(10 Marks)**

b. State sampling theorem. Find the Nyquist sampling rate for the signal.
$g(t) = 10 \cos(50\pi t) \cos^2(150\pi t)$ where t is in mscecs. **(06 Marks)**

c. Represent the binary data given below interms of i) unipolar NRZ signaling ii) Split phase.
Binary data : 0 1 1 0 1 0 0 1. **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC42

Fourth Semester B.E. Degree Examination, Jan./Feb.2021
Microprocessors

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Microprocessor. With a neat diagram, describe the architecture of 8086. **(08 Marks)**

b. Explain the significance of following pins of 8086:
(i) ALE (ii) MN/$\overline{MX}$ (iii) M/$\overline{I/O}$ (iv) DT/$\overline{R}$. **(04 Marks)**

c. Write an ALP to reverse a data block without using a dummy block. **(04 Marks)**

OR

2 a. The Opcode for MOV instruction is "100010" . Determine Machine Language code for the following instructions:
(i) MOV BL, CL (ii) MOV [S1], DL **(04 Marks)**

b. Explain the following instructions, with examples:
(i) XLAT (ii) LDS (iii) AAM **(06 Marks)**

c. Write an ALP to add two, 16 bit (4 digit) BCD numbers. Ignore the end-around carry. **(06 Marks)**

Module-2

3 a. Write an ALP to convert a 16 bit binary number to BCD. **(06 Marks)**

b. If AX = 1234 H, Trace the output in AX after the execution of following instructions :
(i) SHL AX, 1 (ii) ROR AX, 1. **(04 Marks)**

c. Explain any three string instructions of 8086. **(06 Marks)**

OR

4 a. Write an ALP to find number of 1's and 0's in a given 16 bit number. **(06 Marks)**

b. What are assembler directives? Explain the following assembler directives with an example:
(i) DW (ii) OFFSET. **(06 Marks)**

c. Explain any four Flag Manipulation Instructions of 8086. **(04 Marks)**

Module-3

5 a. Explain the stack structure of 8086. **(06 Marks)**

b. Explain the Interrupt cycle of 8086. **(04 Marks)**

c. Write an ALP to find factorial of a 8 bit binary number. **(06 Marks)**

OR

6 a. Explain passing parameters to procedures with an example program. **(06 Marks)**

b. Explain MACROS in 8086, with an example. **(04 Marks)**

c. Write a program to generate a delay of 10 minutes using 8086 microprocessor operating on 10 MHz frequency. Show delay calculation in detail. **(06 Marks)**

Module-4

7 a. Explain maximum mode of 8086 with a neat block diagram. Write the memory read timing diagram. **(10 Marks)**

b. Explain I/O addressing capability of 8086. **(06 Marks)**

OR

8 a. Design an Interface between 8086 CPU and two chips of 16K × 8 EPROM and two chips of 32K × 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H. **(08 Marks)**

b. Explain the BSR mode of operation of 8255. **(04 Marks)**

c. What do you mean by key debouncing? Explain key debouncing circuit. **(04 Marks)**

Module-5

9 a. Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digitial data outut of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P2 of the ADC and a clock input of suitable frequency. Draw the schematic and write a program to convert an analog data to digital using ADC interface. **(08 Marks)**

b. Explain the following keyboard handling INT21H DOS function:
(i) 01H (ii) 02H (iii) 09H (iv) 0AH **(08 Marks)**

OR

10 a. Interface an 8255 with 8086 at 80 H as an I/O address of port A. Interface five 7 segment displays with the 8255. Write a sequence of instructions to display 1, 2, 3, 4 and 5 over five displays continuously as per their positions starting with 1 at the least significant position. **(10 Marks)**

b. Discuss the interface between 8086 and 8087 Numeric processor with a neat diagram. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | | **15EC44**

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Signals and Systems

Time: 3 hrs.   Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. For the trapezoidal pulse x(t) shown in Fig Q1(a), find the energy of x(t) also energy of signal $y(t) = \frac{d\,x(t)}{dt}$.

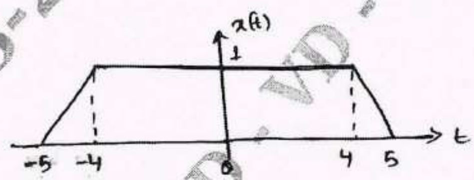


Fig Q1(a) **(04 Marks)**

b. For x(t) and y(t) given in Fig Q1(b) – i) and ii), respectively carefully sketch.
i) $x(t)\,y(-1-t)$ ii) $x(4-t)\cdot y(t)$

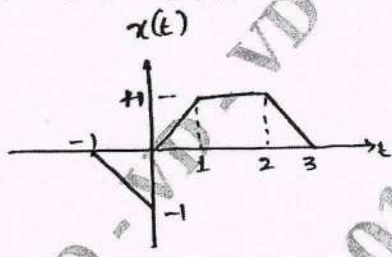


Fig Q1(b) – i)

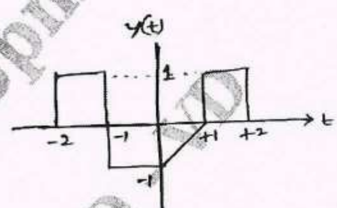


Fig Q1(b) – ii) **(06 Marks)**

c. For the following systems described by the input output relation, determine whether the system is linear, time invariant, causal and stable.
(i) $y(n) = x(n) + u(n+1)$ (ii) $y(t) = e^{-t}\,u(t)$ **(06 Marks)**

OR

2 a. List the elementary continuous time signals with suitable expression and diagram for each. **(06 Marks)**

b. Determine whether the following signals are periodic, if they are periodic, find the fundamental period.
(i) $x(t) = \cos(2\pi t) + \sin(3t)$ (ii) $x(n) = \cos\left(\frac{1}{5}\pi n\right)\cdot\sin\left(\frac{1}{3}\pi n\right)$ **(04 Marks)**

c. Sketch the even and odd components of the signals depicted in Fig Q2(c) i) and ii)

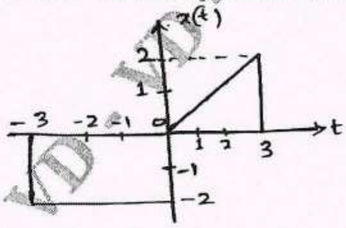


Fig Q2(c) – i)

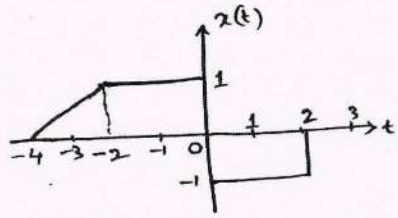


Fig Q2(c) – ii) **(06 Marks)**

Module-2

3 a. Suppose the input x(t) and impulse response h(t) of a LTI system are given by
(i) $x(t) = 2u(t-1) - 2u(t-3)$
(ii) $h(t) = u(t+1) - 2u(t-1) + u(t-3)$
Find the output of this system. **(10 Marks)**

b. State and prove the commutative and distributive properties of the convolution sum. **(06 Marks)**

OR

4 a. A LTI system has impulse response given by $h(n) = u(n) - u(n-10)$
Determine the output of this system when the input x(n) is defined by
$x(n) = u(n-2) - u(n-7)$. **(08 Marks)**

b. State and prove the associative property of convolution integral. **(04 Marks)**

c. A continuous time LTI system has impulse response as shown in Fig Q4(c)

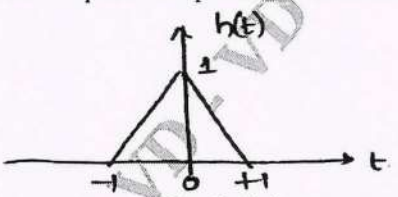


Fig Q4(c)

Find its output, if the input is $x(t) = \delta(t-1) + \delta(t-2) + \delta(t-3)$. **(04 Marks)**

Module-3

5 a. The following are the impulse responses of LTI systems. Determine whether each system is memoryless, causal and stable
i) $h(t) = e^{t}u(-1-t)$
ii) $h(n) = \cos(n).u(n)$
iii) $h(t) = u(t+1) - 2u(t-1)$. **(06 Marks)**

b. Determine the spectra of the signal $x(n) = \cos\left(\frac{\pi}{3}n\right)$. **(05 Marks)**

c. Determine and sketch the magnitude and phase spectra of the signal
$x(n) = (-1)^n ; -\infty < n < \infty$ **(05 Marks)**

OR

6 a. Evaluate the step response for the LTI systems represented by the following impulse responses. i) $h(t) = t \cdot u(t)$ ii) $h(t) = e^{-|t|}$ **(06 Marks)**

b. Evaluate the Fourier series representation for the signal $x(t) = \sin(2\pi t) + \cos(3\pi t)$. **(07 Marks)**

c. Define continuous Time Fourier Series. State any 4 properties of CTFS. **(03 Marks)**

Module-4

7 a. State and prove Parseval's theorem for continuous Time Fourier Transform. **(04Marks)**

b. Find the DTFT for the signals
i) $x(n) = 2^n u(-n)$ ii) $x(n) = a^{|n|} ; |a| < 1$ **(06 Marks)**

c. Find the Fourier Transform of the signal
$x(t) = \text{Sin}(\pi t)e^{-2t} \cdot u(t)$ **(06 Marks)**

OR

8 a. Evaluate the Fourier transform for the signal $x(t) = e^{-3t} u(t-1)$. Sketch the magnitude and phase spectra. **(06 Marks)**

b. Determine the signal x(n) if its DTFT is as shown in Fig Q8(b).

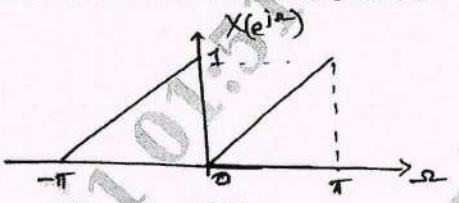


Fig Q8(b) **(05 Marks)**

c. State sampling theorem. Determine the Nyquist rate corresponding to the following signals.
i) $x_1(t) = \cos(150\pi t) \cdot \sin(100\pi t)$ ii) $x_2(t) = \cos^3(200\pi t)$. **(05 Marks)**

Module-5

9 a. State and prove the convolution property of Z transform. **(04 Marks)**

b. Find the Z-transform of the signal

$$x(n) = \left\{ n\left(\frac{-1}{2}\right)^n \cdot u(n) \right\} * \left(\frac{1}{4}\right)^{-n} u(-n)$$ **(06 Marks)**

c. Using power series expansion method, determine the inverse Z-transform of

(i) $X(z) = e^{z^2}$, with ROC all z except $|z| = \infty$

(ii) $X(z) = \dfrac{1}{1+\frac{1}{2}z^{-1}}$ with ROC $|z| > \dfrac{1}{2}$. **(06 Marks)**

OR

10 a. Find the time domain signal corresponding to the Z-transform

$$X(z) = \frac{\frac{1}{4}z^{-1}}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{4}z^{-1}\right)}$$ given the following cases of ROC

i) ROC ; $|z| > \dfrac{1}{2}$ ii) ROC ; $|z| < \dfrac{1}{4}$ iii) ROC $\dfrac{1}{4} < |z| < \dfrac{1}{2}$ **(05 Marks)**

b. A causal system has input x(n) and output y(n). Determine transfer function and impulse response of this system.

$x(n) = (-3)^n \cdot u(n)$ $y(n) = 4(2)^n u(n) - \left(\frac{1}{2}\right)^n u(n)$ **(05 Marks)**

c. A LTI discrete time system is given by the system function $H(z) = \dfrac{3-4z^{-1}}{1-3.5z^{-1}+1.5z^{-2}}$

Specify the ROC of H(z) and determine h(n) for the following conditions.
i) The system is stable ii) The system is causal. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC45

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Define Modulation. Explain need for modulation. **(06 Marks)**

b. Derive expression of AM by both time and frequency domain representation with necessary waveforms. **(06 Marks)**

c. A 400W carrier is modulated on a depth of 75%. Calculate the total power in the modulated wave in the following forms of AM.
i) Double sideband suppressed carrier ii) SSB. **(04 Marks)**

OR

2 a. Explain the generation of DSBSC wave using balanced modulator using diodes with relevant mathematical equations. **(08 Marks)**

b. Explain the generation of SSB wave using phase discrimination method with the help of neat functional block diagram. **(08 Marks)**

Module-2

3 a. Describe angle modulation. **(06 Marks)**

b. Explain the generation of frequency modulated wave using indirect method. **(08 Marks)**

c. The carrier swing of a FM signal 70kHz and the modulating signal is a 7kHz sine wave. Determine the modulation index of FM signal. **(02 Marks)**

OR

4 a. Explain the working of PLL and obtain the modulating signal by using linear model of PLL. **(08 Marks)**

b. Explain the working of a superheterodyne receiver using block diagram. **(08 Marks)**

Module-3

5 a. Describe Mean, Correlation and Covariance functions with respect to stationary random process. **(08 Marks)**

b. Explain the properties of auto correlation function and power spectral density. **(08 Marks)**

OR

6 a. Discuss thermal noise in detail. **(06 Marks)**

b. An amplifier operating over the frequency range from 450 to 460kHz has a 100KΩ input resistor. What is the rms noise voltage at the input to this amplifier if the ambient temperature is 17°C? Also calculate noise power and power spectral density. **(04 Marks)**

c. What is white noise? Plot power spectral density and auto correlation function of white noise. **(06 Marks)**

Module-4

7 a. In any receiver how the noise is produced? Explain. **(06 Marks)**

b. Derive the equation for the signal to noise ratio at the output of DSBSC receiver. **(06 Marks)**

c. An AM receiver operating with a sinusoidal wave and 80% modulation ahs an output signal to noise ratio of 30dB. Calculate the corresponding carrier to noise ratio. **(04 Marks)**

OR

8 a. Discuss about threshold effect in FM receiving system. **(06 Marks)**

b. Derive the equation for figure of merit at the output of the FM receiver. **(10 Marks)**

Module-5

9 a. State the sampling theorem. Explain sampling theorem in frequency domain. **(06 Marks)**

b. Explain the generation of PAM. State its advantages, disadvantages and application. **(10 Marks)**

OR

10 a. With the neat block diagram, explain the generation and reconstruction of PCM signals. **(06 Marks)**

b. Derive an expression for quantization error and signal to quantization noise ratio for non-sinusoidal PCM signals. **(06 Marks)**

c. Write a short note on VOCODER. **(04 Marks)**

* * * * *

2

CBCS SCHEME

USN | | | | | | | | | | |

18EC32

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Network Theory

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Using source transformation and source shifting techniques, find voltage across 2Ω resistor as shown in Fig.Q.1(a). **(07 Marks)**

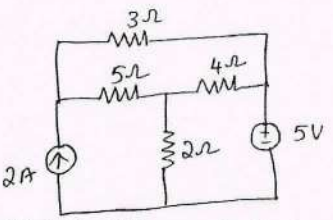


Fig.Q.1(a)

b. For the network shown in Fig.Q.1(b), find the equivalent resistance between A and B using Star-Delta transformation. **(05 Marks)**

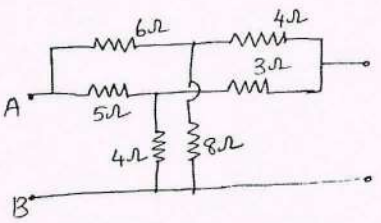


Fig.Q.1(b)

c. Determine the node voltages V_1 and V_2 by nodal analysis for the network in Fig.Q.1(c). **(08 Marks)**

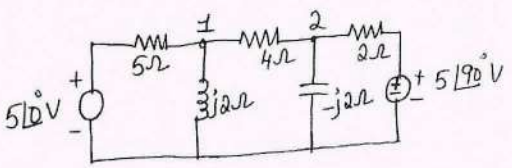


Fig.Q.1(c)

OR

2 a. Find the potential difference between M and N using source transformation, for the network shown in Fig.Q.2(a). **(05 Marks)**

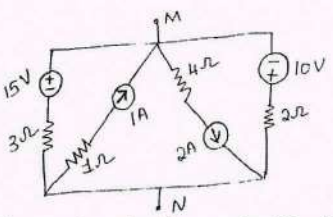


Fig.Q.2(a)

b. Find V_x using nodal analysis for the network shown in Fig.Q.2(b). **(08 Marks)**

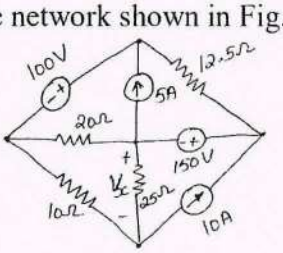
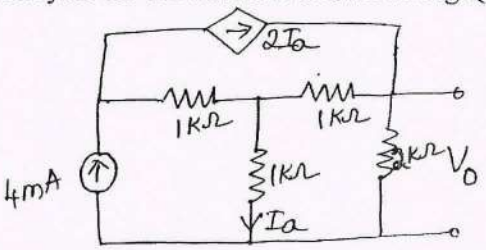


Fig.Q.2(b)

c. Determine V_0 using mesh analysis for the network shown in Fig.Q.2(c). **(07 Marks)**

Fig.Q.2(c)

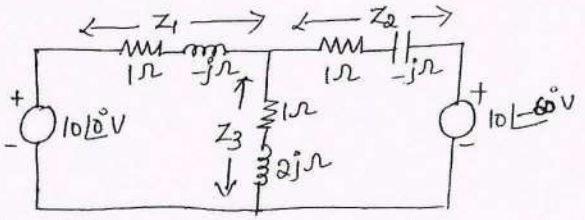


Module-2

3 a. State and prove Millman's theorem. **(06 Marks)**

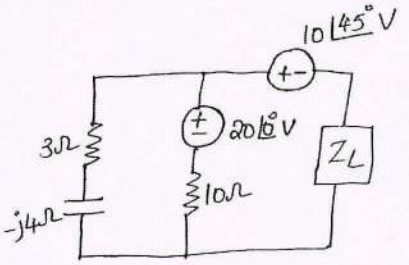
b. Find the current through Z_3 using superposition theorem for the network shown in Fig.Q.3(b). **(10 Marks)**

Fig.Q.3(b)



c. Find the value of Z_L for which maximum power transfer occurs in the network shown in Fig.Q.3(c). **(04 Marks)**

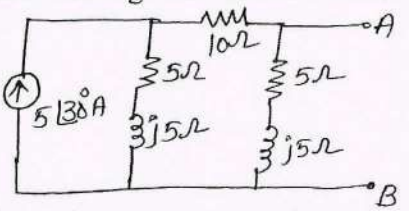
Fig.Q.3(c)



OR

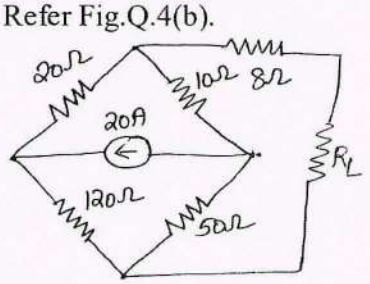
4 a. Obtain Thevenin's and Norton's equivalent circuit at terminals AB for the network shown in Fig.Q.4(a). Hence, find the current through 10Ω resistor across AB. **(12 Marks)**

Fig.Q.4(a)



b. Find the value of R_L for which maximum power is delivered. Also find the maximum power that is delivered to the load R_L. Refer Fig.Q.4(b). **(08 Marks)**

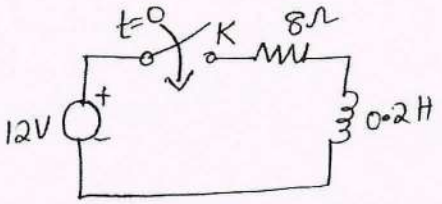
Fig.Q.4(b)



Module-3

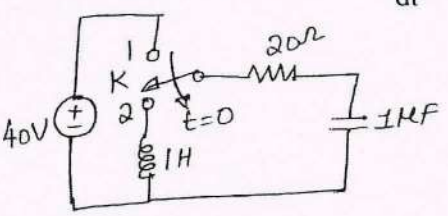
5 a. In the given network Fig.Q.5(a), K is closed at t = 0, with zero current in the inductor. Find the values of i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$. **(05 Marks)**

Fig.Q.5(a)



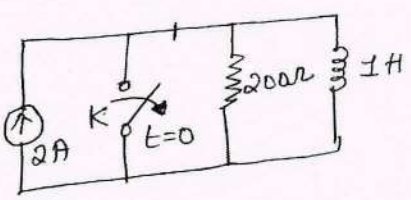
b. In the network Fig.Q.5(b), the switch is moved from position 1 to position 2 at t = 0. The steady-state has been reached before switching. Calculate i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$. **(07 Marks)**

Fig.Q.5(b)



c. In the network Fig.Q.5(c), the switch K is opened at t = 0. At $t = 0^+$, solve for v, $\frac{dv}{dt}$ and $\frac{d^2v}{dt^2}$. **(08 Marks)**

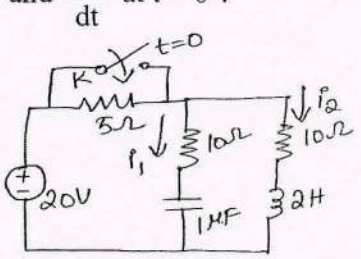
Fig.Q.5(c)



OR

6 a. For the circuit shown in Fig.Q.6(a), steady state is reached with switch K open. The switch is closed at t = 0. Find i_1, i_2, $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$ at $t = 0^+$. **(10 Marks)**

Fig.Q.6(a)



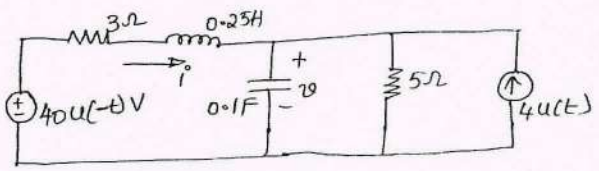
b. For the circuit in Fig.Q.6(b). Find:

i) $v(0^+)$ and $i(0^+)$

ii) $\frac{dv(0^+)}{dt}$ and $\frac{di(0^+)}{dt}$

iii) $v(\infty)$ and $i(\infty)$. **(10 Marks)**

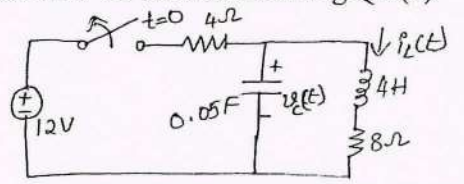
Fig.Q.6(b)



Module-4

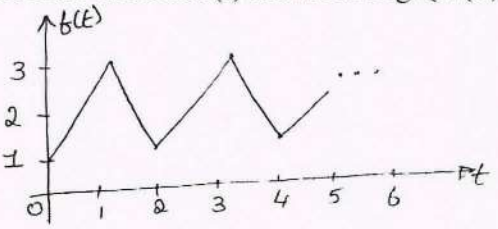
7 a. Determine the current $i_L(t)$ for $t \geq 0$ for the circuit in Fig.Q.7(a). **(10 Marks)**

Fig.Q.7(a)



b. Find the Laplace transform of the function f(t) shown in Fig.Q.7(b). **(10 Marks)**

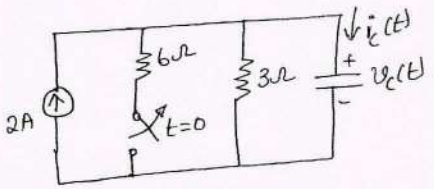
Fig.Q.7(b)



OR

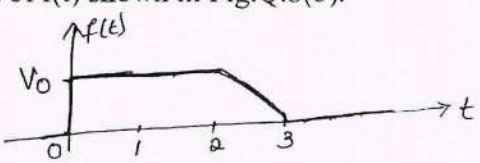
8 a. Determine the voltage $v_c(t)$ and the current $i_c(t)$ for $t \geq 0$ for the circuit shown in Fig.Q.8(a). **(10 Marks)**

Fig.Q.8(a)



b. Find the Laplace transform of f(t) shown in Fig.Q.8(b). **(10 Marks)**

Fig.Q.8(b)

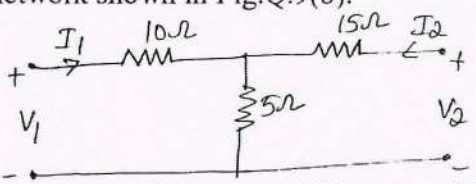


Module-5

9 a. Express Y parameters in terms of h-parameters. **(06 Marks)**

b. Find Z-parameters for the network shown in Fig.Q.9(b). **(06 Marks)**

Fig.Q.9(b)



c. The Z-parameters of a two port network are $z_{11} = 20\Omega$, $z_{22} = 30\Omega$, $z_{12} = z_{21} = 10\Omega$. Find Y and ABCD parameters of the network. **(08 Marks)**

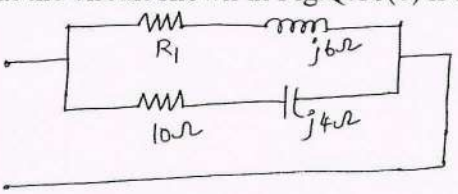
OR

10 a. Prove that the resonant frequency is the geometric mean of the two half power frequencies. **(06 Marks)**

b. A series RLC circuit has R = 10Ω, L = 0.01H and C = 0.01μF and it is connected across 10mv supply. Calculate: i) f_0 ii) Q_0 iii) bandwidth iv) f_1 and f_2 v) I_0. **(06 Marks)**

c. Find the value of R_1 such that the circuit shown in Fig.Q.10(c) is resonant. **(08 Marks)**

Fig.Q.10(c)



* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the figures of the resulting orbitals when isolated atoms brought together and explain the characteristics. **(10 Marks)**

b. Obtain the relationship between mobility and hall coefficient in a p-type bar placed in a magnetic field in the Z-direction. **(10 Marks)**

OR

2 a. Derive the equation which relates current density and mobility in a semiconductor in an applied electric field. **(10 Marks)**

b. A silicon bar 2μm long and 200μm^2 in cross sectional area is doped with 1.5×10^{17}/cm^3 phosphorus. Find the current at 300K with 30V applied voltage. How long does it take an average electron to drift 2μm in pure silicon at an electric field of 80V/cm? Also calculate the time required at 10^5V/cm. Assume mobility of electrons is 0.1350m^2/Vsec. Also assume that saturation of electron drift velocity for silicon is 10^7 cm/s for the electric field above 10^5 V/cm. **(10 Marks)**

Module-2

3 a. Show the effect of bias at a pn junction on transition region width, electric field, electrostatic potential, energy band diagram partic flow and current direction under the following conditions:
i) Equilibrium ii) Forward bias iii) Reverse bias. **(10 Marks)**

b. Illustrate the care and issues to be considered in the design of solar cells. **(10 Marks)**

OR

4 a. Explain Avalanche break down and obtain equation for the electron multiplication factor. **(10 Marks)**

b. Derive the relationship between the open circuit voltage and optic generation rate starting from the expression for the optically generated illuminated pn junction. **(10 Marks)**

Module-3

5 a. Show the hole and electron flow in a pnp transistor with proper biasing. **(08 Marks)**

b. For the circuit shown in Fig.Q.5(b) calculate β, I_B and I_C. Given that τ_p =18μs, and τ_t= 0.2μs. What happens to the output current when I_B increases and β increases?

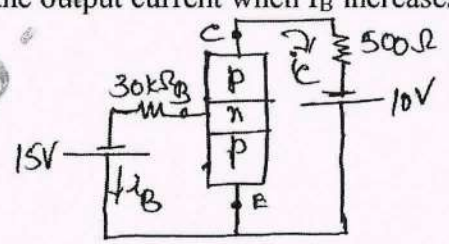


Fig.Q.5(b)

(06 Marks)

c. Explain the concept of base narrowing in a $p^+ - n - p^+$ transistor. **(06 Marks)**

OR

6 a. Obtain the Ebers-Moll equations and represent the same in the model form. **(12 Marks)**

b. Describe the switching effects in a CE transistor circuit. **(08 Marks)**

Module-4

7 a. Analyze the effect on gate-to-channel-space charge region and IV characteristics for the following conditions in a JFET:

i) Zero gate voltage of a small drain voltage

ii) Zero gate voltage of a large drain voltage

iii) Small V_{DS} value and small reverse-biased gate voltage. **(10 Marks)**

b. Draw the energy band diagram in an MOS capacitor structure for the following cases:

i) p-type substrate for a positive gate bias

ii) p-type substrate for a large positive gate bias

iii) n-type substrate for a positive gate bias. **(10 Marks)**

OR

8 a. Write the small signal equivalent circuit of a JFET, ideal low frequency small signal equivalent circuit and ideal equivalent circuit including r_s. **(10 Marks)**

b. Show the channel formation in the MOS structure and I_D versus V_{DS} curve for the following cases:

i) $V_{gs} > V_t$ and small V_{DS} value

ii) $V_{gs} > V_t$ and large V_{DS} value

iii) $V_{gs} > V_t$ and $V_{DS} = V_{DS}$ (sat) **(10 Marks)**

Module-5

9 a. What are the fabrication steps used in the fabrication of pn junctions? **(10 Marks)**

b. With figures, describe the complementary MOS structure. **(10 Marks)**

OR

10 a. Illustrate the evolution of integrated circuits. **(10 Marks)**

b. Explain the formation of resistors in integrated circuits. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Design a logic circuit that has 4 inputs, the output will be high, when the majority of the inputs are high. Use K-map to simplify. **(07 Marks)**

b. Express the following functions into canonical form:
(i) $f_1 = ab' + ab' + bc$ (ii) $f_2 = (a + b')(b' + c)$ **(06 Marks)**

c. Identify all the prime implicants and essential prime implicants of the following using K-map.
i) $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + dc(1, 4, 5, 11, 15)$
ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 9, 10) + dc(0, 14, 15)$
iii) $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ **(07 Marks)**

OR

2 a. Simplify the following using tabulation methods:
$Y = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$ **(07 Marks)**

b. Simplify the following expression using K-map. Implement the simplified expression using NAND gates only. $F = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$. **(07 Marks)**

c. Explain briefly K-map, incompletely specified functions, essential prime implicants and gray codes. **(06 Marks)**

Module-2

3 a. Design a two bit magnitude comparator. **(10 Marks)**

b. Realize the following functions expressed in maxterm canonical form in two possible ways using 3:8 decodes. $f_1(a, b, c) = \pi M(1, 2, 6, 7)$ and $f_2(a, b, c) = \pi M(1, 3, 6, 7)$ **(10 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$, using;
(i) 8:1 mux with a, b, c, as select lines (ii) 4:1 mux with a, b as select lines. **(08 Marks)**

b. Explain 4-bit carry look-ahead adder with necessary diagram and relevant expressions. **(04 Marks)**

c. Draw a PLA circuit to implement the logic function $A'BC + AB'C + AC'$ and $A'B'C' + BC$. **(08 Marks)**

Module-3

5 a. Explain with timing diagrams the workings of SR latch as a switch debouncer. **(08 Marks)**

b. What is race around condition? Explain JK Master Slave flipflop with a diagram, function table and timing diagram. **(07 Marks)**

c. List the difference between combinational and sequential circuits. **(05 Marks)**

OR

6 a. Explain the operation of clocked SR flipflop using NAND gates. **(07 Marks)**

b. What is the significance of Edge Triggering? Explain the working of positive edge triggered D-FF with their function table. **(07 Marks)**

c. Explain the working of 4-bit twisted ring counter using necessary diagram and logic table. **(06 Marks)**

Module-4

7 a. Using positive edge triggering SR flipflops design a counter which counts in the following sequence: 000, 111, 110, 101, 100, 011, 010, 001, 000 … **(10 Marks)**

b. Design a synchronous mod-6 counter using D-flipflop to generate the sequence (0, 2, 3, 6, 5, 1, 0) **(10 Marks)**

OR

8 a. Write the difference between Mealy and Moore model with necessary diagrams. **(10 Marks)**

b. Explain state machine notations with an example. **(10 Marks)**

Module-5

9 a. Construct Mealy state diagram that will detect input sequence 10110, when input pattern is detected, Z is asserted high. Give state diagram for each state. **(10 Marks)**

b. With necessary diagram, explain the concept of serial adder with accumulators. **(10 Marks)**

OR

10 a. Design a sequential circuit to convert BCD to excess 3 code. **(10 Marks)**

b. Explain the design of sequential circuit using CPLD's and give CPLD implementation of a shift register and parallel adder with accumulator. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Write neat diagrams wherever necessary.

Module-1

1 a. With a neat diagram, describe the functional units of a computer. Give few examples for I/O devices. **(06 Marks)**

b. Discuss IEEE standard for single-precision and double-precision floating point numbers, with standard notations. **(06 Marks)**

c. Develop an Assembly Language Program (ALP) for the expression $Y = Ax^2 + BCx + D$ using 3-address, 2-address and 1-address instruction formats. Assume A, B, C, D, Y as memory locations and x as immediate data. **(08 Marks)**

OR

2 a. With a neat diagram, discuss the operational concepts in a computer highlighting the role of PC, MAR, MDR and IR. **(08 Marks)**

b. Perform subtraction on the following pairs of numbers using 5-bit signed 2's-complement format. Indicate about overflow in each case:
i) +10 and -8 ii) +12 and +9 iii) -15 and -9 iv) -14 and +5 **(08 Marks)**

c. Distinguish between Big-endian and little-endian memory assignment. With a neat sketch, show how the number 26789435 is stored using these methods. **(04 Marks)**

Module-2

3 a. Define addressing mode. Explain any four basic addressing modes with syntax and examples. **(08 Marks)**

b. What is subroutine? With a pseudocode or program segment, illustrate parameter passing using registers. **(06 Marks)**

c. Consider a database of marks scored by students in 3 tests, stored in memory starting at address LIST. Each student record consists of studentID followed by marks in 3 tests. Assume each of these to be 4 bytes in size. There are 50 students in the class and this value is stored at location NUM.
i) Sketch the memory map showing all details
ii) Develop an ALP using Indexed Addressing mode, to compute the sum of scores by all the students in Test2 and store the result in location SUM. Write appropriate comments. **(06 Marks)**

OR

4 a. Discuss Auto-increment and Auto-decrement addressing modes with syntax. Consider a set of numbers (each 4 bytes in size) stored in memory starting at address TABLE. Total numbers are N and this value is stored at location LOCN.
i) Sketch the memory map showing all details
ii) Develop an ALP using Auto-increment addressing mode, to compute the sum of all numbers and store the result at memory address RESUTL. Write appropriate comments. **(08 Marks)**

b. Define stack. Explain PUSH and POP operations on stack with neat sketches and examples. **(06 Marks)**

c. Consider a register R1 to size 16-bits with initial data 5867_d. With neat sketches, depict the output in each case, after performing the following operations:
i) LshiftL #2, R1 ii) AshiftR #1, R1 iii) RotateR #1, R1
Note: For each operation, R1 value is to be taken as 5867_d and carry flag is indicated cleared. **(06 Marks)**

Module-3

5 a. Distinguish between memory mapped I/O and standard I/O. Write a program segment to read a line of text from keyboard and display it. **(08 Marks)**

b. What is interrupt priority? Why is it necessary? With relevant diagram, discuss daisy-chain method of handling multiple interrupt requests. **(06 Marks)**

c. Explain distributed arbitration mechanism in DMA with a neat diagram. **(06 Marks)**

OR

6 a. With a neat diagram, discuss implementation of interrupt priority using individual request and acknowledge lines. **(06 Marks)**

b. Briefly explain: i) Vectored interrupts and ii) Registers in a DMA interface. **(06 Marks)**

c. Explain centralized arbitration mechanism in DMA with a neat sketch and timing diagram. **(08 Marks)**

Module-4

7 a. Classify memory in a computer. With a neat diagram, describe the organization of 2M × 8 DRAM chip. **(08 Marks)**

b. What is cache memory? Explain direct mapping technique with a neat diagram. **(08 Marks)**

c. Briefly discuss the concept of virtual memory with a diagram. **(04 Marks)**

OR

8 a. Briefly explain the working of 1-bit CMOS SRAM cell with a schematic. **(06 Marks)**

b. What is mapping function? Explain set-associative cache mapping technique with a relevant diagram. **(08 Marks)**

c. With a neat diagram, explain the principle of working of magnetic disk. **(06 Marks)**

Module-5

9 a. Explain single-bus organization of data path in a processor with a neat diagram. Highlight the importance of gating signals. **(08 Marks)**

b. Develop the complete control signal sequence for the instruction Add (R1), R3 with appropriate remarks. **(06 Marks)**

c. Discuss micro programmed control unit design with relevant diagrams. **(06 Marks)**

OR

10 a. List different ways of improving CPU performance. With a neat diagram, discuss three-bus organization of CPU. Compare the performance with single-bus organization. **(08 Marks)**

b. Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z_{in} control signal. **(08 Marks)**

c. Define the following:
i) Gating signal ii) Control word iii) Microroutine iv) Control store. **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Power Electronics and Instrumentation

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Discuss various power converter circuits with necessary sketches and applications of each. **(07 Marks)**

b. With necessary sketches, explain the static V-I characteristics of SCR and its operation. **(08 Marks)**

c. List different turn-on methods, explain all in brief. **(05 Marks)**

OR

2 a. Explain turn-ON/turn-OFF dynamic characteristics of SCR with neat diagram. **(07 Marks)**

b. With suitable diagram and waveform, explain the working of RC full wave firing circuit. **(08 Marks)**

c. Describe the operation of UJT with neat sketches. **(05 Marks)**

Module-2

3 a. Explain the working of 1ϕ full wave center tapped controlled rectifier for resistive load with necessary sketches and also develop mathematical model to evaluate performance parameter of same (V_{dc}, V_{rms}, Efficiency). **(10 Marks)**

b. Evaluate performance parameter of 1ϕ half controlled rectifier with resistive load, has a transformer secondary voltage of 230V, 50Hz with R = 10Ω and firing angle $\alpha = 60°$. Determine:

i) Average voltage and current
ii) Rms value of voltage and current
iii) Efficiency
iv) Ripple factor
v) Form factor. **(10 Marks)**

OR

4 a. Input to the step-up chopper is 200V the output required is 600V, if the conduction time of thyristor is 200µsec. Compute:

i) Chopping frequency
ii) If the pulse width is halved for constant frequency operation, find the new output voltage. **(07 Marks)**

b. Explain the operation step-up chopper with neat diagram and derive an expression for output voltage. **(08 Marks)**

c. Elaborate on the control techniques used in choppers and also give detailed classification of choppers. **(05 Marks)**

Module-3

5 a. With neat circuit diagram and waveforms. Explain the operation of 1ϕ full bridge inverter for RL load. **(07 Marks)**

b. Design a multi range ammeter with range 0-1A, 0-5A and 0-10A employing individual shunt in each a D'Arsonval movement with an internal resistance of 500Ω and full scale deflection of 10mA is available. **(08 Marks)**

c. What are the errors encountered in measurement process? Explain all with suitable example. **(05 Marks)**

OR

6 a. Design modified multirange voltmeter with basic D'Arsonval movement with an internal resistance of 50Ω and full scale deflection of 2mA, with voltage ranges of 0-10V, 0-50V, 0-100V and 0-250V. Draw the schematic diagram and show all values after design. **(07 Marks)**

b. Explain the various static characteristics of measuring instruments. **(08 Marks)**

c. With neat diagram, explain the operation of isolated flyback converter. **(05 Marks)**

Module-4

7 a. With neat block diagram, explain the operation of Ramp type Digital voltmeter. **(07 Marks)**

b. Explain the operation of Time measurement with neat block diagram. **(08 Marks)**

c. Draw the schematic diagram of Wheatstone's bridge and derive an expression for calculating unknown resistance and explain. **(05 Marks)**

OR

8 a. Explain the operation inductance comparision bridge with necessary equations. **(07 Marks)**

b. Discuss the operation of successive approximation type DVM with necessary diagram. **(08 Marks)**

c. An unbalanced Wheatstone bridge shown in Fig.Q.8(c), calculate the current through the galvanometer. **(05 Marks)**

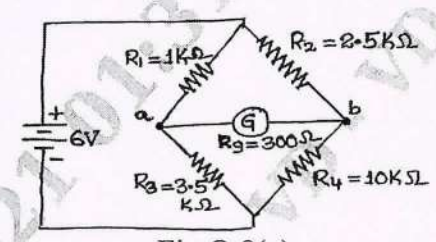


Fig.Q.8(c)

Module-5

9 a. Draw the schematic diagram to measure displacement using resistive transducer and explain. **(07 Marks)**

b. Explain the operation of PLC with neat block diagram. **(05 Marks)**

c. Explain the operation of Instrumentation amplifier using transducer bridge and derive equation for output voltage. **(08 Marks)**

OR

10 a. Explain the construction and working principle of LVDT with characteristic curve. **(07 Marks)**

b. What are factors to be considered for selecting the transducer? **(08 Marks)**

c. Illustrate working of analog weight scale. **(05 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is BJT transistor modeling? Obtain the expression for voltage gain, Z_{in} and Z_o of CB configuration using AC equivalent circuit with re model. **(05 Marks)**

b. Derive the expression for A_i, A_v, Z_i and Z_o for a voltage divider bias circuit of BJT, with unbypassed RE, using re equivalent model of BJT. Show the phase relationship between input and output wave form. **(10 Marks)**

c. State the characteristic features of Darlington connection. Calculate the DC bias voltages and currents in the circuit.

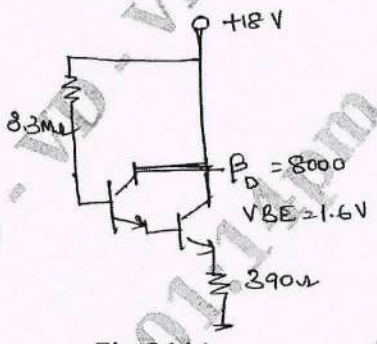


Fig.Q1(c) **(05 Marks)**

OR

2 a. Give the relation between re parameters and h parameters. What are the advantages of h parameters? **(05 Marks)**

b. Derive the expressions for current gain, voltage gain, input impedance and output impedance for an emitter follower circuit using approximate hybrid equivalent circuit. (Without the effect of r_o). **(10 Marks)**

c. For the network shown in Fig.Q2(c), determine re, Z_i, Z_o, A_v (with $r_o = \infty\Omega$) and A_v (with $r_o = 50\ K\Omega$)

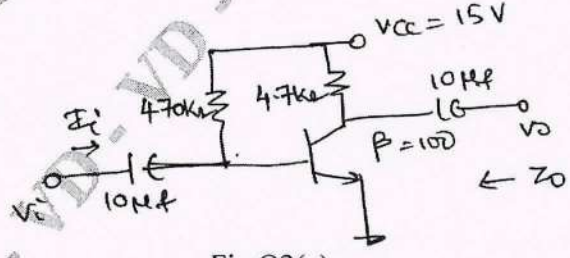


Fig.Q2(c) **(05 Marks)**

Module-2

3 a. Explain the construction of N channel JFET. Also explain the drain and transfer characteristics of the JFET. **(06 Marks)**

b. With equivalent circuit obtain the expression for Z_o and A_v for JFET self bias configuration. **(08 Marks)**

c. The fixed bias configuration shown in Fig.Q3(c) has $V_{GSQ} = -2V$, $I_{DQ} = 5.625$ mA with $I_{DSS} = 10$ mA, $V_P = -8V$ and $Y_{OS} = 40$ μS. Determine g_m, r_d, Z_o and A_v.

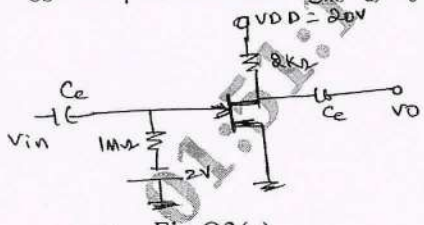


Fig.Q3(c) **(06 Marks)**

OR

4 a. Differentiate between enhancement and depletion MOSFET. **(05 Marks)**

b. With necessary equivalent circuit, obtain the expression for A_v for a JFET source follower configuration. **(05 Marks)**

c. Calculate the DC bias, voltage gain, input impedance and output impedance and resulting output voltage for the cascade amplifier shown in Fig.Q4(c). Calculate the load voltage if a 10 KΩ load is connected across the output.

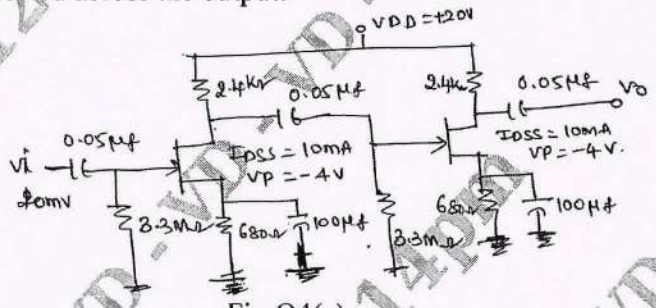


Fig.Q4(c) **(10 Marks)**

Module-3

5 a. Determine the lower cutoff frequency f_L s for the voltage divider bias network using the following parameters:
$C_S = 10$ μf, $C_E = 20$ μf, $C_C = 1$ μf, $R_S = 1$ KΩ, $R_1 = 40$ KΩ, $R_2 = 10$ KΩ, $R_E = 2$ KΩ, $R_C = 4$ KΩ, $R_L = 2.2$ KΩ, $\beta = 100$, $r_o = \infty\Omega$, $V_{CC} = 20$ V, re = 15.76 Ω. **(04 Marks)**

b. Explain the following: (i) Logarithm (ii) Decibel. With respect to transistor amplifier calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(06 Marks)**

c. Discuss the low frequency response of BJT amplifier and give expression for lower cut off frequency due to C_C, C_E and C_S. **(10 Marks)**

OR

6 a. Draw the Hybrid π model for the transistor in CE configuration and explain the significance of each component. **(06 Marks)**

b. Describe the Miller effect and derive an equation for Miller input capacitance. **(06 Marks)**

c. Determine the high cutoff frequencies for the network shown in Fig.Q6(c).

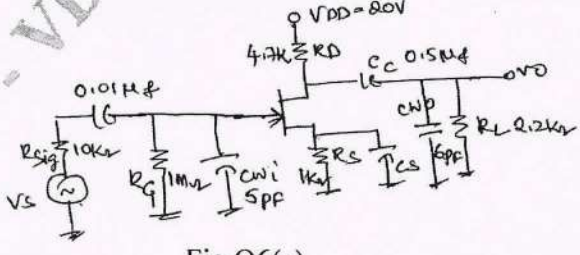


Fig.Q6(c) **(08 Marks)**

Module-4

7 a. With a block diagram, explain the concept of feedback amplifier and derive the expression for $A_f = \frac{A}{1+A\beta}$. **(06 Marks)**

b. Derive the expression for Z_{if} and Z_{of} for current series feedback amplifier. **(08 Marks)**

c. Explain a practical voltage series feedback circuit. **(06 Marks)**

OR

8 a. What is an oscillator? Discuss the concept of generating oscillations with the help of Barkhausen criteria. **(05 Marks)**

b. With a neat circuit diagram and necessary expressions, explain the Wein bridge oscillator. **(10 Marks)**

c. Design a unijuction transistor for a operation at 1 kHz and 150 kHz assuming $\eta = 0.58$. **(05 Marks)**

Module-5

9 a. Give the definition of power amplifiers and list the types of power amplifiers based on the location of Q point. **(05 Marks)**

b. Explain the working of class B complementary symmetry class B push pull amplifier. Obtain an expression for maximum conversion efficiency of this amplifier. **(10 Marks)**

c. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V and also calculate the total harmonic distortion for the amplitude components given above. **(05 Marks)**

OR

10 a. With necessary circuit diagram and characteristic curve, explain the class-A transformer coupled amplifier. Show that the maximum efficiency can be expressed as 50%. **(10 Marks)**

b. Describe the block diagram of series and shunt type voltage regulators. **(05 Marks)**

c. Calculate the output voltage and Zener current un the regulator circuit of Fig.Q10(c) for $R_L = 5\ K\Omega$.

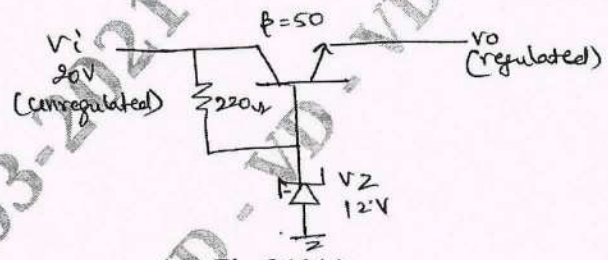


Fig.Q10(c) **(05 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define the following:
i) Combinational circuit
ii) Sequential circuit
iii) Canonical SOP
iv) Canonical POS
v) Prime Implicant
vi) Essential prime implicant. **(08 Marks)**

b. Express the following equations into decimal notations:
i) $H = f(A, B, C) = A'BC + A'BC + ABC$
ii) $T = f(a, b, c) = (a + b' + c)\ (a + b' + c')\ (a' + b' + c)$ **(08 Marks)**

c. Write mirror image version 5-variable K-map. **(04 Marks)**

OR

2 a. Obtain minimal expression using k-map for the following incompletely specified function $F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw circuit diagram using gates. **(10 Marks)**

b. Simplify the following using Quine-Mcclusky method
$s = f(w, x, y, z) = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ **(10 Marks)**

Module-2

3 a. Explain the analysis and design procedure for combinational circuit with example. **(10 Marks)**

b. Implement full substractor using 3:8 decoder and write truth table. **(10 Marks)**

OR

4 a. Design full adder using i) 8:1 MUX ii) 4:1 MUX. **(10 Marks)**

b. Design 4 to 16 decoder using 3 to 8 decoder. **(05 Marks)**

c. Explain look ahead carry adder and give its advantages and disadvantages. **(05 Marks)**

Module-3

5 a. What is flipflop? Discuss working principle of SR flipflop with its TT and write characteristics equations. **(10 Marks)**

b. Sketch timing diagram for JK flipflop and D-flipflop. **(05 Marks)**

c. Explain the operation of a switch debouncer built using SR-latch with the help of waveforms. **(05 Marks)**

OR

6 a. Explain the working of a master-slave JK flip-flop with timing diagram. Show how race around condition is eliminated. **(10 Marks)**

b. Explain setup time, hold time and propagation delay for timing considerations. **(05 Marks)**

c. Write characteristics equation for D and T flip-flop. **(05 Marks)**

Module-4

7 a. Explain with diagram, operation and waveforms Serial In Serial Out (SISO) shift left mode register. **(10 Marks)**

b. Design BCD ripple counter using JK flip-flop. **(10 Marks)**

OR

8 a. Design an synchronous mod 5 counter using JK flip-flop and draw its timing diagram. **(10 Marks)**

b. Explain ring counter with timing sequence. **(05 Marks)**

c. Write a note on Johnson counter. **(05 Marks)**

Module-5

9 a. Draw and explain the block diagram of Moore and Mealy model with example and also compare both. **(10 Marks)**

b. Define, present state, next state, state diagram state table and state assignment. **(05 Marks)**

c. Draw and explain Moore JK-flipflop state diagram. **(05 Marks)**

OR

10 a. Analyze the synchronous sequential circuit show below in Fig.Q.10(a).

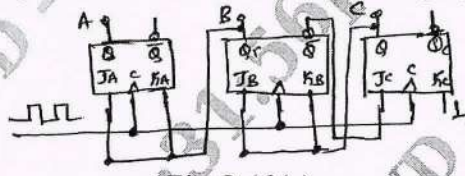


Fig.Q.10(a)

(12 Marks)

b. Design a synchronous counter using JK flipflops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define controlled source and mention its types. Also, mention its applications. **(05 Marks)**

b. Using source shift and source transformations, determine the voltage across the current source in Fig Q1(b).

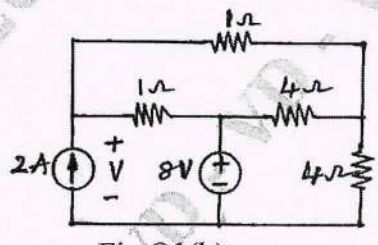


Fig Q1(b) **(05 Marks)**

c. For the circuit of Fig Q1(c), use nodal analysis to determine the voltage labeled V_x

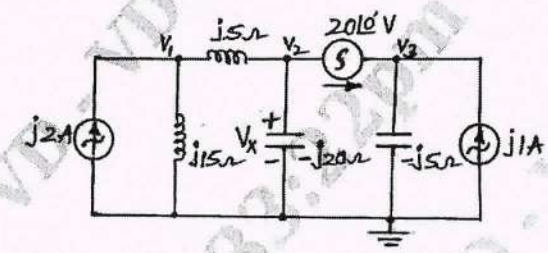


Fig Q1(c) **(10 Marks)**

OR

2 a. Define and explain supermesh. **(04 Marks)**

b. Use Star-Delta transformations to find the equivalent resistance at AB in Fig Q2(b).

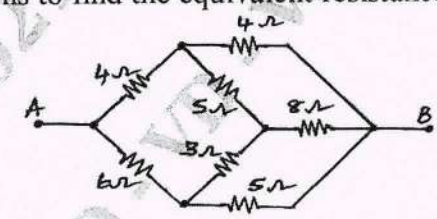


Fig Q2(b) **(06 Marks)**

c. Use Mesh analysis to determine V_1 and the power being supplied by the dependent current source in the circuit shown in Fig Q2(c).

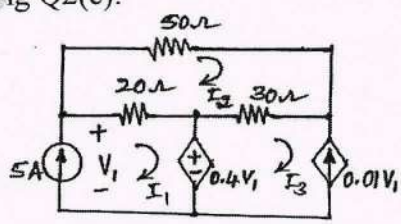


Fig Q2(c) **(10 Marks)**

Module-2

3 a. State and explain Millman's theorem for AC circuit. **(05 Marks)**

b. Use superposition on the circuit shown in Fig Q3(b) to find the current i_x.

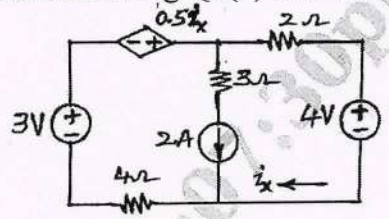


Fig Q3(b) **(05 Marks)**

c. Use Norton's theorem for the circuit of Fig Q3(c) to determine the power absorbed by the 20Ω resistor.

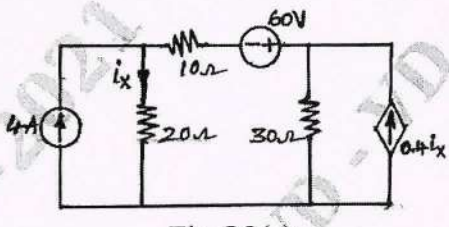


Fig Q3(c) **(10 Marks)**

OR

4 a. State and prove maximum power transfer theorem for AC voltage source with internal impedance connected to variable impedance. **(06 Marks)**

b. Verify reciprocity theorem for the circuit of Fig Q4(b).

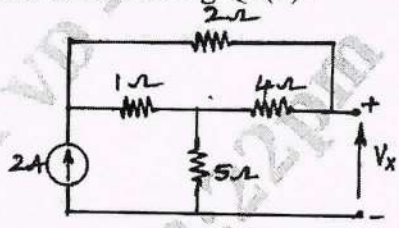


Fig Q4(b) **(04 Marks)**

c. For the circuit of Fig Q4(c), what value of R_L will absorb a maximum average power, and what is the value of this power?

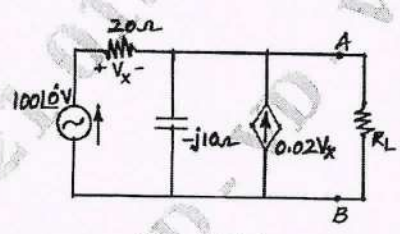


Fig Q4(c) **(10 Marks)**

Module-3

5 a. Explain the behavior of R, L and C elements for transients. Mention their representation at $t = 0^+$ **(06 Marks)**

b. In the network of the Fig Q5(b), is in the steady state with the switch K closed. At t = 0, the switch is opened. Find the values of v_1, v_2, $\frac{dv_1}{dt}$ and $\frac{dv_2}{dt}$ at $t = 0^+$.

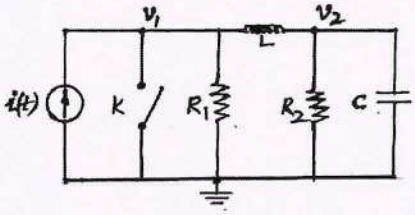


Fig Q5(b) **(08 Marks)**

c. Find the Laplace transform of the waveform shown in Fig Q5(c)

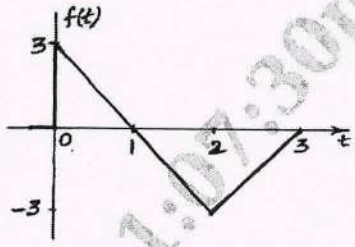


Fig Q5(c) **(06 Marks)**

OR

6 a. In the network of the Fig Q6(a), a steady state is reached with the switch K open. AT time t = 0, the switch is closed. Find the values of i_1, i_2, $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$ at $t = 0^+$.

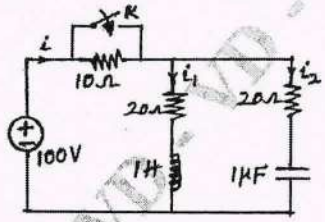


Fig Q6(a) **(10 Marks)**

b. In the network of the Fig Q6(b), the switch K is closed at t = 0 a steady state having previously excited. Draw the transform network and find the current i(t), using the Laplace transformation method.

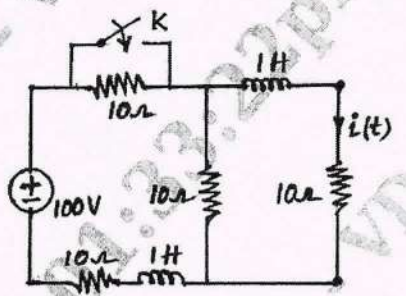


Fig Q6(b) **(10 Marks)**

Module-4

7 a. In a series resonant circuit, show that resonant frequency is equal to the geometric mean of half-power frequencies. **(06 Marks)**

b. An R-L-C series circuit of 8Ω resistance should be designed to have a bandwidth of 50Hz. Determine the values of L and C, so that the system resonates at 250Hz. Also determine the half power frequencies. **(06 Marks)**

c. For the network shown in Fig Q7(c), determine the value of C at which it resonates when f = 100Hz. Also find the values of R_L and R_C at which the circuit resonates at all frequencies.

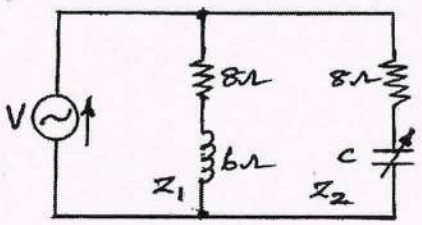


Fig Q7(c) **(08 Marks)**

OR

8 a. Define the following terms pertaining to a series R-L-C circuit, i) Resonance ii) Quality factor iii) Bandwidth iv) Selectivity. **(04 Marks)**

b. A series R-L-C circuit with an input voltage $5\angle 0°$ V resonates at a frequency of 8400Hz. The peak value of current is 500mA at resonance and the bandwidth is 120Hz. Determine the values of R, L, C and cut-off frequencies. **(06 Marks)**

c. For the network shown in Fig Q8(c), determine: i) Resonance frequency ii) Input admittance iii) Quality factor iv) Bandwidth and v) half power frequencies.

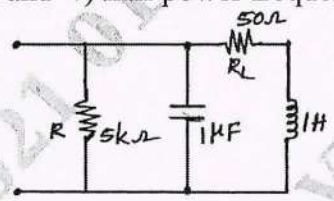


Fig Q8(c) **(10 Marks)**

Module-5

9 a. Obtain Y-parameters in terms of z-parameters. **(06 Marks)**

b. Find hybrid parameters for the two part shown in Fig Q9(b). What value of K in the two-part of figure shown will produce reciprocal network.

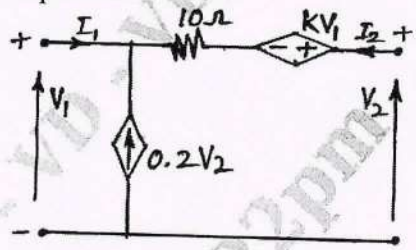


Fig Q9(b) **(06 Marks)**

c. Determine the ABCD parameters for the network of Fig Q9(c).

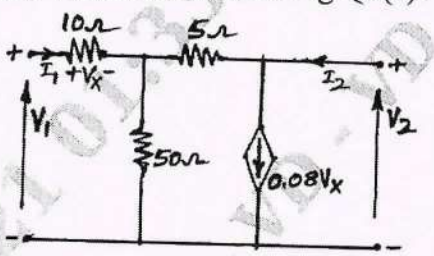


Fig Q9(c) **(08 Marks)**

OR

10 a. Explain h-parameters with equivalent circuit. Also obtain t-parameters in terms of h-parameters and hence show that AD – BC = 1. **(10 Marks)**

b. Find the Z-parameters and the Y-parameters for the network of Fig Q10(b)

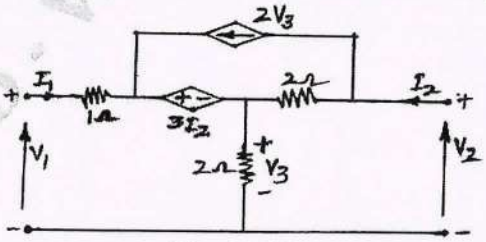


Fig Q10(b) **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Engineering Electromagnetics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. State and explain Coulomb's Law in vector form. **(04 Marks)**

b. Derive the expression for electric field intensity due to infinite line charge. **(08 Marks)**

c. Let a point charge Q_1 = 25nc be located at A(4, –2, 7) and a charge Q_2 = 60nc be at B(–3, 4, –2). Find $\vec{E}$ at C(1, 2, 3). Also find the direction of the electric field. Given $\epsilon_0 = 8.854 \times 10^{-12}$F/M. **(08 Marks**

OR

2 a. Define electric field intensity and flux density also derive an expression for electric field intensity $\vec{E}$ at a point due to many charges. **(07 Marks)**

b. Point charges of 50nc each are located at A(1, 0, 0), B(–1, 0, 0), C(0, 1, 0) and D(0, –1, 0)m find the total force on the charge at A and also find $\vec{E}$ at A. **(08 Marks)**

c. A uniform line charge of infinite length with P_L = 40nc/m, lies along the Z-axis. Find $\vec{E}$ at (–2, 2, 8) in air. **(05 Marks)**

Module-2

3 a. State and prove Gauss Law for point charge. **(06 Marks)**

b. Define potential difference and absolute potential. **(04 Marks)**

c. In the given relation $D = 4xy\hat{a}_x + 2(x^2 + y^2)\hat{a}_y + 4yz\hat{a}_z\, c/m^2$. Evaluate both sides of the divergence theorem and find the charge enclosed within the rectangular parallelpiped $(0 \le x \le 2)$, $(0 \le y \le 3)$ and $(0 \le z \le 5)$m. **(10 Marks)**

OR

4 a. State and prove divergence theorem. **(04 Marks)**

b. Derive point form of continuity equation for current. **(08 Marks)**

c. A point charge of 6nc is located at origin in free space, find potential of point P, if P is located at (0.2, –0.4, 0.4) and

i) V = 0 at infinity

ii) V = 0 at (1, 0, 0)

iii) V = 20V at (–0.5, 1, –1). **(08 Marks)**

Module-3

5 a. State and prove uniqueness theorem. **(08 Marks)**

b. By applying Laplace equation find the expression for capacitance between the two concentric spheres. Make suitable assumptions. **(12 Marks)**

OR

6 a. Derive the expressions for Poisson's and Laplace's equation. **(04 Marks)**

b. State and explain Biot – Savart Law. **(06 Marks)**

c. Given the potential field $V = [Ar^4 + Br^{-4}]\sin 4\phi$:

i) Show that $\nabla^2 V = 0$

ii) Find A and B such that V = 10V and $\vec{E}$ = 500V/m at P(r = 1, ϕ = 22.5°, z = 2). **(10 Marks)**

Module-4

7 a. Derive an expression for magnetic forces on :

i) Moving point charge and

ii) Differential current element. **(10 Marks)**

b. Two differential current elements,

$I_1 \Delta \vec{L}_1 = 10^{-5} \hat{a}_z$ A.M at $P_1(1, 0, 0)$ and

$I_2 \Delta \vec{L}_2 = 10^{-5}(0.6\hat{a}_x - 2\hat{a}_y + 3\hat{a}_z)$ A.M at $P_2(-1, 0, 0)$

are located in free space. Find vector force exerted on $I_2 \Delta \vec{L}_2 = I_1 \Delta \vec{L}_1$. **(10 Marks)**

OR

8 a. Drive the magnetic boundary conditions at the interface between the two different magnetic materials. Discuss the conditions. **(10 Marks)**

b. A sq. loop carrying 2mA current is placed in the field of an infinite filament carrying current of 15Amp as shown in Fig.Q8(b). Find the force exerted on the sq loop.

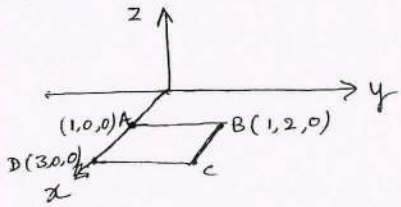


Fig.Q8(b). **(10 Marks)**

Module-5

9 a. Write a Maxwell's equations in point form and integral form. **(06 Marks)**

b. A uniform plane wave with an intensity of electric field equal to 1volt/m is travelling in free space. Find the magnitude of the associated magnetic field. **(04 Marks)**

c. State and explain pointing theorem. **(10 Marks**

OR

10 a. State and explain Faraday's Law of electromagnetic induction. **(04 Marks)**

b. Starting from Maxwell's equation obtain the general wave equations in electric magnetic fields. **(08 Marks)**

c. A UPW with 10MHz frequency has average pointing vector $1 W/m^2$ if the medium is perfect dielectric with $\mu_r = 2$, and $\epsilon_r = 3$, $\mu_0 = 4\pi \times 10^{-7}$H/m, $\epsilon_0 = 8.854 \times 10^{-12}$F/m ;

Find :

i) Velocity

ii) Wavelength

iii) Intrinsic impedance

iv) rms value of electric field. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC45

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define the following terms with respect to op-amp and mention their typical values
(i) CMRR (ii) PSRR (iii) Slew Rate (iv) I/P Offset voltages (v) Input bias current **(10 Marks)**

b. Sketch the circuit of an op-amp difference amplifier. Discuss the working common mode nulling capability with necessary circuit modifications and equations. **(10 Marks)**

OR

2 a. With a neat circuit diagram, explain the basic operational amplifier circuit. **(06 Marks)**

b. A non-inverting amplifier is to amplify a 100 mV signal to a level 5V. Using 741 op-amp design a suitable circuit. Also calculate the input and output impedances. **(08 Marks)**

c. With a neat circuit diagram, explain inverting summing amplifier and derive for output voltage and show how it can be converted into averaging circuit. **(06 Marks)**

Module-2

3 a. Sketch the circuit of a High Z_{in} capacitor Coupled Non-inverting amplifier and explain its working with necessary design steps. Show that the input impedance is very high compared to capacitor coupled Non-Inverting amplifier. **(10 Marks)**

b. Design a capacitor coupled Inverting amplifier using op-amp 741 to have a voltage gain of 50 and an output voltage of 2.5 V. The input signal frequency ranges from 10 Hz to 1 kHz with a load resistance of 250 Ω. **(06 Marks)**

c. What are the advantages of precision rectifiers over ordinary rectifiers? **(04 Marks)**

OR

4 a. Draw the circuit of an instrumentation amplifier and explain. Also show the method of nulling common mode outputs and how dc output voltage can be level shifted and list the features of instrumentation amplifier. **(10 Marks)**

b. With a neat sketch, explain the working of a precision voltage source with zener diode and op-amp. **(05 Marks)**

c. Explain how upper cutoff frequency can be set in Non-Inverting and Inverting capacitor coupled circuits. **(05 Marks)**

Module-3

5 a. Draw and explain an op-amp sample and hold circuit with necessary waveforms. **(08 Marks)**

b. Explain the working of Weinbridge oscillator using op-amp with a neat sketch of circuit, waveforms and equations. Design the same to get output frequency of 15 kHz with +/– 12 power supply using IC 741. **(08 Marks)**

c. With a neat circuit diagram, explain a multiplier using op-amp. **(04 Marks)**

OR

6 a. With a neat sketch, explain Inverting Schmitt trigger circuit with necessary waveforms and equations. Also design the same using IC741 op-amp to have UTP = 0V and LTP =– 2V with +/– 12V power supply. **(10 Marks)**

b. Sketch the circuit of fundamental log amplifier. Explain its working and derive for output voltage. What is the drawback of fundamental log amplifier and how it can be eliminated in temperature compensated log amplifier. **(10 Marks)**

Module-4

7 a. Sketch the circuit of second order active high pass filter using bipolor op-amp and explain its working. Design the same for a cutoff frequency of 7 kHz. **(08 Marks)**

b. Show how a bandpass filter can be constructed by the use of lowpass and high pass filters. Draw the circuit of a single stage band pass filter and explain the operation with necessary design equations. **(08 Marks)**

c. List the advantages of active filters over passive filters. **(04 Marks)**

OR

8 a. With a neat diagram, explain the operation of IC 723 as high voltage regulator. Design the same to have $V_0 = 12V$ and $I_0 = 2A$. **(08 Marks)**

b. Discuss the performance parameters of a three terminal IC regulator can be used as a current source. **(08 Marks)**

c. List the important characteristics of a three terminal IC regulator. **(04 Marks)**

Module-5

9 a. With a neat circuit diagram, explain the working of IC 566 voltage controlled oscillator with necessary waveforms. Also derive for output frequency. **(08 Marks)**

b. With a neat circuit diagram and waveforms explain the working of R-2R network D-A converter and derive the expression for output voltage. **(08 Marks)**

c. What is the output voltage produced by a DAC with output range of 0V to 10V for the given binary input number is (i) 0110 (for 4 bit DAC) (ii) 10111011 (for 8 bit DAC). **(04 Marks)**

OR

10 a. Draw the internal schematic of IC 555, configure it for astable operation and explain with necessary equations and waveforms. **(10 Marks)**

b. Explain the working of successive approximation Analog to Digital Converter (ADC). **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC46

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Microprocessors

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw and explain the internal architecture of 8086 microprocessor. **(10 Marks)**

b. Explain the concept of segmented memory. What are its advantages? **(06 Marks)**

c. If (CS) = 2000H, (DS) = 1234H, (SS) = 5678H, (BP) = 09ABH, calculate the physical address generated by the microprocessor when the following instruction is executed: MOV AL, [BP + 55H]. **(04 Marks)**

OR

2 a. With one example for each, describe any five addressing modes of 8086, used to access the data present in memory. **(10 Marks)**

b. List out any six conditional branch instruction that work based on the condition of any one flag. Mention the flag corresponding to each instruction. **(06 Marks)**

c. With numerical examples, illustrate the use of CBW and CWD instructions. **(04 Marks)**

Module-2

3 a. List out the five string manipulation instructions of 8086 and explain the operation of each. **(10 Marks)**

b. Write an Assembly Language Program (ALP) to add the data word located at address 2000H : 0500H to another data word available at offset 0600H in the same segment, and store the result and carry starting at 0700H in the same segment. **(06 Marks)**

c. With numerical examples, bring out the difference between SAR and SHR instructions. **(04 Marks)**

OR

4 a. Write an ALP using assembler directives to convert a 4-digit packed BCD number into equivalent 16-bit binary number, and store the result in memory. Write comments in your program. **(10 Marks)**

b. Explain the following instructions with one example each: RCR, XOR, SAHF. **(06 Marks)**

c. State the difference between the following two instructions: AND, TEST. What is the use of these instructions? **(04 Marks)**

Module-3

5 a. Explain the structure of stack in 8086 microprocessor. What is the role of stack during CALL and RET instructions? Illustrate with example. **(10 Marks)**

b. Explain any three methods of passing the parameters to and from a procedure. **(06 Marks)**

c. What is a macro? Give any two differences between macro and procedure. **(04 Marks)**

OR

6 a. Draw the interrupt vector table of 8086 and explain how an interrupt request is serviced, taking the example of type N interrupt. **(10 Marks)**

b. Write an ALP to generate a time delay of 10 seconds using an 8086 system that runs on 10MHz frequency. **(06 Marks)**

c. Bring out any four differences between maskable and non-maskable interrupts. **(04 Marks)**

Module-4

7 a. With a neat diagram, explain the maximum mode 8086 system. **(10 Marks)**

b. Write the functions of the following signals of 8086 : i) ALE ii) $\overline{DEN}$ iii) $\overline{BHE}$. **(06 Marks)**

c. Draw the minimum mode read cycle timing diagram, and explain briefly. **(04 Marks)**

OR

8 a. Design an interface between 8086 and two ICs of 32KB RAM and two ICs of 16KB EPROM. The RAM address must start at 00000H, and the EPROM address must end at FFFFFH. **(10 Marks)**

b. Draw the internal architecture of 8255 PIO and explain in brief. **(06 Marks)**

c. Explain Mode-1 and BSR modes of 8255. **(04 Marks)**

Module-5

9 a. Interface ADC 0808 with 8086 CPU using 8255 ports. Use port A for transferring digital data of ADC to CPU, and port C for control signals. Assume that analog input is present at input-3 of ADC. Draw the schematic and write the required ALP. **(10 Marks)**

b. Interface DAC0800 with 8086 CPU using port B of 8255. Write an ALP to generate a triangular waveform of frequency 400Hz. Assume that the system operates at 8MHz and the amplitude of the wave is 5V. **(10 Marks)**

OR

10 a. Write an ALP to read a 2-digit hexadecimal number from keyboard, and display its 4-digit square value on the computer screen, using appropriate DOS function calls. Use assembler directives and comments in your program. **(12 Marks)**

b. Write short notes on Von-Neumann architecture and Harvard architecture of computers with neat block diagrams. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. State the assumptions made.

Module-1

1 a. Define the following parameters with respect to op-amp.
i) Input offset current
ii) Input offset voltage
iii) CMRR
iv) PSRR **(08 Marks)**

b. Sketch an illustration to show the effect of op-amp slew rate and explain. **(04 Marks)**

c. If a Non-inverting amplifier is designed for a gain of 50, using op-amp with 90dB CMRR, calculate common mode output (V_{ocm}) for a common mode input (V_{icm}) of 100mV. **(04 Marks)**

OR

2 a. Design a direct-coupled non-inverting amplifier and explain its design steps. **(08 Marks)**

b. Two signals each ranging from 0.1V to 1V are to be summed. Using 741 op-amp design a suitable inverting summing circuit. **(04 Marks)**

c. Design a inverting amplifier using 741 op-amp with voltage gain of 50. The output voltage amplitude is 2.5V. **(04 Marks)**

Module-2

3 a. Draw the circuit to set the upper cut-off frequency using inverting amplifier and explain. **(08 Marks)**

b. A capacitor coupled non-inverting op-amp is to have gain of $A_v = 66$ and $V_i = 15mV$ with $R_L = 2.2K\Omega$ and $f_l = 120Hz$. Design the circuit. **(08 Marks)**

OR

4 a. Explain with a neat circuit design, precision full wave rectifier and also its design steps. **(08 Marks)**

b. Design a precision voltage source, with $V_o = 9V$ and supply voltage is $\pm 12V$. Allow 10% tolerance in zener diode [Assume 1N749 with $V_z = 4.3V$]. **(08 Marks)**

Module-3

5 a. Design a precision clipper to clip both ends, using dead zone circuit with relevant waveforms, explain the same. **(08 Marks)**

b. Design capacitor coupled zero-crossing detector with $f_l = 1kHz$ square wave input and $V_{o(p-p)} = 6V$. Use 741 op-amp with $\pm 12V$ supply [Assume $\Delta V = 1V$, $V_B = 0.1V$] **(08 Marks)**

OR

6 a. Define Barhausen's criteria. Explain with design, phase shift oscillator and with relevant waveforms. **(08 Marks)**

b. Show the realization of logarithmic amplifier using an op-amp. Obtain the expression for the output voltage. **(08 Marks)**

Module-4

7 a. Write a brief note on the following op-amp applications:

i) First order low pass filter

ii) Second order high pass filter. **(08 Marks)**

b. Design a single stage bandpass filter with frequency of $f_1 = 300$Hz and $f_2 = 30$kHz. Also state whether the design is narrow band or wide band. Use 741 op-amp for designing. [Assume $c_2 = 1000$pF]. **(08 Marks)**

OR

8 a. Explain the working of a series regulator using op-amp. **(06 Marks)**

b. With a neat internal diagram of IC723. Explain the functions of each block. Mention the advantages. **(10 Marks)**

Module-5

9 a. Explain D to A converter using R-2R network. **(08 Marks)**

b. With a neat block diagram, explain the blocks of PLL. **(08 Marks)**

OR

10 a. Explain 555 timer as Monostable muiltivibrator with waveforms. **(08 Marks)**

b. Explain the working of A to D converter using successive approximation method. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC32

Third Semester B.E. Degree Examination, Jan./Feb.2021
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With necessary equivalent diagram obtain the expression for Z_{in}, A_V, Z_0 for Darlington Emitter follower. **(10 Marks)**

b. For an Emitter bias circuit (capacitor bypassed), determine r_e, Z_i, Z_O and A_V. Given $R_B = 470\ K\Omega$, $R_C = 2.2\ K\Omega$, $V_{CC} = 20\ V$, $R_E = 0.56\ K\Omega$, $C_E = 10\ \mu F$, $\beta = 120$, $r_0 = 40\ K\Omega$, $C_C = 10\ \mu F$. **(06 Marks)**

OR

2 a. Derive the expression for A_V, A_i, Z_i and Z_0 for C_E fixed bias configuration using complete hybrid equivalent model. **(10 Marks)**

b. Consider a single stage CE amplifier with $R_S = 1\ K$ and $R_L = 1.2\ K\Omega$. Calculate A_i, R_i, A_V, A_{is}, if $h_{ie} = 1.1\ K$, $h_{re} = 2.5\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\ \mu A/V$. **(06 Marks)**

Module-2

3 a. Derive the expression for transconductance g_m for FET. **(06 Marks)**

b. For the circuit shown in the Fig. Q3 (b), calculate (a) V_{GS} (b) I_{DQ} (c) V_{DSQ} (d) V_D. **(10 Marks)**

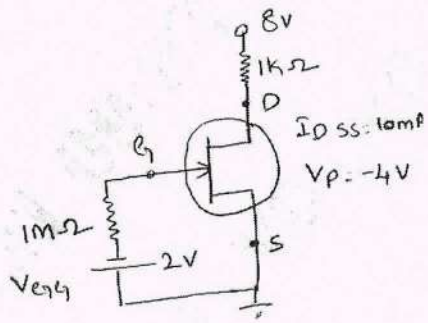


Fig. Q3 (b)

OR

4 a. With necessary equivalent circuit obtain the expression for A_V, Z_{in}, Z_O for a fixed biased JFET amplifier. **(08 Marks)**

b. Derive the expression for Z_i, Z_0, A_V considering common drain amplifier circuit. **(08 Marks)**

Module-3

5 a. Derive the expression for lower cut-of frequencies due to various RC networks in CE amplifiers. **(10 Marks)**

b. Determine the lower cut-off frequency for the emitter follower using BJT amplifier with $C_S = 0.1\ \mu F$, $R_S = 1\ K\Omega$, $R_1 = 12\ K\Omega$, $R_2 = 4\ K\Omega$, $R_E = 1.5\ K\Omega$, $C_C = 0.1\ \mu F$, $\beta = 100$, $r_0 = \infty$, $V_{CC} = 15\ V$, $V_{BE} = 0.7\ V$. **(06 Marks)**

OR

6 a. Describe Miller effect and derive an equation for Miller input and output capacitance. **(08 Marks)**

b. Calculate the overall lower 3 dB and upper 3 dB frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

Module-4

7 a. Derive the expression for input resistance for a voltage of series and current series feedback. **(08 Marks)**

b. With a neat circuit diagram, explain FET based phase shift oscillator. **(08 Marks)**

OR

8 a. With the help of neat circuit diagram. Explain the operation of Colpitts and Hartley oscillator. Write the expression for the frequency of oscillation. **(12 Marks)**

b. In a transistor Colpitts oscillator $C_1 = 1$ nF, $C_2 = 100$ nF. Find the value of L for a frequency of 100 kHz. **(04 Marks)**

Module-5

9 a. Show that the transformer coupled class A power amplifier has maximum efficiency of 50%. **(08 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as,

$B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA

(i) Determine the percentage total harmonic distortion.

(ii) Assume a second identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion. **(08 Marks)**

OR

10 a. Explain with the block diagram, the basic types of voltage regulation circuit. **(08 Marks)**

b. Explain the operation of complementary symmetry class B amplifier. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC34

Third Semester B.E. Degree Examination, Jan./Feb.2021
Network Analysis

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define the terms with an example,
(i) Linear and non linear elements.
(ii) Lumped and distributed elements.
(iii) Unilateral and Bilateral elements.
(iv) Active and Passive elements. **(08 Marks)**

b. Find the current in 28 Ω resistor using mesh analysis in Fig. Q1 (b). **(08 Marks)**

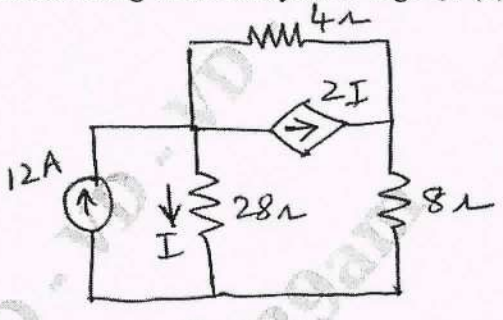


Fig. Q1 (b)

OR

2 a. Reduce the network in Fig. Q2 (a) to a single voltage source in series with a resistance using source shift and source transformation.

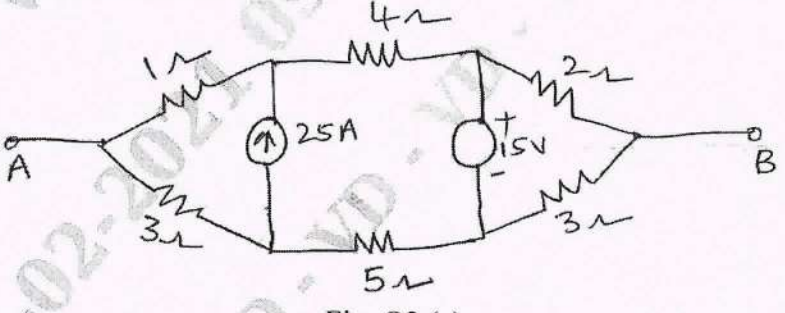


Fig. Q2 (a)

(08 Marks)

b. The node voltage equations of a network are,

$$\left[\frac{1}{5}+\frac{1}{j2}+\frac{1}{4}\right]V_1-\frac{1}{4}V_2=\frac{50\angle 0^0}{5}$$

and

$$-\frac{1}{4}V_1+\left[\frac{1}{4}+\frac{1}{-2j}+\frac{1}{2}\right]V_2=\frac{50\angle 90^0}{2}.$$

Derive the network. **(08 Marks)**

Module-2

3 a. State and prove superposition theorem. **(08 Marks)**

b. For the circuit shown in fig. Q3 (b), find the current through R_L using Thevenins theorem. **(08 Marks)**

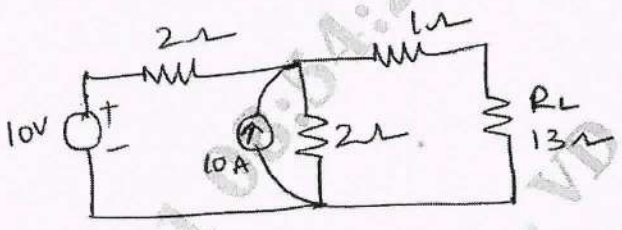


Fig. Q3 (b)

OR

4 a. State and prove Millers theorem. **(08 Marks)**

b. Find the value of Z_L for which power transferred to the load is maximum and also determine the maximum power for the circuit shown in Fig. Q4 (b). **(08 Marks)**

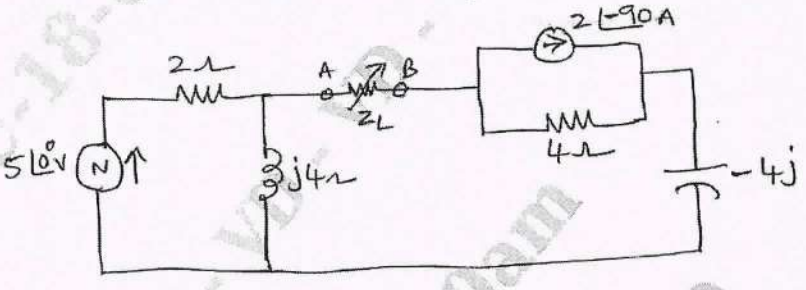


Fig. Q4 (b)

Module-3

5 a. In the circuit of Fig. Q5 (a). Switch K is opened at t = 0. Find the value of V, $\frac{dV}{dt}$ and $\frac{d^2V}{dt^2}$ at $t = 0^+$. **(08 Marks)**

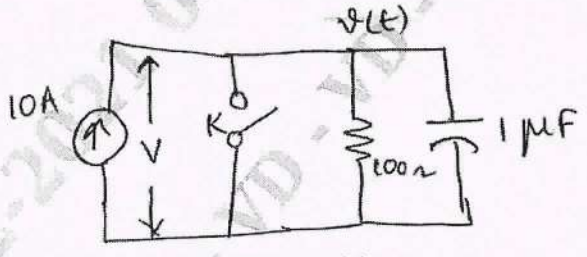


Fig. Q5 (a)

b. Obtain the Laplace transform of the square wave shown in Fig. Q5 (b). **(08 Marks)**

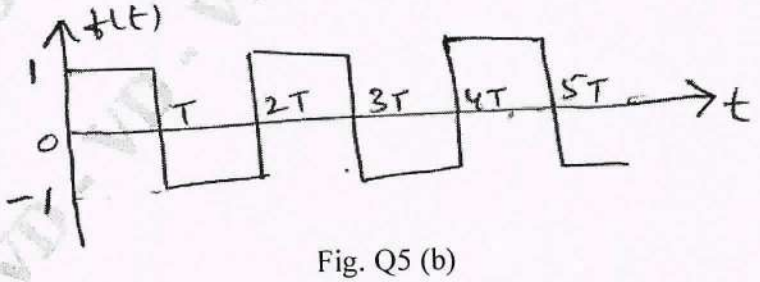


Fig. Q5 (b)

OR

6 a. State and prove initial value and final value theorem. **(08 Marks)**

b. For the network shown in Fig. Q6 (b) the switch is moved from position 1 to position 2 at t = 0 the steady state has been reached before switching. Calculate i, $\frac{di}{dt}$, $\frac{d^2i}{dt^2}$ at $t = 0^+$. **(08 Marks)**

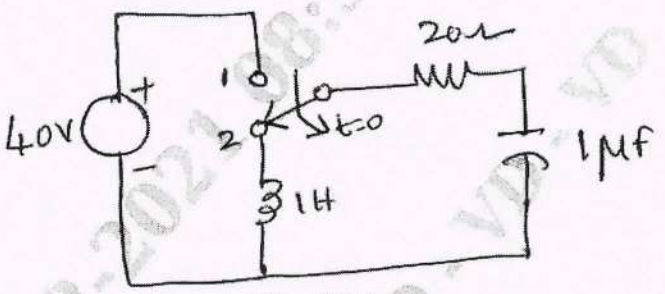


Fig. Q6 (b)

Module-4

7 a. Define the following terms :
(i) Resonance
(ii) Q-factor
(iii) Bandwidth
(iv) Selectivity. **(04 Marks)**

b. Derive an expression for frequency of resonance of a parallel resonant circuit containing resistance in both the branches. **(06 Marks)**

c. It is required that a series RLC circuit should resonate at 500 kHz. Determine the values of R, L and C if the bandwidth of the circuit is 10 kHz and its impedence is 100 Ω at resonance. Also find the voltages across L and C at resonance if the applied voltage is 75 volts. **(06 Marks)**

OR

8 a. Show that a two branch parallel resonant circuit is resonant at all the frequencies if $R_L = R_C = \sqrt{\frac{L}{C}}$ where R_L = Resistance in the inductor branch, R_C = Resistance in the capacitor branch. **(06 Marks)**

b. Give the comparison between series and parallel resonance. **(04 Marks)**

c. Find the value of R_1 such that the circuit given in Fig. Q8 (c) is resonant. **(06 Marks)**

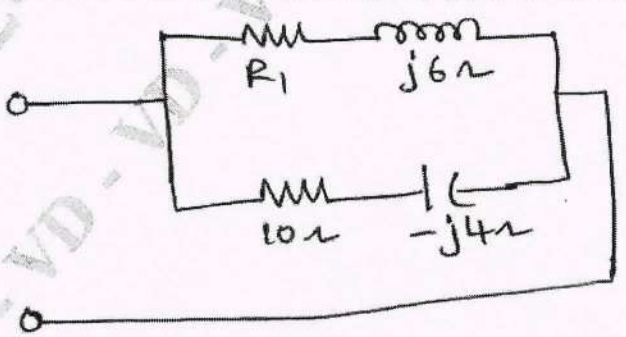


Fig. Q8 (c)

Module-5

9 a. Express Y parameters in terms of Z and T parameters. **(08 Marks)**

b. Find the transmission parameters for the network shown in Fig. Q9 (b). **(08 Marks)**

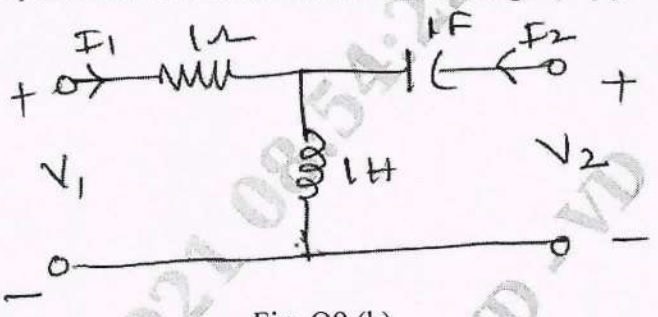


Fig. Q9 (b)

OR

10 a. Express ABCD parameters in terms of Y and h parameters. **(08 Marks)**

b. Find the h parameters of the network shown in Fig. Q10 (b). **(08 Marks)**

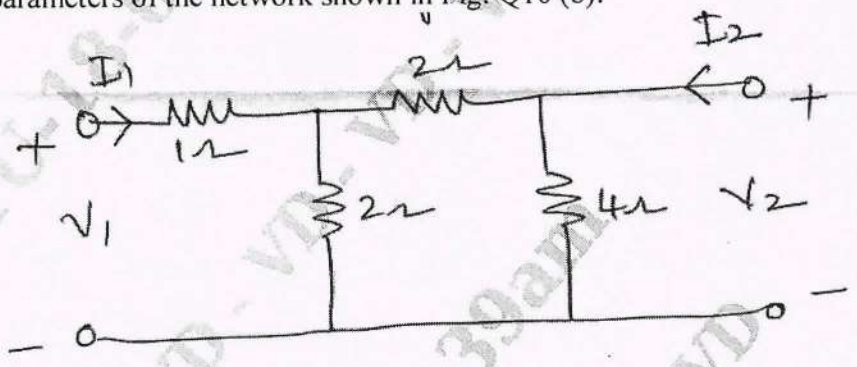


Fig. Q10 (b)

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC36

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Engineering Electromagnetics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. A charge $Q_A = -20$ μC is located at A(−6, 4, 7) and a charge $Q_B = 50$ μC is located at B(5, 8, −2) in free space. If distances are given in meters, find the vector force exerted on Q_A by Q_B. **(06 Marks)**

b. A charge of −0.3 μC is located at A(25, −30, 15) (in cm) and a second charge of 0.5 μC is located at B(−10, 8, 12) cm. Find Electric field intensity (E) at
(i) the origin (ii) P(15, 20, 50,)cm. **(08 Marks)**

c. Define electric flux density. **(02 Marks)**

OR

2 a. Calculate the total charge within the universe of $\rho_v = \frac{e^{-2r}}{r^2}$. **(04 Marks)**

b. Infinite uniform line charges of 5 nC/m lie along the (positive and negative) x and y axes in free space. Find Electric field intensity (E) at $P_A(0, 0, 4)$ **(04 Marks)**

c. Calculate Electric flux Density (D) in rectangular coordinates at point P(2, −3, 6) produced by
(i) a point charge QA = 55 mC at Q(−2, 3, −6);
(ii) a uniform line charge $\rho_{LB} = 20$ mC/m on the x-axis. **(08 Marks)**

Module-2

3 a. State and explain Gauss law in electrostatics. **(04 Marks)**

b. Derive the expression for electric field intensity due to an infinite line charge using Gauss law. **(04 Marks)**

c. In the region of free space that includes the volume $2 < x, y, z < 3$, $D = \frac{2}{z^2}(yza_x + xza_y - 2xya_z)$ c/m^2.
(i) Evaluate the volume integral side of the divergence theorem for the volume defines here.
(ii) Evaluate surface integral side for the corresponding closed surface. **(08 Marks)**

OR

4 a. Derive an expression for continuity equation in point form. **(04 Marks)**

b. If $\hat{E} = 120\ a_\rho$ V/m, find the incremental amount of work done in moving a 50 μC charge a distance of 2 mm from (i) P(1, 2, 3) toward Q(2, 1, 4) (ii) Q(2, 1, 4) toward P(1, 2, 3). **(05 Marks)**

c. Current density is given in cylindrical coordinates as $J = -10^6\ z^{1.5}a^z$ A/m^2 in the region $0 \le \rho \le 20$ μm; for $\rho \ge 20$ μm J = 0.
(i) Find the total current crossing the surface z = 0.1 m in the a_z direction.
(ii) If the charge velocity is 2×10^6 m/s at z = 0.1m, find ρ_v (volume charge density). **(07 Marks)**

Module-3

5 a. Starting from Gauss law, derive Poisson's and Laplace's equation. **(04 Marks)**

b. Calculate numerical value for potential V and volume charge density ρ_v at $P\left(3,\frac{\pi}{3},2\right)$ if $V = 5\rho^2 \cos 2\phi$. **(06 Marks)**

c. Given the spherically symmetric potential field in free space, $V = V_0 e^{-r/a}$, find:
(i) ρ_v at r = a (ii) the electric field at r = a (iii) total charge. **(06 Marks)**

OR

6 a. State and explain Ampere's law. **(04 Marks)**

b. Evaluate both sides of Stoke's theorem for the field $H = 10\sin\theta\, a_\phi$ and the surface r = 3, $0 \le \theta \le 90°$, $0 \le \phi \le 90°$. Let the surface have the a_r direction. **(06 Marks)**

c. Using the concept of vector magnetic potential, find the magnetic flux density at a point due to long straight filamentary conductor carrying current 'I' in the a_z direction. **(06 Marks)**

Module-4

7 a. Derive an expression for the force on a differential current element placed in a magnetic field. **(04 Marks)**

b. A point charge for which $Q = 2 \times 10^{-16}$ C and $m = 5 \times 10^{-26}$ kg is moving in the combined fields $E = 100\, a_x - 200\, a_y + 300\, a_z$ V/m and $B = -3a_x + 2a_y - a_z$ mT. If the charge velocity at t = 0 is V(0). $V(0) = (2a_x - 3a_y - 4a_z)10^5$ m/s.
(i) Give the unit vector showing the direction in which the charge is accelerating at t = 0.
(ii) Find the kinetic energy of the charge at t = 0. **(06 Marks)**

c. A rectangular loop of wire in free space joins points A(1, 0, 1) to B(3, 0, 1) to C(3, 0, 4) to D(1, 0, 4) to A. The wire carries a current of 6 mA, flowing in the a_z direction from B to C. A filamentary current of 15A flows along entire z axis in the a_z direction.
(i) Find 'F' on side BC (ii) Find 'F' on side AB (iii) Find F_{total} on the loop. **(06 Marks)**

OR

8 a. Given a material for which $x_m = 3.1$ and within which $B = 0.4ya_zT$, find:
(i) H (ii) μ (iii) μ_r (iv) M (v) J **(04 Marks)**

b. Let $\mu_{r_1} = 2$ in region 1 defined by $2x + 3y - 4z > 1$ while $\mu_{r_2} = 5$ in region 2 where $2x + 3y - 4z < 1$. In region 1, $H_1 = 50a_x - 30a_y + 20a_z$ A/m. Find:
(i) H_{N_1} (ii) H_{t_1} (iii) H_{t_2} (iv) H_{N_2} (v) θ_1 the angle between H_1 and a_{N21} **(08 Marks)**

c. Obtain an expression for the total energy stored in a steady magnetic filed in which 'B' is linearly related to 'H'. **(04 Marks)**

Module-5

9 a. Write Maxwell's equations in integral and point forms. **(06 Marks)**

b. Using Faraday's law, deduce Maxwell's equation, to relate time varying electric and magnetic fields. **(06 Marks)**

c. Explain the displacement current and displacement current density. **(04 Marks)**

OR

10 a. Derive wave equations for uniform plane wave in free space. **(06 Marks)**

b. Derive an expression for propagation constant intrinsic impedance and phase velocity for a uniform plane wave propagating in a conducting media. **(06 Marks)**

c. In free space $E(x,t) = 50\cos(\omega t - \beta x)a_y$ V/m. find the average power crossing a circular area of radius 5m in the plane x = constant. **(04 Marks)**

CBCS SCHEME

USN | | | | | | | | | | |

17EC42

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Signals and Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define a signal. List the elementary signals. Differentiate between even and odd signals, energy and power signals. **(08 Marks)**

b. Sketch the signal $x(t) = r(t+1) - r(t) + r(t-1)$. **(04 Marks)**

c. Check whether the following signals are periodic or not. If periodic, determine the fundamental period:

i) $x(n) = \cos\left(\frac{\pi n}{2}\right) + \sin\left(\frac{\pi n}{4}\right)$ ii) $x(t) = \cos(2\pi t)\ \sin\ 4\pi t$ **(08 Marks)**

OR

2 a. Determine and sketch the even and odd components of the signal x(t) shown in Fig.Q.2(a). **(08 Marks)**

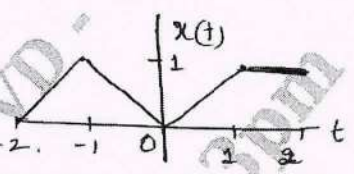


Fig.Q.2(a)

b. Find and sketch the derivatives of the following signals: $x(t) = u(t) - u(t-a)$, $a > 0$. **(04 Marks)**

c. Check whether the following system is
i) Static or dynamic
ii) Linear or nonlinear
iii) Time invariant or time variant
iv) Causal or non causal
v) Stable or unstable
vi) Invertible or non invertible. $y(n) = \log[x(n)]$. **(08 Marks)**

Module-2

3 a. Derive the expression for convolution integral. **(07 Marks)**

b. Prove the following: i) $x(n) * \delta(n) = x(n)$ ii) $x(n) * u(n) = \sum_{k=-\infty}^{n} x(k)$ **(06 Marks)**

c. Consider a LTI system with unit impulse response $h(t) = e^{-t}u(t)$. If the input applied to this system is $x(t) = e^{-3t}(u(t) - u(t-2))$. Find the output y(t) of the system. **(07 Marks)**

OR

4 a. State and prove commutative and distributive properties of convolution integral. **(08 Marks)**

b. The impulse response of LTI system is $h(n) = \{1, \underset{\uparrow}{2}\}$. Determine the response of the system to input signal $x(n) = \{1, \underset{\uparrow}{3}, 1\}$ using graphical method. **(06 Marks)**

c. Find the discrete time convolution sum given below:
$y(n) = \beta^n u(n) * \alpha^n u(n)$, $|B| < 1$, $|\alpha| < 1$ **(06 Marks)**

Module-3

5 a. The LTI systems are connected as shown in Fig.Q.5(a). If $h_1(n) = u(n-2)$, $h_2(n) = nu(n)$ and $h_3(n) = \delta(n-2)$. Find the overall response. **(10 Marks)**

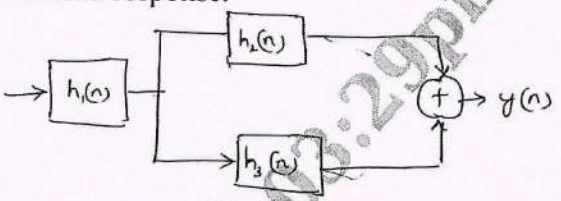


Fig.Q.5(a)

b. Evaluate the DTFS representation for the signal

$$x(n) = \sin\left(\frac{4\pi}{21}n\right) + \cos\left(\frac{10\pi}{21}n\right) + 1$$

Sketch the magnitude and phase spectra. **(10 Marks)**

OR

6 a. State and explain following continuous time Fourier series properties:
i) Time shift ii) Convolution iii) Parseval's Theorem. **(06 Marks)**

b. Check whether the system whose impulse response is
i) $h(n) = (1/2)^n u(-n)$ ii) $h(t) = e^{2t} u(t-1)$ stable, causal and memory less. **(09 Marks)**

c. Evaluate the step response for the LTI system represented by the following impulse response. $h(t) = t^2 u(t)$. **(05 Marks)**

Module-4

7 a. State the following properties of DTFT: i) Linearity ii) Frequency shift iii) Frequency differentiation iv) Modulation v) Convolution. **(10 Marks)**

b. Obtain the FT of the signal $x(t) = e^{-at} u(t)$; $a > 0$. **(10 Marks)**

OR

8 a. Find DTFT of the signal $x(n) = \{1, 3, \underset{\uparrow}{5}, 3, 1\}$ and evaluate $X(e^{j\Omega})$ at $\Omega = 0$ **(06 Marks)**

b. With neat diagrams, state and explain sampling theorem. **(08 Marks)**

c. Determine the Nyquist sampling rate and Nyquist sampling interval for
i) $x_1(t) = \text{Cos}(5\pi t) + 0.5\cos(10\pi t)$ ii) $x_2(t) = \text{Sinc}^2(200t)$ **(06 Marks)**

Module-5

9 a. Define Z-transform. Mention the properties of Region of Convergence (ROC). **(06 Marks)**

b. Determine the Z transform of these signals

i) $x_1(n) = n\left(\frac{5}{8}\right)^n u(n)$ ii) $x_2(n) = (0.9)^n u(n) * (0.6)^n u(n)$ **(08 Marks)**

c. Find Inverse Z transform, if $X(z) = \dfrac{\left(\frac{1}{4}\right)z^{-1}}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{4}z^{-1}\right)}$ for all possible ROCs. **(06 Marks)**

OR

10 a. Prove the following properties of Z-transform: i) Linearity ii) Time Reversal. **(08 Marks)**

b. A system has impulse response $h(n) = \left(\frac{1}{2}\right)^n u(n)$. Determine the input to the system if the output is given by $y(n) = \frac{1}{3}u(n) + \frac{2}{3}\left(-\frac{1}{2}\right)^n u(n)$. **(12 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC43

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Control Systems

Time: 3 hrs. Max. Marks: 100

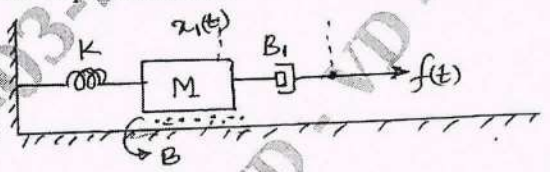
Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Differentiate between Open loop control system and Closed loop control system. **(06 Marks)**

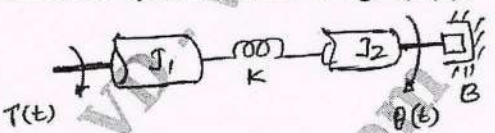
b. For the mechanical system, shown in fig. Q1(b), write the i) Mechanical network ;
ii) Differential equations of performance. **(06 Marks)**

Fig.Q1(b)



c. Obtain the transfer function of the system shown in fig. Q1(c). **(08 Marks)**

Fig.Q1(c)

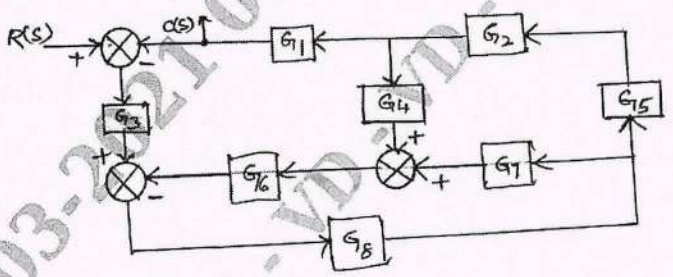


OR

2 a. Explain the block diagram rule regarding : i) Combining blocks in cascade
ii) Moving a take off point beyond a block. **(04 Marks)**

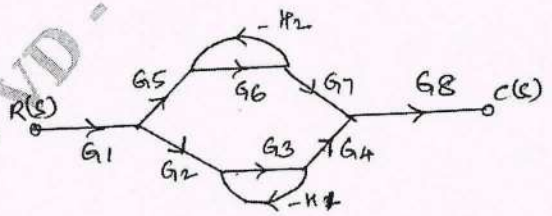
b. Determine the transfer function C(s)/R(s) for the block diagram shown in fig. Q2(b), using block diagram reduction techniques. **(08 Marks)**

Fig.Q2(b)



c. Find $\frac{C(s)}{R(s)}$ for the following signal flow graph of fig. Q2(c). **(08 Marks)**

Fig.Q2(c)



Module-2

3 a. With usual notation, derive an expression for the Peak time (t_p) and Rise time (t_r) of a response of second order system to a unit step input. **(06 Marks)**

b. Explain PI and PID controllers of a control system. **(06 Marks)**

c. A second order control system is represented by a transfer function given below :

$\frac{Q(s)}{T(s)} = \frac{1}{Js^2 + Bs + K}$, where Q(s) is the proportional output and T(s) is the input torque. A step unit of 10N-mt is applied to the system and test results are given below :

i) Maximum overshoot is 6% ii) Peak time is 1 sec iii) Steady static value of the output is 0.5 radian. Determine the values of J , F and K. **(08 Marks)**

OR

4 a. Define Steady state error and Static error coefficients with respect to step input, velocity input and acceleration inputs. **(06 Marks)**

b. For a unity feedback system $G(s) = \frac{s(s+1)}{s^2(s+3)(s+10)}$. Determine the type of system, error coefficients and steady state error for input $\gamma(t) = 1 + 3t$. **(06 Marks)**

c. A signal is represented by the equation $\frac{d^2\theta}{dt^2} + 10.\frac{d\theta}{dt} = 150.e$. Where $e = (r-\theta)$ is the actuating signal. Calculate the value of damping ratio, undamped and damped frequency of oscillation. Also determine Open loop transfer function. **(08 Marks)**

Module-3

5 a. State R – H criterion and discuss its limitation. **(06 Marks)**

b. State the different rules for the construction Root locus. **(06 Marks)**

c. The open loop transfer function of a unity feedback system is given by

$G(s) = \frac{K}{s(s+3)(s^2+s+1)}$. Determine the value of K that will cause sustained oscillations in the closed loop system. Also find the frequency of sustained oscillations. **(08 Marks)**

OR

6 a. A unity feedback control system has $G(s) = \frac{K}{s(s+2)(s+5)}$. Sketch the root locus and show clearly i) Break away points ii) The frequency at which root locus crosses imaginary axis and corresponding value of K. **(12 Marks)**

b. The open loop transfer function of a unity feedback system is given by

$G(s) = \frac{K(s+1)}{s^3 + as^2 + 2s + 1}$. Determine the value of K and a, so that the system oscillates at a frequency of 2 rad/sec^2. **(08 Marks)**

Module-4

7 a. With figure, define the frequency domain specifications. **(06 Marks)**

b. Construct the Bode plot for a unity feedback control system with

$G(s) = \frac{10(s+10)}{s(s+2)(s+5)}$. Find the Gain margin and Phase margin. Comment on the stability. **(14 Marks)**

OR

8 a. Explain Lag – lead compensating networks. **(06 Marks)**

b. Given $G(s)H(s) = \frac{12}{s[s+1][s+2]}$. Draw the Polar plot and hence determine if system is stable? **(06 Marks)**

c. The open loop transfer function of a control system is $G(s)H(s) = \frac{1}{s^2(s+2)}$. Sketch the Nyquist plot, Path and asertain the stability. **(08 Marks)**

Module-5

9 a. What is Signal Reconstruction? Explain it with SAMPLE and HOLD circuit. **(06 Marks)**

b. Find the State – transition Matrix for $A = \begin{bmatrix} 0 & -1 \\ +2 & -3 \end{bmatrix}$. **(06 Marks)**

c. Consider the system given by $\dddot{y} + 9\ddot{y} + 26\dot{y} + 24y = 6\,U$. Obtain its state model. **(08 Marks)**

OR

10 a. List the properties of State transition matrix. **(06 Marks)**

b. Explain Spectrum analysis of Sampling process. **(06 Marks)**

c. Obtain the transition matrix Q(t) of the following system

$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$. Also obtain the inverse of the transition matrix $\phi^{i}(t)$. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC44

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Illustrate the amplitude modulation process. What is envelope distortion? **(10 Marks)**

b. With the aid of neat block diagram, describe coherent detection of DSB-SC modulated wave. What is quadrature null effect? **(07 Marks)**

c. A single of 5KHz frequency signal is modulated on a carrier wave of a frequency 2 MHz. What are the frequencies of the resultant signal? **(03 Marks)**

OR

2 a. Describe ring modulator. Why the ring modulator is referred as a double balanced modulator? **(10 Marks)**

b. Describe quadrature carrier multiplexing. **(06 Marks)**

c. What are the factors influencing the choice of VSB modulation for the transmission of analog TV signals? **(04 Marks)**

Module-2

3 a. Derive an expression for FM signal. **(08 Marks)**

b. With the aid of neat block diagram, explain AM super heterodyne receiver. **(08 Marks)**

c. The resulting FM signal is $10 \cos[(2\pi\ 10^5 t) + 15 \sin(2\pi\ 100t)]$. Find the approximate bandwidth of the FM signal. **(04 Marks)**

OR

4 a. Describe the PLL working. **(08 Marks)**

b. With the aid of neat circuit diagram balanced frequency discriminator. **(08 Marks)**

c. What are the RF frequency range and intermediate frequency for AM and FM ratio? **(04 Marks)**

Module-3

5 a. Define Mean, correlation and covariance Functions of a random process x(t). **(08 Marks)**

b. Discuss Gaussian process and its properties. **(08 Marks)**

c. Draw the characteristics of white noise. **(04 Marks)**

OR

6 a. Write the important properties of autocorrelation function. **(08 Marks)**

b. Discuss shot noise, and thermal noise. **(08 Marks)**

c. Define noise equivalent bandwidth. **(04 Marks)**

Module-4

7 a. Discuss noise in DSB-SC. Show that figure of merit for DSB-SC receiver is one. **(10 Marks)**

b. Discuss pre-emphasis and de-emphasis in FM. **(10 Marks)**

OR

8 a. Derive the expression for figure of merit for FM. **(14 Marks)**

b. Show that figure of merit for single tone AM modulation is equal to 1/3 for 100% modulation. **(06 Marks)**

Module-5

9 a. With the aid of block diagram, describe PPM Generation and detection. **(10 Marks)**

b. Design a PCM multiplexing system using 256 levels signal quantizer for the transmission of 3 signals: m_1 m_2 and m_3 band limited to 5KHz, 10KHz and 5KHz respectively. Assuming that each signal is sampled at its Nyquist rate and 8 bits are transmitted simultaneously. Compute :

i) Maximum bit duration

ii) Channel Bandwidth required to pass PCM signal

iii) The commutator speed in RPM. **(10 Marks)**

OR

10 a. Describe the basic elements of a PCM system. **(10 Marks)**

b. State sampling theorem. Find the Nyquist sampling rate for the signal.
$g(t) = 10 \cos(50\pi t) \cos^2(150\pi t)$ where t is in mscecs. **(06 Marks)**

c. Represent the binary data given below interms of i) unipolar NRZ signaling ii) Split phase.
Binary data : 0 1 1 0 1 0 0 1. **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC42

Fourth Semester B.E. Degree Examination, Jan./Feb.2021
Microprocessors

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Microprocessor. With a neat diagram, describe the architecture of 8086. **(08 Marks)**

b. Explain the significance of following pins of 8086:
(i) ALE (ii) MN/$\overline{MX}$ (iii) M/$\overline{I/O}$ (iv) DT/$\overline{R}$. **(04 Marks)**

c. Write an ALP to reverse a data block without using a dummy block. **(04 Marks)**

OR

2 a. The Opcode for MOV instruction is "100010" . Determine Machine Language code for the following instructions:
(i) MOV BL, CL (ii) MOV [S1], DL **(04 Marks)**

b. Explain the following instructions, with examples:
(i) XLAT (ii) LDS (iii) AAM **(06 Marks)**

c. Write an ALP to add two, 16 bit (4 digit) BCD numbers. Ignore the end-around carry. **(06 Marks)**

Module-2

3 a. Write an ALP to convert a 16 bit binary number to BCD. **(06 Marks)**

b. If AX = 1234 H, Trace the output in AX after the execution of following instructions :
(i) SHL AX, 1 (ii) ROR AX, 1. **(04 Marks)**

c. Explain any three string instructions of 8086. **(06 Marks)**

OR

4 a. Write an ALP to find number of 1's and 0's in a given 16 bit number. **(06 Marks)**

b. What are assembler directives? Explain the following assembler directives with an example:
(i) DW (ii) OFFSET. **(06 Marks)**

c. Explain any four Flag Manipulation Instructions of 8086. **(04 Marks)**

Module-3

5 a. Explain the stack structure of 8086. **(06 Marks)**

b. Explain the Interrupt cycle of 8086. **(04 Marks)**

c. Write an ALP to find factorial of a 8 bit binary number. **(06 Marks)**

OR

6 a. Explain passing parameters to procedures with an example program. **(06 Marks)**

b. Explain MACROS in 8086, with an example. **(04 Marks)**

c. Write a program to generate a delay of 10 minutes using 8086 microprocessor operating on 10 MHz frequency. Show delay calculation in detail. **(06 Marks)**

Module-4

7 a. Explain maximum mode of 8086 with a neat block diagram. Write the memory read timing diagram. **(10 Marks)**

b. Explain I/O addressing capability of 8086. **(06 Marks)**

OR

8 a. Design an Interface between 8086 CPU and two chips of 16K × 8 EPROM and two chips of 32K × 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H. **(08 Marks)**

b. Explain the BSR mode of operation of 8255. **(04 Marks)**

c. What do you mean by key debouncing? Explain key debouncing circuit. **(04 Marks)**

Module-5

9 a. Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digitial data outut of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P2 of the ADC and a clock input of suitable frequency. Draw the schematic and write a program to convert an analog data to digital using ADC interface. **(08 Marks)**

b. Explain the following keyboard handling INT21H DOS function:
(i) 01H (ii) 02H (iii) 09H (iv) 0AH **(08 Marks)**

OR

10 a. Interface an 8255 with 8086 at 80 H as an I/O address of port A. Interface five 7 segment displays with the 8255. Write a sequence of instructions to display 1, 2, 3, 4 and 5 over five displays continuously as per their positions starting with 1 at the least significant position. **(10 Marks)**

b. Discuss the interface between 8086 and 8087 Numeric processor with a neat diagram. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC44

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Signals and Systems

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. For the trapezoidal pulse x(t) shown in Fig Q1(a), find the energy of x(t) also energy of signal $y(t) = \frac{dx(t)}{dt}$.

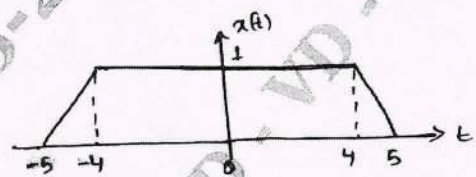


Fig Q1(a) **(04 Marks)**

b. For x(t) and y(t) given in Fig Q1(b) – i) and ii), respectively carefully sketch.
i) x(t) y(–1–t) ii) x(4 – t)· y(t)

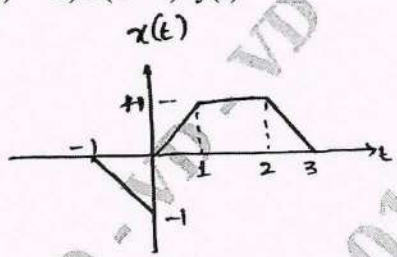


Fig Q1(b) – i)

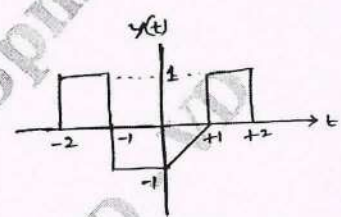


Fig Q1(b) – ii) **(06 Marks)**

c. For the following systems described by the input output relation, determine whether the system is linear, time invariant, causal and stable.
(i) $y(n) = x(n) + u(n+1)$ (ii) $y(t) = e^{-t}\, u(t)$ **(06 Marks)**

OR

2 a. List the elementary continuous time signals with suitable expression and diagram for each. **(06 Marks)**

b. Determine whether the following signals are periodic, if they are periodic, find the fundamental period.
(i) $x(t) = \cos(2\pi t) + \sin(3t)$ (ii) $x(n) = \cos\left(\frac{1}{5}\pi n\right) \cdot \sin\left(\frac{1}{3}\pi n\right)$ **(04 Marks)**

c. Sketch the even and odd components of the signals depicted in Fig Q2(c) i) and ii)

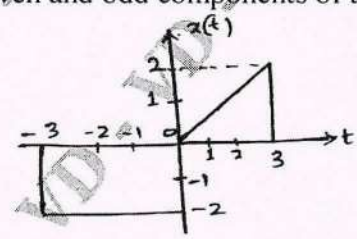


Fig Q2(c) – i)

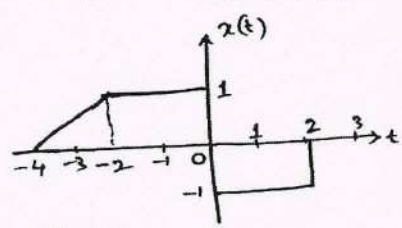


Fig Q2(c) – ii) **(06 Marks)**

Module-2

3 a. Suppose the input x(t) and impulse response h(t) of a LTI system are given by
(i) $x(t) = 2u(t-1) - 2u(t-3)$
(ii) $h(t) = u(t+1) - 2u(t-1) + u(t-3)$
Find the output of this system. **(10 Marks)**

b. State and prove the commutative and distributive properties of the convolution sum. **(06 Marks)**

OR

4 a. A LTI system has impulse response given by $h(n) = u(n) - u(n-10)$
Determine the output of this system when the input x(n) is defined by
$x(n) = u(n-2) - u(n-7)$. **(08 Marks)**

b. State and prove the associative property of convolution integral. **(04 Marks)**

c. A continuous time LTI system has impulse response as shown in Fig Q4(c)

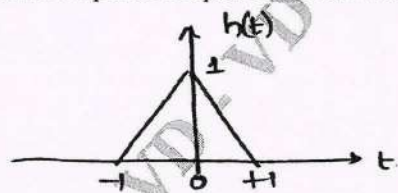


Fig Q4(c)

Find its output, if the input is $x(t) = \delta(t-1) + \delta(t-2) + \delta(t-3)$. **(04 Marks)**

Module-3

5 a. The following are the impulse responses of LTI systems. Determine whether each system is memoryless, causal and stable
i) $h(t) = e^{t}u(-1-t)$
ii) $h(n) = \cos(n).u(n)$
iii) $h(t) = u(t+1) - 2u(t-1)$. **(06 Marks)**

b. Determine the spectra of the signal $x(n) = \cos\left(\frac{\pi}{3}n\right)$. **(05 Marks)**

c. Determine and sketch the magnitude and phase spectra of the signal
$x(n) = (-1)^{n}$; $-\infty < n < \infty$ **(05 Marks)**

OR

6 a. Evaluate the step response for the LTI systems represented by the following impulse responses. i) $h(t) = t \cdot u(t)$ ii) $h(t) = e^{-|t|}$ **(06 Marks)**

b. Evaluate the Fourier series representation for the signal $x(t) = \sin(2\pi t) + \cos(3\pi t)$. **(07 Marks)**

c. Define continuous Time Fourier Series. State any 4 properties of CTFS. **(03 Marks)**

Module-4

7 a. State and prove Parseval's theorem for continuous Time Fourier Transform. **(04Marks)**

b. Find the DTFT for the signals
i) $x(n) = 2^{n}u(-n)$ ii) $x(n) = a^{|n|}$; $|a| < 1$ **(06 Marks)**

c. Find the Fourier Transform of the signal
$x(t) = \text{Sin}(\pi t)e^{-2t} \cdot u(t)$ **(06 Marks)**

OR

8 a. Evaluate the Fourier transform for the signal $x(t) = e^{-3t}\,u(t-1)$. Sketch the magnitude and phase spectra. **(06 Marks)**

b. Determine the signal x(n) if its DTFT is as shown in Fig Q8(b).

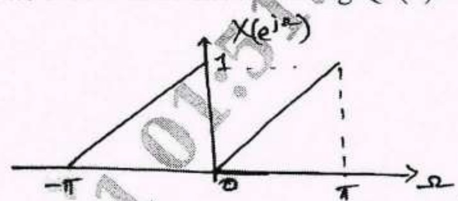


Fig Q8(b) **(05 Marks)**

c. State sampling theorem. Determine the Nyquist rate corresponding to the following signals.
i) $x_1(t) = \cos(150\pi t)\cdot\sin(100\pi t)$ ii) $x_2(t) = \cos^3(200\pi t)$. **(05 Marks)**

Module-5

9 a. State and prove the convolution property of Z transform. **(04 Marks)**

b. Find the Z-transform of the signal

$$x(n) = \left\{ n\left(\frac{-1}{2}\right)^n \cdot u(n) \right\} * \left(\frac{1}{4}\right)^{-n} u(-n)$$ **(06 Marks)**

c. Using power series expansion method, determine the inverse Z-transform of

(i) $X(z) = e^{z^2}$, with ROC all z except $|z| = \infty$

(ii) $X(z) = \dfrac{1}{1+\frac{1}{2}z^{-1}}$ with ROC $|z| > \dfrac{1}{2}$. **(06 Marks)**

OR

10 a. Find the time domain signal corresponding to the Z-transform

$$X(z) = \frac{\frac{1}{4}z^{-1}}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{4}z^{-1}\right)}$$ given the following cases of ROC

i) ROC ; $|z| > \frac{1}{2}$ ii) ROC ; $|z| < \frac{1}{4}$ iii) ROC $\frac{1}{4} < |z| < \frac{1}{2}$ **(05 Marks)**

b. A causal system has input x(n) and output y(n). Determine transfer function and impulse response of this system.

$x(n) = (-3)^n \cdot u(n)$ $y(n) = 4(2)^n\, u(n) - \left(\frac{1}{2}\right)^n u(n)$ **(05 Marks)**

c. A LTI discrete time system is given by the system function $H(z) = \dfrac{3-4z^{-1}}{1-3.5z^{-1}+1.5z^{-2}}$

Specify the ROC of H(z) and determine h(n) for the following conditions.
i) The system is stable. ii) The system is causal. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

15EC45

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Modulation. Explain need for modulation. **(06 Marks)**

b. Derive expression of AM by both time and frequency domain representation with necessary waveforms. **(06 Marks)**

c. A 400W carrier is modulated on a depth of 75%. Calculate the total power in the modulated wave in the following forms of AM.
i) Double sideband suppressed carrier ii) SSB. **(04 Marks)**

OR

2 a. Explain the generation of DSBSC wave using balanced modulator using diodes with relevant mathematical equations. **(08 Marks)**

b. Explain the generation of SSB wave using phase discrimination method with the help of neat functional block diagram. **(08 Marks)**

Module-2

3 a. Describe angle modulation. **(06 Marks)**

b. Explain the generation of frequency modulated wave using indirect method. **(08 Marks)**

c. The carrier swing of a FM signal 70kHz and the modulating signal is a 7kHz sine wave. Determine the modulation index of FM signal. **(02 Marks)**

OR

4 a. Explain the working of PLL and obtain the modulating signal by using linear model of PLL. **(08 Marks)**

b. Explain the working of a superheterodyne receiver using block diagram. **(08 Marks)**

Module-3

5 a. Describe Mean, Correlation and Covariance functions with respect to stationary random process. **(08 Marks)**

b. Explain the properties of auto correlation function and power spectral density. **(08 Marks)**

OR

6 a. Discuss thermal noise in detail. **(06 Marks)**

b. An amplifier operating over the frequency range from 450 to 460kHz has a 100KΩ input resistor. What is the rms noise voltage at the input to this amplifier if the ambient temperature is 17°C? Also calculate noise power and power spectral density. **(04 Marks)**

c. What is white noise? Plot power spectral density and auto correlation function of white noise. **(06 Marks)**

Module-4

7 a. In any receiver how the noise is produced? Explain. **(06 Marks)**

b. Derive the equation for the signal to noise ratio at the output of DSBSC receiver. **(06 Marks)**

c. An AM receiver operating with a sinusoidal wave and 80% modulation ahs an output signal to noise ratio of 30dB. Calculate the corresponding carrier to noise ratio. **(04 Marks)**

OR

8 a. Discuss about threshold effect in FM receiving system. **(06 Marks)**

b. Derive the equation for figure of merit at the output of the FM receiver. **(10 Marks)**

Module-5

9 a. State the sampling theorem. Explain sampling theorem in frequency domain. **(06 Marks)**

b. Explain the generation of PAM. State its advantages, disadvantages and application. **(10 Marks)**

OR

10 a. With the neat block diagram, explain the generation and reconstruction of PCM signals. **(06 Marks)**

b. Derive an expression for quantization error and signal to quantization noise ratio for non-sinusoidal PCM signals. **(06 Marks)**

c. Write a short note on VOCODER. **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC32

Third Semester B.E. Degree Examination, July/August 2021
Network Theory

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Find the equivalent resistance Rab for circuit in Fig. Q1 (a) and use it to find i. **(06 Marks)**

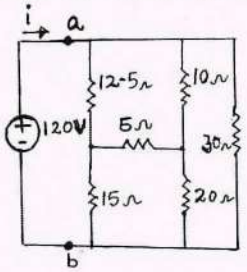


Fig. Q1 (a)

b. Determine power supplied by the dependent source of Fig. Q1 (b), using nodal analysis. **(06 Marks)**

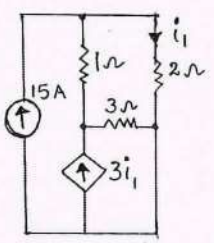


Fig. Q1 (b)

c. Determine current through 2 Ω resistor of Fig. Q1 (c) using mesh analysis. **(08 Marks)**

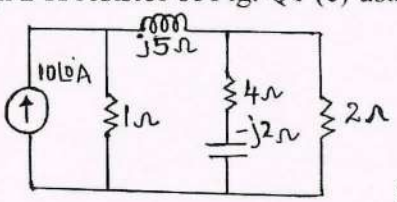


Fig. Q1 (c)

2 a. Using source transformation and source shifting techniques, find voltage across 2 Ω resistor in Fig. Q2 (a). **(06 Marks)**

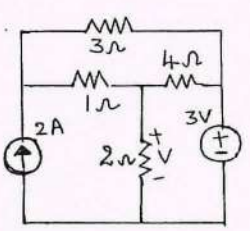


Fig. Q2 (a)

b. Find I_1, I_2, I_3 in the circuit of Fig. Q2 (b) using mesh analysis. **(06 Marks)**

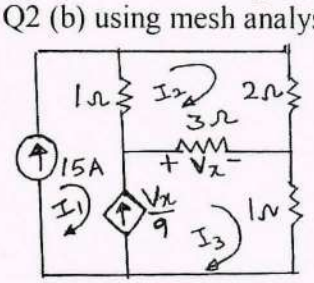


Fig. Q2 (b)

c. Compute V_1, V_2 in the circuit of Fig. Q2 (c) using nodal analysis. **(08 Marks)**

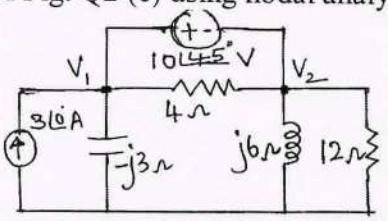


Fig. Q2 (c)

3 a. For the circuit in Fig. Q3 (a), use the superposition theorem to find I. **(06 Marks)**

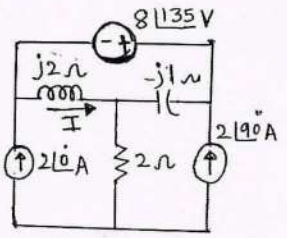


Fig. Q3 (a)

b. Using Norton's theorem, find current through 5 Ω resistor in Fig. Q3 (b). **(06 Marks)**

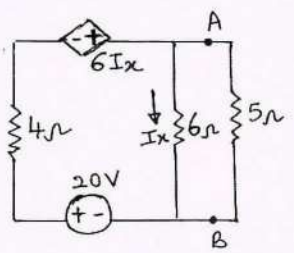


Fig. Q3 (b)

c. State Millman's theorem, using Millman's theorem find I_L in Fig. Q3 (c). **(08 Marks)**

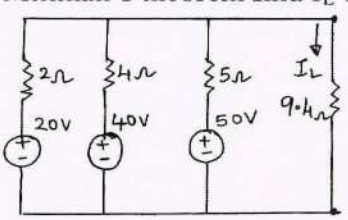


Fig. Q3 (c)

4 a. Determine the Thevenin equivalent at terminals A-B of the circuit in Fig. Q4 (a). **(06 Marks)**

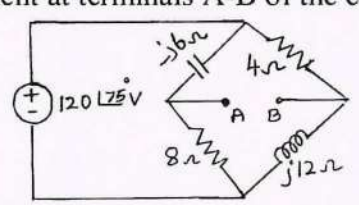


Fig. Q4 (a)

b. Compute the value of R that results in maximum power transfer to it in Fig. Q4 (b). Find the maximum power. **(06 Marks)**

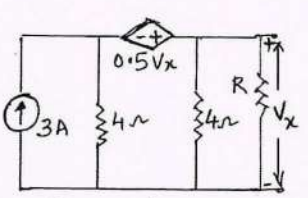


Fig. Q4 (b)

c. State Reciprocity theorem. Find V_x and verify Reciprocity theorem for circuit in Fig. Q4 (c). **(08 Marks)**

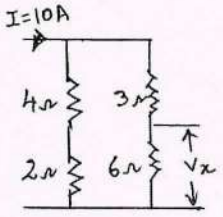


Fig. Q4 (c)

5 a. In the network shown in Fig. Q5 (a), the switch K is opened at t = 0. Solve for the values of V, $\frac{dV}{dt}$ and $\frac{d^2V}{dt^2}$ at $t = 0^+$. **(10 Marks)**

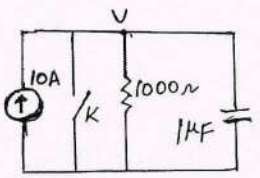


Fig. Q5 (a)

b. In the network shown in Fig. Q5 (b), a steady state is reached with the switch K open. At t = 0 switch K is closed. Solve for the values of I_1, I_2, V_C, $\frac{dI_1}{dt}$, $\frac{dI_2}{dt}$ at $t = 0^+$. **(10 Marks)**

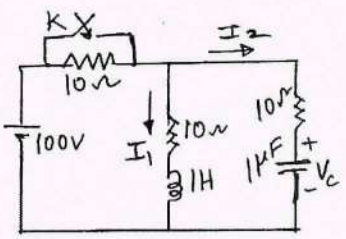


Fig. Q5 (b)

6 a. In the network shown in Fig.6(a), K is changed from position a to b at t = 0. Solve for i, $\frac{di}{dt}$, $\frac{d^2i}{dt^2}$ at $t = 0^+$, The steady state having reached before switching. **(10 Marks)**

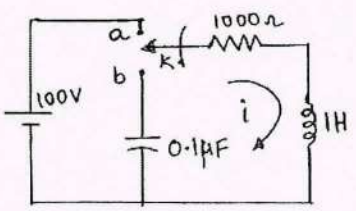


Fig. Q6 (a)

b. In the network of Fig. Q6(b), the switch K is closed at t = 0 with zero capacitor voltage and zero inductor current. Solve for (a) V_1 and V_2 at $t = 0^+$ (b) V_1 and V_2 at $t = \infty$, (c) $\frac{dV_1}{dt}$ and $\frac{dV_2}{dt}$ at $t = 0^+$, (d) $\frac{d^2V_2}{dt^2}$ at $t = 0^+$. **(10 Marks)**

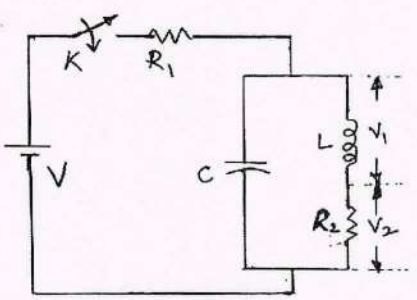


Fig. Q6 (b)

7 a. In the circuit given in the Fig. Q7 (a) switch is closed on position 1 at t = 0 and at t = 500 μs, switch is moved to position 2. Obtain the equation of current in both intervals. Use Laplace transforms. **(10 Marks)**

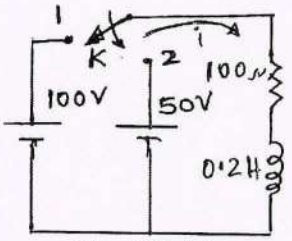


Fig. Q7 (a)

b. Determine the Laplace transform of the periodic sawtooth waveform, as shown in Fig. Q7 (b). **(10 Marks)**

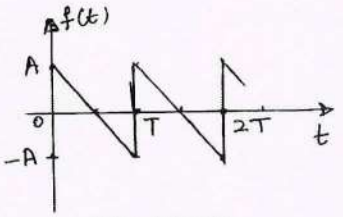


Fig. Q7 (b)

8 a. A voltage pulse, of unit height and width T is applied to the circuit in the Fig. Q8 (a) at t = 0. Determine the voltage across the capacitance C as a function of time. **(10 Marks)**

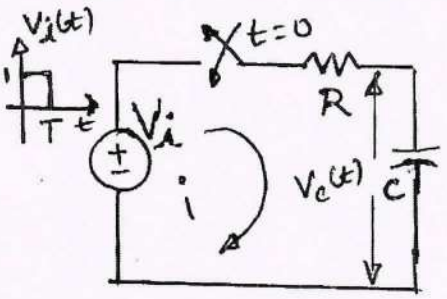


Fig. Q8 (a)

b. Determine the Laplace transform of waveform given in Fig. Q8 (b). **(10 Marks)**

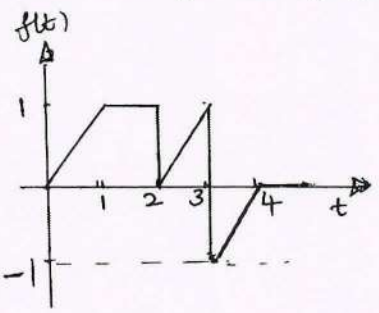


Fig. Q8 (b)

9 a. With respect to series resonant circuit, show that resonant frequency is equal to the geometric mean of two half power frequencies. **(08 Marks)**

b. A series resonant circuit includes 1 μF capacitor, resistance of 16 Ω and an inductance of L henry. If the bandwidth is 500 rad/sec, determine (i) ω_r (ii) Q (iii) L. **(06 Marks)**

c. Find the value of L for which the circuit resonates at a frequency of 1000 rad/sec for the circuit in the Fig. Q9 (c). **(06 Marks)**

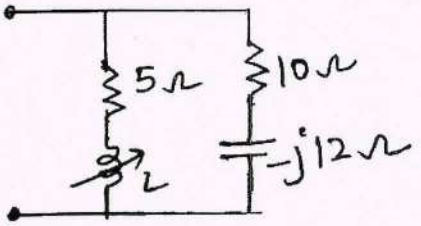


Fig. Q9 (c)

10 a. Derive Z-parameters in terms of hybrid parameters. **(08 Marks)**

b. Determine the Z-parameters of the network shown in Fig. Q10 (b). **(06 Marks)**

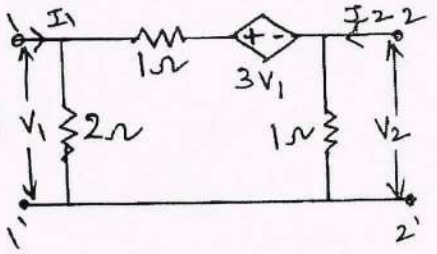


Fig. Q10 (b)

c. For the network shown in Fig. Q10 (c), find the Y parameters. **(06 Marks)**

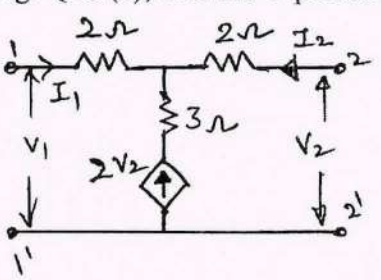


Fig. Q10 (c)

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC33

Third Semester B.E. Degree Examination, July/August 2021
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. What are the different types of Bonding Forces in solids and explain any one. **(06 Marks)**
b. Draw the typical band structures at OK for insulator, semiconductor and metal and explain it. **(06 Marks)**
c. With mathematical equations, describe the hall effect. **(08 Marks)**

2 a. Explain Electron-hole pair in a semiconductor with the help of the graph. **(06 Marks)**
b. Explain the effects of temperature and doping on mobility. **(06 Marks)**
c. Describe the drift of electrons and holes in a semiconductor bar. **(08 Marks)**

3 a. Draw the I-V characteristic of a Pn-junction with current equation under equilibrium, forward and reverse bias and explain it. **(06 Marks)**
b. Explain the concept of Zener breakdown with energy band diagram. **(06 Marks)**
c. Explain the solar cells with structures. **(08 Marks)**

4 a. Draw the piece wise linear approximations of junction diode characteristics for ideal diode, ideal diode with offset voltage and ideal diode with offset voltage and resistance. **(06 Marks)**
b. Draw the schematic representation of a P-i-n photodiode and explain it. **(06 Marks)**
c. Explain the Avalanche Breakdown with energy diagram. **(08 Marks)**

5 a. Explain the working of P-n-P device and also draw the curve of I_C versus V_{BC}. **(06 Marks)**
b. Describe the various mechanisms of a switching cycle of a PnP transistor. **(06 Marks)**
c. Write the step-by-step fabrication of a BJT with diagrams. **(08 Marks)**

6 a. Define the following parameters:
i) Emitter injection efficiency
ii) Current transfer ratio
iii) Base to collector current amplification factor. **(06 Marks)**
b. Draw the simple switching circuit of PnP transistor and explain it. **(06 Marks)**
c. Discuss Base Narrowing in PnP transistor. **(08 Marks)**

7 a. Explain the operation of a basic Pn JFET for different gate voltage. **(10 Marks)**
b. Draw the small signal equivalent circuit of JFET and explain it. **(10 Marks)**

8 a. Draw the energy band diagram of an two terminal MOS capacitor with a P-type substrate for a negative gate bias and a moderate positive gate bias and explain it. **(10 Marks)**
b. Explain the structure of n-channel enhancement mode and depletion mode MOSFET. **(10 Marks)**

9 a. Describe the Rapid thermal processing with the help of diagram. **(10 Marks)**
b. Explain the method of ION implementation with schematic diagram. **(10 Marks)**

10 a. What are the types of integrated circuits and explain it. **(06 Marks)**
b. Mention the Advantages of Integration. **(06 Marks)**
c. With input and output waveforms, explain the working of CMOS inverter. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, July/August 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Define combinational logic circuit and place the following equation into the proper canonical form:
$P = f(a, b, c) = ab' + ac' + bc$ **(04 Marks)**

b. Obtain minimal expression using k-map for the following incompletely specified function:
$F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw the circuit diagram using basic gates. **(06 Marks)**

c. Minimize the expression using Quine Mecluskey method.
$Y = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + A\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D}$ **(10 Marks)**

2 a. Place the following equations into the proper canonical form:
i) $G = f(w, x, y, z) = \overline{w}x + y\overline{z}$
ii) $T = f(a, b, c) = (a + \overline{b})(\overline{b} + c)$ **(04 Marks)**

b. Obtain minimal logical expression for the given maxterm expression using K-map $f(a, b, c, d) = \pi M(0, 1, 4, 5, 6, 7, 9, 14) . \pi d(13, 15)$. **(06 Marks)**

c. Obtain all the prime implicants of the following Boolean function using Quine-Meckluskey method
$f(a, b, c, d) = \sum(0, 2, 3, 5, 8, 10, 11)$. Verify the result using K map technique. **(10 Marks)**

3 a. Draw the circuit for 3 to 8 decoder and explain. **(08 Marks)**

b. Implement the following Boolean function using 4:1 multiplexer.
$F[A, B, C, D] = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. **(06 Marks)**

c. A combinational circuit is defined by the functions $F_1 = \sum m(3, 5, 7)$, $F_2 = \sum m(4, 5, 7)$. Implement the circuit with a programmable logic array having 3 inputs, 3 product terms and two outputs. **(06 Marks)**

4 a. Draw the key pad interfacing diagram to a digital system using 10-line decimal to BCD encoder and explain. **(06 Marks)**

b. Explain Look-Ahead carry adder with neat diagram and relevant expression. **(06 Marks)**

c. Design 2-bit comparator using gates. **(08 Marks)**

5 a. Explain the operation of a switch debouncer using S-R. Latch with the help of circuit and waveforms. **(06 Marks)**

b. Find characteristic equations for S-R and T. Flip flops with the help of function tables and explain. **(06 Marks)**

c. Explain the working principle of 4-bit synchronous binary counts. **(08 Marks)**

6 a. Draw the logic diagram, functional table and timing diagram of master-slave JK flip flop and explain briefly. **(10 Marks)**

b. Explain four bit binary ripple counter with logic and timing diagram. **(10 Marks)**

7 a. Design mod-6 synchronous counter by using JK flip-flop, with excitation table. **(10 Marks)**

b. Draw and explain Mealy and Moore sequential circuit model and compare mealy and Moore circuit models. **(10 Marks)**

8 a. Design a Mod-6 synchronous counter using clocked T Flip-Flop. **(10 Marks)**

b. Construct the transition table, state table and state diagram for the sequential circuit shown in Fig.Q.8(b). **(10 Marks)**

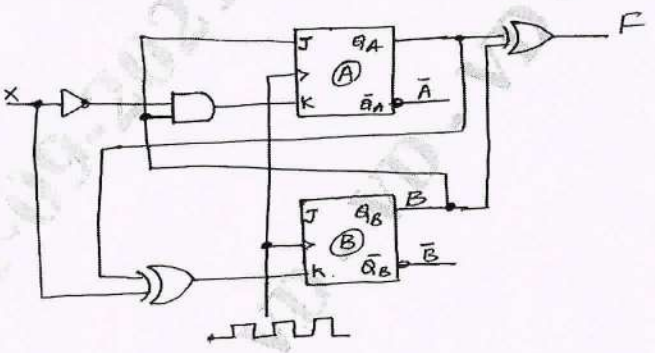


Fig.Q.8(b)

9 a. Design and draw Mealy model of sequential detector circuit to detect the pattern 101. **(10 Marks)**

b. Draw the block diagram of serial adder with accumulator and explain its working operation. **(10 Marks)**

10 a. State the guidelines for construction of state graph. **(06 Marks)**

b. Draw the block diagram of binary multiplier and explain its working principle. **(08 Marks)**

c. Draw and explain the operation of FPGA implementation of a parallel adder with accumulator. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC35

Third Semester B.E. Degree Examination, July/August 2021
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Explain following registers: (i) PC (ii) IR (iii) MAR **(06 Marks)**
b. Explain how user program and OS routine are sharing processor with printer. **(08 Marks)**
c. Explain basic performance equation. **(06 Marks)**

2 a. Perform using 2's complement arithmetic: (i) −5 + (−2) (ii) Subtract −5 from −7 **(06 Marks)**
b. Explain BIG-ENDIAN and LITTLE-ENDIAN assignment. **(06 Marks)**
c. Illustrate instruction execution and straight line sequencing for the program C ←[A] + [B]. [Assume that each instruction is 4 byte]. **(08 Marks)**

3 a. List the generic addressing modes with assembler syntax and addressing function. **(10 Marks)**
b. Explain shift and any two rotate instructions with relevant diagrams. **(10 Marks)**

4 a. Write assembly language program to add 'N' numbers and store the result in 'SUM'. Assume the following address:
(i) Program should start from '100'.
(ii) 'N' is stored at 204
(iii) Numbers are stored in memory from the address 208. Each number is 4 bytes.
(iv) 'SUM' is stored at 200
(v) Assume each instruction is 4 byte **(08 Marks)**
b. Explain stack concept with relevant diagrams. **(08 Marks)**
c. List the steps involved in 'CALL' and 'RETURN' instructions. **(04 Marks)**

5 a. Explain I/O interface for input device and also write the assembly program that reads the one LINE from the keyboard and echoes it back to the display. **(10 Marks)**
b. Explain methods used for enabling and disabling interrupts. **(10 Marks)**

6 a. Explain daisy chain method used for handling simultaneous interrupt request. **(06 Marks)**
b. Explain memory mapped I/O access. **(06 Marks)**
c. Explain use of DMA controller in computer system. **(08 Marks)**

7 a. Calculate number of address lines required to access following memory:
(i) 64 KB (ii) 512 MB (iii) 256 KB (iv) 8 GB **(04 Marks)**
b. Explain internal organization of 2M × 8 dynamic memory chip. **(08 Marks)**
c. Explain different types of nonvolatile memory. **(08 Marks)**

8 a. Explain cache memory and its relevant terms. **(08 Marks)**
b. Explain virtual memory organization. **(06 Marks)**
c. Explain magnetic disk principles. **(06 Marks)**

9 a. Explain single bus organization of the data path inside a processor. **(10 Marks)**
b. List the steps involved in memory read operation and also draw corresponding timing diagram. **(10 Marks)**

10 a. Write the control sequence for execution of the instruction Add (R_3), R_1. **(06 Marks)**
b. Explain block diagram of a complete processor. **(06 Marks)**
c. Explain micro programmed control concept. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18EC36

Third Semester B.E. Degree Examination, July/August 2021
Power Electronics and Instrumentation

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Briefly explain power electronic system with neat block diagram. **(04 Marks)**
b. Mention and explain the different types of power electronic converters and mention their any two applications. **(08 Marks)**
c. Explain an operation of resistance firing circuit with neat waveforms. **(08 Marks)**

2 a. Explain with a neat circuit diagram VI characteristics of SCR, define the latching current, break over voltage and holding current. **(08 Marks)**
b. Explain briefly about the gate triggering circuits with waveforms. **(08 Marks)**
c. Explain with a neat circuit diagram basic operation of uJT. **(04 Marks)**

3 a. Explain with neat waveforms phase angle control and PWM control. **(09 Marks)**
b. Explain briefly how choppers are classified. **(06 Marks)**
c. A DC chopper circuit connected to a 100V DC source supplies an inductive load having 40mH in series with a resistance of 5Ω. A freewheeling diode is placed across the load. The load current varies between the limits of 10A and 12A. Determine the time ratio of the chopper. **(05 Marks)**

4 a. Explain the working principle of stepdown chopper with neat circuit diagram and waveforms. And drive the equations for rms voltage and current. **(10 Marks)**
b. With necessary waveforms explain the operation of a single phase half wave controller with inductive load. Derive the expression for average load voltage. **(10 Marks)**

5 a. How inverters are classified. **(04 Marks)**
b. With a neat circuit diagram and waveforms explain the operation of single phase half bridge inverter with resistive load. **(08 Marks)**
c. A basic D'Arsonval movement with an internal resistance of 50Ω and a full scale deflection current of 2mA is to be used as a multi range voltmeter. Determine the series resistance to obtain the voltage ranges of D-10V, 0-50V, 0-100V. **(08 Marks)**

6 a. Briefly explain the discontinuous mode fly back converter. **(10 Marks)**
b. What are the different types of static characteristics and define each term. **(10 Marks)**

7 a. Draw the block diagram and explain the working principle of dual slope integrating type DVM. **(08 Marks)**
b. Explain the working principle of digital frequency meter with basic circuit. **(06 Marks)**
c. Derive an balance bridge equation for wheat stone's bridge. **(06 Marks)**

8 a. With help of staircase waveform and block diagram explain the working of staircase ramp-type voltmeter. **(06 Marks)**
b. With block diagram, explain the time base selector. **(06 Marks)**
c. Derive an equation for unbalanced wheat stone's bridge. **(08 Marks)**

9 a. Write a brief note on potentiometer type resistive transducer. **(06 Marks)**
b. Explain the working of analog weight scale. **(06 Marks)**
c. With a neat diagrams, explain the PLC structure. **(08 Marks)**

10 a. With a neat sketch, explain construction and working of LVDT. **(10 Marks)**
b. Write a note on PLC operation and relays. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC33

Third Semester B.E. Degree Examination, July/August 2021
Analog Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Mention the steps involved for obtaining the AC equivalent of a transistor network. **(04 Marks)**

b. Derive an expressions for input impedance, output impedance and voltage gain for CE fixed bias configuration using re equivalent model. **(08 Marks)**

c. Define hybrid parameters and explain hybrid π model with neat sketch. **(08 Marks)**

2 a. Draw the circuit diagrams, for transistor r_e model in common Emitter and common base configuration. **(04 Marks)**

b. Derive expressions for Z_i, Z_0, A_V and A_i for emitter follower configuration using approximate hybrid equivalent model. **(08 Marks)**

c. For the network shown in Fig.Q2(c), without C_E(unbypassed), determine r_e, Z_i, Z_0 and A_v.

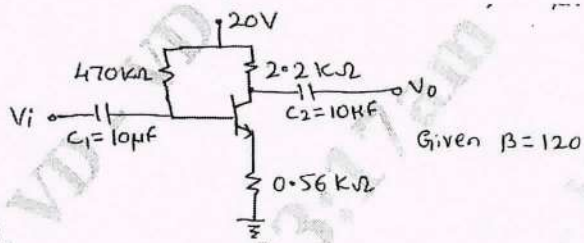


Fig.Q2(c) **(08 Marks)**

3 a. Mention the differences between JFET and MOSFET. **(04 Marks)**

b. Explain with neat sketches operation and characteristics of n-channel enhancement MOSFET. **(08 Marks)**

c. Find r_d, Z_i, Z_0, and A_V for the circuit shown in Fig.Q3(c).

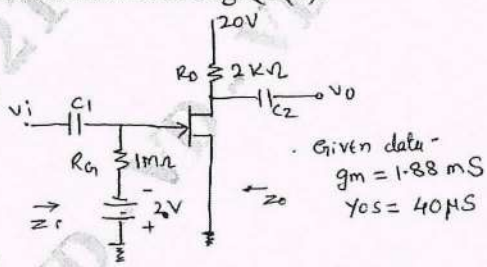


Fig.Q3(c) **(08 Marks)**

4 a. Sketch the following circuit diagrams :
i) JFET AC equivalent model of source follower ii) Cascaded FET amplifier. **(04 Marks)**

b. Derive an expressions for Z_i, Z_0, and A_V using small signal JFET amplifier for self bias configuration (Bypassed Rs). **(08 Marks)**

c. For the source follower network shown in Fig.Q4(c), determine : i) r_d ii) Z_i iii) Z_0 iv) A_V.

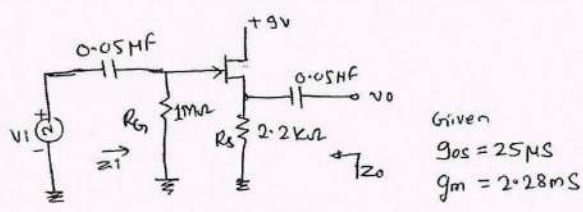


Fig.Q4(c) **(08 Marks)**

5 a. An amplifier rated at a 40W output is connected to a 10 Ω speaker find :
i) Input power required for full output if power gain is 25dB
ii) Input voltage for rated output if the amplifier voltage gain is 40dB. **(06 Marks)**

b. Explain high frequency response of JEFT amplifiers. **(08 Marks)**

c. Explain multistage frequency effects. **(06 Marks)**

6 a. Derive an expressions for Miller input and output capacitors. **(06 Marks)**

b. Determine r_e, A_V and R_i for the low frequency response of BJT amplifier circuit shown in Fig.Q6(b). Assume $r_0 = \infty$.

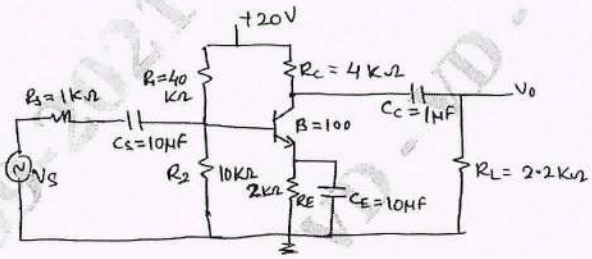


Fig.Q6(b) **(08 Marks)**

c. Draw the circuit diagram of :
i) High frequency response of BJT amplifier in CE mode with capacitances effects
ii) Low frequency response of FET amplifier in common source mode with capacitive elements effects. **(06 Marks)**

7 a. List the conditions for sustained oscillations. **(04 Marks)**

b. Explain with neat circuit diagram, series resonant crystal oscillator using BJT. **(08 Marks)**

c. Design the RC elements of a Wein bridge oscillator for the operation at f = 10KHz and draw the oscillator circuit using op-Amp. **(08 Marks)**

8 a. Explain effect of negative feedback on gain and Bandwidth. **(05 Marks)**

b. Explain with neat circuit diagram, the operation of BJT Colpitt oscillator and mention its advantages over Hartely oscillator. **(08 Marks)**

c. Explain UJT relaxation oscillator with necessary equations and waveforms. **(07 Marks)**

9 a. Classify the power amplifiers and define them with necessary waveforms and 'Q' point. **(06 Marks)**

b. Explain series transistor voltage regulator with neat diagram. **(06 Marks)**

c. Calculate input power, output power and efficiency of the series fed class A power amplifier circuit shown in Fig.Q9(c).

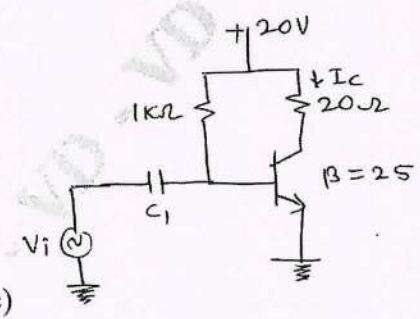


Fig.Q9(c) **(08 Marks)**

10 a. Define : i) Cross over distortion ii) percentage voltage regulation iii) amplifier efficiency iv) harmonic distortion v) voltage regulator. **(10 Marks)**

b. Explain transformer coupled class A power amplifier with necessary equations. **(06 Marks)**

c. For class 'B' amplifier using a supply of V_{CC} = 30V and driving a load of 16Ω, determine maximum input power and output power. **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC34

Third Semester B.E. Degree Examination, July/August 2021
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Define the following with an example: (i) Sum of products (ii) Product of sums (iii) Canonical sum of products (iv) Canonical product of sums (v) Minterm. **(10 Marks)**

b. Obtain the minimal logical expression for the given minterm using K-map.
$T = f(a,b,c,d,e) = \sum(0,2,8,10,16,18,24,26)$ **(05 Marks)**

c. Simplify the following maxterm expression using K-map:
A= f(w, x, y, z) = π(2, 3, 8, 9, 10, 11, 12, 13, 14, 15) **(05 Marks)**

2 a. Simplify the following using Quine-McClusky minimization technique and also verify the same.
$D = f(a,b,c,d) = \sum(0,1,2,3,6,7,8,9,14,15)$ **(10 Marks)**

b. Express the following SOP equations in the form of minterms:
(i) $G = f(A,B,C) = A'BC + A'B'C + ABC$
(ii) $P = f(w,x,y,z) = wxyz' + wx'yz' + w'xyz' + w'x'yz'$ **(04 Marks)**

c. Place the following equations into proper canonical form:
(i) $P = f(a,b,c) = ab' + ac' + bc$
(ii) $T = f(a,b,c) = (a + b')(b' + c)$ **(06 Marks)**

3 a. Define : (i) Subtractors (ii) Binary comparators (iii) Full Adder **(06 Marks)**

b. Realize the following using 745151 8 : 1 MUX :
(i) $F = f(x,y,z) = \sum(1,2,4,5,7)$
(ii) $T = f(w,x,y,z) = \sum(0,1,2,4,5,7,8,9,12,13)$ **(06 Marks)**

c. Write the truth table of two-bit magnitude comparator. Write the K-map for each Output of two-bit magnitude comparator and the resulting equation. **(08 Marks)**

4 a. Design a 4-to-16 Decoder using two 74XX138 decoders. **(05 Marks)**

b. With a neat diagram, explain carry look ahead adder. **(10 Marks)**

c. Distinguish between decoder and encoder. Implement full adder using IC74153. **(05 Marks)**

5 a. Explain Master Slave JK flip-flop with the help of timing diagram and waveforms. **(08 Marks)**

b. Find the characteristic equation of T and SR flip-flops with the help of functional tables. **(06 Marks)**

c. With a neat diagram, explain positive edge triggered D-flip flop and explain for different input conditions. **(06 Marks)**

6 a. Explain the operation of switch debouncer built using SR latch with the help of waveforms. **(04 Marks)**

b. What is a flip-flop? Discuss the working principle of Master Slave SR f/f with the help of timing diagram and truth table. **(08 Marks)**

c. Define : (i) Propagation delay (ii) Minimum pulse width (iii) Setup time and (iv) Hold time **(08 Marks)**

7 a. Design a mod-6 synchronous counter using clocked D flip flop. **(08 Marks)**

b. Explain SIPO and SISO using flip flop. **(06 Marks)**

c. Design synchronous mod-6 counter using clocked JK flip flops. **(06 Marks)**

8 a. Explain mod-8 and mod-7 twisted ring counter with a neat diagram and counting sequence. **(08 Marks)**

b. Explain 4-bit binary ripple counter with logic diagram, timing diagram and counting sequence. **(08 Marks)**

c. Explain mod-4 ring counter with logic diagram and counting sequence. **(04 Marks)**

9 a. Explain Kealy and Moore sequential circuit model with neat diagrams. **(06 Marks)**

b. Define : (i) Input variable (ii) Output variable (iii) State variable and (iv) State. **(04 Marks)**

c. Give Mealy state notation, Moore circuit notation and Mealy and Moore mixed circuit diagram notation for JK flip flop. **(10 Marks)**

10 a. Give the steps for analyzing the function of a sequential circuit. **(04 Marks)**

b. Explain JK flip flop characteristic table excitation table with K-maps for excitation variables. **(10 Marks)**

c. Explain the excitation realization for T and D-flip-flops. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC35

Third Semester B.E. Degree Examination, July/August 2021
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Using source transformation techniques, find 'v' for the circuit in Fig.Q1(a).

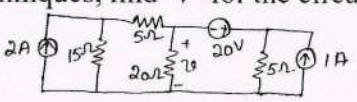


Fig.Q1(a) **(07 Marks)**

b. Obtain equivalent resistance R_{ab} for the circuit in Fig.Q1(b) and hence find 'i'.

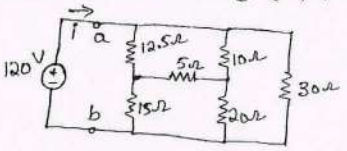


Fig.Q1(b) **(07 Marks)**

c. Explain ideal and practical current sources. **(06 Marks)**

2 a. Determine the current I_0 in the circuit of Fig.Q2(a) using Mesh analysis.

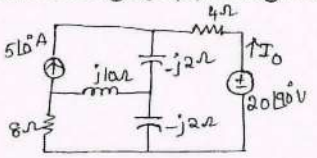


Fig.Q2(a) **(08 Marks)**

b. Use nodal analysis to find v_0 in the network of Fig.Q2(b).

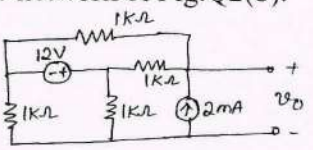


Fig.Q2(b) **(08 Marks)**

c. Explain the concept of super node with an illustration. **(04 Marks)**

3 a. State and prove Reciprocity theorem. **(06 Marks)**

b. Use superposition theorem to find i_0 in the circuit shown in Fig.Q3(b).

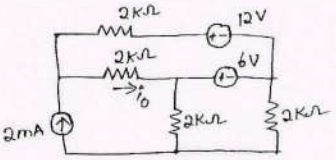


Fig.Q3(b) **(06 Marks)**

c. Find Thevenin's equivalent circuit across the terminals a – b for the circuit shown in Fig.Q3(c). **(08 Marks)**

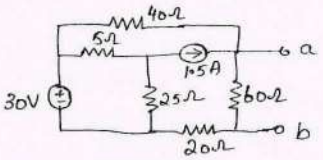


Fig.Q3(c)

4 a. State and prove maximum power transfer theorem for the case of AC source, hence show that $\rho_{max} = \frac{|V_{TH}|^2}{8R_L}$ **(08 Marks)**

b. Find the current through 16 Ω resistor using Norton's theorem in Fig.Q4(b).

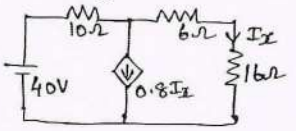


Fig.Q4(b) **(08 Marks)**

c. Find the current through (10 – 3j)Ω using Millman's theorem in Fig.Q4(c). **(04 Marks)**

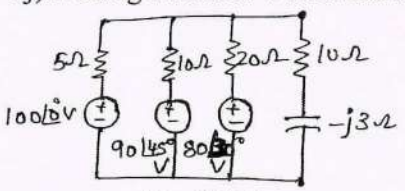


Fig.Q4(c)

5 a. The switch 'K' is changed from position 1 to position 2 at t = 0. Steady state condition having been reached at position 1. Find the values of i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$. [Refer Fig.Q5(a)] **(06 Marks)**

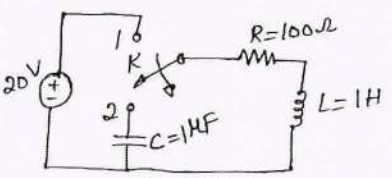


Fig.Q5(a)

b. In the network shown in Fig.Q5(b), $V_1(t) = e^{-t}$ for $t \geq 0$ and is zero for all $t < 0$. If the capacitor is initially uncharged. Determine the value of $\frac{d^2v_2}{dt^2}$ and $\frac{d^3v_2}{dt^3}$ at $t = 0^+$.

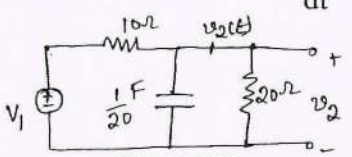


Fig.Q5(b) **(08 Marks)**

c. Explain initial and final conditions in case of a capacitor. **(06 Marks)**

6 a. For the circuit shown in Fig.Q6(a),
(i) Find the differential equation for $i_L(t)$
(ii) Find Laplace transform of $i_L(t)$
(iii) Solve for $i_L(t)$

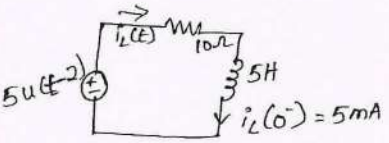


Fig.Q6(a) **(08 Marks)**

b. For the circuit shown in Fig.Q6(b), (i) Find the differential equation for $i_L(t)$, (ii) Find Laplace transform of $i_c(t)$, (iii) Solve for $i_L(t)$. **(08 Marks)**

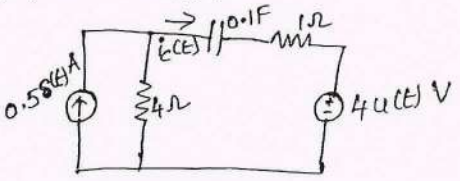


Fig.Q6(b)

c. Obtain Laplace transform for a decaying exponential signal. **(04 Marks)**

7 a. Prove that the resonant frequency is the geometric mean of the two half power frequencies i.e., Show that $\omega_0 = \sqrt{\omega_1 \omega_2}$ **(08 Marks)**

b. Obtain an expression for quality factor of an capacitor. **(07 Marks)**

c. In a series circuit, R = 6 Ω, $\omega_0 = 4.1 \times 10^6$ rad/sec, bandwidth = 10^5 rad/sec. Compute L, C half power frequencies and Q. **(05 Marks)**

8 a. Obtain an expression for the resonant frequency in a parallel resonant circuit. **(08 Marks)**

b. Show that a two branch parallel resonant circuit is resonant at all frequencies when

$$R_L = R_C = \sqrt{\frac{L}{C}}$$ **(07 Marks)**

c. Find the value of R_L for which the circuit is at resonance, as shown in Fig.Q8(c). **(05 Marks)**

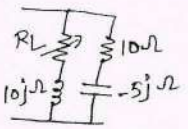


Fig.Q8(c)

9 a. Obtain an expression for h-parameters in terms of Z-parameters. **(08 Marks)**

b. Find Z and Y parameters for the network shown in Fig.Q9(b). **(08 Marks)**

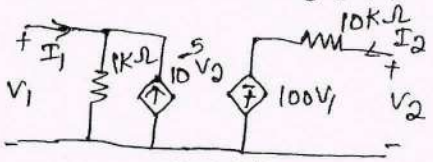


Fig.Q9(b)

c. Explain ABCD parameters. **(04 Marks)**

10 a. Obtain an expression for Y-parameters in terms of ABCD parameters. **(08 Marks)**

b. Find ABCD parameters for the network shown in Fig.Q10(b).

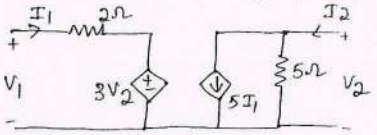


Fig.Q10(b) **(08 Marks)**

c. State reciprocity condition for
(i) Z – parameters
(ii) Y – parameters
(iii) h – parameters
(iv) ABCD – parameters **(04 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC36

Third Semester B.E. Degree Examination, July/August 2021
Engineering Electromagnetics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. State and explain Coulomb's law in vector form. **(06 Marks)**

b. Point charge $Q_1 = 300\ \mu c$ located at (1, –1, 3) experiences a force $F = 8a_x - 8a_y - 4a_z$ N due to charge Q_2 at (3, –3, 2). Find Q_2. **(06 Marks)**

c. Find the total charge within the volume indicated:

i) $\rho_v = 10z^2e^{-0.1x}\sin\pi y, \quad 1 \le x \le 2; \quad 0 \le y \le 1; \quad 3 \le z \le 3.6$

ii) $\rho_v = 4xyz^2, \quad 0 \le \rho \le 2; \quad 0 \le \phi \le \frac{\pi}{2}; \quad 0 \le z \le 3$ **(08 Marks)**

2 a. Derive the expression for electric field intensity 'E' at any point due to uniform line charge of density ρ_ℓ c/m. **(07 Marks)**

b. Two uniform surface charge densities of density ρ_s c/m^2 are located at x = ±4m. Determine the electric field at all the points. **(06 Marks)**

c. Given $D = 5x^2a_x + 10za_z$ c/m^2, find the net outward flux for the surface of a cube of 2m on an edge centered at origin. The edges of the cube are parallel to coordinate axes. **(07 Marks)**

3 a. State and prove Gauss law in integral form. **(06 Marks)**

b. Find the numerical value of Divergence of D at the point indicated if:

(i) $D = 20xy^2(z+1)a_x + 20x^2y(z+1)a_y + 10x^2y^2a_z$ c/m^2 at $P_A(0.3, 0.4, 0.5)$

(ii) $D = 4\rho z\sin\phi a_\rho + 2\rho z\cos\phi a_\phi + 2\rho^2\sin\phi a_z$ c/m^2 at $P_B\left(1, \frac{\pi}{2}, 2\right)$ **(06 Marks)**

c. Given $D = \left(\frac{5r^2}{4}a_r\right)$ c/m^2 in spherical coordinates evaluate both sides of divergence theorem for the volume enclosed between r = 1 m and r = 2 m. **(08 Marks)**

4 a. Define scalar electric potential. Derive the expression for potential due to a point charge. **(06 Marks)**

b. Find the work done in moving a 5 μc point charge from origin to p(2, –1, 4) through the field $E = 2xyza_x + x^2za_y + x^2ya_z$ V/m via the path:

(i) Straight line segments (0, 0, 0) to (2, 0, 0) to (2, –1, 0) to (2, –1, 4)

(ii) Straight line x = –2y; z = 2x **(08 Marks)**

c. Given $V = 50x^2yz + 20y^2$ v in free space,

(i) Find voltage at P(1, 2, –3)

(ii) Field strength E at P. **(06 Marks)**

5 a. Using Laplace equation derive the expression for capacitance of a co-axial cylindrical capacitor. The boundary conditions are $V = V_0$ at ρ = a and V = 0 at ρ = b, b > a. **(10 Marks)**

b. In spherical coordinates V = 865 V at r = 50 cm and E = 748.2 a_r V/m at r = 85 cm. Determine the location of voltage reference if the potential depends only on 'r'. **(10 Marks)**

6 a. State and explain Biot-Savart's law. **(05 Marks)**

b. Find 'H' at origin due to an infinite conductor carrying a current of 5A in a_y direction and located at x = 2 and z = –2. **(07 Marks)**

c. Given $H = \frac{x+2y}{z^2}a_y + \frac{2}{z}a_z$ A/m, find J. Find total current passing through z = 4; $1 \le x \le 2$; $3 \le y \le 5$. **(08 Marks)**

7 a. The point charge Q = 18 nc has a velocity of 5×10^6 m/s in the direction $a_v = 0.60a_x + 0.75a_y + 0.30a_z$. Calculate the magnitude of force exerted on the charge by:

(i) $B = -3a_x + 4a_y + 6a_z$ mT (ii) $E = -3a_x + 4a_y + 6a_z$ KV/m **(06 Marks)**

b. Derive the expression for the force on a differential current element moving through a steady magnetic field. **(08 Marks)**

c. The field $B = -2a_x + 3a_y + 4a_z$ mT is present in free space. Find vector force exerted on a straight wire carrying 12 A in a_{AB} direction, given A(1, 1, 1) and (i) B(2, 1, 1) (ii) B(3, 5, 6). **(06 Marks)**

8 a. Define Magnetization. Given a ferrite material which is operating in a linear mode with B = 0.05 T and $\mu_r = 50$. Calculate χ_m, M and H. **(06 Marks)**

b. Derive the boundary conditions for magnetic fields B, H and M for the interface between the different magnetic media. **(07 Marks)**

c. Let $\mu_1 = 4$ μH/m in region 1 where z > 0 while $\mu_2 = 7$ μH/m in region 2 where z < 0, $K = 80\,a_x$ A/m on the surface z = 0. If $B_1 = 2a_x - 3a_y + a_z$ mT in region 1, find B_2. **(07 Marks)**

9 a. An area of 0.65 m^2 in z = 0 plane is enclosed by a filamentary conductor. Find the induced voltage given $B = 0.05\cos 10^3 t\left[\frac{a_y + a_z}{\sqrt{2}}\right]$T. **(06 Marks)**

b. What is inconsistency of Ampere's law with continuity equation? How it was modified by Maxwell? Derive the modified equation. **(06 Marks)**

c. Given $E = E_m \sin(\omega t - \beta z)a_y$ V/m in free space, find D, B, H. Sketch E and H at t = 0. **(08 Marks)**

10 a. Prove that the intrinsic impedance of a perfect dielectric $\eta = \frac{|E|}{|H|} = \sqrt{\frac{\mu}{\epsilon}}$ **(06 Marks)**

b. Derive expressions for attenuation constant 'α' and phase constant 'β' for any conducting media. **(06 Marks)**

c. Calculate attenuation constant, wave velocity and intrinsic impedance in sea water for a uniform plane wave at 10 GHz. The constants are $E_r = 80$, $\mu_r = 1$, $\sigma = 4$ Mho s/m. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC42

Fourth Semester B.E. Degree Examination, July/August 2021
Signals and Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Distinguish between :
   i) Periodic and non-periodic signals
   ii) Even and odd signals. **(04 Marks)**

b. Determine whether the following systems are linear, causal, dynamic, time-variants and stable. i) $y(n) = 3x(n-1)$ ii) $y(t) = x(t^2)$. **(08 Marks)**

c. Given the signal x(t) as shown, sketch the following : i) $x(-2t+3)$ ii) $x(t/2-2)$.

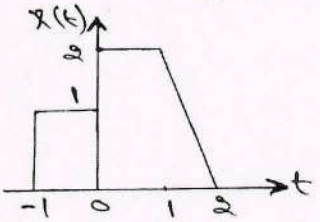


Fig.Q1(c) **(08 Marks)**

2 a. Check whether the following signals are periodic or not. If periodic, determine their fundamental period. i) $x(t) = \cos 2t + \sin 3t$ ii) $x(n) = \cos\left(\frac{\pi n}{5}\right)\sin\left(\frac{\pi n}{3}\right)$. **(06 Marks)**

b. Sketch the even and odd parts of the following signal, $x(t) = u(t+2) + u(t) - 2u(t-1)$. **(08 Marks)**

c. Express : x(t) interms of g(t), if x(t) and g(t) are as shown in Fig.Q2(c).

Fig.Q2(c) **(06 Marks)**

3 a. Prove the following :
   i) $x(t) * \delta(t - t_0) = x(t - t_0)$
   ii) $x(n) * h(n) = h(n) * x(n)$. **(04 Marks)**

b. Compute the convolution integral of $x(t) = e^{-3t}[u(t) - u(t-2)]$ and $h(t) = e^{-t}u(t)$. **(08 Marks)**

c. Evaluate $y(t) = x(t) * h(t)$. x(t) and h(t) are shown in Fig.Q3(c).

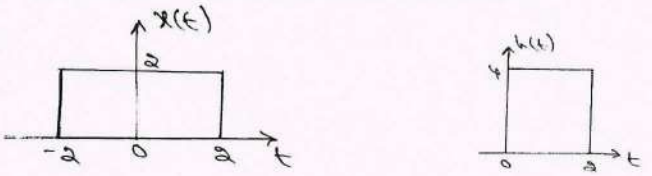


Fig.Q3(c) **(08 Marks)**

4 a. Evaluate $y(n) = x(n) * h(n)$. If $x(n)$ and $h(n)$ are given as :
$x(n) = \left\{2, \underset{\uparrow}{4}, -2, 1, 7\right\}$ and $h(n) = \left\{2, 3, \underset{\uparrow}{1}, 4\right\}$. **(05 Marks)**

b. Compute the convolution sum of $x(n) = a^n u(n)$ and $h(n) = b^n u(n)$. **(07 Marks)**
i) when $a > b$ ii) when $a < b$ iii) when $a = b$.

c. Determine the response of an LTI system with input $x(n) = (1/3)^n u(n)$ and impulse response $h(n) = u(n) - u(n-5)$. **(08 Marks)**

5 a. Calculate the step response of the LTI systems represented by following impulse responses.
i) $h(n) = (1/2)^n u(n-3)$ ii) $h(t) = \begin{cases} 1, & -2 \le t \le 0 \\ 0, & \text{elsewhere} \end{cases}$. **(06 Marks)**

b. State any six properties of CTFS. **(06 Marks)**

c. Determine the DTFS coefficients of $x(n) = \sin\left(\frac{4\pi n}{21}\right) + \cos\left(\frac{10\pi n}{21}\right) + 1$. Also sketch its magnitude and phase spectrum. **(08 Marks)**

6 a. Check the following LTI system for memoryless, causality and stability :
i) $h(t) = e^t u(-1, -t)$ ii) $h(n) = \left\{\underset{\uparrow}{2}, 3, -1, 4\right\}$. **(06 Marks)**

b. Determine the Fourier series coefficients of the signal shown in Fig.6(b) and also plot $|X \times (k)|$ and $< X(k)$.

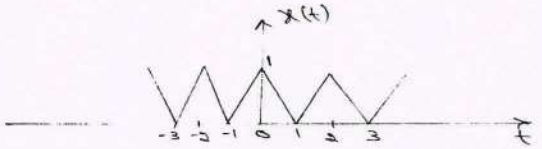


Fig.Q6(b) **(08 Marks)**

c. State the following properties DTFS :
i) Time shifting
ii) Frequency shifting
iii) Convolution
iv) Modulation
v) Parseval's theorem
vi) Duality. **(06 Marks)**

7 a. Determine the Fourier transforms of the following :
i) $x(t) = e^{at} u(-t)$ ii) $x(t) = e^{-a|t|}$, $a > 0$. **(08 Marks)**

b. State and prove the following properties of DTFT :
i) Convolution in time ii) Parseval's theorem. **(06 Marks)**

c. Determine the Nyquist sampling rate and Nyquist sampling interval for the following signals:
i) $x(t) = \frac{1}{2\pi}[\cos(4000\pi t)\cos(1000\pi t)]$ ii) $y(t) = \sin C^2(200t)$. **(06 Marks)**

8 a. State and prove the following properties of CTFT :
i) Time shifting ii) Frequency differentiation. **(08 Marks)**

b. Determine the DTFTs of the following :
i) $x(n) = (1/2)^n u(n-4)$ ii) $x(n) = -a^n u(-n-1)$. **(08 Marks)**

c. State the sampling theorem and briefly explain how to practically reconstruct the signal. **(04 Marks)**

9 a. Define region of convergence. Mention its properties. **(04 Marks)**

b. Using appropriate properties, find the z – transforms of the following signals :

i) $x(n) = n(n + 1)\, u(n)$ ii) $x(n) = n(\frac{1}{3})^{n+3}\, u(n + 3)$. **(08 Marks)**

c. Evaluate the inverse Z – transform of the following for all possible ROCs.

$$X(z) = \frac{z(z^2 - 4z + 5)}{(z-3)(z^2 - 3z + 2)}.$$ **(08 Marks)**

10 a. State and prove the following properties of Z-transform :

i) Time Reversal ii) Scaling in Z–domain. **(06 Marks)**

b. Find the Z–transform of $x(n) = 2^n u(n) + 3^n u(-n - 1)$ and draw its pole – zero plot. **(04 Marks)**

c. Compute the response of the system : $y(n) = 0.7y(n - 1) - 0.12y(n - 2) + x(n - 1) + x(n - 2)$ to the input $x(n) = n\, u(n)$. Also check whether the system is stable. **(10 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC43

Fourth Semester B.E. Degree Examination, July/August 2021
Control Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Write the difference between open loop and closed loop control system. **(04 Marks)**

b. For the mechanical system shown in Fig. Q1 (b). Write the analogous electrical network based on force-current analogy. **(08 Marks)**

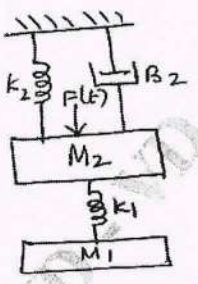


Fig. Q1 (b)

c. Obtain the overall transfer function of the block diagram, shown in Fig. Q1 (c) by block diagram reduction technique. **(08 Marks)**

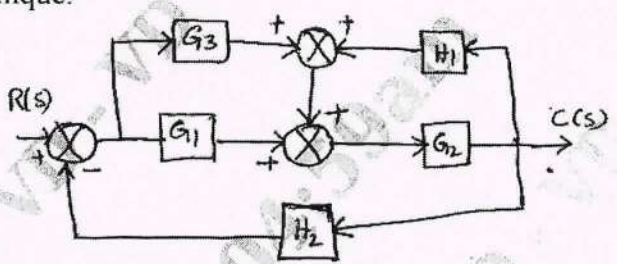


Fig. Q1 (c)

2 a. For the rotational system shown in Fig. Q2 (a), draw the torque voltage analogous circuit. **(08 Marks)**

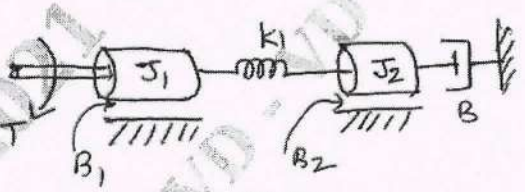


Fig. Q2 (a)

b. Explain Mason's gain formula for determining the transfer function from signal flow graph. **(04 Marks)**

c. For the system described by the signal flow graph shown in Fig. Q2 (c), obtain the closed loop transfer function $\frac{C(s)}{R(s)}$ using Mason's Gain formula. **(08 Marks)**

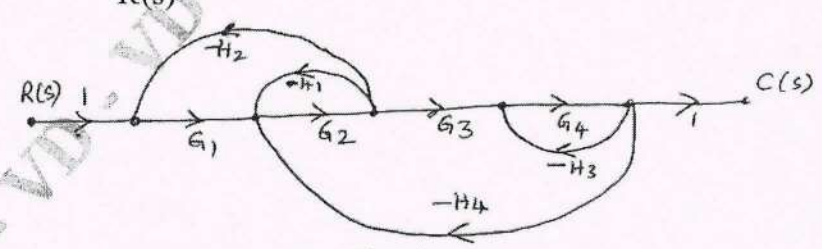


Fig. Q2 (c)

3 a. Derive an expression for rise time in a second order underdamped system subjected to unit step input. **(04 Marks)**

b. The transfer function of a second order system subjected to a unit step input, given by $\frac{C(s)}{R(s)} = \frac{16}{s^2 + 2s + 16}$

Calculate the rise time, peak time, peak overshoot and settling time. **(08 Marks)**

c. For a negative unity feed back control system with $G(s) = \frac{100}{s^2(s+4)(s+12)}$. Determine

(i) Type of the system (ii) Error co-efficients (iii) Steady state error when the input $r(t) = 2t^2 + 5t + 10$ **(08 Marks)**

4 a. With general block diagram, explain PD controller and PI controller. **(06 Marks)**

b. In PD controller system shown in Fig. Q4 (b), determine the value of T_d, so that the system will be critically damped, calculate its settling time. **(06 Marks)**

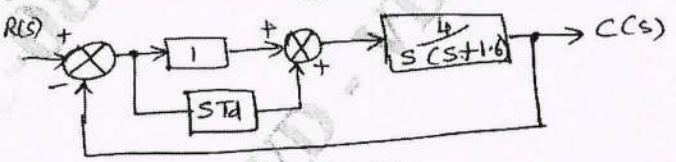


Fig. Q4 (b)

c. For the system shown in Fig. Q4 (c), obtain the closed loop transfer function, damping ratio, natural frequence, damping frequency and the expression for the output response if subjected to unit step input. **(08 Marks)**

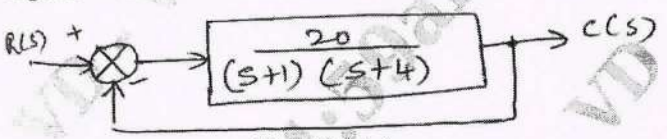


Fig. Q4 (c)

5 a. Investigate the stability of a closed loop system whose characteristic equation is given by, $s^5 + s^4 + 2s^3 + 3s + 5 = 0$ using R–H criteria. **(06 Marks)**

b. The open loop transfer function of a unity feedback system is given by, $G(s) = \frac{K}{s(s+3)(s^2+s+1)}$, using RH criteria find the value of 'K' that will cause sustained oscillation, hence find the oscillation frequency. **(06 Marks)**

c. Consider the characteristic equation, $s^6 + 2s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + 16 = 0$, using RH criteria investigate the stability of the system. **(08 Marks)**

6 a. Determine the value of 'K' and 'a' so that the system shown in Fig. Q6 (a) oscillates with frequency of 2 rad/sec. **(06 Marks)**

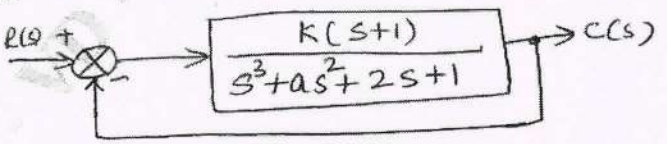


Fig. Q6 (a)

b. Sketch the Root locus for a unity feedback system with $G(s) = \frac{K}{s(s^2+8s+17)}$. From root locus determine the value of K for a damping factor of 0.5. **(14 Marks)**

7 a. Construct the Bode plot for a unity feedback control system having $G(s) = \frac{K}{s(1+s)(1+0.1s)}$, find the (i) Value of K for a gain margin of 10 dB. (ii) Value of K to give a phase margin of 24°. **(12 Marks)**

b. Find the transfer function of the system whose Bode plot is given in Fig. Q7 (b). **(08 Marks)**

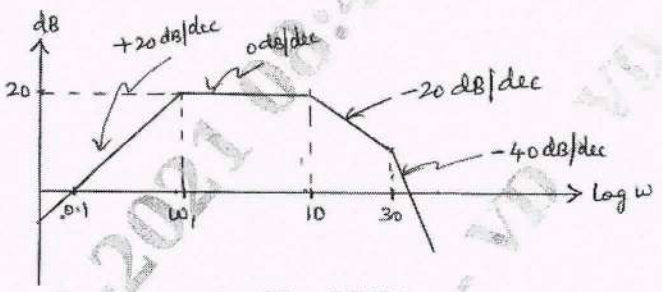


Fig. Q7 (b)

8 a. Plot the polar plot for the open loop transfer function, $G(s)H(s) = \frac{1}{1+0.1s}$. **(06 Marks)**

b. A unity feedback system has $G(s) = \frac{10}{s(s+1)(s+2)}$. Draw Nyquist plot and comment on closed loop stability. **(14 Marks)**

9 a. With a block diagram, explain a system with digital controller. **(06 Marks)**

b. Obtain state transition matrix for $A = \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix}$. **(08 Marks)**

c. State the properties of state transition matrix. **(06 Marks)**

10 a. Explain signal reconstruction using sampler and zero order hold. **(06 Marks)**

b. Obtain the state model for the system represented by a differential equation,

$\frac{d^3y}{dt^3} + 3\frac{d^2y}{dt^2} + 6\frac{dy}{dt} + 7y(t) = 2u(t)$ **(06 Marks)**

c. For the electrical network shown in Fig. Q10 (c), find the state space representation if the output is the current through the resistor. **(08 Marks)**

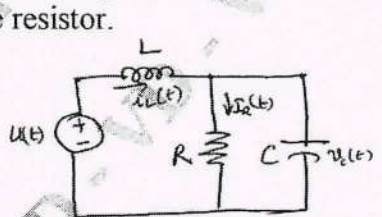


Fig. Q10 (c)

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC44

Fourth Semester B.E. Degree Examination, July/August 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Explain the operation of the switching modulator with circuit diagram, waveforms and relevant expressions. **(08 Marks)**

b. Explain the operation of the costas receiver for detection of DSB-SC waves. **(06 Marks)**

c. Explain the importance of vestigial sideband modulation in communication system. Describe the frequency domain description with message spectrum and VSB modulated wave spectrum. **(06 Marks)**

2 a. Explain the operation of the envelope detector with circuit diagram, waveforms and relevant mathematical expressions. **(08 Marks)**

b. Explain the principle of operation of the Quadrature-carrier-Multiplexing with block diagram approach. **(06 Marks)**

c. Explain the principle of operation of the frequency-division-multiplexing with suitable block-diagram. **(06 Marks)**

3 a. Explain the narrow band frequency modulation, with block diagram approach. Explain the generation of narrowband FM using DSB-SC modulator. **(07 Marks)**

b. An FM wave with a frequency deviation of 10kHz at a modulation frequency of 5kHz is applied to two frequency doublers connected in cascade. Determine the frequency deviation and the modulation index of the FM wave at the output of second frequency multiplier. What is the frequency of the adjacent side-frequencies of this FM wave? **(05 Marks)**

c. Explain the operation of the superhetero dyne receiver. Mention the function of each block with suitable diagram. **(08 Marks)**

4 a. Explain the Demodulation of FM signals using circuit diagram and relevant graphs (Any one of the method). **(07 Marks)**

b. Briefly explain about FM stereo multiplexing with multiplexer of FM stereo transmitter and Demultiplexer of FM stereo receiver. **(08 Marks)**

c. Derive an expression for linear model of phase locked loop in FM system. **(05 Marks)**

5 a. Explain the conditional probability with mathematical expressions. State and prove Baye's rule. **(07 Marks)**

b. Define and write the expressions for mean, correlation and covariance function. **(07 Marks)**

c. Explain the properties of auto correlation function with mathematical expressions. **(06 Marks)**

6 a. Briefly explain the noises such as shot noise, thermal noise and white noise. **(09 Marks)**

b. Derive an expression for noise equivalent Bandwidth, with relevant circuit and equations. **(07 Marks)**

c. Briefly explain the Noise factor and noise figure with equations. **(04 Marks)**

7 a. Derive an expression for noise in DSBSC receivers with model and relevant expressions. **(08 Marks)**

b. Find the figure of merit when the depth of modulation is i) 100% ii) 50% iii) 30% **(04 Marks)**

c. Explain the FM threshold effect with phasor diagram, graph and relevant expressions. **(08 Marks)**

8 a. An AM receiver operating with a sinusoidal wave and 80% modulation has an output signal to noise ratio of 30dB. Calculate the corresponding carrier to noise ratio. Prove the formula used (optional). **(04 Marks)**

b. Explain the FM threshold reduction process with graph representing the extending threshold effect and block diagram of FM feedback demodulator. **(08 Marks)**

c. Explain the significance of Pre-emphasis and De-emphasis in FM system. **(08 Marks)**

9 a. Why we digitize Analog sources? Explain the sampling process with graph showing CT and its DT signal. **(08 Marks)**

b. Explain the pulse width modulation with generation circuit, waveforms. Mention the advantages, disadvantages and applications of PWM. **(08 Marks)**

c. Explain the Digital Multiplexing with diagram. Mention the number of inputs and rates. **(04 Marks)**

10 a. Explain the generation of pulse amplitude modulation with block diagram and waveforms. Mention the importance of flat-top sampling with waveform. **(08 Marks)**

b. For a pulse-amplitude modulation transmission of noise signal with W = 3kHz. Calculate Bandwidth B_T, if f_s = 8kHz and $\tau = 0.1T_s$. **(04 Marks)**

c. Explain the Application to vocoders such as voice model and vocoder with relevant block-diagrams. **(08 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC45

Fourth Semester B.E. Degree Examination, July/August 2021
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. With a neat circuit diagram and relevant equations, explain the basic op-amp circuit. **(07 Marks)**

b. Define the following terms as applied to an op-amp and mention their typical values for IC741: (i) CMRR (ii) Slew rate (iii) PSRR (iv) Input offset voltage **(08 Marks)**

c. Show that $V_{O_{CM}} = \frac{V_{i_{CM}}}{CMRR} \times A_V$ **(05 Marks)**

2 a. Explain the operation of direct coupled non inverting amplifier. Mention the design steps. **(07 Marks)**

b. Explain the working of a three input inverting summer amplifier and show how it can be modified into averaging circuit. **(08 Marks)**

c. For the op-amp circuit shown in Fig.Q2(c), calculate the gain.

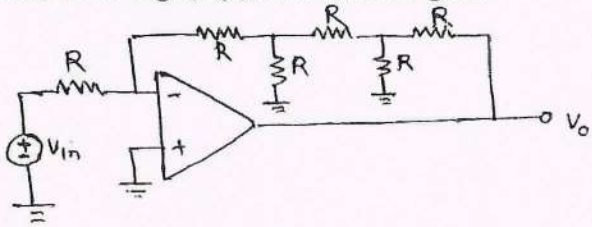


Fig.Q2(c) **(05 Marks)**

3 a. With a neat circuit diagram, explain the operation of high input impedance capacitor coupled non inverting amplifier. **(09 Marks)**

b. A capacitor coupled voltage follower circuit is to be designed to have a lower cut-off frequency of 120 Hz. The load resistance is 8.2 KΩ and the op-amp used has a maximum bias current of 600 nA. Design a suitable circuit. Calculate the new cut-off frequency when the load resistance is changed to 4.7 KΩ. **(06 Marks)**

c. Explain the operation of capacitor coupled inverting amplifier using single polarity supply. **(05 Marks)**

4 a. With a neat circuit diagram, explain the operation of instrumentation amplifier. **(09 Marks)**

b. Design a low resistance voltage source to provide an output of 8V using 741 op-amp with ±15V supply and maximum output current is to be 60 mA. Use a suitable Zener diode. For 741 op-amp $I_{B_{(max)}} = 500$ nA. **(06 Marks)**

c. Explain how a fullwave precision rectifier is implemented using Halfwave rectifier and a summer. **(05 Marks)**

5 a. With a neat circuit diagram, explain the operation of inverting Schmitt trigger circuit. **(08 Marks)**

b. Explain the working of Wien bridge oscillator using op-amp. **(06 Marks)**

c. Design a capacitor coupled Zero Cross Detector (ZCD) using 741 op-amp having $I_{B_{(max)}} = 500$ nA and minimum signal frequency of 500 Hz. the supply voltage are ± 12V. **(06 Marks)**

6 a. Draw an op-amp sample and hold circuit. Sketch the signal, control and output waveforms and explain the operation of the circuit. **(08 Marks)**

b. Explain the operation of logarithmic amplifier using op-amp. **(06 Marks)**

c. Design a RC phase shift oscillator to have an output frequency of 3.5 kHz using 741 op-amp with a supply voltage of ±12V. **(06 Marks)**

7 a. List the advantages and limitations of Active filters. **(06 Marks)**

b. Explain the operation of First order low pass filter using op-amp and mention the design steps. **(08 Marks)**

c. A single stage band pass filter is to be designed using 715 op-amp. The center frequency is to be 3.3 kHz with a passband approximately 50 Hz on each side. Determine the suitable component values. For 715 op-amp choose $I_{B_{(max)}} = 1.5\ \mu A$. **(06 Marks)**

8 a. With a neat circuit diagram, explain the working of voltage follower series regulator. **(06 Marks)**

b. Explain the functional block of 723 general purpose regulator. **(08 Marks)**

c. Design an adjustable regulator using IC7810 regulator to get an output voltage of 15 V and 25 mA. Given Quiscent current = 4.2 mA. **(06 Marks)**

9 a. With a neat block diagram, explain the operation of Phase Locked Loop (PLL). Also define: (i) Pull in time (ii) Lock range (iii) Capture range for a PLL **(08 Marks)**

b. Explain the working of 3-bit R-2R Ladder types DAC. **(06 Marks)**

c. What output voltage is produced by a DAC whose output range is 0 to 10V and whose input binary is :
(i) 10 (for a 2 bit DAC)
(ii) 0110 (for a 4 bit DAC)
(iii) 10111100 (for a 8 bit DAC) **(06 Marks)**

10 a. With a neat functional diagram, explain the operation of monostable multivibrator using 555 timer and obtain the expression for its pulse width. **(08 Marks)**

b. With a neat block diagram, explain the working of successive approximation type ADC. **(06 Marks)**

c. A 555 timer Astable multivibrator has $R_A = 2.2\ K\Omega$, $R_B = 6.8\ K\Omega$ and $C = 0.01\ \mu F$. Calculate T_{high}, T_{Low}, free running frequency and duty cycle. Draw the circuit. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

17EC46

Fourth Semester B.E. Degree Examination, July/August 2021
Microprocessors

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. What advantage does 8086 processor have by having two independent units Bust Interface Units (BIU) and Execution Unit (EU)? **(04 Marks)**

b. With suitable examples, explain various addressing modes of 8086 processor. **(08 Marks)**

c. The machine code of an instruction is 8907H, explain how these two bytes are interpreted? What is the Instruction? Given, Opcode of MOV instruction '100010'. **(08 Marks)**

2 a. Explain the following :
i) Offset address ii) Physical address
iii) Paragraph Boundary iv) Memory relocation. **(04 Marks)**

b. Explain the (MOD – REG – R/M) byte of an 8086 instructions. **(08 Marks)**

c. At a certain instant during the execution of a program the 8086 processor has the following data in the registers AX = 1234H , BX = 5678H , SI = 1200H , DI = ABCDH , CS = AB00H and IP = 789AH , DS = ES = 4567H.
State the addressing modes and find physical addresses of source and destination of data, when each of the following instruction is executed.
i) MOV BX , AX ii) MOV [BX + DI + 120FH] , AB46H
iii) MOV AX, [1200H] iv) LODSW. **(08 Marks)**

3 a. Use appropriate logical instruction which performs :
i) Set higher nibble of AL register ii) Clear AX register
iii) Invert even bits of BX register iv) Clear 5^{th} and 6^{th} bits of CH register. **(04 Marks)**

b. Write an 8086 ALP to transfer a block of data stored at SRC to another memory area DST. The length of the block is specified at location BLK – LEN. **(08 Marks)**

c. Consider the registers of 8086 loaded with the following data :
ES = 1234H , DS = 1224H , DI = 200H , SI = 100H , CX = 10H , DFlag = '1'.
If now, the instruction REP MOVSW is completely executed workout the contents of above defined registers after the execution of the REP MOVSW instruction. **(08 Marks)**

4 a. What are Assembler directives? With examples, explain the data definition directives DB, DW and DD. **(04 Marks)**

b. Write an 8086 ALP to arrange an array of 'N' bytes in ascending order. **(08 Marks)**

c. Explain five string primitives of 8086. Also specify necessary initializations to be done before using the string instructions. **(08 Marks)**

5 a. Distinguish between MACROS and Procedures. **(04 Marks)**

b. Explain working of Interrupt and Trap flags of 8086 processor. Write a procedure to set trap flag and procedure to reset trap flag. **(08 Marks)**

c. With neat schematic, explain generation of NMI interrupt during power failure. **(08 Marks)**

6 a. Explain how the 8086 processor finds the address of interrupt service subroutine for particular interrupt. **(04 Marks)**

b. Explain Interrupt system of 8086 processor. Write the sequence of events takes place when an interrupt occurs. **(08 Marks)**

c. What is meant by Modular Programming? Also write a procedure to generate a delay of 2 msec, for the 8086 operated at 5 MHz. **(08 Marks)**

7 a. Compare memory mapped I/O and I/O mapped I/O interfacing schemes. **(04 Marks)**

b. Why the address demultiplexing is required in 8086 processor? Explain how it is done for minimum mode of operation. **(08 Marks)**

c. What is Wait State? How do you introduce it? Explain with necessary timing diagram with respect to 8086 processor. **(08 Marks)**

8 a. Explain the function of following 8086 pins :

i) $\overline{BHE}$ ii) ALE iii) INTR iv) $DT/\overline{R}$. **(04 Marks)**

b. Sketch memory read bus cycle of 8086 and explain. **(08 Marks)**

c. Explain 8255 modes of operations. **(08 Marks)**

9 a. Write 8255 control word to set PC_5. **(04 Marks)**

b. Interface a stepper motor to 8086 processor using 8255 and write an ALP to it for 180^0 in clock wise direction. **(08 Marks)**

c. Explain Mode - 0 and Mode – 3 operations of 8254. **(08 Marks)**

10 a. Bring out the differences between CICS and RISC processors. **(04 Marks)**

b. Describe any five DOS functions related with INT21H. **(08 Marks)**

c. Using DOS functions write an 8086 ALP to read a two digit hexadecimal number and display the same on the console. **(08 Marks)**

* * * * *