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18ES51

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Technological Innovation Management and Entrepreneurship

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Give different definitions of management as interpreted by management scholars. **(07 Marks)**
b. Discuss modern approaches of management. **(06 Marks)**
c. Describe the levels of management. **(07 Marks)**

OR

2 a. Discuss various steps involved in planning. **(07 Marks)**
b. List some of the standing plans and single use plans and explain. **(06 Marks)**
c. Explain steps involved in rational decision making. **(07 Marks)**

Module-2

3 a. Explain principles of organization. **(07 Marks)**
b. Discuss factors affecting span of management. **(06 Marks)**
c. Distinguish between Job Analysis, Job description and Job specification. **(07 Marks)**

OR

4 a. Illustrate Maslow's theory of hierarchy of needs. **(07 Marks)**
b. Discuss essentials of effective control system. **(06 Marks)**
c. Describe different leadership styles from authority point of view. **(07 Marks)**

Module-3

5 a. Discuss the benefits of social audit. **(07 Marks)**
b. What do you understand by business ethics? What are the factors which affect the decision is ethical or unethical? **(06 Marks)**
c. Describe Corporate Governance. Explain the benefits of Corporate Governance. **(07 Marks)**

OR

6 a. Identify different types of barriers to Entrepreneurship. **(07 Marks)**
b. Explain the need of capacity building to Entrepreneurship. **(06 Marks)**
c. Discuss the contribution of Entrepreneurship Development cycle. **(07 Marks)**

Module-4

7 a. Explain in brief, the characteristics of family owned business in India. **(07 Marks)**
b. Discuss "13-circle" model of family business. **(06 Marks)**
c. What are the various types of family business? Explain. **(07 Marks)**

OR

8	a.	List four fundamental features of business opportunities and explain.	**(07 Marks)**
	b.	Describe various methods of generating new ideas.	**(06 Marks)**
	c.	Explain market entry strategies.	**(07 Marks)**

Module-5

9	a.	Explain the need and scope of business plan.	**(07 Marks)**
	b.	List the contents of a business plan and explain.	**(06 Marks)**
	c.	Discuss the role of Angel Investors and Debt financing in financing a business.	**(07 Marks)**

OR

10	a.	Explain the growth and development of MSME in India.	**(07 Marks)**
	b.	Explain the importance of Network Analysis in project design and execution.	**(06 Marks)**
	c.	Compare and Contrast Program Evaluation Review Technique (PERT) with Critical Path Method (CPM).	**(07 Marks)**

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18EC52

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Signal Processing

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Show that the multiplication of two DFT's leads to circular convolution of the corresponding time sequences. **(08 Marks)**

b. Compute the N – point OFT's of the signals :

i) $x(n) = \begin{cases} 1, & 0 \le n \le \frac{N}{2} - 1 \\ 0, & \frac{N}{2} \le n \le N-1 \end{cases}$.

ii) $x(n) = \cos \frac{2\pi}{N} k_0 n$, $0 \le n \le N\text{-}1$. **(07 Marks)**

c. Given $x(n) = \{1, 2, 3, 4\}$, find $y(n)$, if $y(k) = x((k-2))_4$. **(05 Marks)**

OR

2 a. State and prove the Circular time shift property of DFT. **(06 Marks)**

b. Determine the circular convolution of $x_1(n) = \{1, 2, 3, -1\}$ and $x_2(n) = \{4, 3, 2, -2\}$, using Time domain formula. Verify the result using Frequency domain approach. **(09 Marks)**

c. For the sequence $x(n) = \{-1, 2, 3, 0, -4, 1, 2, -3\}$, Calculate

i) $\sum_{k=0}^{7} x(k)$ and ii) $\sum_{k=0}^{7} |x(k)|^2$, without computing the DFT. **(05 Marks)**

Module-2

3 a. Write the computational procedure to find the filtered output using Overlap Add method. **(07 Marks)**

b. Find the 8 – point DFT of the sequence $x(n) = \{-1, 0, 2, 3, -4, -2, 0, 5\}$, using radix – 2 DIT – FFT algorithm. **(09 Marks)**

c. Compare the complex additions and complex multiplications for the direct computation of DFT versus the FFT algorithm for N = 128. **(04 Marks)**

OR

4 a. Derive the radix – 2 DIF – FFT algorithm and draw the signal flow graph for N = 8. Comment on the number of computations required to find N – point DFT. **(07 Marks)**

b. Using Overlap save method, find the output of a filter whose impulse response $h(n) = \{1, -2, 3\}$ and input $x(n) = \{2, 3, -1, 0, 5, 2, -3, 1\}$.
Use 6 – point circular convolution. **(09 Marks)**

c. Given $X(k) = \{1, j4, 1, -j4\}$, find x(n) using radix – 2 DIT – FFT algorithm. **(04 Marks)**

Module-3

5 a. Design an FIR filter for the following desired frequency response

$$H_d(w) = \begin{cases} e^{-j3w}, & \text{if } |w| \le \pi/4 \\ 0, & \text{if } |w| > \pi/4 \end{cases}.$$

Use the Hamming window function, obtain the frequency response of the designed FIR filter. **(10 Marks)**

b. For the System function $H(z) = 1 + 2.8z^{-1} + 3.4z^{-2} + 1.7z^{-3} + 0.4z^{-4}$. Obtain the Lattice coefficients and sketch the Lattice structure. **(10 Marks)**

OR

6 a. Find the Impulse response of an FIR filter with the following desired frequency response,

$$H_d(w) = \begin{cases} 0 & ; \text{ if } |w| \le \pi/6 \\ e^{-j4w} & ; \text{ if } |w| > \pi/6 \end{cases}.$$

Use Rectangular window function. Draw the direct form structure for the designed filter. **(10 Marks)**

b. Consider an FIR Lattice filter coefficients $K_1 = 0.65$, $K_2 = 0.5$, $K_3 = 0.9$. Find its impulse response and draw the direct form structure. **(10 Marks)**

Module-4

7 a. Define the First order analog low pass filter prototype. How this prototype is transformed into a different filter types. **(05 Marks)**

b. Design a Second order digital low pass Butterworth filter with a cutoff frequency of 3.4 kHz at a sampling frequency of 8000Hz. Draw the direct Form – II structure of this filter. Use Bilinear transformation. **(10 Marks)**

c. Discuss the general mapping properties of bilinear transformation and show the mapping between the S – plane and the the Z – plane. **(05 Marks)**

OR

8 a. Define the Normalized low pass prototype function of Butterworth filter and derive the expression for the filter order. **(05 Marks)**

b. Using Bilinear transformation, design a digital low pass Butterworth fitler with the following specifications : Sampling frequency : 8000Hz , 3 dB attenuation at 1.5 kHz. 10 dB stop band attenuation at 3kHz. **(10 Marks)**

c. Realize the following digital filter using direct Form – II

$$H(z) = \frac{0.7 + 1.4z^{-1} + 0.7z^{-2} + 0.5z^{-3}}{1 + 1.3z^{-1} + 0.5z^{-2} + 0.7z^{-3} + 0.3z^{-4}}.$$ **(05 Marks)**

Module-5

9 a. With a neat diagram, explain the Harvard architecture used in DS processors. **(06 Marks)**

b. Illustrate the operation of circular buffers used for address generation in DS processors. **(07 Marks)**

c. Convert the following decimal numbers into the floating point representation

i) 0.640492×2^{-2} ii) -0.638454×2^{5}.

Use 4 – bits to represent exponent and 12 – bits for mantissa. **(07 Marks)**

OR

10 a. With a neat diagram, explain the basic architecture of TMS320C54X family DS processors. **(10 Marks)**

b. Describe the IEEE single precision floating point format used in DS processors. **(05 Marks)**

c. Find the signed Q – 15 representation for the decimal number 0.560123. **(05 Marks)**

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18EC53

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Principles of Communication System

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain in detail the working of switching modulator with diagram and necessary derivations. **(10 Marks)**

b. Explain the generation of DSBSC modulated waves using ring modulator. **(10 Marks)**

OR

2 a. Illustrate the amplitude modulation process and draw the waveform for modulation index $M > 1$ & $M < 1$. **(08 Marks)**

b. Explain with relevant block diagram and working of FDM system. **(08 Marks)**

c. A 400 W carrier is modulated on a depth of 75 percent. Calculate the total power in the modulated wave of following form AM.
(i) Double Side Band with Full Carrier (DSBFC)
(ii) Double Side Band Suppressed Carrier (DSBSC) **(04 Marks)**

Module-2

3 a. Derive the equations for frequency modulated wave. Define modulation index and frequency deviation. **(12 Marks)**

b. A 93.2 MHz carrier is frequency modulated by 5 kHz sine wave the resultant FM signal has frequency deviation of 40 kHz:
(i) Find the carrier swing of FM signal
(ii) What are highest and lowest frequencies of FM signal?
(iii) Calculate the modulation index of FM
(iv) B.W of FM signal **(08 Marks)**

OR

4 a. Explain the Narrow band FM with relevant expressions and phasor diagrams. **(10 Marks)**

b. Discuss the nonlinear effects in FM system. **(06 Marks)**

c. Assume that the maximum value of frequency deviation Δf is fixed at 50 kHz for a certain FM transmission. Given that the maximum modulating frequency is 15 kHz. Calculate the necessary transmission bandwidth. **(04 Marks)**

Module-3

5 a. Derive the expression for figure of merit for DSB-SC receiver. **(10 Marks)**

b. Find figure of merit for single tone FM. **(06 Marks)**

c. Write short notes on:
(i) Shot Noise
(ii) White Noise **(04 Marks)**

OR

6 a. With FM receiver model, derive the expression for figure of merit. **(10 Marks)**

b. Briefly explain the following as application to FM.
(i) Pre-emphasis
(ii) De-emphasis **(06 Marks)**

c. An AM receiver operating with a sinusoidal modulating signal has a following specifications: m = 0.8 and $(SNR)_0$ = 30 dB. What is carrier to noise ratio? **(04 Marks)**

Module-4

7 a. State sampling theorem and explain same with neat sketches and equation. **(10 Marks)**

b. With neat block diagram, explain the TDM. **(06 Marks)**

c. A Compact Disc (CD) audio signals digitally using PCM. Assume the audio signal bandwidth to be 20 kHz.
(i) What is the Nyquist rate?
(ii) If the Nyquist samples are quantized to L = 65, 536 levels and then binary coded, determine the number of bits required to encode a sample. **(04 Marks)**

OR

8 a. What are advantages digitizing the analog signals? **(06 Marks)**

b. With a block diagram, explain the generation and detection of PPM. **(10 Marks)**

c. Discuss Bandwidth – Noise trade off. **(04 Marks)**

Module-5

9 a. With a neat diagram, explain the basic elements of a PCM. **(08 Marks)**

b. Discuss the concept and operation of delta modulation in detail. **(08 Marks)**

c. PCM system uses uniform quantizer followed by a 7 bit binary encoder. The bit rate of the system is 50×10^6 bps. What is minimum message bandwidth? **(04 Marks)**

OR

10 a. Write a note on MPEG + Video. **(10 Marks)**

b. Draw the resulting waveform for 01101001 using unipolar NRZ, polar NRZ, unipolar Z2, Bipolar RZ. **(06 Marks)**

c. A TV signal with a bandwidth of 4.2 MHz is transmitted using binary PCM. The number of representation level is 512. Calculate:
(i) Codeword length
(ii) Final bit rate
(iii) Transmission bandwidth **(04 Marks)**

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18EC54

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Information Theory and Coding

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression for average information contents of symbols in long independent sequence. **(06 Marks)**

b. Find the relationship between Hartley's, nats and bits. **(06 Marks)**

c. A code is composed of dots and dashes. Assuming that a dash is 3 times as long as a dot and has one-third the probability of occurrence. Calculate:
(i) The information in a dot and dash
(ii) The entropy of dot-dash code
(iii) The entropy rate of information, if a dot losts for 10 ms and this time is allowed between symbols. **(08 Marks)**

OR

2 a. Consider a second order mark-off source as shown in Fig.Q2(a). Here s = {0, 1} and states are A{0, 0}, B = {0, 1}, C = {1, 0} and D = {1, 1}.
(i) Compute the probability of states (ii) Compute the entropy of the source

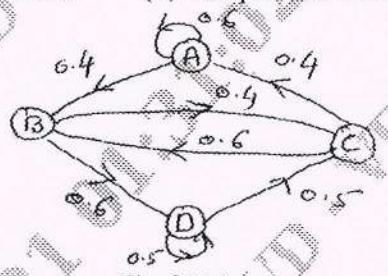

Fig.Q2(a) **(10 Marks)**

b. Prove that entropy of zero memory extension source is given by $H(s^n) = nH(s)$. **(10 Marks)**

Module-2

3 a. A Discrete Memory Source (DMS) has an alphabet $X = \{x_1, x_2, x_3, x_4, x_5, x_6\}$ and source statistics. $P = \{0.3, 0.25, 0.20, 0.12, 0.08, 0.05\}$. Construct binary Huffman code. Also find the efficiency and redundancy of coding. **(10 Marks)**

b. Apply Shannon encoding algorithm to the following set of messages and obtain code efficiency and redundancy. **(10 Marks)**

m_1	m_2	m_3	m_4	m_5
1/8	1/16	3/16	1/4	3/8

OR

4 a. A source having alphabet $s = \{s_1, s_2, s_3, s_4, s_5\}$ produces a symbols with respective probabilities 1/2, 1/6, 1/6, 1/9, 1/18.
(i) When the symbols are coded as shown 0, 10, 110, 1110, 1111 respectively.
(ii) When the code is as 00, 01, 10, 110, 111
Find code efficiency and redundancy **(12 Marks)**

b. State and prove Kraft McMillan inequality. **(08 Marks)**

Module-3

5 a. Discuss the binary Erasure Channel (BEC) and also derive channel capacity equation for BEC. **(08 Marks)**

b. A channel has the following characteristics

$$P\left[\frac{Y}{X}\right] = \begin{array}{c} \\ X_1 \\ X_2 \end{array} \begin{array}{c} \begin{array}{cccc} Y_1 & Y_2 & Y_3 & Y_4 \end{array} \\ \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{6} & \frac{1}{6} \\ \frac{1}{6} & \frac{1}{6} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \end{array}$$

Find H(X), H(Y), H(X, Y) and channel capacity if r = 1000 symbols/sec. **(12 Marks)**

OR

6 a. Determine the rate of transmission of information through a channel whose noise characteristics is as shown in Fig.Q6(a).

Given $P(X_1) = P(X_2) = \frac{1}{2}$. Assume $r_s = 10{,}000$ symbols/sec.

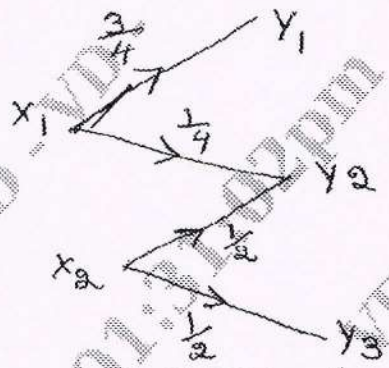

Fig.Q6(a) **(10 Marks)**

b. What is mutual information? Mention its properties and prove that $I(X:Y) = H(X) - H\left(\frac{X}{Y}\right)$; $I(X,Y) = H(Y) - H\left(\frac{Y}{X}\right)$. **(10 Marks)**

Module-4

7 a. For a (6, 3) linear block code the check bits are related to the message bits as per the equations given below:

$c_1 = d_1 \oplus d_2$

$c_2 = d_1 \oplus d_2 \oplus d_3$

$c_3 = d_2 \oplus d_3$

i) Find the generator matrix G
ii) Find all possible code words
iii) Find error detecting and error correcting capabilities of the code. **(12 Marks)**

b. The generator polynomial of a (7, 4) cyclic code is $g(x) = 1 + x + x^2$. Find the 16 code words of this code by forming the code polynomial v(x) using V(X) = D(X)G(X) where D(X) is the message polynomial. **(08 Marks)**

OR

8 a. Design a linear block code with a minimum distance of 3 and a message block size of 8 bits. **(08 Marks)**

b. For a (6, 3) cyclic code, find the following:
(i) G(x)
(ii) G in systematic form
(iii) All possible code words
(iv) Show that every code polynomial is multiple of g(x). **(12 Marks)**

Module-5

9 a. For the convolution encoder shown in Fig.Q9(a) the information sequence is d = 10011. Find the output sequence using the following two approaches.
(i) Time domain approach
(ii) Transfer domain approach

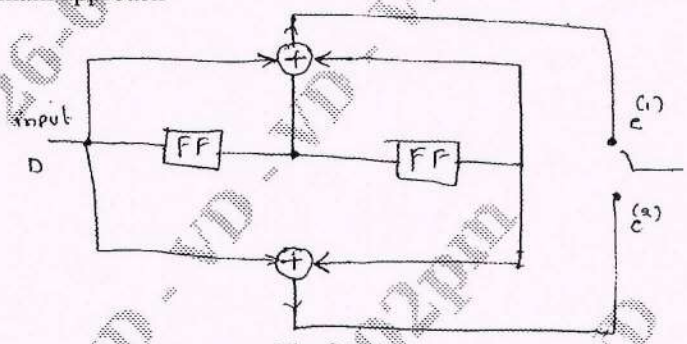

Fig.Q9(a) **(10 Marks)**

b. Consider a (3, 1, 2) convolution encoder with $g^{(1)} = 110$, $g^{(2)} = 101$ and $g^{(3)} = 111$.
(i) Draw the encoder diagram
(ii) Find the code word for message sequence (11101) using Generator matrix and Transfer domain approach. **(10 Marks)**

OR

10 a. Consider the rate $r = \frac{1}{2}$ and constraint length K = 2 convolution encoder shown in Fig.Q10(a).
(i) Draw the state diagram.
(ii) Draw the code tree
(iii) Draw Trellis diagram,
(iv) Trace the path through the tree that corresponds to the message sequence {1, 0, 1}.

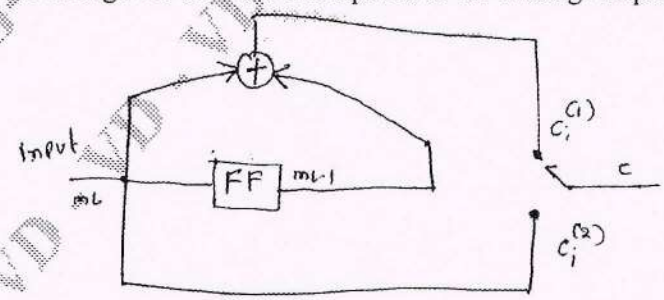

Fig.Q10(a) **(14 Marks)**

b. Explain Viterbi decoding. **(06 Marks)**

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18EC55

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Electromagnetic Waves

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. State and explain Coulomb's law in vector form. **(05 Marks)**

b. Derive the relationship between dot products between unit vectors of the three coordinate systems. Transform the following vectors to spherical system at the point given :
   i) $10a_x$ at P(3, 2, 4)
   ii) $10a_y$ at Q(5, 30°, 4) **(07 Marks)**

c. Four 10nc positive charges are located in z = 0 plane at the corners of a square 8cm on a side. A fifth 10nc charge is located at a point 8cm distant from other charges. Calculate the magnitude of total force on this fifth charge for $E = E_0$. **(08 Marks)**

OR

2 a. Using Coloumb's law, derive the expression for electric field Intensity 'E' due to an infinite sheet of charge of surface charge density ρ_s c/m^2. **(08 Marks)**

b. Four uniform sheets of charge are located as 20 Pc/m^2 at y = 7 ; −8 Pc/m^2 at y = 3 ; 6 P c/m^2 at y = −1 ; −18Pc/m^2 at y = −4. Find E at i) P_A (2, 6, -4) ii) P_B (10^6, 10^6, 10^6). **(06 Marks)**

c. Find the net outward flux (ψ) through the surface of a cube 2m on an edge centered at origin if $D = 5x^2a_x + 10za_z$ c/m^2. (The edges of cube are parallel to coordinate axes). **(06 Marks)**

Module-2

3 a. State and prove Gauss law in Integral form. **(05 Marks)**

b. Find the volume charge density at the points indicated if

   i) $D = 4\rho z \sin\phi\, a_\rho + 2\rho z \cos\phi\, a_\phi + 2\rho^2 \sin\phi\, a_z$ c/m^2 at $P_A\left(1, \frac{\pi}{2}, 2\right)$

   ii) $D = \sin\theta \cos\phi\, a_r + \cos\theta \cos\phi\, a_\phi - \sin\phi\, a_\phi$ c/m^2 at $P_B\left(2, \frac{\pi}{3}, \frac{\pi}{6}\right)$ **(07 Marks)**

c. Evaluate both sides of Divergence Theorem if $D = \frac{5r^2}{4} a_r$ c/m^2 in spherical co-ordinate for the volume enclosed between r = 1m and r = 2m. **(08 Marks)**

OR

4 a. Find the work done in moving a 5μc charge from origin to P(2, −1, 4) through $E = 2xyza_x + x^2 2a_y + x^2 y\, a_z$ V/m via the path :
   i) Straight line segments (0, 0, 0) to (2, 0, 0) to (2, −1, 0) to (2, −1, 4)
   ii) Straight line x = −2y ; z = 2x. **(08 Marks)**

b. Find 'E' at P(3, 60°, 25°) in free space, given $V = \frac{60\sin\theta}{r^2}$ V. **(06 Marks)**

c. Derive equation of continuity. Given $J = -10^6 z^{1.5} a_z$ A/m^2 in a region $0 \le \rho \le 20\mu$m, find the total current crossing a surface z = 0.1m. **(06 Marks)**

Module-3

5 a. Derive the expression for capacitance of a cylindrical capacitor using Laplace equation.

b. Assume $V = V_0$ at $\rho = a$ and $V = 0$ at $\rho = b$, $b > a$. **(08 Marks)**

In spherical co-ordinate $V = 865$ V at $r = 50$cm and $E = 748.2\ a_r$ at $r = 85$cm. Determine the location of voltage reference if potential depends only on 'r'. **(08 Marks)**

c. Verify whether the potential function $V = 2x^2 - 3x^2 + z^2$ satisfies Laplace equation. **(04 Marks)**

OR

6 a. Derive the expression for magnetic field intensity 'H' at the centre of a square current carrying loop of I amps with side 'L' meters using Biot Savart's law. **(08 Marks)**

b. Given $H = \frac{x+2y}{z^2}a_y + \frac{2}{z}a_z$ A/m. find J. Use J to find total current passing through the surface $z = 4$, $1 \le x \le 2$, $3 \le y \le 5$. **(08 Marks)**

c. Explain the concept of scalar and vector magnetic potential. **(04 Marks)**

Module-4

7 a. The point charge $Q = 18$nc has a velocity of 5×10^6m/s in the direction $a_v = 0.6\ a_x + 0.75a_y + 0.3a_z$. Calculate the magnitude of the force exerted on the charge by the field.

i) $B = -3a_x + 4a_y + 6a_z$ mT

ii) $E = -3a_x + 4a_y + 6a_z$ kV/m **(08 Marks)**

b. The magnetization in a magnetic material for which $\chi_m = 8$ is $150z^2\ a_x$ A/m. At $z = 4$cm, find the magnitude of i) J ii) J_T iii) J_B. **(06 Marks)**

c. Derive the expression for the force between two differential current elements. **(06 Marks)**

OR

8 a. Derive the expression for the boundary conditions between two magnetic medias. **(06 Marks)**

b. Let the permitivity be 5μH/m in region A where $x < 0$ and 20 μH/m in region B where $x < 0$. and 20 μH/m in region B where $x > 0$. If $K = 150a_y - 200a_z$ A/m at $x = 0$ and $H_A = 300a_x - 400a_y + 500a_z$ A/m. Find : i) $|H_{tA}|$ ii) $|H_{NA}|$ iii) $|H_tB|$ iv) $|H_{NB}|$. **(08 Marks)**

c. A circular loop of radius 10cm radius is located in x – y plane in a magnetic field $B = 0.5 \cos(377t)(3a_y + 4a_z)$ T. Determine the voltage induced in the loop. **(06 Marks)**

Module-5

9 a. What is the inconsistency of Ampere's law with continuity equation? Derive the modified Ampere's law by Maxwell for time varying fields. **(06 Marks)**

b. Given $E = E_m \sin(\omega t - \beta z)\ a_y$ V/m, find i) D ii) B iii) H. sketch E and H at $t = 0$. **(08 Marks)**

c. Prove that the conduction current is equal to the displacement current between the two plates for $V = V_0 e^{j\omega t}$ in a parallel plate capacitor. **(06 Marks)**

OR

10 a. Show that the intrinsic impedance of the perfect dielectric $\eta = \frac{|E|}{|H|} = \sqrt{\frac{\mu}{E}}$ and show that its value in free space is 377Ω. **(08 Marks)**

b. A uniform plane wave of a frequency 300MHz travels in +x direction in a lossy medium with $E_r = 9$, $\mu_r = 1$ and $\sigma = 10$ mhos/m. Calculate γ, α, β and η. **(06 Marks)**

c. State and prove Poynting theorem. **(06 Marks)**

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18EC56

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the typical design flow for VLSI IC circuit using block diagram. **(08 Marks)**

b. Explain the trends in HDLs (Hardware Description Languages). **(04 Marks)**

c. Apply the bottom-up methodology to demonstrate the design of 4-bit ripple carry counter. **(08 Marks)**

OR

2 a. Define Module and Instance. Describe 4 different levels of abstractions used in Verilog HDL to describe target design. **(10 Marks)**

b. Explain top down design methodology and bottom up design methodology. **(10 Marks)**

Module-2

3 a. What are system tasks and compiler directives? Explain with example. **(08 Marks)**

b. Check the correctness of the following legal strings. If not, write the correct strings.

i) "This is a string displaying the % sign"
ii) "Out = in1 + in2"
iii) "Please ring a bell \ 007"
iv) "This is a backslash \ character \ n" **(04 Marks)**

c. Declare the following variables in verilog:

i) An 8-bit vector net called a_in
ii) A 32 bit storage register called address. Bit 31 must be in MSB. Set the value of the reg. to a 32 bit decimal number equal to 3.
iii) An integer called count
iv) A time variable called snap_shot
v) An array called delays, Array contains 20 elements of the type integer
vi) A memory MEM containing 256 words of 64 bits each
vii) A parameter cache-size equal to 512. **(08 Marks)**

OR

4 a. With a neat block diagram, explain the components of a verilog module by highlighting mandatory blocks. **(08 Marks)**

b. Explain the port connection rules of verilog HDL. **(08 Marks)**

c. A 4-bit parallel shift register has I/O pins as shown in Fig.Q.4(c) below. Write the module definition for this module shift_reg. Include the list of ports and port declaration. **(04 Marks)**

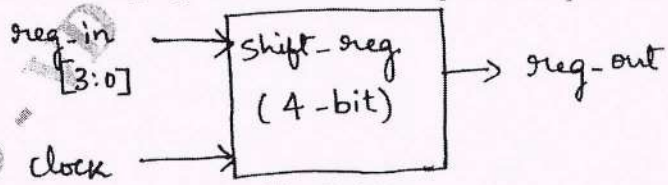

Fig.Q.4(c)

Module-3

5 a. Use gate level description of verilog HDL to design 4:1 MUX truth table, gate level block, logic expression and logic diagram. Write the stimulus block. **(10 Marks)**

b. Write gate level description to implement y = ab + c with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveforms. **(10 Marks)**

OR

6 a. Write the dataflow modeling verilog code for 4-to-1 multiplexer using
i) Logic equation ii) Conditional operator. **(10 Marks)**

b. Explain assignment delay, implicit assignment delay and net declaration delay for continuous assignment statements with examples. **(04 Marks)**

c. Write a dataflow level verilog code using + and { } operators for 4-bit full adders. **(06 Marks)**

Module-4

7 a. Explain the blocking assignments and non-blocking assignment statements with relevant examples. **(08 Marks)**

b. Explain briefly the different types of event based timing control in verilog. **(08 Marks)**

c. Write a note on the following loop statements:
i) While loop ii) Forever loop. **(04 Marks)**

OR

8 a. Write a verilog behavioral code for 4 to 1 MUX using CASE statement. **(08 Marks)**

b. Explain the sequential and parallel blocks with examples. **(08 Marks)**

c. Define a function to multiple two 4-bit numbers 'a' and 'b'. The output is an 8 bit value. Invoke function by using stimulus and check results. **(04 Marks)**

Module-5

9 a. Write a note on:
i) Assign and deassign
ii) Overriding parameters. **(10 Marks)**

b. Create a design that uses the full adder. Use a conditional compilation ('if def.). Compile the fulladder 4 with def param statement if the text macro DPARAM is defined by the 'define statement; otherwise, compile the Fulladder4 with module instance parameter values. **(06 Marks)**

c. What will be the output of the $display statement shown below

```
Module TOP;
A a1( );
end module
Module A;
B b1( );
end module
Module B;
initial
$display {"I am inside instance % m"); end module.
```

(04 Marks)

OR

10 a. With a neat flow chart explain computer-aided logic synthesis process. **(10 Marks)**

b. Write RTL description for magnitude comparator. **(06 Marks)**

c. What is logic synthesis? **(04 Marks)**

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CBCS SCHEME

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17EC/TE/BM/ML/EI/ES51

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Management and Entrepreneurship Development

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Management. Explain different Management functions. **(10 Marks)**
b. What are the different roles of a Manager? **(05 Marks)**
c. Draw the diagram of Skill – mix at different Managerial levels and explain. **(05 Marks)**

OR

2 a. What is the importance of Planning? **(05 Marks)**
b. Distinguish between two forms of Planning. **(05 Marks)**
c. Explain essential steps in decision making. **(10 Marks)**

Module-2

3 a. List and explain principles of Organizing. **(10 Marks)**
b. What is the meaning of delegation of Authority? Discuss the advantages of effective delegation. **(05 Marks)**
c. Describe : i) Job analysis ii) Job description iii) Job specification. **(05 Marks)**

OR

4 a. Discuss Maslow's Need - Hierarchy theory. **(05 Marks)**
b. Briefly explain the principle of effective communication. **(05 Marks)**
c. i) What are the benefits of Control system in Management?
ii) List the requisites of Excellent Communication. **(10 Marks)**

Module-3

5 a. Discuss Social responsibilities of business man towards different groups. **(10 Marks)**
b. Describe : i) Social Audit ii) Corporate Governance.
List out their benefits. **(10 Marks)**

OR

6 a. Define Entrepreneur. List and explain characteristics of an Entrepreneur. **(10 Marks)**
b. Discuss Myths of Entrepreneurship. **(10 Marks)**

Module-4

7 a. Outline the importance of Small Scale Industry. **(05 Marks)**
b. List out Internal and External problems faced by Small – Scale Industries and explain. **(10 Marks)**
c. Summarize the role of Small Scale Industries. **(05 Marks)**

OR

8 a. Discuss the services provided by the Small Industries Development Organization (SIDO). **(10 Marks)**

b. List out the schemes of : i) State Finance Corporations (SFCs).
ii) Small Scale Industrial Development Corporations (SSIDCs). **(10 Marks)**

Module-5

9 a. Explain Product – Planning and Development process. **(10 Marks)**

b. Briefly explain the sequential stages of Project formulation. **(10 Marks)**

OR

10 a. List out the 'Check list' for Feasibility report in Project report. **(10 Marks)**

b. Distinguish between PERT and CPM. **(10 Marks)**

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17EC52

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Signal Processing

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain frequency domain sampling and reconstruction of discrete time signals. **(10 Marks)**

b. Compute circular convolution of two sequences, $x_1(n) = \{1, 2, 3, 4\}$ and $x_2(n) = \{1, -1, 3, 2\}$, using DFT-IDFT method. **(06 Marks)**

c. Compute 16-point DFT of the sequence $x(n) = 8,\ 0 \le n \le 15$. **(04 Marks)**

OR

2 a. Compute N-point DFT of the sequence $x(n) = \sin\left(\dfrac{2\pi K_0 \eta}{N}\right),\ 0 \le n \le N-1$. **(08 Marks)**

b. Compute DFT of the sequence $x(n) = \sin\left(\dfrac{3\pi n}{4}\right) + \cos\left(\dfrac{\pi n}{4}\right),\ 0 \le n \le 3$, using linearity property of DFT. **(06 Marks)**

c. Derive the relationship between DFT and DTFS coefficients. **(06 Marks)**

Module-2

3 a. The 4-point DFT of a length-4 sequence x(n) is given by X(k) = {8, -1+j, -2, -1-j}. Obtain y(k), the 4-point DFT of the sequence $y(n) = e^{\frac{-j\pi n}{2}} x((n-1))_4$. **(05 Marks)**

b. Given a sequence x(n) = {1, -1, 2, -2}, determine DFT{DFT{DFT{DFT{x(n)}}}}, using complex conjugate properties of DFT. **(07 Marks)**

c. Determine the filter output y(n), whose impulse response h(n) = {1, -1, 2} and input x(n) = {1, 4, 3, 2, 1, -1, 2, 1, 5, 3, 2, 4}, using overlap-save method. Consider 8-point circular convolution approach. **(08 Marks)**

OR

4 a. The 4-point DFT of a sequence x(n) is given by x(k) = {16, -4+j4, -4, -4-j4}. Determine the energy of x(n) using Parseval's theorem. **(04 Marks)**

b. The IDFT {x(k)} is given by x(n) = {1, 2, 3, 4}. Determine IDFT of the following sequences: i) x(4-k) ii) j^k x(k) iii) Re{x(k)} iv) Im {x(k)} **(10 Marks)**

c. Discuss the need of FFT algorithms for computation of DFT. **(06 Marks)**

Module-3

5 a. Compute 8-point DFT of the sequence x(n) = {0.707, 0, -0.707, -1, -0.707, 0, 0.707, 1} using DIT-FFT algorithm. **(08 Marks)**

b. Starting from the expression of Z-transform of an N-point sequence x(n), derive chirp z-transform algorithm. **(08 Marks)**

c. Mention the similarities and differences between DIT-FFT and DIF-FFT algorithm. **(04 Marks)**

OR

6 a. Develop the radix-2 DIF-FFT algorithm for N = 8 and draw the signal flow graph. **(10 Marks)**

b. Given x(n) = {1, 2, 3, -1}, obtain x(1) using Goertzel algorithm and also explain Goertzel Algorithm. **(10 Marks)**

Module-4

7 a. Obtain a parallel realization for the transfer function H(z) given below:

$$H(z)=\frac{8z^3-4z^2+11z-2}{\left(z-\frac{1}{4}\right)\left(z^2-z+\frac{1}{2}\right)}$$ **(06 Marks)**

b. Derive an expression for order and cut-off frequency of low-pass Butterworth filter. **(08 Marks)**

c. Transform the analog filter,

$$H_a(s)=\frac{s+1}{s^2+5s+6}$$

into digital filter, H(z) using impulse invariant transformation. Consider T = 0.1 sec. **(06 Marks)**

OR

8 a. Design a digital filter H(z) that when used in A/D – H(z) – D/A structure gives an equivalent analog filter with the following specifications: Passband attenuation ≤ 3.01dB, Passband edge frequency = 500Hz, Stopband attenuation ≥15dB, Stopband edge frequency = 750Hz and sampling rate = 2kHz. The filter is to be designed by performing bilinear transformation on Butterworth analog filter. **(12 Marks)**

b. A linear time-invariant digital IIR filter is specified by the transfer function,

$$H(z)=\frac{(z^2-1)(z^2-2z)}{\left(z^2+\frac{1}{16}\right)\left(z^2-z+\frac{1}{2}\right)}$$

Obtain direct form-I and direct form-II realizations of the system. **(08 Marks)**

Module-5

9 a. A filter is to be designed with the following desired frequency response:

$$H_d(w)=\begin{cases}0, & |w|<\pi/4\\ e^{-j2w}, & \pi/4<|w|<\pi\end{cases}$$

Find the frequency response of the FIR filter designed using rectangular window. **(10 Marks)**

b. Given the FIR filter with the following difference equation:
y(n) = x(n) + 3.1x(n-1) + 5.5x(n-2) + 4.2x(n-3) + 2.3x(n-4)
Sketch the lattice realization of the filter. **(10 Marks)**

OR

10 a. The frequency response of an ideal band pass filter is given by;

$$H_d(w)=\begin{cases}e^{-j3w}, & 1<|w|<2\\ 0, & |w|<1 \text{ or } 2<|w|<\pi\end{cases}$$

Design an FIR bandpass filter which approximates the above filter, using Hamming window. **(10 Marks)**

b. Realize the linear-phase FIR filter having the following impulse response:

$$h(n)=\delta(n)+\frac{1}{4}\delta(n-1)-\frac{1}{8}\delta(n-2)+\frac{1}{4}\delta(n-3)+\delta(n-4)$$ **(05 Marks)**

c. Realize an FIR filter with impulse response h(n) given by, $h(n)=\left(\frac{1}{2}\right)^n[u(n)-u(n-4)]$, using direct form-I. **(05 Marks)**

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17EC53

Fifth Semester B.E. Degree Examination, Jan./Feb.2021
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the typical design flow for designing VLSI IC circuits with neat block diagram. **(10 Marks)**

b. Explain the Top down and Bottom up design methodology with an suitable example. **(10 Marks)**

OR

2 a. Explain the following components in a simulation (i) Design block (ii) Stimulus block. **(06 Marks)**

b. Make use of T-Flip Flop build a 4-bit Ripple carry counter and explain the design hierarchy. **(10 Marks)**

c. Explain the Trends in HDLs. **(04 Marks)**

Module-2

3 a. List all the lexical convention used is verilog and explain with examples. **(08 Marks)**

b. Explain the two methods of connecting ports to external signal with an example. **(08 Marks)**

c. Explain the compiler directives in verilog HDL. **(04 Marks)**

OR

4 a. What are the data types in verilog? Explain the following data types with suitable example:
(i) Nets (ii) Parameter (iii) Array (iv) Memory **(08 Marks)**

b. Write the Verilog code for SR Latch using gate level mode and also write stimulus code. **(06 Marks)**

c. With neat block diagram, explain the components of verilog module. **(06 Marks)**

Module-3

5 a. Explain the following gate primitives used in verilog HDL with truth table:
(i) Bufif (ii) notif **(04 Marks)**

b. Construct a 4-bit Ripple carry adder and develop the verilog code using gate level model, also write stimulus code. **(08 Marks)**

c. What should be the output of the following: $A = 4'd_{10}$, $B = 4'd_{13}$, $C = 4'b_{|0X|}$.
(i) A^ B (ii) |B (iii) B >> 2 (iv) A >>>2 (v) Y = {3{A},2{B}}
(vi) Y = {A[2:0], B[3:1]} (vii) A & C (viii) A || B **(08 Marks)**

OR

6 a. Construct a 4-bit carry look ahead adder and develop the verilog code using data flow description. **(08 Marks)**

b. Write the verilog code for 4 to l multiplexer using conditional operator. **(06 Marks)**

c. What are Rise, Fall and Turnoff delays? How they are specified in verilog? **(06 Marks)**

Module-4

7 a. Explain the blocking and non blocking assignment statements with suitable example. **(06 Marks)**

b. What are the different delay based timing controls are associated with verilog HDL and explain with relevant example. **(08 Marks)**

c. Using case statement, design an 8-function ALU that takes 4-bit inputs 'a' and b and a 3-bit input signal select 1, and gives a 5-bit output 'out'. The ALU implements the following functions based on a 3 bit input signal select. Ignore any overflow or underflow bits.

Select signal	$3'd_0$	$3'd_1$	$3'd_2$	$3'd_3$	$3'd_4$	$3'd_5$	$3'd_6$	$3'd_7$
Function (out)	a	a + b	a – b	a/b	a % b	a<<1	a>>1	a>b

(06 Marks)

OR

8 a. Explain the sequential and parallel blocks with suitable example. **(08 Marks)**

b. Write a verilog code for 4 to 2 priority encoder using casex. **(04 Marks)**

c. List the loop statements in verilog. Explain the following loops with examples:
(i) For loop (ii) Repeat **(08 Marks)**

Module-5

9 a. Compare VHDL and Verilog HDL. **(04 Marks)**

b. Explain the synthesis process with a neat block diagram. **(08 Marks)**

c. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL? **(08 Marks)**

OR

10 a. Explain the following Data Objects in VHDL with examples :
(i) Constant (ii) Signals (iii) Variables. **(09 Marks)**

b. What are the data types in VHDL? Explain the Scalar data types with examples. **(07 Marks)**

c. Write the VHDL code for a 4-bit wide register ensure that the input DATA [3 : 0] is stored only when the 'CLOCK' signal is detected on its rising edge. **(04 Marks)**

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17EC54

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Information Theory and Coding

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Obtain an expression for average information content of long independent messages. **(05 Marks)**

b. A block and white TV picture consists of 256 lines of picture information. Assume that each line consists of 526 picture elements and that each can have 255 brightness levels. Picture is repeated at the rate of 30 frames/sec. Calculate the average rate of information conveyed by TV picture. **(05 Marks)**

c. For the Markov model shown in Fig.Q1(c). Find :
i) State probabilities
ii) State and source entropy
iii) G_1, G_2 and show that $G_1 > G_2 > H$.

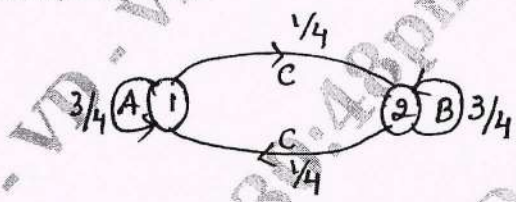

Fig.1(c) **(10 Marks)**

OR

2 a. A source emits one of four probable messages M_1, M_2, M_3 and M_4 with probabilities of 7/16, 5/16, 1/8 and 1/8 respectively. Find the entropy of the source. List all the elements of second order extension of this source. Hence show that $H(s^2) = 2H(s)$. **(06 Marks)**

b. Define the following :
i) Unit of information
ii) Entropy
iii) Self information
iv) Information rate. **(04 Marks)**

c. For the Markov model shown in Fig.Q2(c). Find :
i) State probabilities
ii) State entropy
iii) Source entropy
iv) Rate of information if $r_s = 1$ sym/sec.

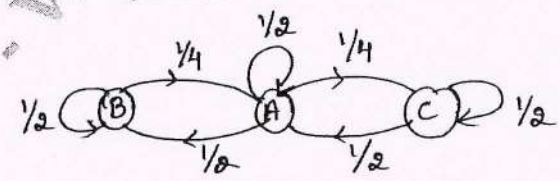

Fig.Q2(c) **(10 Marks)**

Module-2

3 a. Using Shannon's binary encoding algorithm, find all the codewords for the symbols, P = {0.55, 0.15, 0.15, 0.1, 0.05}. Also find its efficiency and redundancy. **(10 Marks)**

b. Consider the source, S = {A, B, C, D, E, F} with P = {0.1, 0.15, 0.25, 0.35, 0.08, 0.07}. Find the codewords for the source using Shannon – Fano algorithm. Also find the source efficiency and redundancy. **(05 Marks)**

c. Encode the following information using LZ algorithm : "THIS_IS_HIS_HIT". **(05 Marks)**

OR

4 a. An information source has a sequence of independent symbols with probabilities as follows :
S = {A, B, C, D, E, F, G, H}
P = {0.4, 0.25, 0.12, 0.08, 0.05, 0.05, 0.03, 0.02}.
Construct binary and ternary code using Huffman encoding procedure and find its efficiency redundancy. **(10 Marks)**

b. Explain prefix coding and Kraft – McMillan inequality with an example. Also draw the decision diagram for the prefix codes. **(05 Marks)**

c. Consider a discrete memoryless source with S = {X, Y, Z}, probabilities P = {0.5, 0.3, 0.2}. Find the code word for the message "YYZXZY" using arithmetic coding. **(05 Marks)**

Module-3

5 a. For the joint probability matrix given find :
i) H(X) ii) H(Y) iii) H(X, Y) iv) H(Y/X) v) H(X/Y) vi) I(X, Y).

$$JPM = P(X,Y) = \begin{array}{c} \\ x_1 \\ x_2 \\ x_3 \\ x_4 \end{array} \begin{array}{c} \begin{array}{cccc} y_1 & y_2 & y_3 & y_4 \end{array} \\ \begin{bmatrix} 0.05 & 0 & 0.20 & 0.05 \\ 0 & 0.10 & 0.10 & 0 \\ 0 & 0 & 0.20 & 0.10 \\ 0.05 & 0.05 & 0 & 0.10 \end{bmatrix} \end{array}$$ **(10 Marks)**

b. Prove that mutual information is always positive. **(05 Marks)**

c. Find the channel capacity of the channel shown in Fig.Q5(c), by Muroga's method given $p(x_1) = 0.6$, $p(x_2) = 0.4$.

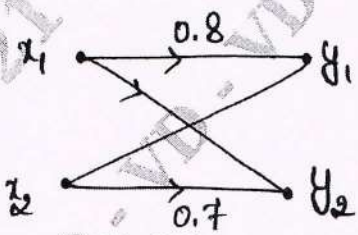

Fig.Q5(c) **(05 Marks)**

OR

6 a. Obtain an expression for the channel capacity of binary symmetric channel. **(05 Marks)**

b. For a channel matrix $p(Y/X) = \begin{bmatrix} 3/4 & 1/4 \\ 1/4 & 3/4 \end{bmatrix}$, given $p(x_1) = 2/3$, $p(x_2) = 1/3$, r_s = 1000 sym/sec. Find H(X), H(Y), H(X, Y), H(Y/X), H(X/Y), I(X, Y) and channel capacity, information rate. **(10 Marks)**

c. Define mutual information and prove that H(X/Y) = P·H(X) for a binary erasure channel. **(05 Marks)**

Module-4

7 a. For a systematic (7, 4) linear block code, parity matrix is given by,

$$P = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}.$$

i) Find all the possible valid code words
ii) Draw the encoding and syndrome calculation circuit.
iii) A single error has occurred in each of the following code words given,
$R_A = [0\ 1\ 1\ 1\ 1\ 1\ 0]$, $R_B = [1\ 0\ 1\ 1\ 1\ 0\ 0]$. Detect and correct the errors. **(10 Marks)**

b. The generator polynomial of a (7, 4) cyclic code is $g(x) = 1 + x + x^3$, find the codewords for message vectors (1010), (1110), (1100) and (1111) using systematic and non-systematic form. **(10 Marks)**

OR

8 a. A (6, 3) linear block code has the following check bits $C_4 = d_1 + d_2$, $C_5 = d_1 + d_3$ and $C_6 = d_2 + d_3$.
i) Write the G and H matrices
ii) Draw the encoding and syndrome calculation circuits.
iii) Construct the standard array and through example illustrate decoding operation. **(10 Marks)**

b. Consider (15, 5) linear cyclic code with generator polynomial,
$g(x) = 1 + x + x^2 + x^4 + x^5 + x^8 x^{10}$
i) Draw the encoder and syndrome circuit
ii) Find the code vector for the message polynomial $d(x) = 1 + x^2 + x^4$ by listing the states of the shift registers.
iii) Is $V(x) = 1 + x^4 + x^6 + x^8 + x^{14}$ a code polynomial? If not find the syndrome. **(10 Marks)**

Module-5

9 a. Consider a(3, 1, 2) convolution code with impulse responses $g^{(1)} = (110)$, $g^{(2)} = (101)$, $g^{(3)} = (111)$.
i) Draw the encoder diagram
ii) Find the generator matrix
iii) Find the code vector for the information sequence (11101) using time domain and transform domain approach. **(10 Marks)**

b. Write short notes on :
i) BCH code
ii) Golay codes. **(10 Marks)**

OR

10 a. Consider the convolutional encoder shown in Fig.Q10(a).
i) Draw the state table, state transition table and state diagram
ii) Using the code tree, find the encoded sequence for the message vector (10111)
iii) Verify the output sequence so obtained using transform domain approach.

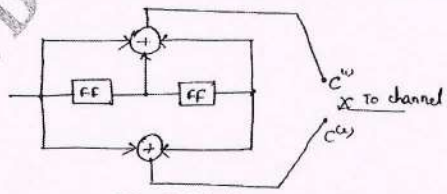

Fig.Q10(a) **(10 Marks)**

b. Explain viterbi decoding algorithm with an example. **(10 Marks)**

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17EC553

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Operating System

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Operating System. Discuss various resource allocation techniques. **(10 Marks)**

b. Explain different computational structures of Operating System with examples. **(10 Marks)**

OR

2 a. Explain different classes of Operating Systems. **(10 Marks)**

b. Discuss using timing chart ;

i) When CPU bound program has higher priority.

ii) When I/O bound program has higher priority. **(10 Marks)**

Module-2

3 a. Define a Process and discuss OS view of a process. **(08 Marks)**

b. Discuss various states transition for a process. **(06 Marks)**

c. Explain the various field of a PCB. **(06 Marks)**

OR

4 a. Explain Long term. Medium and Short term scheduling. **(10 Marks)**

b. Discuss two representative approaches to implementation of threads. **(10 Marks)**

Module-3

5 a. Compare and contrast Contiguous and non Contiguous memory allocation techniques. **(08 Marks)**

b. Write short notes on : i) Paging ii) Segmentation. **(12 Marks)**

OR

6 a. Explain Demand paging preliminaries. **(10 Marks)**

b. With an example, discuss FIFO , LRU page replacement policy. **(10 Marks)**

Module-4

7 a. Explain the interface between File system and IOCS. **(10 Marks)**

b. Compare and contrast Sequential file organization and Direct file organization. **(10 Marks)**

OR

8 a. Explain Directory structures. **(10 Marks)**

b. Discuss briefly File system actions at OPEN and CLOSE. **(10 Marks)**

Module-5

9 a. Define Message passing and Explain how it could be implemented. **(10 Marks)**

b. Discuss the following with respect to main box : i) Features ii) Advantages iii) Air line reservations Server using 3 mail boxes. **(10 Marks)**

OR

10 a. Define Deadlock. Discuss Resource request and allocation graph and Wait – for – graph for a system containing resource class and processes. **(10 Marks)**

b. Explain Deadlock Detection Algorithm. **(10 Marks)**

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17EC561

Fifth Semester B.E. Degree Examination, Jan./Feb.2021
Automotive Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain different strokes of four stroke SI engine, with suitable diagrams. **(10 Marks)**

b. Explain the working of disk brake system with neat diagram. **(10 Marks)**

OR

2 a. Define engine performance terms power, BSFC, torque and thermal efficiency with relevant formulae and their units. **(08 Marks)**

b. Explain the effect of Air/Fuel ratio and spark timing on engine performance. **(12 Marks)**

Module-2

3 a. Explain the working of MAF sensor with neat diagram. **(10 Marks)**

b. Explain the working of magnetic reluctance position sensor with relevant diagram and waveforms. **(10 Marks)**

OR

4 a. What is Hall effect? Explain the working of Hall effect position sensor with neat diagram. **(10 Marks)**

b. Explain the working of fuel Injector and pulse mode fuel control signals with relevant diagrams and waveforms. **(10 Marks)**

Module-3

5 a. What are seven modes of fuel control? Explain engine warmup with relevant equations. **(10 Marks)**

b. Explain Exhaust Gas Recirculation (EGR) control with a neat block diagram. **(10 Marks)**

OR

6 a. With the help of block diagram, explain secondary air control system. **(12 Marks)**

b. Explain the working of Idle air control with relevant block diagram. **(08 Marks)**

Module-4

7 a. Explain briefly the following:
(i) MOST BUS (ii) LIM BUS. **(10 Marks)**

b. Explain Digital Cruise control system with neat block diagram. **(10 Marks)**

OR

8 a. With relevant diagram, explain Antilock brake system. **(10 Marks)**

b. Explain Digital Speed Sensor with relevant diagrams and waveforms. **(10 Marks)**

Module-5

9 a. Explain the Timing light used to measure and set ignition timing with neat block diagram. **(10 Marks)**

b. Explain Accelerometer based Airbag system with relevant diagrams. **(10 Marks)**

OR

10 a. Explain collision avoidance Radar warning system with block diagram. **(12 Marks)**

b. With relevant diagram, explain Dead Reckoning navigation system. **(08 Marks)**

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15ES51

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Management and Entrepreneurship Development

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1	a.	Define Management. Explain the various functions of Management.	(08 Marks)
	b.	What is Scientific Management formulated by F.W. Taylor? Explain.	(04 Marks)
	c.	Differentiate between Management and Administration.	(04 Marks)
		OR	
2	a.	Explain the various steps involved in planning.	(08 Marks)
	b.	What are the important characteristics of decision making?	(04 Marks)
	c.	Explain briefly the levels of management.	(04 Marks)

Module-2

3	a.	What are the principles of an organization? Explain.	(08 Marks)
	b.	Explain the importance of Staffing.	(04 Marks)
	c.	What is Leadership? Explain.	(04 Marks)
		OR	
4	a.	Define Directing and explain the steps involved in controlling.	(06 Marks)
	b.	What is Motivation? Explain Maslow's Need Hierarchy Theory.	(06 Marks)
	c.	Explain the centralization of authority with an example.	(04 Marks)

Module-3

5	a.	Define Social responsibility and its responsibility towards other groups.	(08 Marks)
	b.	Explain the term Corporate Governance.	(04 Marks)
	c.	What are the qualities of an Entrepreneur?	(04 Marks)
		OR	
6	a.	Explain the role of Entrepreneurs in the Economic growth of any country.	(06 Marks)
	b.	What are the functions of Entrepreneur? Explain with examples.	(06 Marks)
	c.	Write a note on Women Entrepreneur.	(04 Marks)

Module-4

7	a.	What are the steps involved in setting up of Small Scale Industry (SSI)? Explain.	(08 Marks)
	b.	Explain briefly the objectives of KSFC and TECSOK.	(08 Marks)
		OR	
8	a.	Explain the role of SSI in Economic development of the Country.	(08 Marks)
	b.	Explain the Impact of Globalization on SSI.	(04 Marks)
	c.	Write short note on SIDO.	(04 Marks)

Module-5

9	a.	Define Project. Explain briefly characteristics of project.	(06 Marks)
	b.	Explain briefly the Project Life Cycle.	(06 Marks)
	c.	Differentiate between PERT and CPM.	(04 Marks)
		OR	
10	a.	Explain briefly the steps in PERT with its advantages and limitations.	(08 Marks)
	b.	Explain the phases in Project Management.	(04 Marks)
	c.	Briefly explain the stages of Project Formulation.	(04 Marks)

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15EC52

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Signal Processing

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Evaluate 8-point DFT of the sequence :

$$x(n)=\begin{cases}\left(\frac{1}{2}\right)^{n+1}; & -2\le n\le 2\\ 0 \quad ; & 3\le n\le 5\end{cases}$$

Also draw the magnitude and phase plots. **(12 Marks)**

b. Given $x_1(n) = \delta(n-1) - \delta(n-3)$ and $x_2(n)=\cos\left(\frac{2\pi n}{4}\right)$; $0 \le n \le 3$ perform $x_1(n) \circledast_4 x_2(n)$ using DFT – IDFT method. **(04 Marks)**

OR

2 a. Find the DFT of the sequence (N = 4) $x(n)=\{\underset{\uparrow}{0.5},0,0.5,0\}$ using Z- transforms. **(04 Marks)**

b. The first five samples of 8-point DFT X(K) are given by X(0) = 6, X(1) = –0.7071 – j1.7071, X(2) = 1 – j, X(3) = 0.7071 + j0.2929, X(4) = 0. Find the remaining samples of X(K) and hence find its time domain sequence x(n). **(10 Marks)**

c. Bring out the differences between linear convolution and circular convolution. **(02 Marks)**

Module-2

3 a. Let x(n) be a finite length sequence with $X(K)=\{\underset{\uparrow}{0},1+j,1,1-j\}$, using the properties of DFT find the DFT's of the following sequences.

i) $x_1(n)=e^{j\frac{\pi}{2}n}x(n)$

ii) $x_2(n)=\cos\{(\pi/2)n\}x(n)$

iii) $x_3(n)=x(4-n)$. **(06 Marks)**

b. Find the output of a FIR filter with impulse response $h(n)=\{\underset{\uparrow}{3},2,1,1\}$ and the input x(n) = {1, 2, 3, 3, 2, 1, –1, –2, –3, 5, 6, –1, 2, 0, 2, 1}. Use overlap add method using 7 point circular convolution. **(10 Marks)**

OR

4 a. Prove the periodicity and symmetric properties of twiddle factor. **(04 Marks)**

b. Evaluate the function $\sum_{K=0}^{15} e^{\frac{-j4\pi K}{8}} X(K)$ without computing DFT for a given 16-point sequence $x(n)=\{\underset{\uparrow}{3},2,1,0,0,4,-1,-2,-4,1,3,2,-1,5,1,4\}$. **(06 Marks)**

c. State and prove Parsaval's theorem as applied to DFT. **(06 Marks)**

Module-3

5 a. What are the total number of complex additions and multiplications required for 32-point DFT by using direct computation of DFT and by FFT methods? Also find the number of stages required, memory requirement and speed improvement factor by considering multiplication. **(07 Marks)**

b. Find the IDFT of the sequence :

$$X(K) = \left\{\underset{\uparrow}{36}, -4+j9.7, -4+j4, -4+j1.7, -4, -4-j1.7, -4-j4, -4-j9.7\right\}$$

Using radix -2 DIF – FFT algorithm. **(09 Marks)**

OR

6 a. Derive radix – 2 DIT –FFT algorithm and draw the complete signal flow graph for N = 8. **(08 Marks)**

b. Explain Goertizel algorithm and obtain the direct from II realization. **(08 Marks)**

Module-4

7 a. A digital filter has input $x(n) = \delta(n) + \frac{1}{4}\delta(n-1) - \frac{1}{8}\delta(n-2)$ and the output $y(n) = \delta(n) - \frac{3}{4}\delta(n-1)$. Realize the filter in direct form – I, direct form – II, cascade and parallel form. **(10 Marks)**

b. Given that $\left|H\left(e^{j\Omega}\right)\right|^2 = \frac{1}{1+64\Omega^6}$, determine the analog Butterworth low pass filter transfer function. **(06 Marks)**

OR

8 a. Compare Butterworth filter with Chebychev filters. **(04Marks)**

b. Design a digital filter H(Z) that when used in an A/D – H(z) – D/A structures given an equivalent analog filter with the following specifications :

Pass band ripple	: ≤ 3.01dB
Pass band edge	: 500Hz
Stop band edge	: 750Hz
Stop band attenuation	: ≥ 15dB

Sample rate f_s = 2KHz and T = 1sec. Use bilinear transformation to design the filter on an analog system. Also obtain the difference equation. **(12Marks)**

Module-5

9 a. Determine the impulse response of a FIR filter with reflection coefficients $K_1 = 0.6$, $K_2 = 0.3$, $K_3 = 0.5$ and $K_4 = 0.9$, also draw the direct form structure. **(12 Marks)**

b. List the advantages of FIR filter over IIR filters. **(04 Marks)**

OR

10 a. Design a FIR lowpass filter with a desired frequency response

$$H_d(e^{j\omega}) = e^{-j3\omega}; \quad \frac{-3\pi}{4} \le \omega \le \frac{3\pi}{4}$$

$$= 0 \; ; \quad \frac{3\pi}{4} < |\omega| < \pi$$

Use Hamming window with m = 7, also obtain the frequency response. **(10 Marks)**

b. Explain the following :

i) Rectangular window
ii) Hamming window
iii) Bartlett window. **(06 Marks)**

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15EC53

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the design flow of VLSI IC circuit steps with a neat flow chart. **(08 Marks)**
b. List the useful features of verilog HDL for hardware design. **(05 Marks)**
c. Explain the importance of HDL compared to traditional schematic based design. **(03Marks)**

OR

2 a. Explain TOP-down methodology applying to design of 4 bit Ripple carry counter. **(08 Marks)**
b. Explain the components of simulation. **(08 Marks)**

Module-2

3 a. Explain any four datatypes in vertilog. **(08 Marks)**
b. Explain in brief the system task and compiler directives. **(08 Marks)**

OR

4 a. Explain the concept of mapping of ports to external signals with one example. **(08 Marks)**
b. Declare top level module stimulus. Define REG – IN(4 bit) and CLK(1 bit) as reg register variables and REG – OUT (4 bit) as wire. Instantiate module shift-reg and call it sr1. Write hierarchical names for variables, REG – IN, CLK and REG – OUT. Also write hierarchical name for instance sr1. **(08 Marks)**

Module-3

5 a. Write a design block and stimulus block for 4 : 1 MUX using gate level modeling. **(08 Marks)**
b. Write a verilog code for function f = (ab + c) with specified delay and also draw neatly the simulated output waveform.(Ref. Fig.Q5(b)).

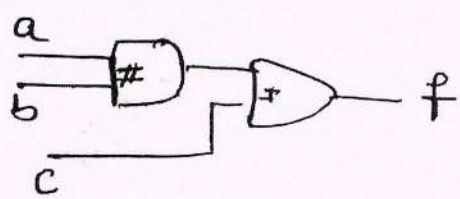

Fig.Q5(b) **(08 Marks)**

OR

6 a. Explain relational, equality and bitwise operators in verilog with example. **(06 Marks)**
b. Write data flow modeling for 4 bit FA with carry look ahead. **(10 Marks)**

Module-4

7 a. Describe multiway branching using case, case X, case Z with example. **(09 Marks)**
b. Write Behavioral modeling for 4 : 1 MUX using case statement. **(07 Marks)**

OR

8	a.	Describe while, for, forever statements in verilog with syntax.	**(09 Marks)**
	b.	Write behavioral modeling for 4 bit counter program in verilog.	**(07 Marks)**

Module-5

9	a.	Explain in brief the design process of using VHDL for design synthesis.	**(10 Marks)**
	b.	Explain the EDA tool flow with neat diagram.	**(06 Marks)**

OR

10	a.	Discuss the scalar data types used in VHDL.	**(08 Marks)**
	b.	Write a note on atlributes in VHDL.	**(08 Marks)**

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15EC54

Fifth Semester B.E. Degree Examination, Jan./Feb.2021
Information Theory and Coding

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define self-information and obtain an expression for entropy of a zero-memory information source emitting independent sequences of symbols. **(08 Marks)**

b. An analog signal is band limited to B Hz and sampled at Nyquist rate. The samples are quantized into 4 levels. Each level represents one message. Thus there are 4 messages. The probability of occurrence of these 4 levels (messages) are $P_1 = P_4 = \frac{1}{8}$ and $P_2 = P_3 = \frac{3}{8}$. Find out information rate of the source. **(08 Marks)**

OR

2 a. Explain Markoff model for information source. **(04 Marks)**

b. Obtain an expression for entropy of Markoff's source. **(04 Marks)**

c. For the first order Markov source with a source alphabet $S = \{A, B, C\}$ shown in Fig. Q2 (c) below. Compute the probabilities of state and entropy of source. **(08 Marks)**

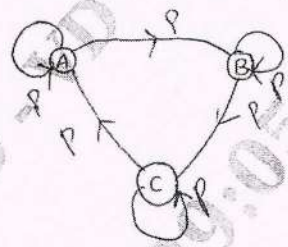


Fig. Q2 (c)

Module-2

3 a. Discuss the various properties of codes. **(04 Marks)**

b. What is Kraft Inequality? Clearly explain with suitable examples. **(06 Marks)**

c. Construct binary code for the following source using Shannon's binary encoding procedure, $S = \{S_1, S_2, S_3, S_4, S_5\}$, $P = \{0.4, 0.25, 0.15, 0.12, 0.08\}$ **(06 Marks)**

OR

4 a. Consider a zero-memory source with,
$S = \{S_1, S_2, S_3, S_4, S_5, S_6, S_7\}$, $P = \{0.4, 0.2, 0.1, 0.1, 0.1, 0.05, 0.05\}$

(i) Construct a binary Huffman code by placing the composite symbol as low as you can.

(ii) Repeat (i) By moving the composite symbol 'as high as possible'.

In each of the cases (i) and (ii) above. Compute the variances of the word-lengths and comment on the result. **(10 Marks)**

b. Compare Huffman coding and Arithmetic coding. **(04 Marks)**

c. State Shannon's first theorem (Noiseless coding theorem). **(02 Marks)**

Module-3

5 a. What is a discrete communication channel? Illustrate the model of a discrete channel. Obtain the equation for P(error) for such a channel. **(08 Marks)**

b. State and discuss Shannon's theorem on channel capacity. **(04 Marks)**

c. For the channel matrix shown below, find the channel capacity,

$$P\left(\frac{b_j}{a_i}\right) = \begin{array}{c} \\ a_1 \\ a_2 \\ a_3 \end{array} \begin{array}{c} \begin{array}{ccc} b_1 & b_2 & b_3 \end{array} \\ \begin{bmatrix} \frac{1}{2} & \frac{1}{3} & \frac{1}{6} \\ \frac{1}{3} & \frac{1}{6} & \frac{1}{2} \\ \frac{1}{6} & \frac{1}{2} & \frac{1}{3} \end{bmatrix} \end{array}$$

(04 Marks)

OR

6 a. State and prove Shannon-Hartley law. **(08 Marks)**

b. Discuss Muroga's method for estimating the channel capacity. **(08 Marks)**

Module-4

7 a. Illustrate the following terms used in error control coding with examples, (i) Block length (ii) Code rate (iii) Hamming weight (iv) Hamming distance (v) Minimum distance. **(10 Marks)**

b. What is the use of syndromes? Explain syndrome decoding. **(06 Marks)**

OR

8 a. The parity check matrix of a particular (7, 4) linear block code is given by,

$$[H] = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}.$$

(i) Find the generator matrix (G).
(ii) List all the code vectors.
(iii) What is the minimum distance between code vectors.
(iv) How many errors can be detected? How many errors can be corrected? **(10 Marks)**

b. For a systematic linear block code, the three parity check digits, C_4, C_5 and C_6 are given by

$C_4 = d_1 \oplus d_2 \oplus d_3$, $C_5 = d_1 \oplus d_2$; $C_6 = d_1 \oplus d_3$

(i) Construct the generator matrix.
(ii) Construct the code generated by this matrix. **(06 Marks)**

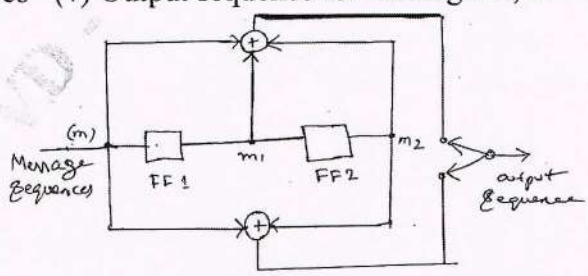
Module-5

9 a. Briefly explain the following codes:
(i) BCH codes (ii) Reed-Soloman codes. (iii) Golay codes. **(08 Marks)**

b. What are convolutional codes? With block diagram explain the operation of convolutional encoder. **(08 Marks)**

OR

10 For the convolutional encoder shown below in Fig.Q10, determine the following:
(i) Dimension of code. (ii) Code rate (iii) Constraint length
(iv) Generating sequences (v) Output sequence for message of, m = {1 0 0 1 1}. **(16 Marks)**



Convolutional encoder Fig. Q10

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15EC553

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Operating Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Operating System. Explain the functions of an Operation System. **(06 Marks)**

b. Explain goals of an Operating System, its operations and resource allocation of OS. **(10 Marks)**

OR

2 a. Briefly explain the different classes of Operating System, specifying the primary concern and key concepts used. **(10 Marks)**

b. Define the following:
i) System call
ii) Turn-around time
iii) Response time. **(06 Marks)**

Module-2

3 a. Define threads. Compare Kernel level threads and user level threads. **(08 Marks)**

b. Define Process Control Block. Explain the general structure of Process Control Block. **(08 Marks)**

OR

4 a. What do you mean by non preemptive and preemptive scheduling policies? **(04 Marks)**

b. With one example explain:
i) First Come First Serve scheduling
ii) Round Robin Scheduling. **(12 Marks)**

Module-3

5 a. Compare contiguous and non contiguous memory allocation techniques. **(08 Marks)**

b. Explain segmentation with paging. **(08 Marks)**

OR

6 a. List the functions performed by virtual memory handler. **(07 Marks)**

b. With suitable example, explain FIFO and LRU page replacement policies. **(09 Marks)**

Module-4

7 a. With neat diagram, write the logic organization in file system. Also list the facilities provided by the file system and the IOCS. **(08 Marks)**

b. List and explain two approaches to Non Contiguous disk space allocation. **(08 Marks)**

OR

8 a. With example explain sequential and direct access file organization. **(08 Marks)**

b. Explain the different operations performed on files. **(08 Marks)**

Module-5

9 a. Explain the inter process communication mechanism in unix Operating System. **(08 Marks)**

b. Define Mailbox. With an example explain mail box and mention its advantages. **(08 Marks)**

OR

10 a. Define Deadlock. List and explain three events concerning resource allocation to a user process. **(08 Marks)**

b. Write a note on Dead Lock prevention. **(08 Marks)**

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15EC561

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Automotive Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Briefly explain the four stroke cycle of an IC engine, with neat diagrams. **(08 Marks)**

b. What is drive train? With neat diagram, explain the planetary gear system. **(08 Marks)**

OR

2 a. Discuss the motivation for electronic engine control. **(08 Marks)**

b. What is Engine Mapping? Discuss the effect of spark timing on performance. **(08 Marks)**

Module-2

3 a. Explain the working of Mass Air Flow (MAF) sensor with relevant diagram. **(08 Marks)**

b. What is ignition system? With neat block diagram, explain the ignition system. **(08 Marks)**

OR

4 a. Explain the working of optical crank shaft position sensor. **(08 Marks)**

b. Explain EGR actuator control with a relevant diagram. **(08 Marks)**

Module-3

5 a. Explain with neat block diagram, components of electronically controlled engine. **(08 Marks)**

b. What are various modules of control unit software? Explain them briefly. **(08 Marks)**

OR

6 a. What is system diagnosis used on digital engine control system? Explain briefly. **(08 Marks)**

b. What is use of secondary air? With the help of a diagram, explain how the secondary air is controlled. **(08 Marks)**

Module-4

7 a. Explain with a neat diagram, digital speed sensor. **(08 Marks)**

b. What are CAM protocol layers? What are the four different frames? Write the message format. **(08 Marks)**

OR

8 a. Explain Digital Cruise control system with the help of relevant diagram. **(08 Marks)**

b. Explain the Antilock braking system with relevant diagrams. **(08 Marks)**

Module-5

9 a. What is occupant protection system? Explain the accelerometer based airbag system. **(08 Marks)**

b. With neat block diagram, explain the Radio Navigation. **(08 Marks)**

OR

10 a. Discuss the Heads Up Display and speech synthesis of a future automotive system. **(08 Marks)**

b. Write a brief note on On-board-Diagnostics and Off-board Diagnostics. **(08 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the nmos enhancement mode transistor operation for different values of V_{GS} and V_{DS}. **(06 Marks)**

b. Obtain the transfer characteristics of a CMOS inverter mark all the region, showing the status of PMOS and nmos transistor. **(10 Marks)**

OR

2 a. Explain the fabrication steps of CMOS P-well process with neat diagram, and write all the mask sequence. **(10 Marks)**

b. Distinguish between CMOS and bipolar technologies **(06 Marks)**

Module-2

3 a. With neat diagram, describe the design rules i) Transistor ii) wires iii) contact cut. **(08 Marks)**

b. Draw the Schematic and Mask Layout for the expression $Y = \overline{AB + CD}$. **(08 Marks)**

OR

4 a. Derive the expression for the Rise time and fall time for CMOS inverter. **(10 Marks)**

b. Two MOS inverters are cascaded to drive a capacitive load C_L = 14cg as shown in Fig Q4(b). Calculate the pair delays V_{in} to V_{out} in terms of τ.

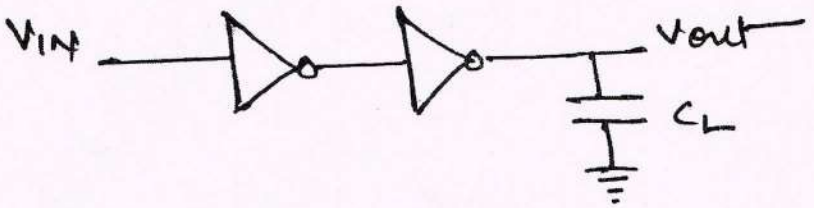

Fig Q4(b) **(06 Marks)**

Module-3

5 a. Why do we require scaling of MOS circuits? **(04 Marks)**

b. Find the scaling factors for the following :

i) Gate capacitance (C_g) ii) Saturation current (I_{ds})

iii) Gate capacitance per unit area (C_{ox}) iv) Carrier density in channel (Q_{ON})

v) Maximum frequency of operation (f_0) vi) Speed power product (P_T) **(12 Marks)**

OR

6 a. Discuss the General considerations of the subsystem Design process. **(06 Marks)**

b. Explain a standard Adder element using nmos version of adder logic. **(10 Marks)**

Module-4

7 a. Explain the multiplexer/Data selections with layout. **(10 Marks)**

b. Explain parity Generator with stick diagram. **(06 Marks)**

OR

8 a. Briefly explain Architecture of FPGA. **(10 Marks)**

b. Explain Antifuse base FPGA. **(06 Marks)**

Module-5

9 a. Explain one transistor DRAM. **(08 Marks)**

b. Explain Three Transistors DRAM. **(08 Marks)**

OR

10 a. Explain objectives of Functional Testing. **(06 Marks)**

b. Define fault model, explain the

i) Stuck – at Faults

ii) Stuck – open and stuck – short Fault

iii) Stuck – open Fault **(10 Marks)**

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