CBCS SCHEME

USN | | | | | | | | | | 18EC33

Third Semester B.E. Degree Examination, Aug./Sept.2020
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain different types of bonding in solids with the help of neat diagram. (10 Marks)
b. With a neat diagram explain direct and indirect semiconductor. (10 Marks)

OR

2 a. Explain Electron-Hole pair concept with the help of neat diagram and equations. (10 Marks)
b. What is Hall-effect? With suitable diagram and equation explain how does Hall-effect works? (10 Marks)

Module-2

3 a. What is tunneling? Explain voltage current characteristics of a tunnel diode with the help of energy band diagram. (10 Marks)
b. Mention the differences between Zener effect and Avalanche effect. (03 Marks)
c. Explain light emitting diode with a neat sketch. (07 Marks)

OR

4 a. Explain qualitative description of current flow at forward and reverse bias junction of a diode. (10 Marks)
b. How does photodiode works? a photovoltaic cell explain with the help of diagram? (10 Marks)

Module-3

5 a. Explain how BJT acts as a amplifier with the help of equation. (10 Marks)
b. Draw the Ebers – Moll model for a PNP transistor and explain its significance. (10 Marks)

OR

6 a. Explain how BJT acts as a switch with necessary equations and diagram. (10 Marks)
b. Explain specification for switching transistor BJT with suitable diagram. (04 Marks)
c. Explain the effect of base narrowing with neat diagram. (06 Marks)

Module-4

7 a. Explain the construction and operation of n-JFET with neat diagram and equations. (06 Marks)
b. Explain small signal equivalent circuit of JFET with neat diagram. (06 Marks)
c. Explain the principle of operation n-channel enhancement mode MOSFET with neat diagram and equations. (08 Marks)

OR

8 a. Explain two-terminal MOS structure using energy band diagram. (10 Marks)
b. Explain the principle of operation of p-channel enhancement mode MOSFET with neat diagram and equations. (10 Marks)

Module-5

9 a. Explain thermal oxidation process with neat diagram. (10 Marks)
b. What is metallization process explain with neat diagram by showing all the steps in the fabrication of p-n junctions. (10 Marks)

OR

10 a. Explain integration of other circuit elements with suitable diagrams. (10 Marks)
b. Explain CMOS process of integration with the help of neat diagram. (10 Marks)

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Subject : Electronic Devices

Sub. Code : 18EC33

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1)

a) Explain different types of bonding in solids with help of neat diag-rams

⇒ Types of bonding in solids are:- — (2M)

* Ionic bonding
* Metallic bonding
* Covalent bonding

→ Ionic bonding:-

* It is a type of chemical bonding formed by electrostatic interac-tion between oppositely charged species/ions
* The interaction between cation and anion of the neighbouring atom of a solids helps in holding the crystal together.
* For ex:- NaCl, each 'Na' atom is surrounded by six nearest Cl atoms
* The Electronic structure of sodium is

$Na = (Z=11) = 1s^2 2s^2 2p^6 3s^1$ i.e $[Ne]3s^1$

$Cl = (Z=17) = 1s^2 2s^2 2p^6 3s^2 3p^5$ i.e $[Ne]3s^2 3p^6$

* In the lattice each Na atom gives its outermost 3s electron to the chlorine atom to attain inert gas configuration of Argon i.e $[Ne]3s^2 3p^6$, Hence outermost shell is completely filled
* As Na atom gives out an electron to attain a net positive charge whereas the Cl^- accept the e^- and attain net negative charge
* As the ions have the closed shell configuration of inert atoms Ne and Ar, so no free e^- hence there is no current flow & D NaCl is good insulator, Na^+ ions attracts 6 neighbouring Cl^- ion to attain equilibrium

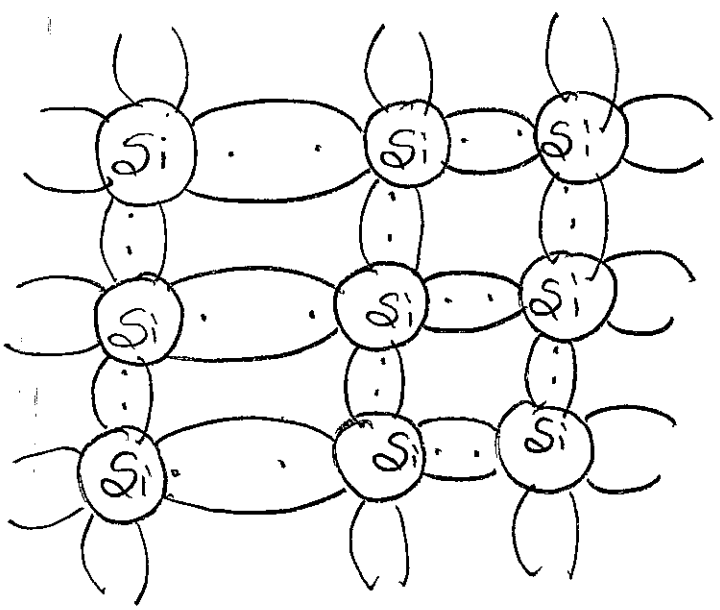
1

⇒ Metallic bonding :-

* It is a type of chemical bonding formed by electrostatic forces between conduction $\bar{e}$ and a positively charged meta ions
* In metal atoms the outermost shell is partially filled, so donate electrons to the lattice it attains compelte configuration, Hence these donated / free $\bar{e}$ helps in conduction
* In the metal outer $\bar{e}$ of each alkali metal is contributing to the crystal, which is made up of ions with closed shell is immersed in a sea of free $\bar{e}$

⇒ Covalent bonding :-

* It is a type of chemical bonding which formed by sharing a valence electron and these type usually see in C, Ge, Si
* Here each $\bar{e}$ pair constitutes a covalent bond
* As the covalent bonds are weak bonds, at lower temperature it posses the properties of insulators
* When the temperature increases the covalent bonds breaks and free electrons are produced which helps in conduction.



— (10m)

b) With a neat diagram explain direct and indirect semiconducto

* The wave function of $\bar{e}$ is assumed to be in the form of a pla wave moving in the x direction with propagation constant k also called a wave vector

* The space dependent wave function for the $\bar{e}$ is $\psi_k(x) = U(k_x, x) e^{ik_x x}$ where the function $U(k_x, x)$ modulates the wave function due to the periodicity of the lattice

* The band structure of GaAs has a minimum in the conduc band and a maximum in the valence band for some value of

* Si has its value band of valence band maximum at a diffrent value of k, than its conduction band is minimum, thus an $\bar{e}$ making a smallest energy transition from the conduction band to the valence band in GaAs can do so without a change in k value

* The transition from the minimum point in the Si conduction band to maximum point of the valence band requires some change in k

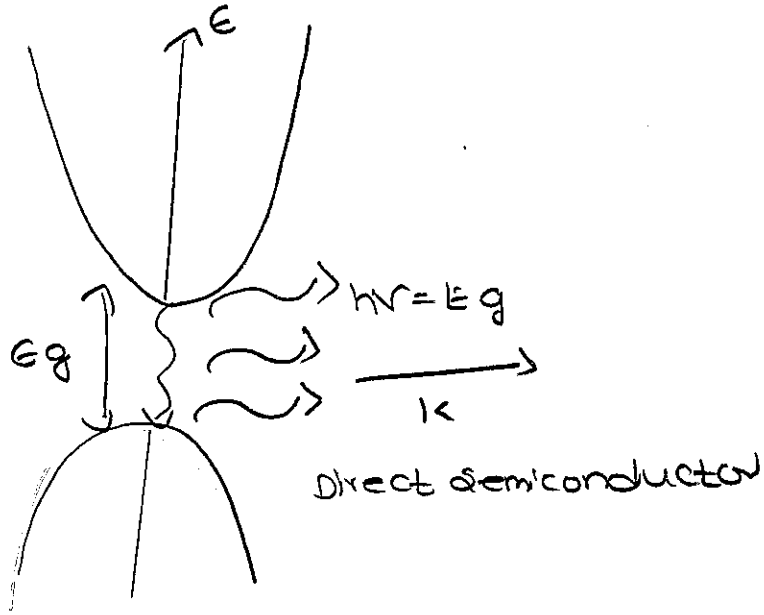
* Thus there are 2 classes of semiconductor energy bands, we can show that an indirect transition involving a change in k, requires a change of momentum for the electrons

* In direct and indirect semiconductors are identified in the Appendix III, In a direct semiconductors such as GaAs an $\bar{e}$

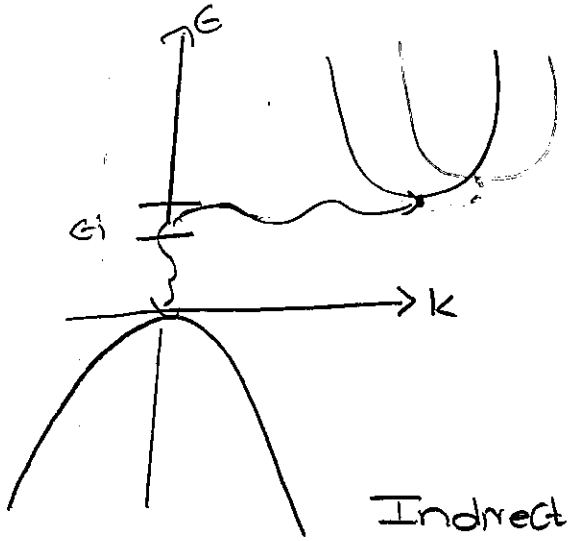
* The conduction band can fall to an empty state in the valence band giving off the energy difference Eg as a photon of light

(7m)

* An $\bar{e}$ in the conduction band minimum of the indirect semiconductor such as Si cannot fall directly to valence band maximum but must undergo a momentum change as well as changing its energy
* In an direct transition which involves a change in k, part of the energy is generally given up as heat to the lattice rather than as an emitted photon
* The difference between direct and indirect band structures is very important for deciding which semiconductor can be used devices requiring light output



(3m)



2)

a) Explain electron-hole pair concept with the help of need diagram and equations

* As the temperature of a semiconductor is raised from 0 k, some e^- in the valance band recieve enough thermal energy to be excited across the bandgap to conduction gap
* A empty state in the valence band is reffered to as hole
* If the conduction band e^- and holes are created by the excitation of a e^- in valence band to conduction band, they are called as electron-hole pair (EHP)
* After the excitation to the conduction band, an e^- is surrounded by a large no of unoccupied energy state, thus the few e^- are free move
* In a filled band, all available energy states are occupied
* For every e^- moving with a given velocity, there is an equal and opposite e^- motion
* If we apply an electric field, the net current is zero because every electron moving with velocity V_j, there is corresponding elec with velocity $-V_j$
* A valence band with all state filled including state j and j', The jth e^- with wave vector k_j is matched by e^- at j' with opposi wave vector $-k_j$, There is no net current in the band
* Since K is propotional to e^- momentum, it is clear the two e^- have oppositely directed velocities

* with $n\bar{e}/cm^3$ in the bond we express the current density, using sum all $\bar{e}$ velocities and including the charge $-q$ on each $\bar{e}$

$$J = (-q)\sum_{i}^{n} v_i = 0 \quad \text{(Filled bond)}$$

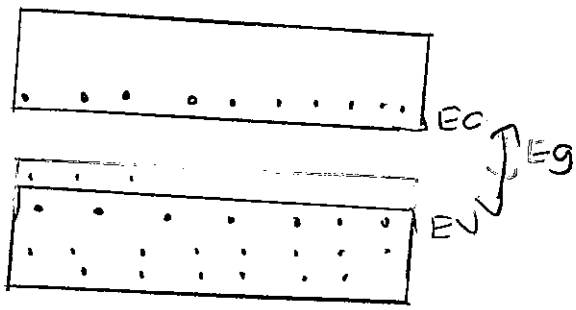
* now if we create a hole by removing the jth $\bar{e}$ the net current density in the volance bond involve sum of all velocities the contribution of jth $\bar{e}$ removed

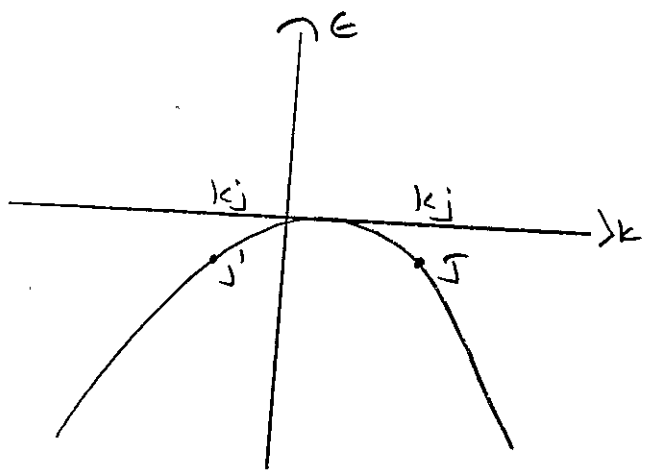
$$J = (-q)\sum_{i}^{n} v_j \; (-q)v_j \quad (j^{th}\ \bar{e} \text{ is removed})$$

$$J = \pm q v_j \quad (\because -q\sum_{i}^{n} v_i = 0)$$

* The net current is $+qv_j$, the current constibution of the hole is equivalent to that of +ve charge particle with velocity v_j
* The bottom of the conduction bond corresponds to zero $\bar{e}$ velocity or kinetic energy (kE)
* For the holes at the top of valence band corresponds to Zero kE
* Energies higher in the bond correponde to additional KE of the electron
* Correspondingly, the $\bar{e}$ stasts at $k=0$, but moves to a non zero vector k_B
* The $\bar{e}$ then looses KE to heat by scattering mechanism and return to the bottom of the bond of B

— (6m)

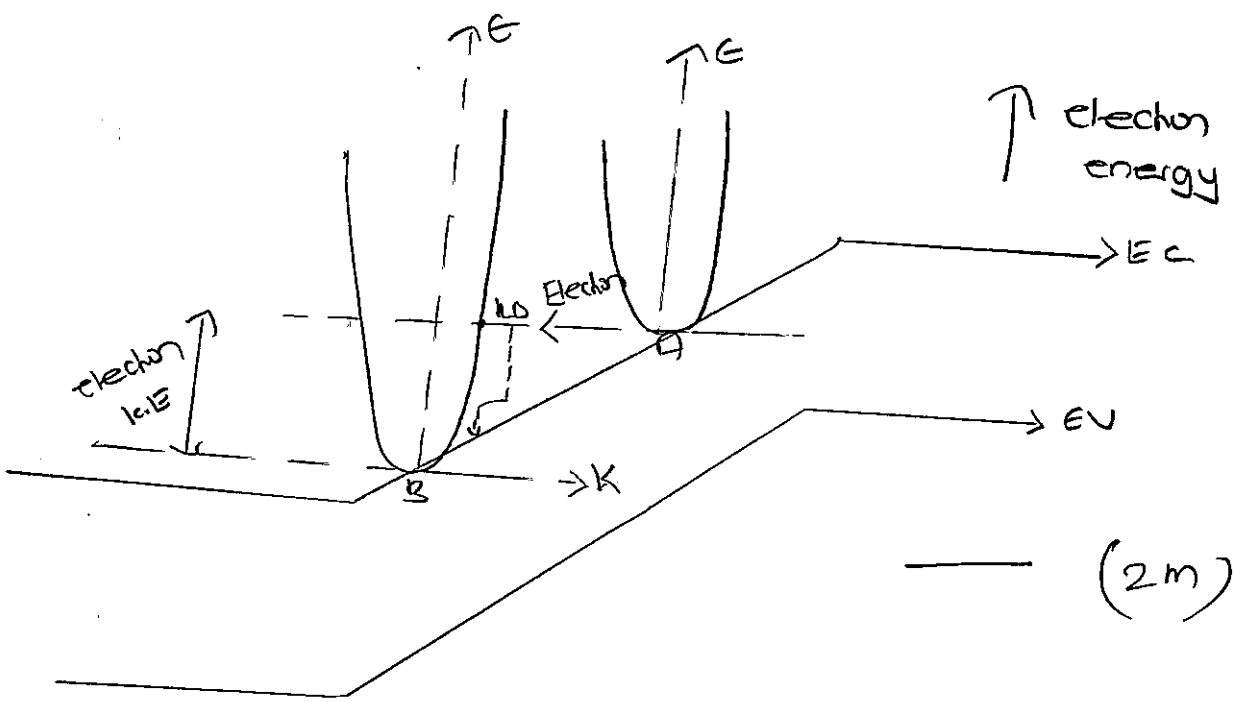




electron energy Vs wave vector in valence band

(2m)

⇒ Electron energy Vs wave vector in conduction band



(2m)

Q2) b) What is Hall-effect? Explain how does Hall-effect Works?

* If a magnitude field is applied perpendicular to the direction in which holes drift in a p-type bar, the path of the holes tends to be deflected
* Using vector motion, notation the total force on a single hole due to electric and magnetic field is

$$F = q(E + V \times B)$$

* In the y-direction the force is

$$y = q(E_y - V_x B_z)$$

* Unless an electric field and E_y is established along the width of bar, each hole will experience a net force in the y-direction due to the $q, V_x B_z$ product
* Therefore to main steady state flow of holes down the length of bar, the electric field is E_y must balance product $V_x B_z$
* So that the net force F_y is zero physically, this electric field is set up when the magnetic field shifts the hole distribution slightly in the y direction
* The establishment of the electric field E_y is known as hall effect $V_{AB} = E_y w$ is called Hall voltage

$$E_y = \frac{J_x}{q p_0} B_z$$

$$E_y = R_H J_x B_z$$

$$R_H = \frac{1}{q p_0}$$

* Thus Hall field is proportional to the product of current density and magnetic flux density

$$R_H = (q p_0)^{-1} \rightarrow \text{Hall co-efficient}$$

$$p_0 = 1/q R_H$$

$$P_0 = \frac{1}{q_0 R_H}$$

$$P_0 = \frac{J_x B_z}{q \cdot E_y}$$

(8m)

$$P_0 = \frac{(I_x/wt)B_z}{q(V_{AB}/w)} \Rightarrow P_0 = \frac{I_x B_z}{q t V_{AB}}$$

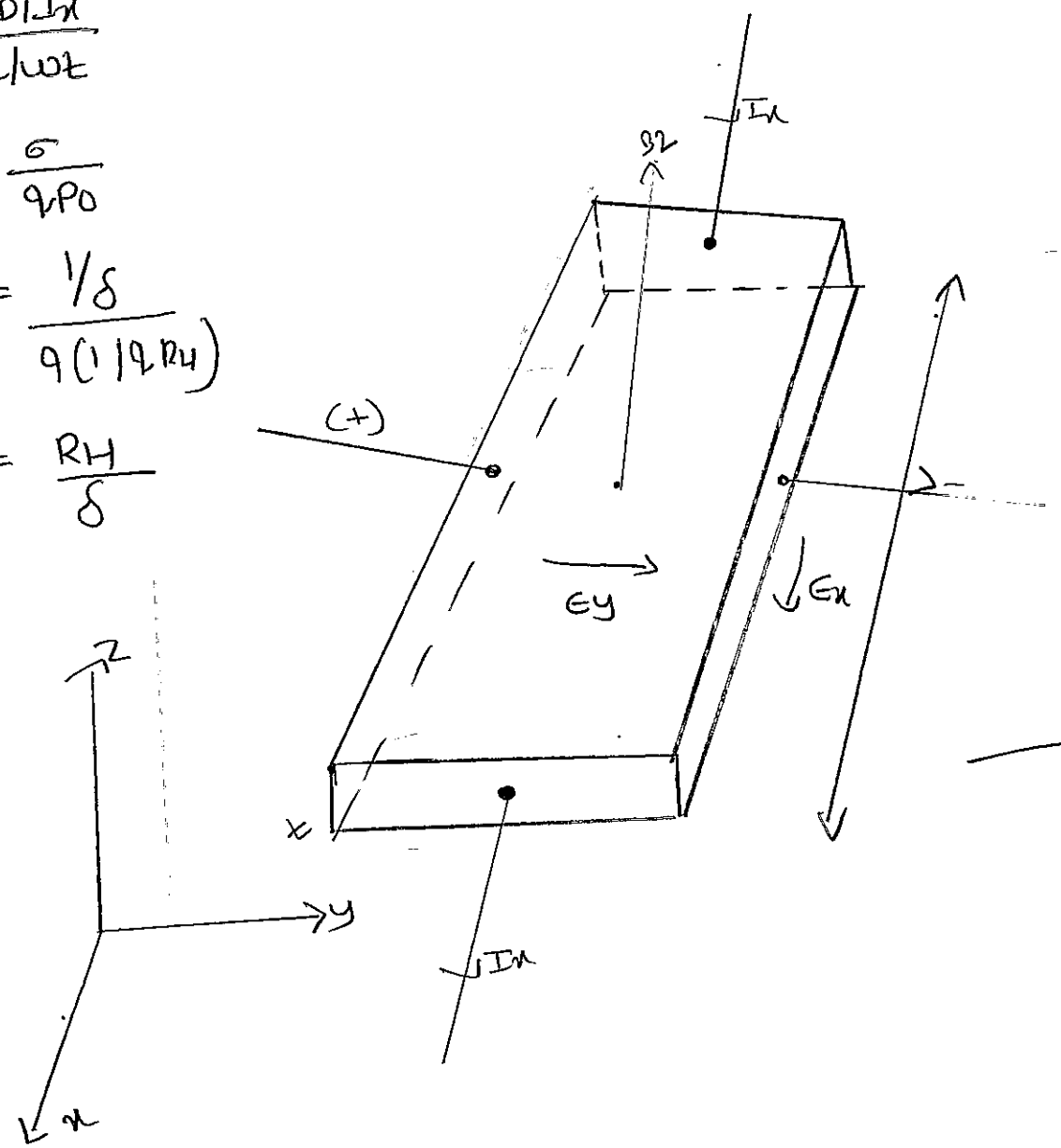
$$\rho = \frac{R_0 t}{L}$$

$$\rho = \frac{V_{CD}/I_x}{L/wt}$$

$$\mu_p = \frac{\sigma}{q P_0}$$

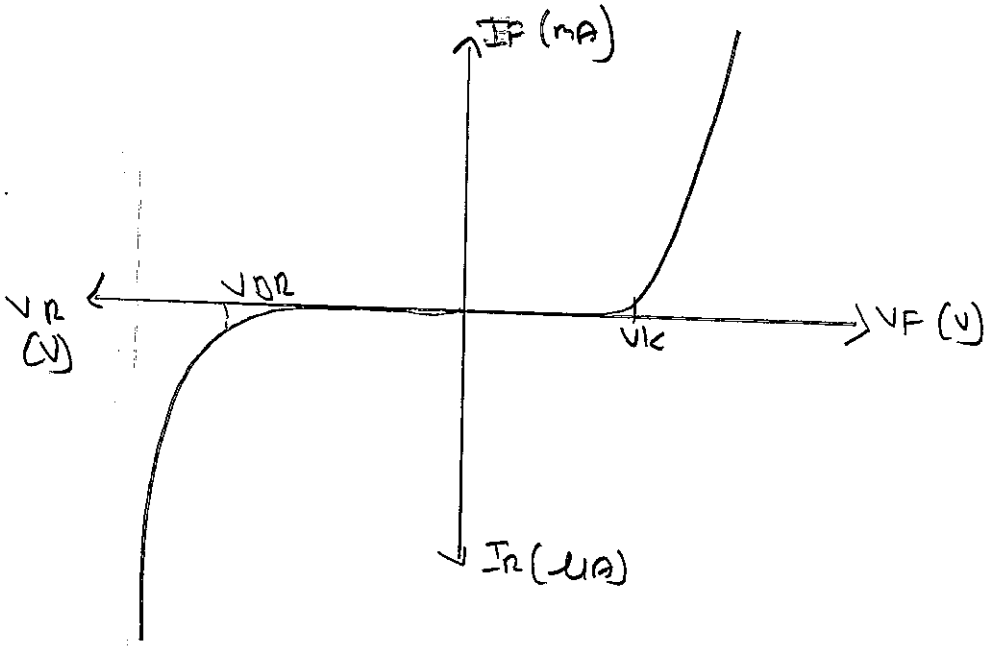
$$\mu_p = \frac{1/\rho}{q(1/q R_H)}$$

$$\mu_p = \frac{R_H}{\rho}$$



(2m)

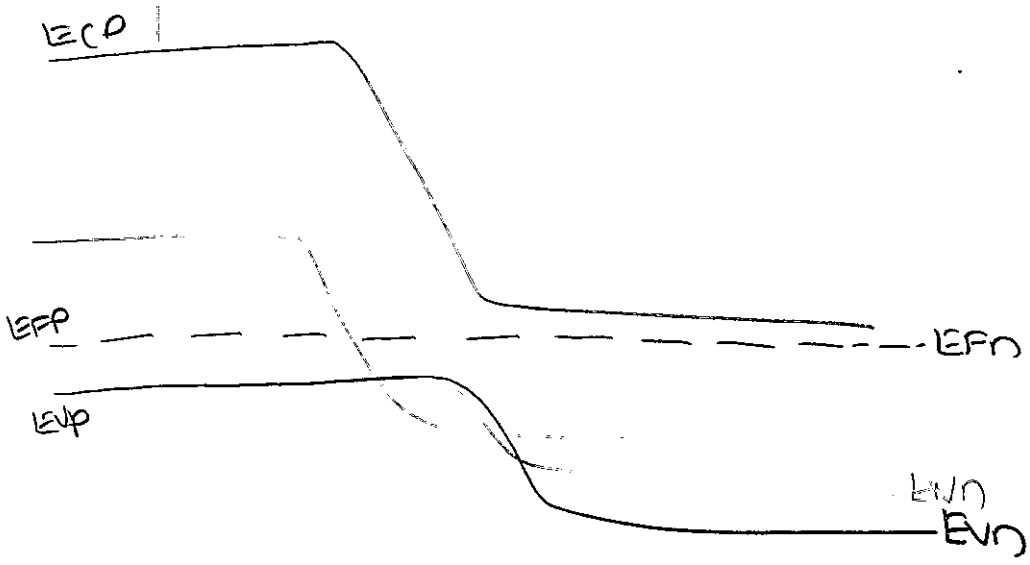
3) a) Explain V-I characteristics of diode.



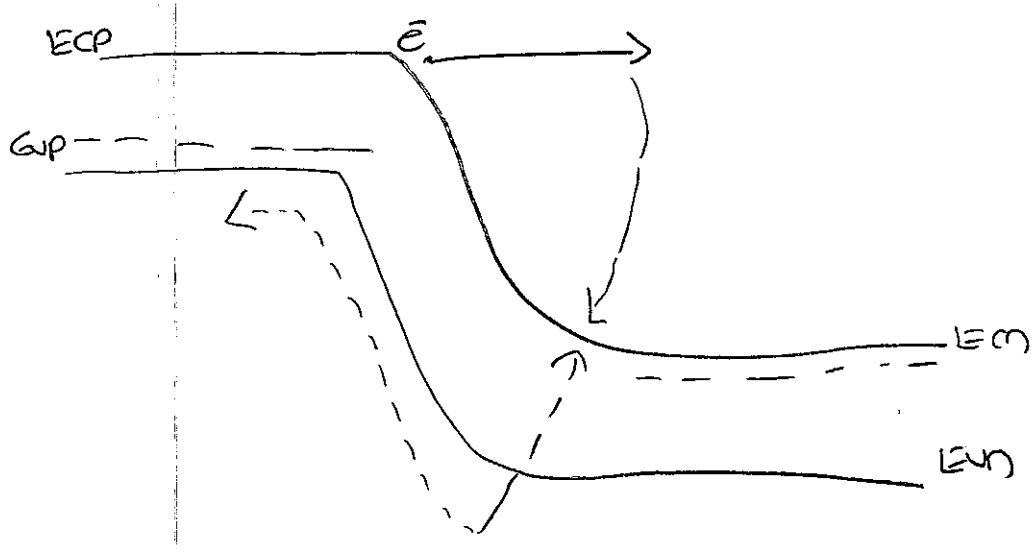
(2m)

* In forward bias the diode do not conduct immediately
* The diode conducts when the forward voltage is more than the knee voltage (V_K)
* V_K → knee voltage
  V_{BR} → Reverse breakdown voltage
  V_K for Si = 0.7V
  V_K for Ge = 0.3V
* If the bands represent these two bands is narrow tunneling of electrons can occur, Tunneling of electrons can occur from p side valence band to the n side conductor band, the constitutes a reverse current from n to p this is called zener effect

* However if zener breakdown does not occurs with bias of a few volts avaloche breakdown will Dominate



* For lightly doped Junctions electron tunneling is negligible and instead the breakdown mechanism involves the impact ionization of hot atoms by energetic carriers:-



(7m)

3)
c) How LED works with need diagram

* When carriers are injected across the a forward biased junct recombination in transition and neutral region takes place

* In semiconductor like GaAsP with direct recombination light wi be emitted, This effect injection electroluminescence

* It provides important application of diode as generation of light another device is a semiconductor laser which will emit more coherent in much narrower bandwidth

* The frequency of the photon is governed by the bandgap of the semiconductor as given by $hr = Eg$

* A very important metric of an LED is the external quantum efficiency η_{ext}, which is defined as the light o/p divided by electrical power

$$\eta_{ext} = (\text{Internal radiative efficiency}) * (\text{Extraction efficiency})$$

* Defects in the material will clearly lead to nonradiative recombination

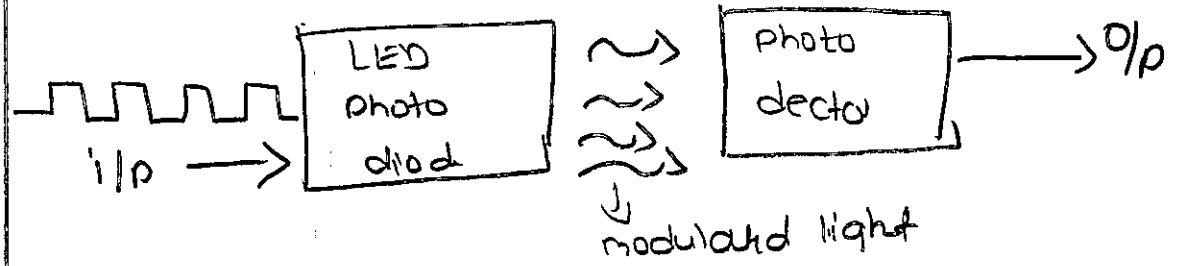
* However if the internal efficiency is high, not all emitted phot are extracted from the LED

* The emitted photons from an LED have wide angular distribu as planar surface

* The internal efficiency is a function of the quality of the material and structure and composition of the layer.

* LED / Laser is used in conjunction with photodiode to transmit data optically

* By varying the current through the photodiode the light o/p can be modulated such that anlog or digital signal is transmitted to the photodector —(5m)



—(2m)

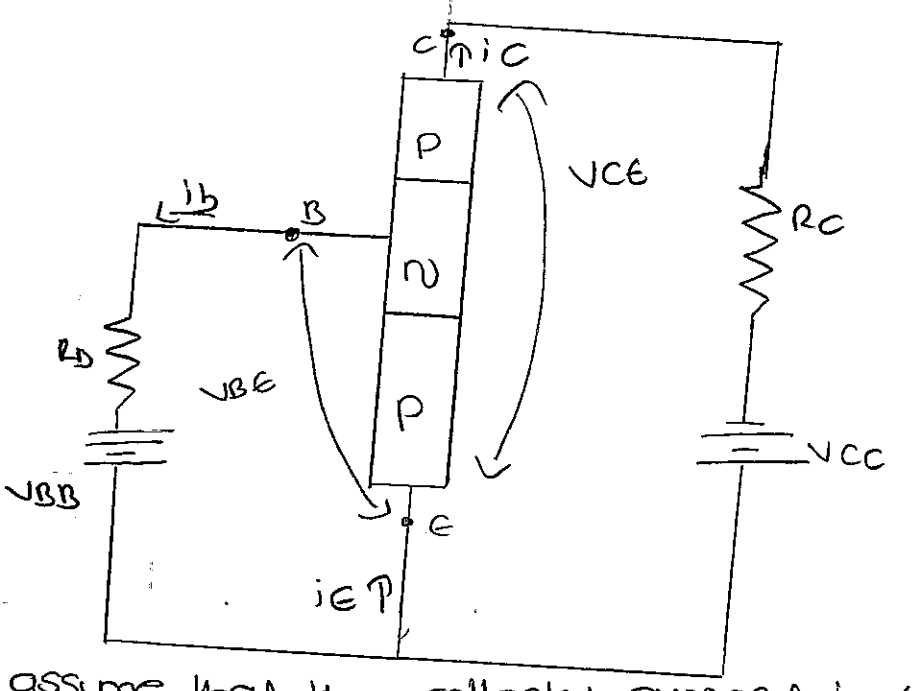
b) Diffrence between zener effect and Avalanche effect

Avalanche effect	Zener effect
→ Lightly doped diode	Heavily doped diode
→ high reverse potential	Low reverse potential
→ weak electric field is produced	Strong electic field is produced
→ Increase in temperature increase breakdown voltage	Increase temperature Decrease the breakdown voltage
→ Depletion region is thick	Depletion region is thin
→ occurs at high reverse potential	occurs at low rever potential
→ Doping concentration is not changed	Doping concentration is changed

—(3m)

5)

a) Explain how BJT act as amplifier with the help of equation



(2m)

* Let us assume that the collector current ic is made up entirely of those holes injected at the emitter which are not lost to the recombination in the base
* Thus ic is proportional to the hole component of the emitter current

  i.e $i_C = \beta i_{EP}$ → (1)

* where β is the proportionality factor known as Base Transport factor
* The total emitted current iE is made up of the hole component i_{EP}, the emitter injection efficiency is

$$\eta = \frac{i_{EP}}{i_{EP} + i_{En}} \rightarrow (2)$$

* For efficient transistor we should like β and η to be very near to unity that is the emitter current should be due to mostly holes

∴ The Relation between collector and emitter current

$$\frac{I_C}{i_E} = \frac{\beta i_{EP}}{i_{EP} + i_{En}} = \beta\eta = \alpha \rightarrow (3)$$

* In each case, the lost $\bar{e}$ must resupplied through the base current i_B; If the fraction of injected holes making it across the base without recombination is β

$$\therefore i_b = i_{en} + (1-\beta) i_E$$

* Neglecting collector saturation current, the relation between collector and base current is found to be

$$\frac{i_C}{i_b} = \frac{\beta i_{ep}}{i_{en} + (1-\beta) i_{ep}}$$

$$= \frac{\beta \left[\frac{i_{ep}}{i_{en} + i_{ep}} \right]}{1 - \beta \left[\frac{-i_{ep}}{i_{en} + i_{en}} \right]}$$

$$\frac{i_C}{i_b} = \frac{\beta_n}{1-\beta_n}$$

$$\frac{i_C}{i_b} = \frac{\alpha}{1-\alpha}$$

$$\frac{i_C}{i_b} = \alpha\beta \Rightarrow \frac{i_C}{i_b} = \beta$$

* β is the amplification factor, since α is near unity, it is clear that β can large for a good transistor

* In particular for each $\bar{e}$ entering from the base contact

T_p / T_t holes can pass from emitter to collector

while a maintaing space charge neutrality

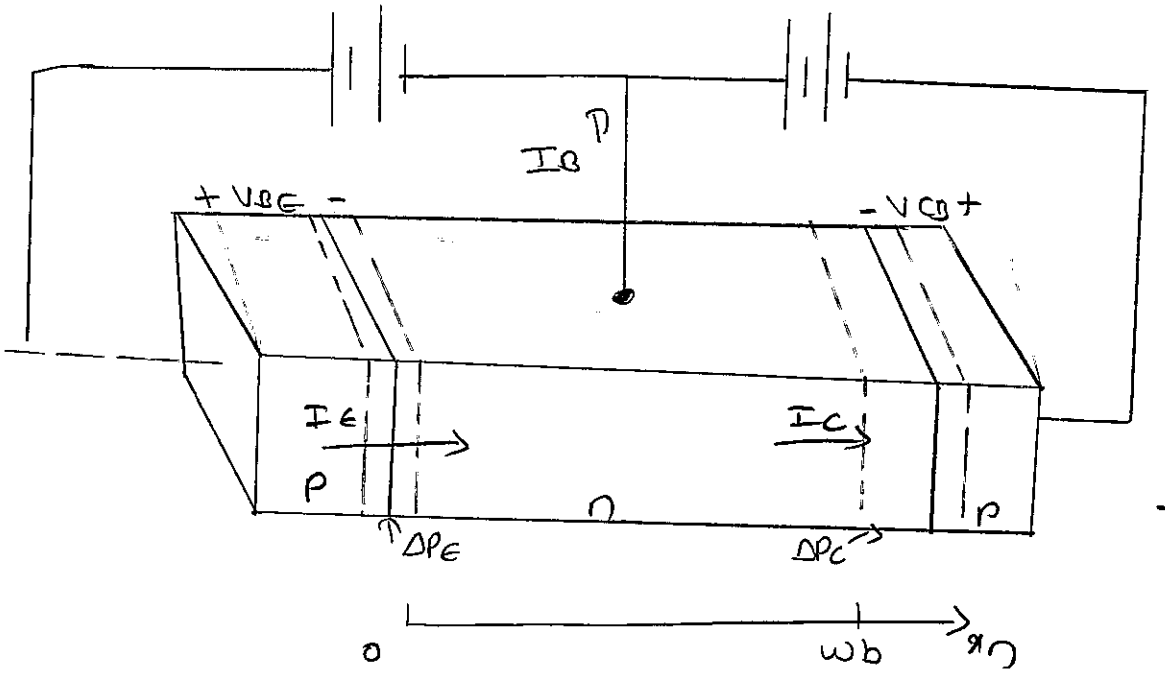
$$\frac{i_C}{i_b} = \frac{\tau_p}{\tau_t} = \beta$$

——— (8m)

b) Draw the Ebers-Moll Model for PNP transistor.

* The ΔP_E represents the excess hole concentration at the edge emitter depletion

* ΔP_C represents the hole concentration at the edge of the emitter depletion region



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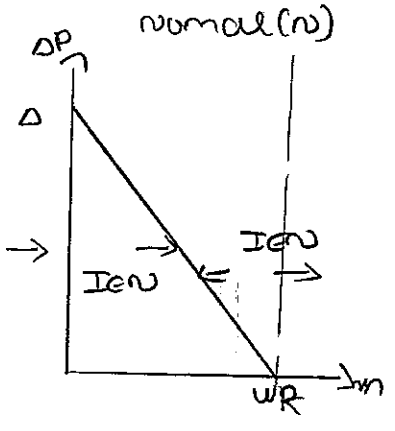
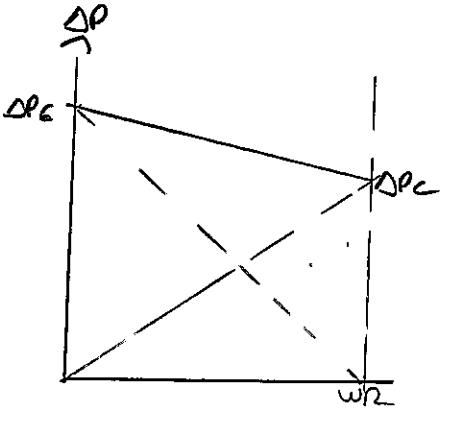
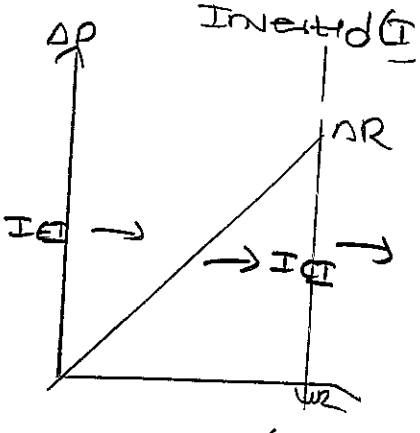






(2m)

* For the symmetrical transistor various components are

$$a = (q_1 A D_p / L_p) \coth(W_b / L_p)$$

$$b = (q A D_p / L_p) \operatorname{cosech}(W_b / L_p)$$

$I_{EN} = a \Delta P_E$ and $I_{EN} = b \Delta P_E$ with $\Delta P_C = 0$

$I_E - I = -b \Delta P_C$ and $I_{CI} = -a \Delta P_C$ with $\Delta P_E = 0$

* Total emitter and collector current

$$I_E = I_{En} + I_{EI}$$

$$= a\Delta P_E - b\Delta P_C$$

$$I_E = A\left(e^{qV_{EB}/kT} - 1\right) - B\left(e^{qV_{CB}/kT} - 1\right)$$

$$\therefore I_C = I_{Cn} + I_{CI}$$

$$I_C = B\left(e^{qV_{EB}/kT} - 1\right) - A\left(e^{qV_{CB}/kT} - 1\right)$$

where $A = aP_n$ and $B = bP_n$

$\Rightarrow I_{En} = I_{ES}\left(e^{qV_{EB}/kT} - 1\right)$, $\Delta P_C = 0$

$I_{CI} = -I_{CS}\left(e^{qV_{CB}/kT} - 1\right)$, $\Delta P_E = 0$

* $I_{Cn} = \alpha_n I_{En} = \alpha_n I_{ES}\left(e^{qV_{EB}/kT} - 1\right)$

$I_{EI} = \alpha_I I_{CI} = -\alpha_I I_{CS}\left(e^{qV_{CB}/kT} - 1\right)$

* Total current is

$$I_E = I_{En} + I_{EI}$$

$$= I_{ES}\left(e^{qV_{EB}/kT} - 1\right) - \alpha_I I_{CS}\left(e^{qV_{CB}/kT} - 1\right)$$

$$I_C = I_{Cn} + I_{CI}$$

$$= \alpha_n I_{ES}\left(e^{qV_{EB}/kT} - 1\right) - I_{CS}\left(e^{qV_{CE}/kT} - 1\right)$$

$$\alpha_n I_{En} = \alpha I_{CS}$$

$\Rightarrow$ The Ebers moll equation is

$$I_E = I_{ES}\frac{\Delta P_E}{P_n} - \alpha_I I_{CS}\frac{\Delta P_C}{P_n}$$

$$I_E = \frac{I_{ES}}{P_n}\left(\Delta P_E - \alpha_n \Delta P_C\right)$$

$$I_C = \alpha_n I_{ES}\frac{\Delta P_E}{P_n} - I_{CS}\frac{\Delta P_C}{P_n} \longleftarrow (6M)$$

$$I_C = \frac{I_{CS}}{P_n}\left(\alpha_I \Delta P_E - \Delta P_C\right)$$

6)

a) How BJT act as switch with necessary diagrams

* Transistor operates in the normal active mode, that is emitter junction is forward biased and collector is reverse biased with a reasonable value of i_B

* on the other hand if base current is zero or negative point 'c' is reached at the bottom end load line and the collector current is negligible

* This is the 'off' state of transistor and device is said to be in cutoff region

* If the base current is positive and sufficiently large end device is said to be in Saturation Region

* This is the on' state of the transistor in which a large value current i_C flows with only very small voltage drop V_{CE}

⇒ Operation in cut-off Region:-

* when the base transistor is given negative the transistor goes to cut off region or state $I_C = 0$

* The voltage V_{CC} applied at the collector, appears across the collector register R_C

$$\therefore V_{CE} = V_{CC}$$

⇒ Operation in Saturation Region:-

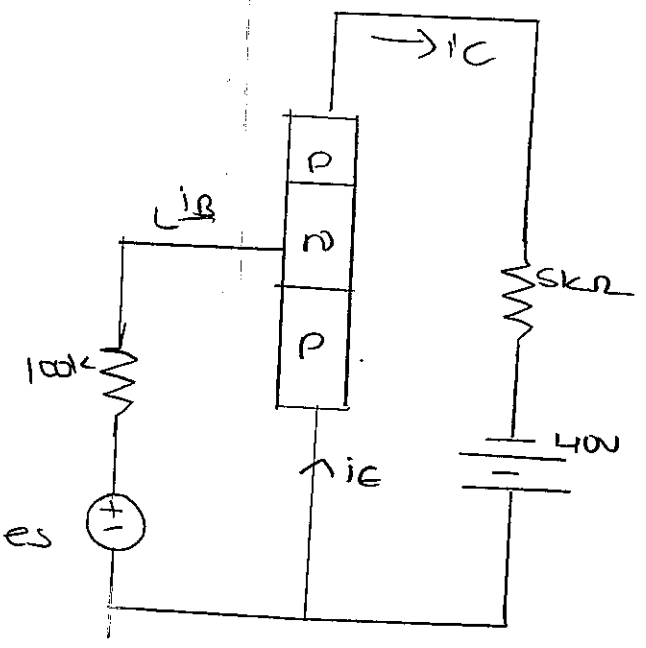
* when large voltage is positive and transistor goes into saturation I_C flows through R_C

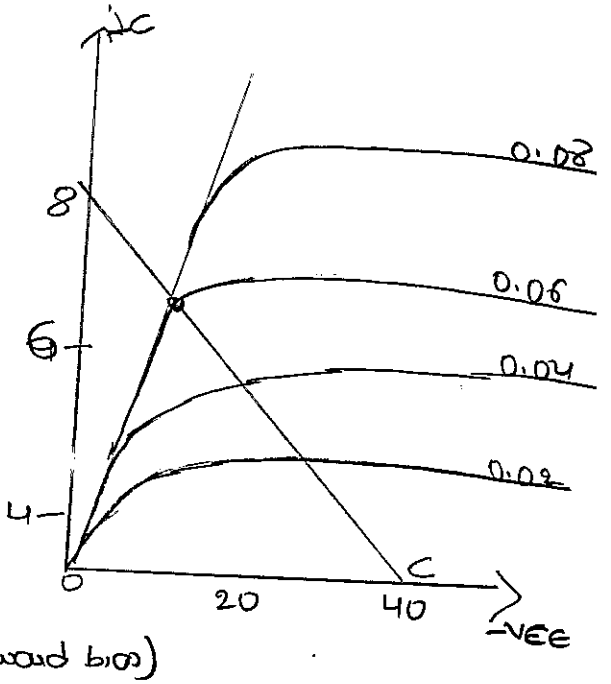
$$I_B = \frac{(V_{CC} - V_{BE})}{R_B} \quad \text{——(7m)}$$

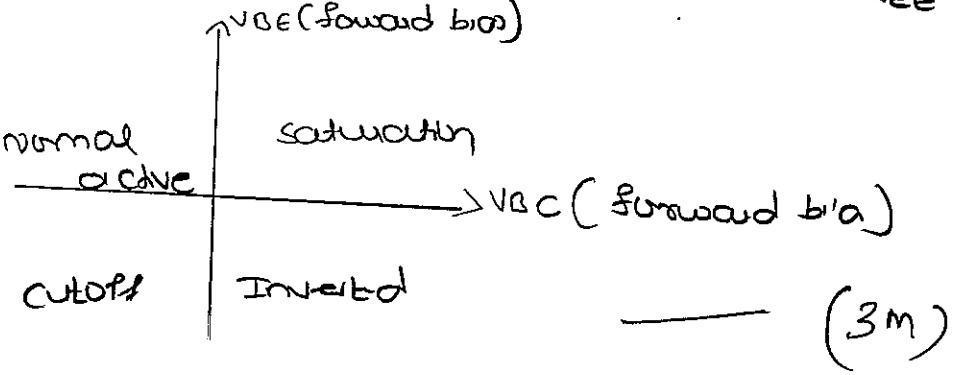
- If the I_B is increase further transistor goes to saturation

$$\therefore I_C = I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad \text{if } V_{CE} = 0$$

$$\therefore I_{C(sat)} = \frac{V_{CC}}{R_C}$$







(3M)

2) Specification of switching transistor BJT

* The charging time of the emitter junction capacitance and to be considered going from cutoff to saturation

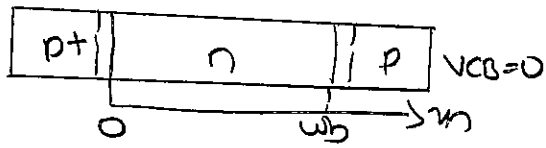
* Since the emitter junction is reverse biased in cutoff, it is necessary for the emitter space charge layer to be changed to the forward bias condition, collector current can flow

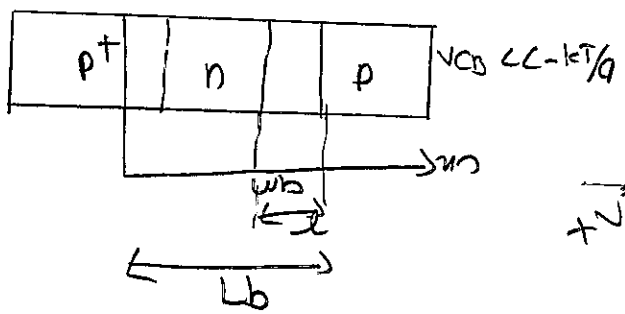
* Therefore we should include a delay time td to account for that effect

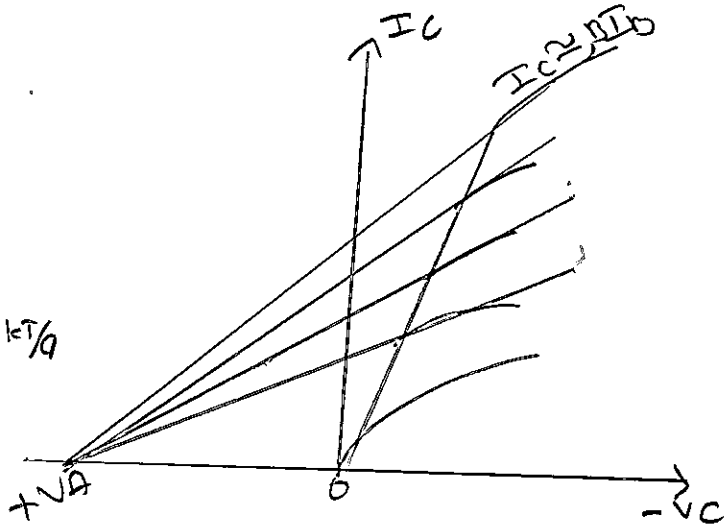
* Typical-value of td are given in the specification information of most switching transistors, along with a rise time by defined as the time required for the collector current to rise from 10 to 90% of its final value

* Third specification is the fall time tf required for ic to fall through similar function its turn off

=> Explain the effect of base narrowing with neat diagram







(4m)

=>

* Base narrowing :-

-> If the base region is lightly doped, the depletion region reversed biased, collector junction can extend significantly into the n type of base region

-> As the collector voltage is increased, the space charge layer make more of metall width of base L_b and as a result the effective base width W_b is decreased

-> decrease in the effective base width as the Reverse bias on the collector junction is increased

(4m)

* The decrease in wb caused β to increases, As a Result the collector current Ic ↑ with collector voltage rather than stay constant as predicted from the above treatment

* The slope introduced by the early effect is almost linear with Ic and the CE characteristics extrapolate to an intersection with voltage axis at VA called early voltage

* The length of the collection junction depletion region in the n material is given by

$$l = \left(\frac{2\epsilon V_{BC}}{q n_d}\right)^{1/2}$$

* If the reverse bias on the collector junction is n for enough, it is possible to decrease wb to the extent that the collector depleton region essentially fills the entire base

* In this condition holes are swept directly from the emitter region to the collector and transistor action is lost

* Breakdown effect that is generally avoided in ckt design, In most cases however avalanche breakdown of the collector junction occurs before pinch of is reached

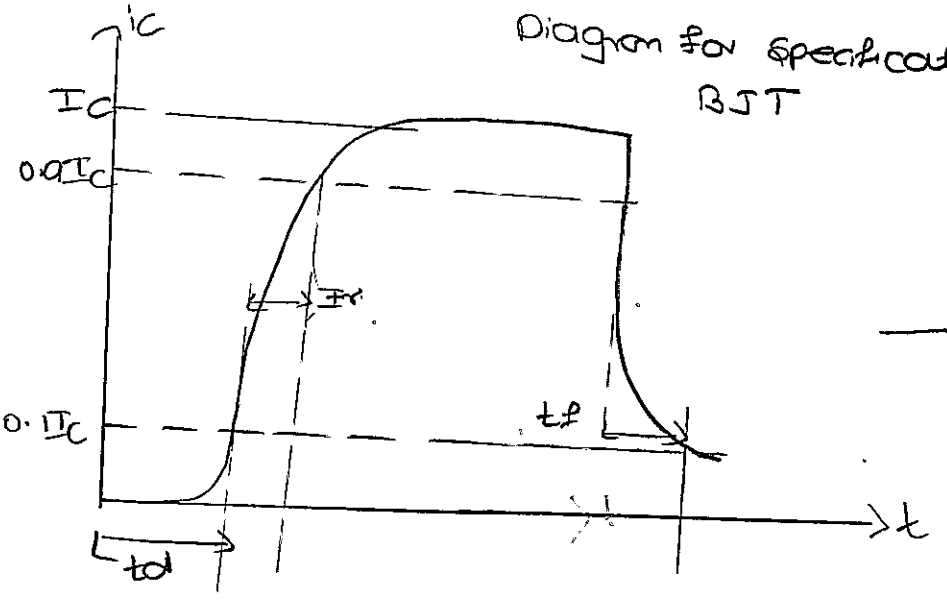
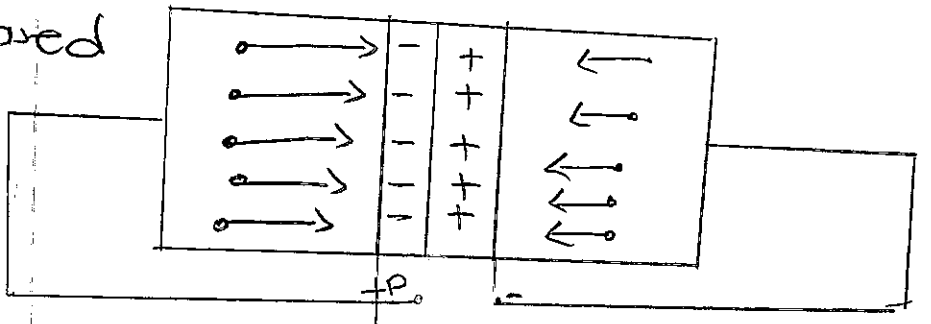


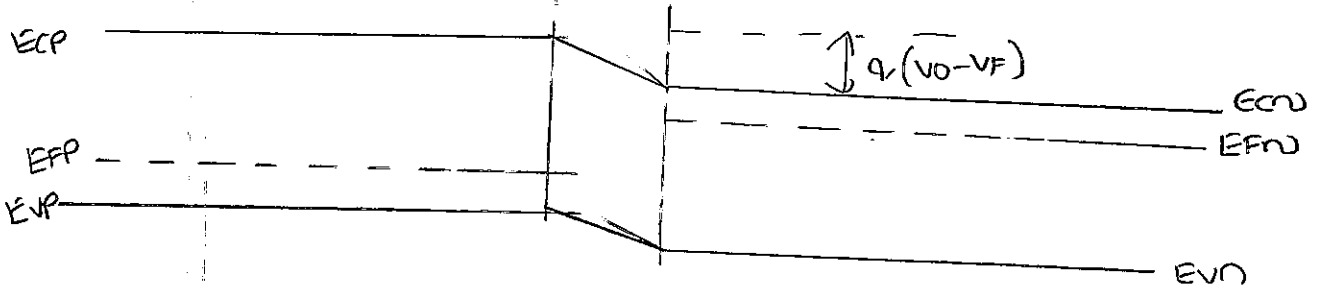
Diagram for specification of BJT

(2m)

4) a) qualitative description of current flow at forward and reverse bias Junction

⇒ Forward biased



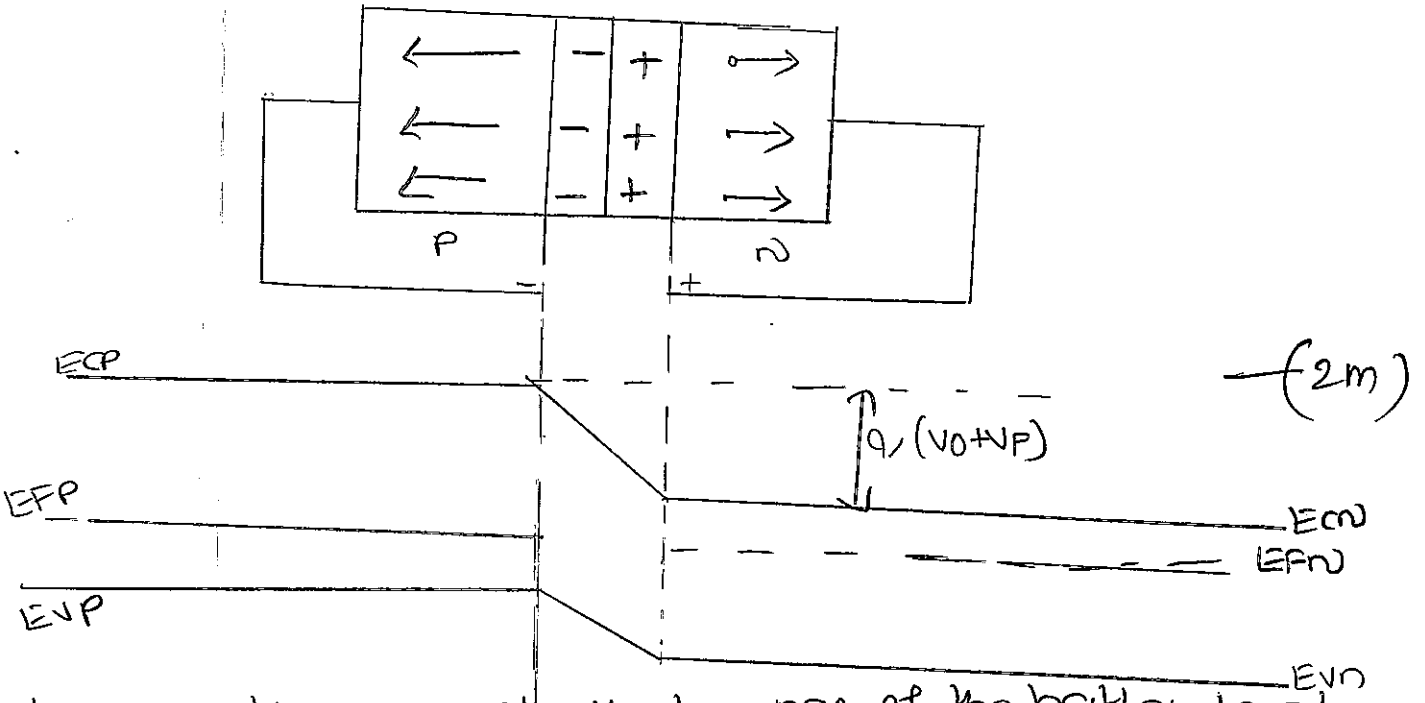


(2M)

* To apply forward bias connect +ve terminal of battery to p side and negative terminal of battery to n side
* In forward biased hole in 'p' region are repelled from +ve terminal of the battery and forced to move towards the junction
* The electons in 'n' region are repelled from the -ve negative terminal of the battery and forced to move toward the Junction
* This reduces the height and width of potential barrier
* Once the potential barrier completely eliminated by the forward voltage junction resistance become almost zero and a low resistance path is established
* The current flowing in the circuit is called forward resistance I_F R_F
* current condition is possible until the applied voltage is greater than barrier voltage

$$V_B = q(V_0 - V_F) \qquad \text{(3m)}$$

⇒ Reverse bias :-



(2m)

* To apply reverse bias connect -ve terminal of the battery to p type and +ve terminal of the battery to n type
* In reverse bas holes in P region are attracted towards -ve terminal electrons are attracted towards +ve terminal of the battery
* This increases the width and height of potential barrier increased potential barrier prevents the flow of charge carrier across the junction
* This high resistance path is established, no current can flow junction reverse resistance R_R and current is called reverse current (I_R)
* The flow of current due to motion of minority charge carrier called reverse saturation current
* The reverse bias P-n junction allows a small reverse current due to movement of Minority carriers

$$V_B = q(V_0+V_F)$$

(3m)

* Reverse breakdown voltage is the Reverse voltage at which p-n junction breakdown with sudden rise in reverse current
Here breakdown happing is avalanche breakdown, which is personally

b) How does photo diode works as photovoltaic cell,

* current and voltage in an illuminated junction
* photodiodes are two terminal devices designed to respond to pho absorption
* In PN junction diode, the drift of minority carries result in curr the charge carries generated within the depletion region will be drifted and $\bar{e}$ will move towards n region and holes towards p region
* Also the minority charge carriers will generated within diffusion length will cross the Junction
* If a Junction of cross-sectional area A is uniformly illuminated by photons with $hr > Eg$
* A photogeneration rate G (EHP/cm^3s) gives rise to a photocurrent
* The numbe of holes created per second within a diffusion length L_r of depletion region on the n side is AL_rG
* The number of electron created per second within a diffusion lengt L_e of the depleton region on p side AL_eG
* Similarly, AWG carrir generated with in the depleton region of width W
* The resulting photocurrent

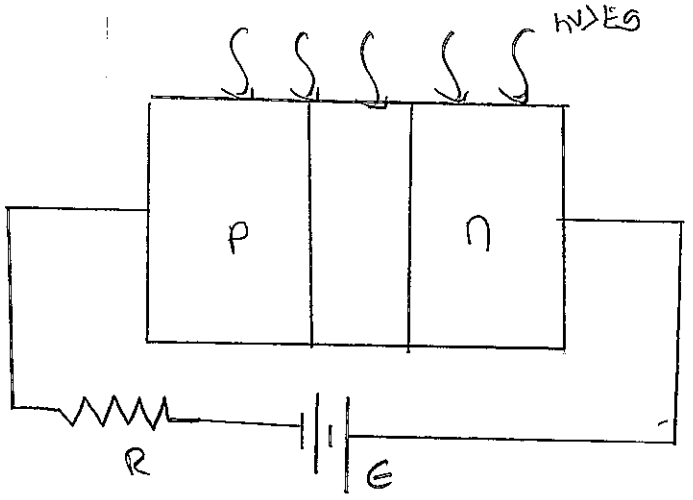
$$I_p = eA(L_h + L_e + W)G$$

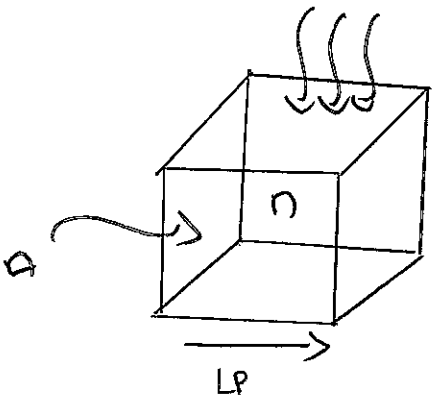
* The current voltage (I-V) characteristics of the given Junction is given by the diode equation

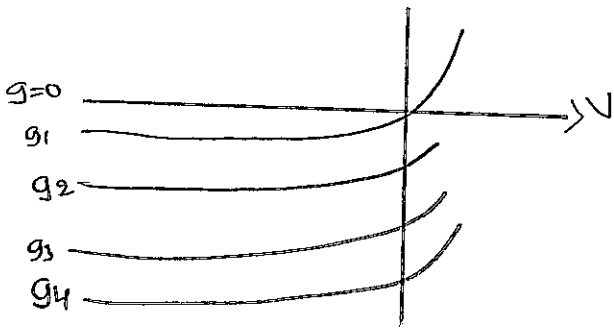
$$I = I_0(e^{V_{DI}/\eta kT} - 1) - I_p$$

* $$I = qA\left(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p\right)\left(e^{V/\eta T} - 1\right) - I_p \quad \text{——— (8m)}$$

* The current I is the injection current under forward bias V
Io is the saturation current represents thermal generated free carriers which flow through the Junction (dark current)



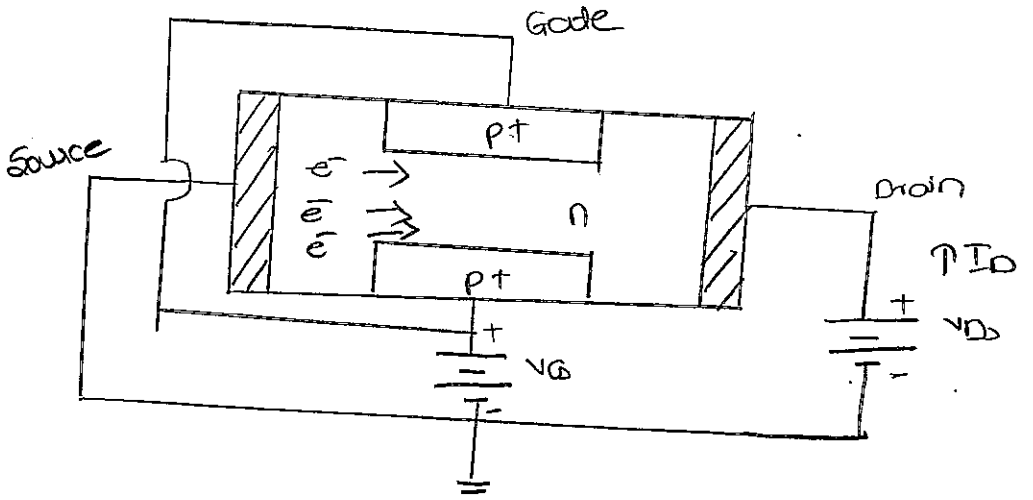




g3>g2>g1 (2m)

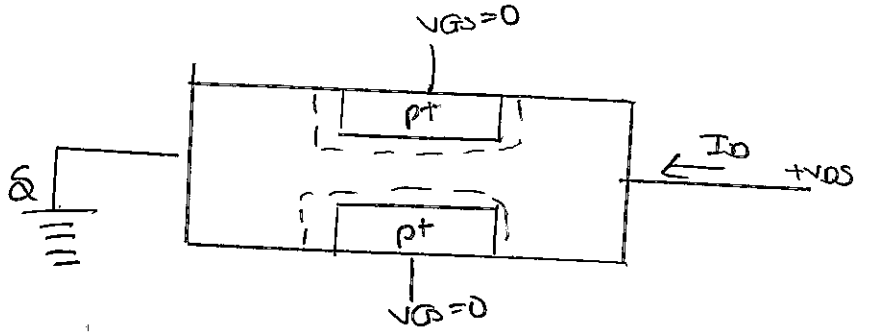
7) a) construction and operation of n-JFET with neat diagram

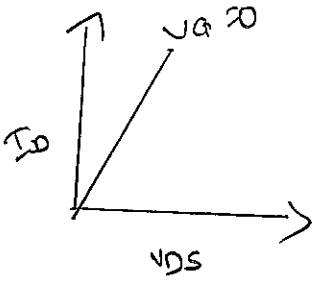
* The n-region between the two p' region is known as the chan
* In the n-channel device, majority carrier electrons flow between the source and drain terminals
* The drain is the terminal whereas carriers leave or are drained from the device and gate is the control terminal



(2m)

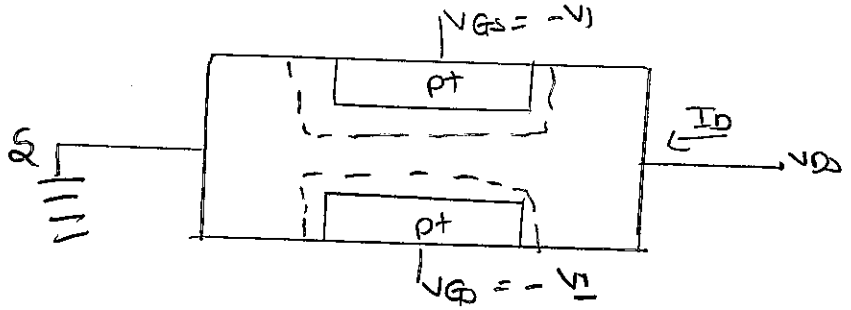
⇒ zero gate bias

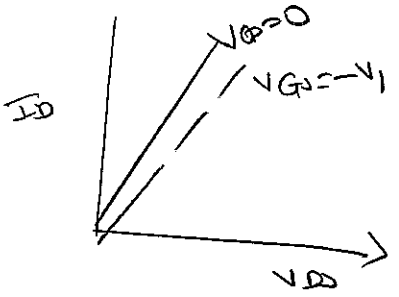




* If the source is at ground potential and if a small positive drain voltage is applied, drain current ID is produced between source and drain terminals
* The n channel is essentially a resistance so that ID versus VDS characteristic for small VDS value is approximately linear

⇒ small negative gate voltage

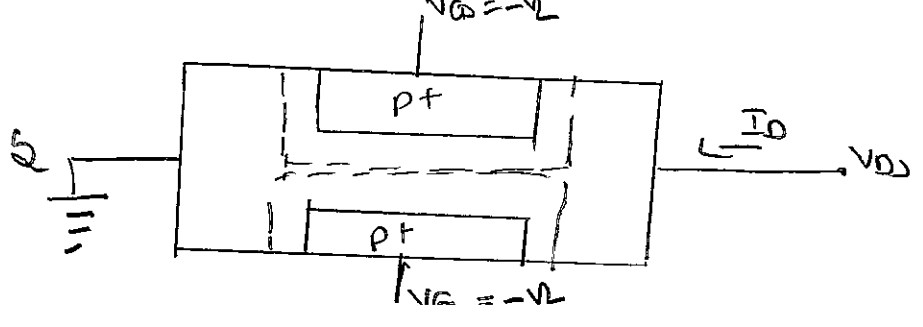


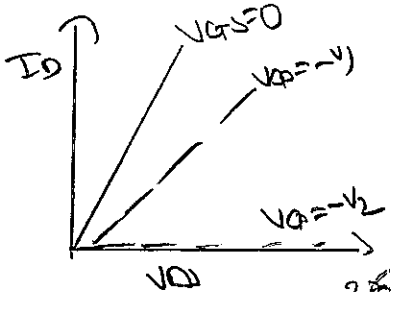


* If a negative voltage is applied to the gate of n-channel an JFET gate-to-channel junction becomes reverse biased
* The space charge region now widens so that channel region becomes narrower and resistance of the n channel increase

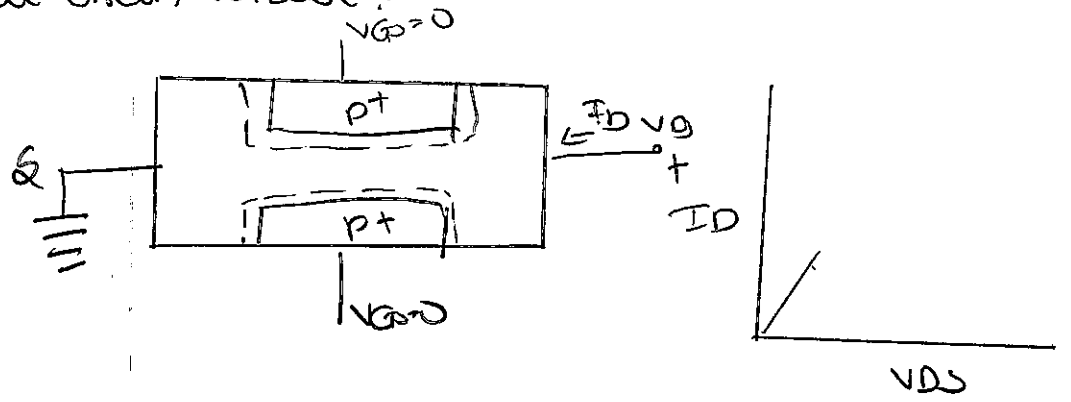
⇒ Large negative gate voltage:-

* The reverse-biased gate-to-channel space charge region has completely filled the channel region called Pinch-off
*





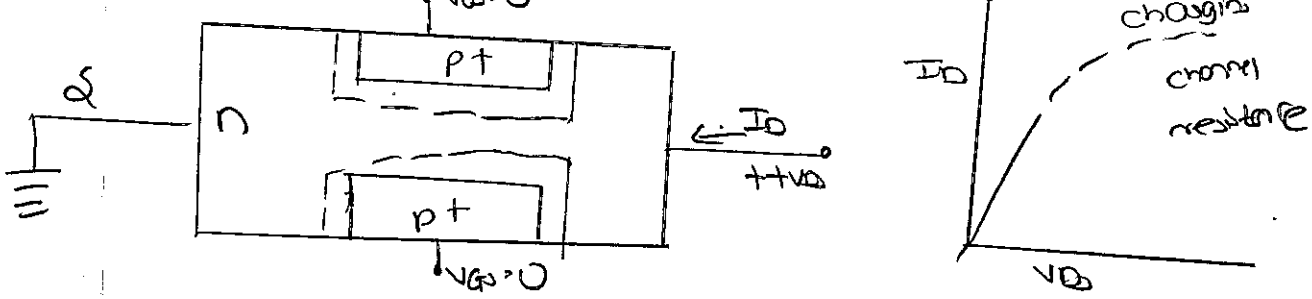
⇒ A small drain voltage:-



⇒ A Large Drain Voltage:-

* As the drain voltage increase, the gate-to-channel pn Junction be
- comes reverse biased near the drain channel or terminal so
that space charge region extends further into channel

* The effective channel resistance now varies along the channel leng
Since channel current must be constant

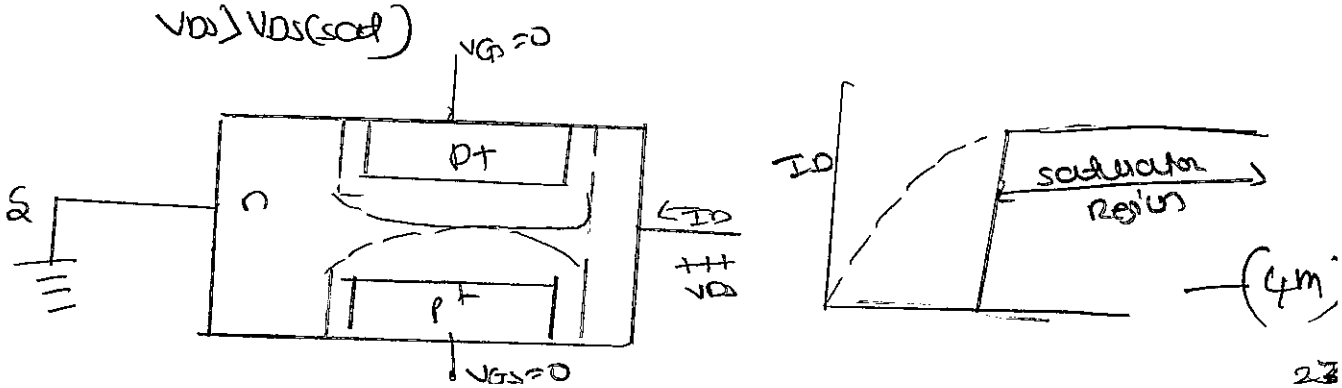


⇒ A drain voltage to achieve pinch off :-

* If the drain voltage increase further, the channel has been pinch
off at the drain terminal

* Any further increase in drain voltage will not cause an increase in
drain current

* The drain voltage at pinchoff is referred to as VD(sat) Fo
VD ⟩ VDS(sat)



7.b) Explain small signal equivalent circuit for JFET.

* The cross section of an n-channel pn JFET including source and drain series resistance
* The substrate may be semi-insulating gallium arsenide
* The voltage $v_{g's'}$ internal gate-to source voltage that controls the drain current
* The r_{gs} and C_{gs} parameters are the gate-to-source diffusion resistance and junction capacitance
* The parameters r_{gd} and C_{gd} are the gate-to-drain resistance and capacitance respectively
* The Resistance r_{ds} is the finite drain resistance, which is a function of the channel length Modulation effect
* The C_{db} capacitance is mainly a drain-to-source parasitic capacitance and C_s in the drain-to-substrate capacitance
* All diffusion resistance are infinite, the series resistance are zero and at low frequency the capacitance become open circuit

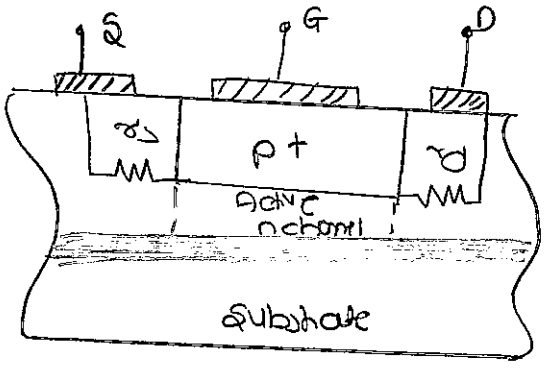
$$I_{ds} = g_m V_{gs}$$

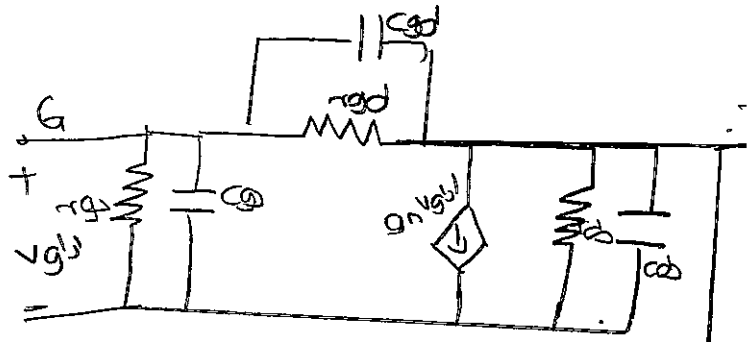
* $I_{ds} = g_m v_{g's'}$
* The Relation between V_{gs} and $v_{g's'}$ can be found

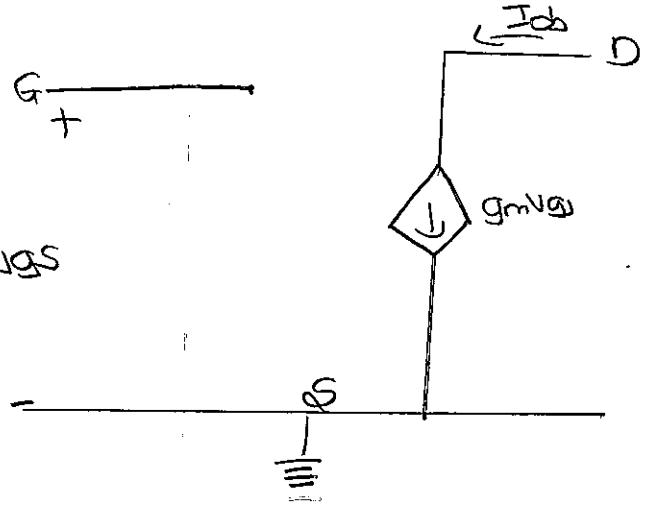
$$V_{gs} = v_{g's'} + (g_m v_{g's'}) r_o = (1 + g_m r_o) v_{g's'} \rightarrow (3)$$

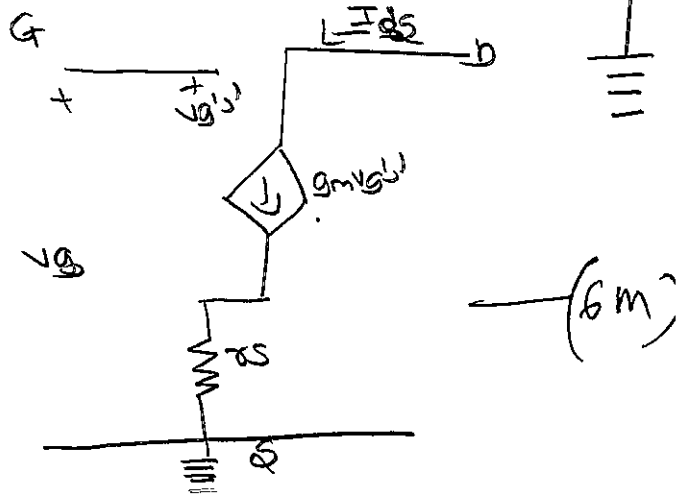
$$I_{ds} = \left(\frac{g_m}{1 + g_m r_o}\right) V_{gs} = g_m' V_{gs} \rightarrow (4)$$

* The g_m is a function of dc-to gate-to source voltage g_m' will be function of V_{GS}









c) Explain two of n-channel enhancement mode MOSFET

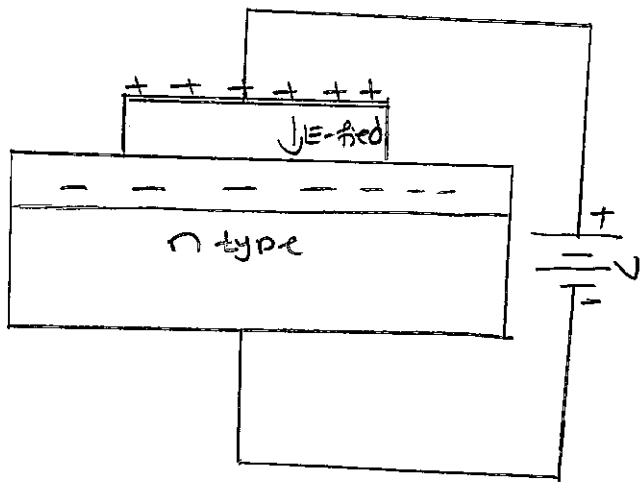
* MOS capacitor structure with a positive voltage applied to the top gate terminal
* A positive charge exists on the top gate and electric field is induced
* An accumulation layer of electron will be induced in the n-type substrate
* The case when a negative voltage is applied to the top gate
* positive space charge region induced in the n-type semiconductor
* The energy band diagrams for the MOS capacitor with n-type substrate
* The positive voltage is applied to the gate and an accumulation layer of electron is formed
* Figure 12b shows the energy band when negative voltage is applied to the gate

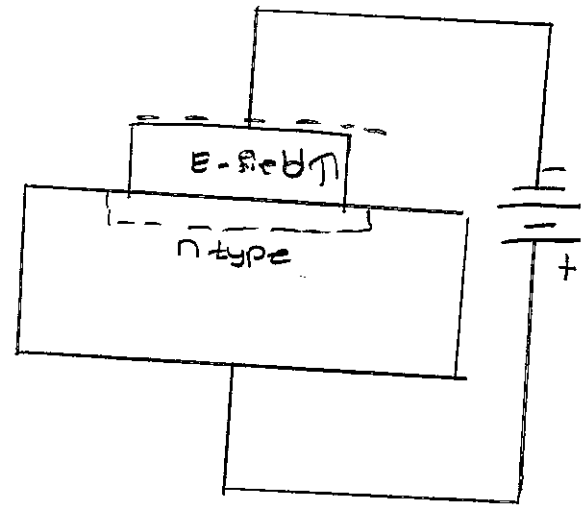
* The conduction and valence band now bend upward indicating that space charge region has been induced in the n-type substrate

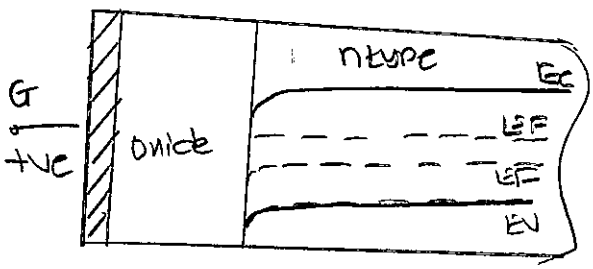
* Figure 12 shows the energy when a large negative voltage is applied to the gate

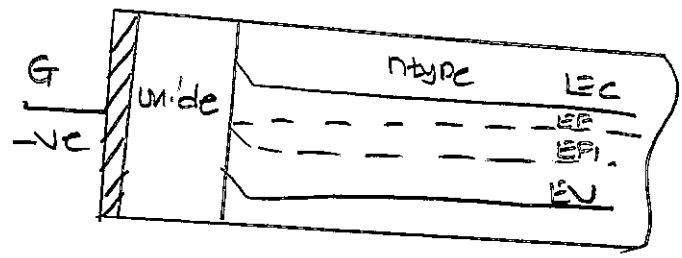
* The conduction and valence band are bent over even more and the instricsic Fermi level has moved above the Fermi level

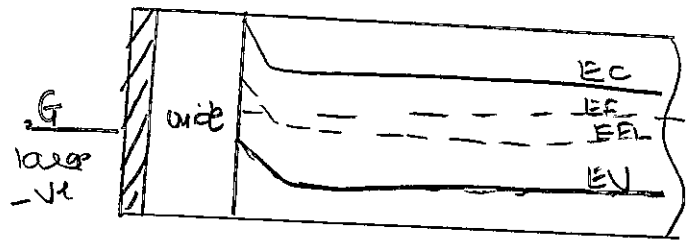
* The valence band at the surface is now close to the Fermi level whereas conduction band is close to the Fermi level in bulk semiconductor











(8m)

8)
a) Explain two-terminal MOS structure.

* The heart of the MOSFET is MOS capacitor
* t_{ox} is thickness of oxide and ϵ_{ox} is the permittivity of the oxide
* parallel-plate capacitor with the top plate at negative voltage with respect to the bottom plate
* $C' = \frac{\epsilon}{d}$

ϵ -> permittivity of a insulator, d is the distance between two plates

* $Q' = CV$

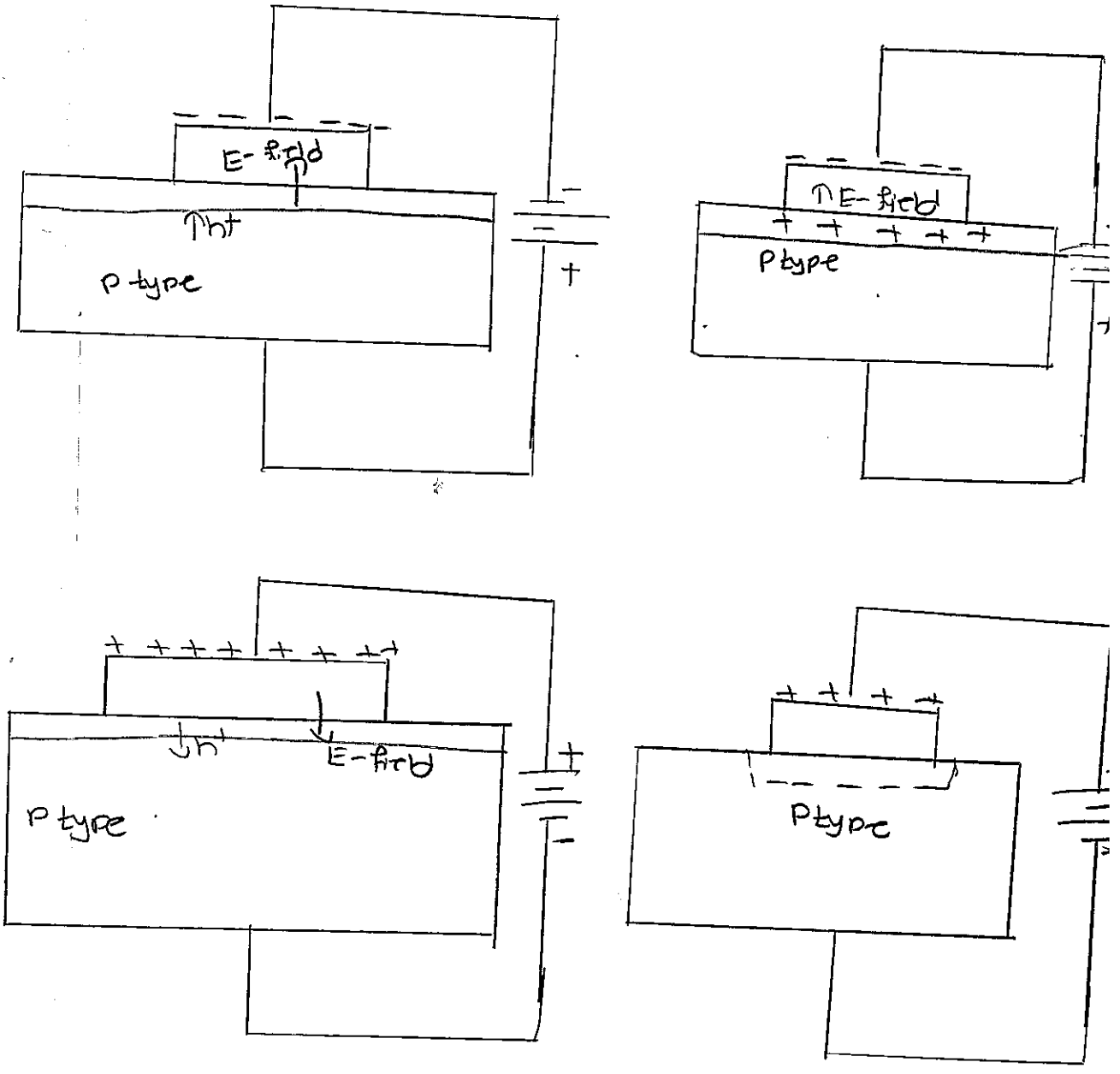
-> The magnitude of the electric field is

$$E = V/d$$

* The top metal gate is at a negative voltage wrt to the semiconductor, a negative charge will exist on the top metal plate
* If the electric field were to penetrate into semiconductor the majority carrier holes would experience a force toward oxide
* accumulation layer of holes at the oxide-semiconductor Junction correspond to the positive charge on the bottom plate of the MOS capacitor
* When positive charge is applied on the top metal plate and the direction of induced electric field
* If the electric field penetrates the semiconductor majority carriers will be force away from the oxide-semi hole

* As the holes are pushed away from the interface a negative space charge region is created because of fixed ionized acceptor atoms

* The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor

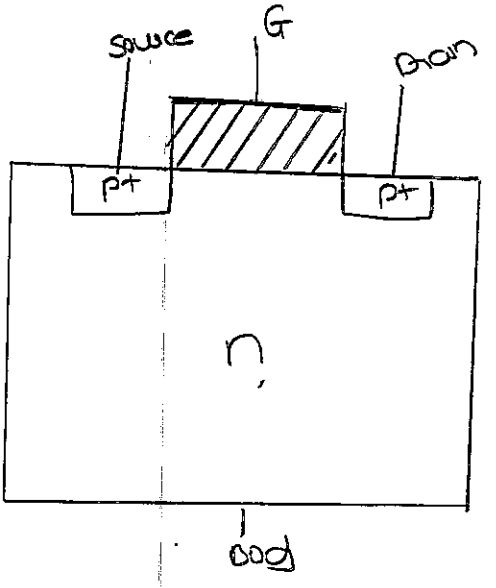


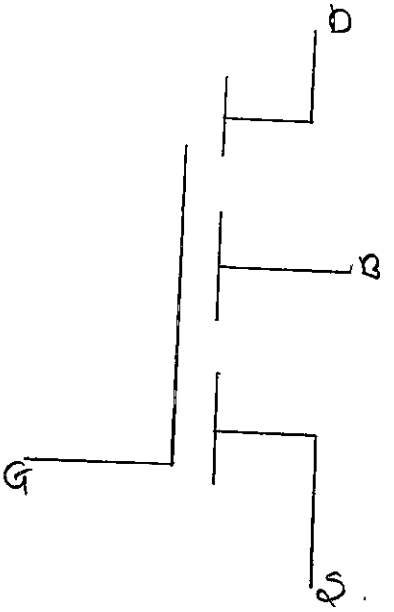
(10M)

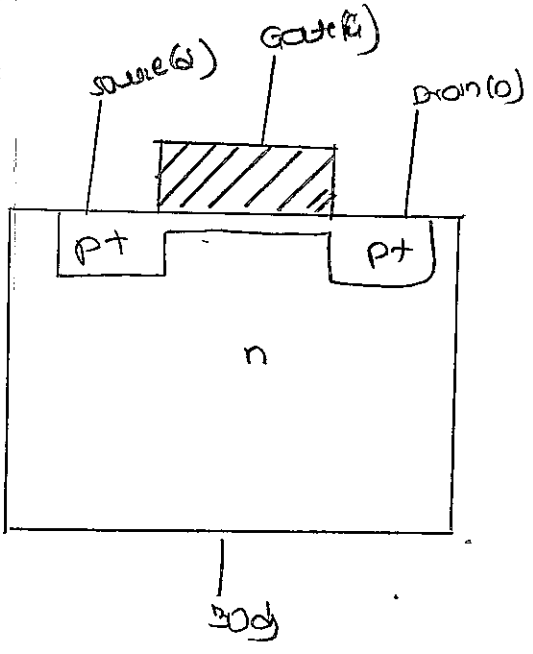
b) p-channel enhancement Mode MOSFET

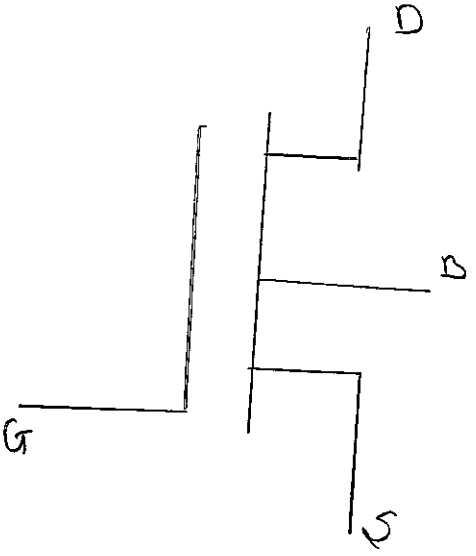
* In the p-channel enhancement Mode device, a negative gate voltage must be applied to create an inversion layer of holes that will "connect" the p type source and drain regions

* The holes flow from the source to the drain, so that conventional current will enter the source and drain leave









9)

a) Thermal oxidation proces with neat diagram

* many fabrication steps involve the heating up the wafer in order to enhance a chemical process

* An important example of this thermal oxidation of Si (Silico to form SiO_2, Basically involves placing of batch of wafe in clear, silica

* when can be heated to high temperature (800-100°C) using heating coils in a furnace with ceramic brick insulating liner

* An oxygen containing a gas such as dry O_2 or H_2O followed in the tube at a atmosphere pressure, flowed out at the other end

* A batch of Si wafers is placed in the Si wafer holdred

* The Gases flow from the top and flow out at the bottom providing more uniform flow than in conventio horizontal furnace

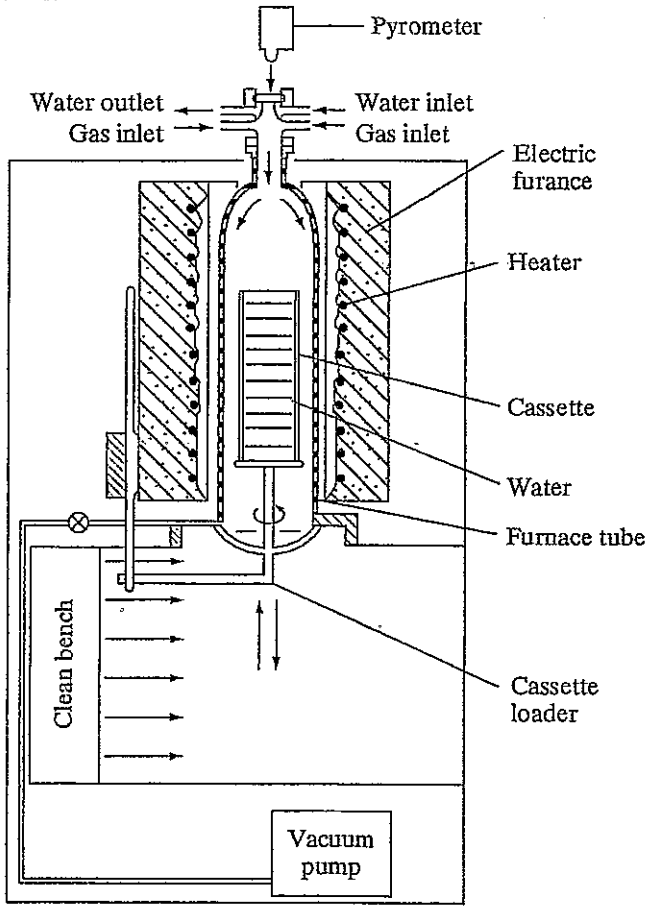
$$Si + O_2 \rightarrow SiO_2 \quad \text{[dry oxidation]} \qquad \text{—(2M)}$$

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2 \text{ [wet oxidation]}$$

* In both the case Si is consumed from the surface o the substrate

* Oxidation proceed by hows the oxidant (O_2/H_2O) molecul diffuse through the already grown to the si-sio interface

* plots of oxidation as a function of time at diffrent temp as shown from dry and wet oxidation of Si



(3m)

2) What is metallization process? Explain the metallization process

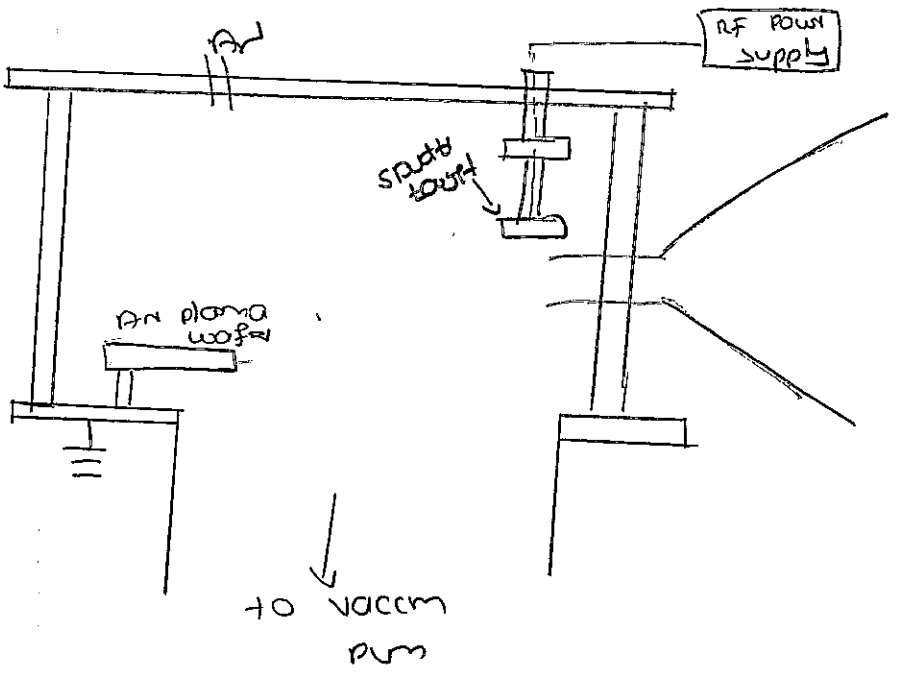
* metal films are generally deposited by a physical vapour deposition technique as evaporation

* Many of the Al atoms ejected from the target deposited on Si wafers held in close proximity to the target

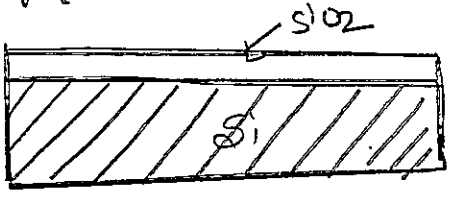
* The Al is then patterned using metalisation subsequently etched by RIE, Finally it is sintered at ~ 450° for the 30 minutes to form a good electrically Ohmic contact to Si

* After the interconnection metallisation is completed a protective over coat of silicon nitrade is deposited using plasma enhance CVD, then individual integrated circuit

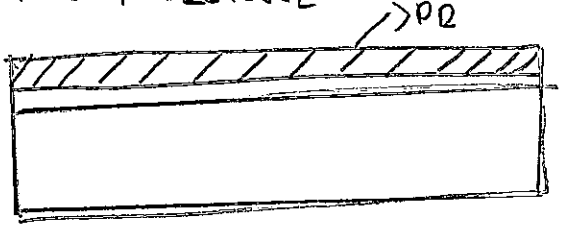
(5m)



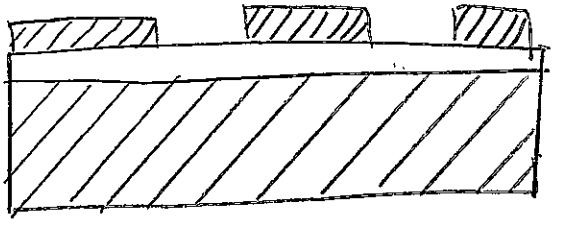
=> oxidize the Si sample :-



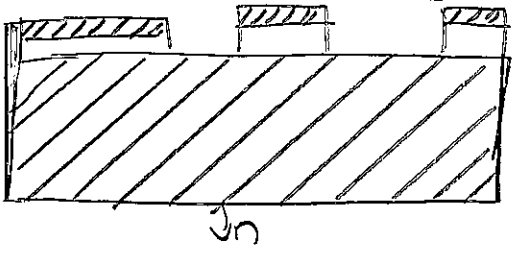
=> Apply a layer of +ve photoresist



=> Remove Exposed PR



=> Implant boron through window in the PR



10)

a) Explain integration of other circuit elements with diagrams

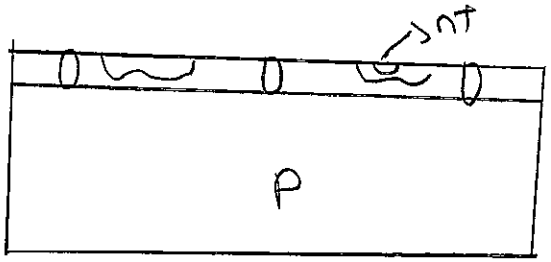
⇒ Diodes:-

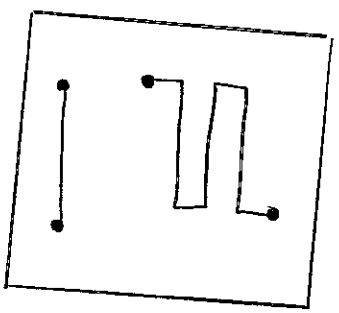
* It is simple to build p-n junction diodes in Monolithic circuit
* It is also common practise to use transistor to perform diode function
* Most common method is to use the emitter junction as the diode with the collector and base shorted
* having narrow base diode structure, which has high switching speed with little charge

——— (2m)

⇒ Resistors:-

* Diffused or implanted resistor can be obtained in monolithic circuit by using shallow junctions
* Design of diffused resistors begins with a quantity called sheet resistance diffused layer
* If the average resistivity of a diffused region is ρ the resistor of a given length L is $R = \rho L/wt$
* R_S is measured for a given layer is numerically the same for any size square L=w

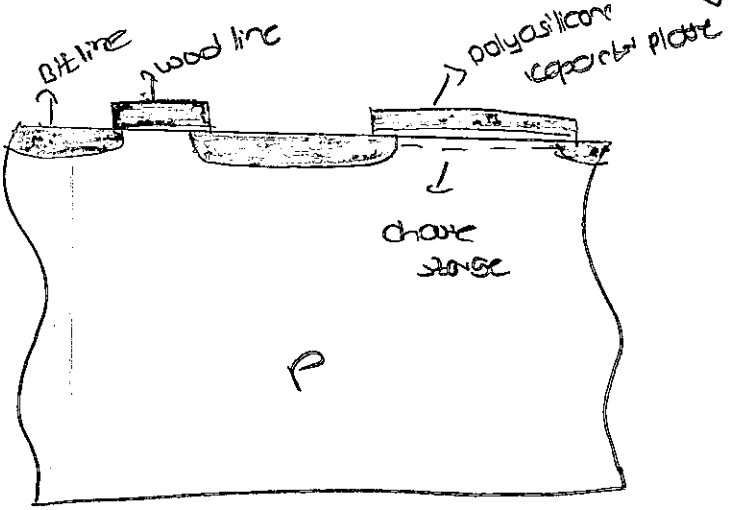




——— (3m)

⇒ Capacitors:-

* One of the most important element
* This is particularly true in the case of memory circuits, where charge is stored in a capacitor for each bit of information
* The top plate of the capacitor is polysilicon, and bottom plate is charge inversion contacted by an n+ region
* The terms bit line and word line refer the row and column organization of the memory



—— (3m)

⇒ Inductors:-

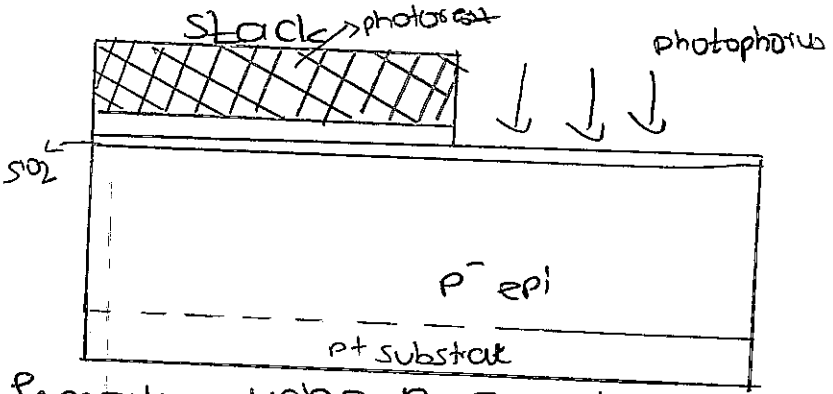
* They has changed because of the growing need for rf chips Ic for the portable communication
* applications such as resonable Q factor using spiral wound thin metal films on an Ic
* Such spiral pattern can be defined by photolitography and etching technique compatible with Ic processing
* They are harder to integrate inductor than the other circuit elements

—— (2m)

b) Explain CMOS process integration with help of neat diagrams

⇒ n-well formation using P, donor implant

* First grow thermally "pad" oxide (≈ 20nm) on Si substrate
* Followed by low pressure chemical deposition LPCVD of silicon nitride (≈ 120nm)
* Reactive ion etching (RIE) is then used to etch the oxide-nit



⇒ p-well formation using B acceptor implant

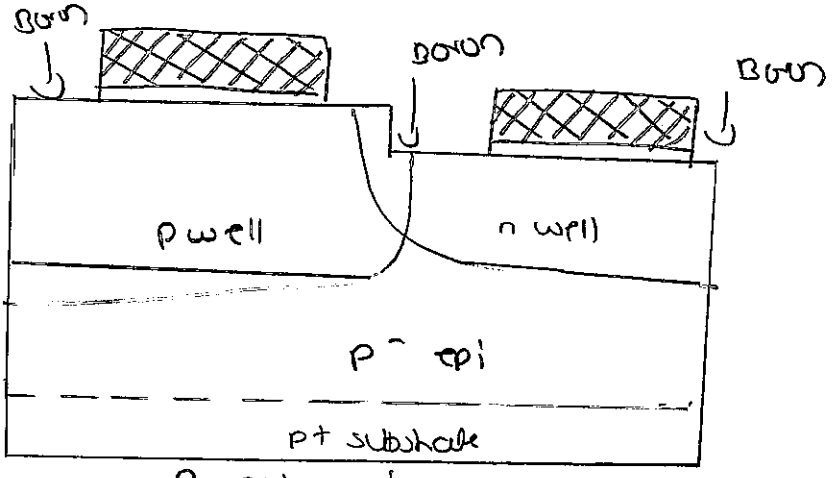
* After the implant the photoresist is removed and patterned wafer is subjected to wet oxidation to grow tank (≈ 600nm)
* The tank oxidation process consumes Si from the substrate and Resulting oxide swells up

⇒ Self-aligned implant mask

* It allows a tighter packing density of the twin wells because it is not required to account for lithographic misalignment during layout
* After this diffusion, the silicon nitride-oxide stack and tank oxide are etched away

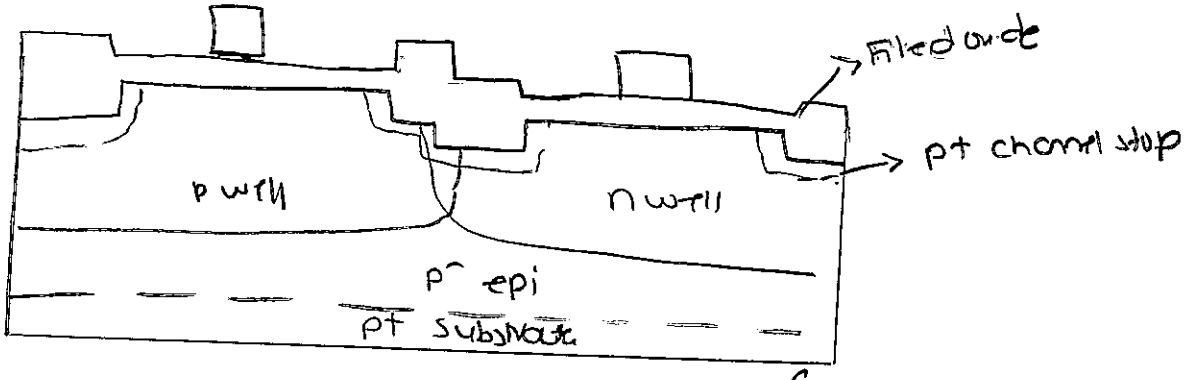
⇒ Isolation Region:-

* A stack of silicon dioxide - silicon nitride is photolithography pat-terned in subjected to RIE
* There will no electrical cross talk between adjacent transistors, unless they are intentionally interconnected
* V_T and so such that leakage current is minimal



⇒ Local oxidation of Silicon:-

* After the channel stop implant, the photoresist is removed and wafer with the patterned nitride oxide stack
* It is subjected to wet oxidation to selectively grow a field oxide ≈300nm thick
* Procedure is called Local oxidation of silicon (LOCOS)



(10 M)