CBCS SCHEME

USN | | | | | | | | | |

18CS33

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain the working principle of photocoupler. **(08 Marks)**

b. List the different types of BJT biasing. Derive the expression for collector emitter voltage (V_{CE}) for fixed bias circuit. **(08 Marks)**

c. Write a note on light emitting diode. **(04 Marks)**

OR

2 a. Explain with neat diagram, the construction, working principle and characteristics equation of photodiode. **(08 Marks)**

b. With a neat waveform and circuit diagram, explain the working of monostable multivibrator. **(06 Marks)**

c. Explain with neat diagram R-2R ladder type DAC and derive the expression for V_0. **(06 Marks)**

Module-2

3 a. Minimize the following function for SOP using K-map and implement it using basic gates:
$f(a,b,c,d) = \Pi M(5,7,13,14,15) + d(1,2,3,9)$ **(06 Marks)**

b. Design the function EX-OR using (i) NAND gates only (ii) NOR gates only **(06 Marks)**

c. A switching circuit has two control inputs (C_1 and C_2), two data inputs (X_1 and X_2) and one output Z. The circuit performs one of the logic functions such as OR, XOR, AND, EQU for control inputs combination C_1, C_2 as 00, 01, 10, 11 respectively:
(i) Derive the truth table for Z
(ii) Use a K-map to find minimum AND-OR gate circuit to realize Z. **(04 Marks)**

OR

4 a. Minimize the following function for POS using Kmap and realize it by using basic gates:
$f(a,b,c,d) = \Pi M(0,1,6,8,11,12) + d(3,7,4,15)$ **(06 Marks)**

b. Plot the following function on a K-map (Do not expand to minterm before plotting):
$F(A,B,C,D) = \overline{A}\,\overline{B} + C\overline{D} + ABC + \overline{A}\,\overline{B}C\overline{D} + ABC\overline{D}$, find the minimum sum of products. **(06 Marks)**

c. A digital system is to be designed in which the month of the year is given as I/P is four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess number in the I/P beyond '1011' as don't care condition:
(i) Write truth table, SOP Σm and POSΠM form
(ii) Simplify for SOP using K-map
(iii) Realize using basic gates **(08 Marks)**

Module-3

5 a. Explain with neat diagram static hazard 0 and its recover method. (06 Marks)

b. Implement the following function using $3 \times 4 \times 2$ PLA:
$A(x,y,z) = \sum m(0,1,3,4)$; $B(x,y,z) = \sum m(1,2,3,4,5)$ (08 Marks)

c. Using EVM method simplify the following function and implement it by using 8:1 MUX
$F(a,b,c,d) = \Sigma m(0, 1, 2, 4, 5, 6, 9, 10, 12, 13, 14, 15)$ (06 Marks)

OR

6 a. With a neat diagram, explain 3 to 8 line decoder. (04 Marks)

b. Construct 32:1 MUX using 8:1 MUX and 2:4 decoder. (08 Marks)

c. Design 7 segment decoder and realize using PLA. (08 Marks)

Module-4

7 a. Explain with a neat diagram, VHDL program structure. (06 Marks)

b. Construct SR gates latch using NAND gates and derive the characteristics equation for the same. (08 Marks)

c. Explain T-flipflop with characteristics equation. (06 Marks)

OR

8 a. Explain with neat diagram, working of JK flipflop and derive its characteristic equation. (08 Marks)

b. Write VHDL code for 4 bit adder. (06 Marks)

c. Explain the application of SR latch in switch debouncing technique. (06 Marks)

Module-5

9 a. With neat diagram, explain 4 bit parallel adder with accumulator. (08 Marks)

b. With diagram explain 4 bit SISO register. (08 Marks)

c. Write a note on Johnson tail counter. (04 Marks)

OR

10 a. Design Mod 5 counter using JK flipflops. (10 Marks)

b. Explain 4 bit PIPO shift register with block diagram. (06 Marks)

c. Write a note on ring counter. (04 Marks)

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Third Semester B.E Degree Examination,

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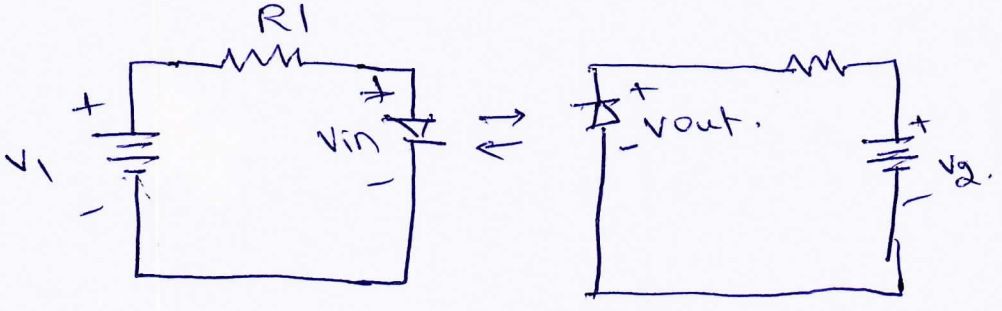
Time: 3 hrs. 18CS33.

Analog and Digital Electronics. Max marks: 100

Module 01.

1a. With a neat diagram, explain the working principle of photocoupler? 08 marks



working principle of photocoupler.

When the light from LED hits the photodiode, this sets up a reverse current in the output circuit. The reverse current produces a voltage ~~drops~~ at the o/p resistor. When the input voltage is varying, the amount of light is fluctuating. This means the the output voltage is varying in step with the input voltage. The combination of an LED & a photodiode is called an opto coupler.

1b. List the different types of BJT Biasing. Derive the expression for Collector – emitter voltage for fixed bias current. 08 marks

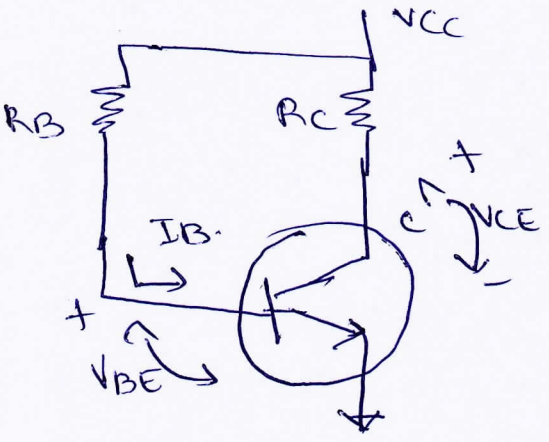
There are, mainly 3 types of Biasing a

a) Base bias or fixed bias

b) collector to base ↑Bias

c) voltage divider Bias.

a) Base Bias or fixed bias



Base resistors R_B is used between V_{CC} & Base to establish this base current I_B.

As V_{CC} & R_B are fixed quantity it remains fixed & hence called fixed or Base Bias.

Applying KVL for base circuit

$$V_{CC} - I_B R_B - V_{BE} = 0.$$

$$I_B R_B = V_{CC} - V_{BE}.$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Applying KVL for collector circuit.

$$V_{CC} - I_C R_C - V_{CE} = 0.$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}.$$

Q: Write a note on light emitting diode? 04mark

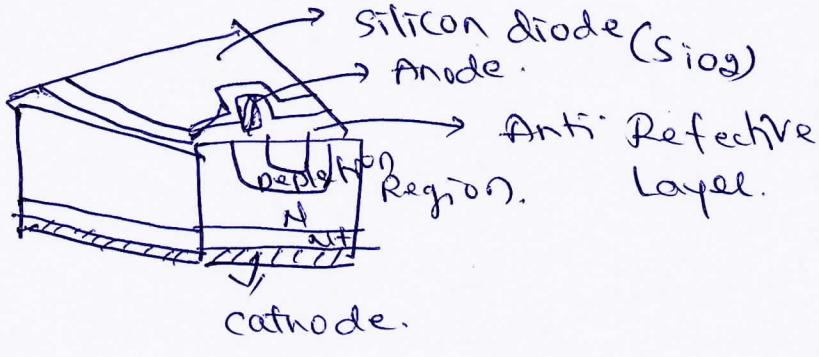
LED is a PN function diode which emits light when an electric current passes through the forward direction.

The energy converted during recombination at the junction is dissipated in the form of heat within the structure & the emitted light.

When the device is forward biased, electrons from the P-N junction from the N-type material recombine with holes in the P-type material.

Example / Applications – TV Remote, Calculator, Watches & Traffic Signals.

2a. Explain with neat diagram, the construction, working principle & characteristic equation of photodiode. 08m



Photodiode is a light detection semi-conductor device that converts light energy into electric current or voltage which depends upon the mode of operation.

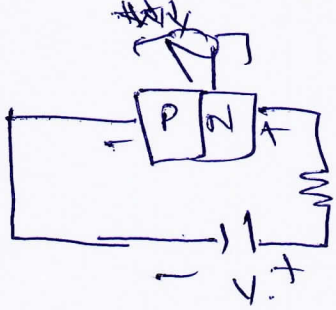
Construction.

→ The surface of a layer of N-type is bombarded with P-type silicon ions to produce a P-type layer about 1μm thick.

During the formation of the diode, electrons from

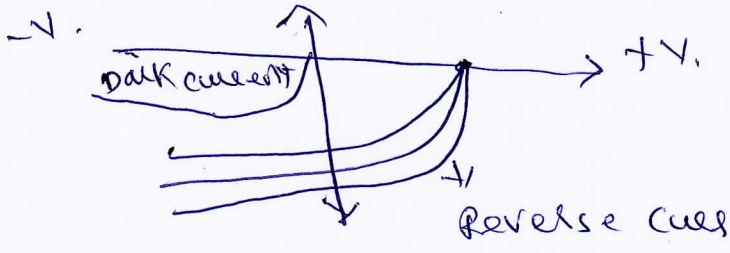
the p-type material & holes from the p-type are attracted into the N-type layer. resulting in the removal of free charge carriers close to the PN junction, so creating a depletion region.

The top of the diode is protected by a layer of Silicon dioxide in which there is a window for light to shine on the semiconductor. Beneath the N-type layer is a more heavily doped N+ layer to provide a low resistance connection to the cathode.



photodiode.

Symbol.



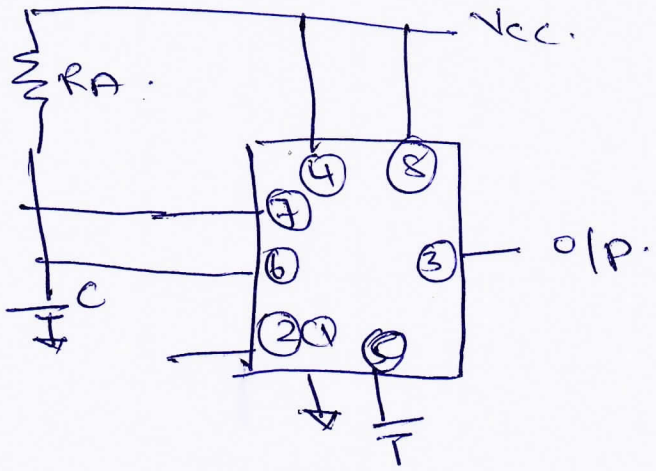
VI characteristics of photodiode.

When PN junction of photodiode is exposed to light, the reverse current increases with increase in light intensity. The reverse-biased current is produced by thermally generated electron-hole pairs in the depletion region.

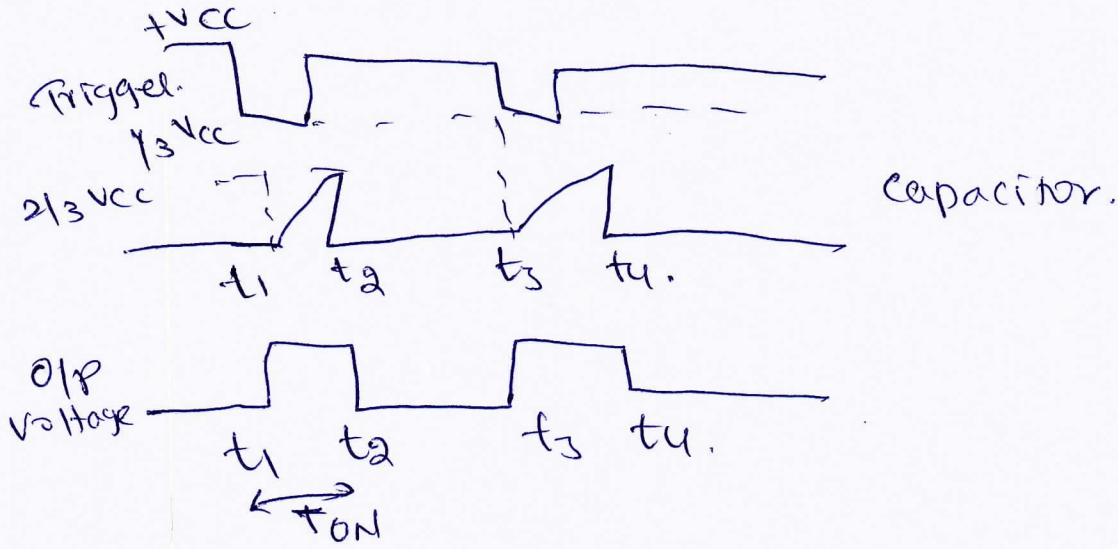
2.b. With a neat waveform and circuit diagram, Explain the working of monostable multivibrator? 8 Marks

monostable multivibrator is circuit which contains one Stable State.

Circuit diagram.



waveform.



$T_{ON} = T_2 - T_1$

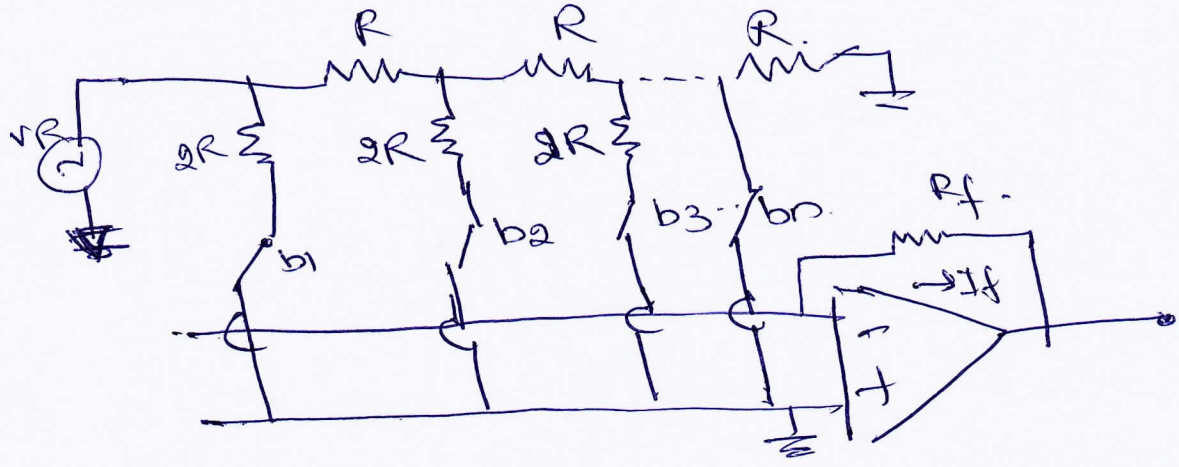
Working: Initially the SR flip flop is set (Q=1) transistor T is driven into saturation & capacitor is by-passed by the transistor.

$V_C = 0$ and o/p V_g is also zero. when -ve pules applied to trigger input of compalator then compalator

output goes high & SR flipflop is reset & Q goes high.

Then, $T_{ON} = 1.7\, R_{AC}$.

2.C. Explain the with neat diagram R-2R ladder type DAC & delive the expression for V_o? 06 marks



DAC is a circuit which converts digital signals into analog signals. It has n- electronic switches as shown in the figure, which are connected to resistor 2R & R. If binary input is high, then switch connects to resistance path. Similarly for binary input lo it disconnects.

Mathematically,

for ON switch, current $I_1 = \frac{V_R}{2R}$.

for OFF switch, current $I_1 = 0$

111 for $I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R}$.

$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R}$.

$$I_n = \frac{V_R / 2^n - 1}{2R}$$

W.K.T $V_o = -I_f R_f$

$$V_o = -R_f \left[\frac{V_R}{2R} b_1 + \frac{V_R}{R_1 R} b_2 + \frac{V_R}{8R} b_3 + \cdots \frac{V_R}{2^n R} b_n \right]$$

$$V_o = -\frac{R_f}{R} V_R \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right].$$

When $R_f = R$.

$$V_o = -V_R \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right].$$

⇒

Module 02.

3a. Minimize the following function for SOP using k-map and implement it using basic gates. ORmarks

$f(a,b,c,d) = \Pi M(5,7,13,14,15) + d(1,2,3,9)$

Given $f(a,b,c,d) = \Pi M(5,7,13,14,15) + d(1,2,3,9)$

Converting into minterm form for SOP.

$f(a,b,c,d) = \Sigma m(4,6,8,10,11,12) + d(1,2,3,9)$

ab \ cd	00	01	11	10
00	0 (0)	X (1)	X (3)	X (2)
01	1 (4)	0 (5)	0 (7)	1 (6)
11	1 (12)	0 (13)	0 (15)	0 (14)
10	1 (8)	X (9)	1 (11)	1 (10)

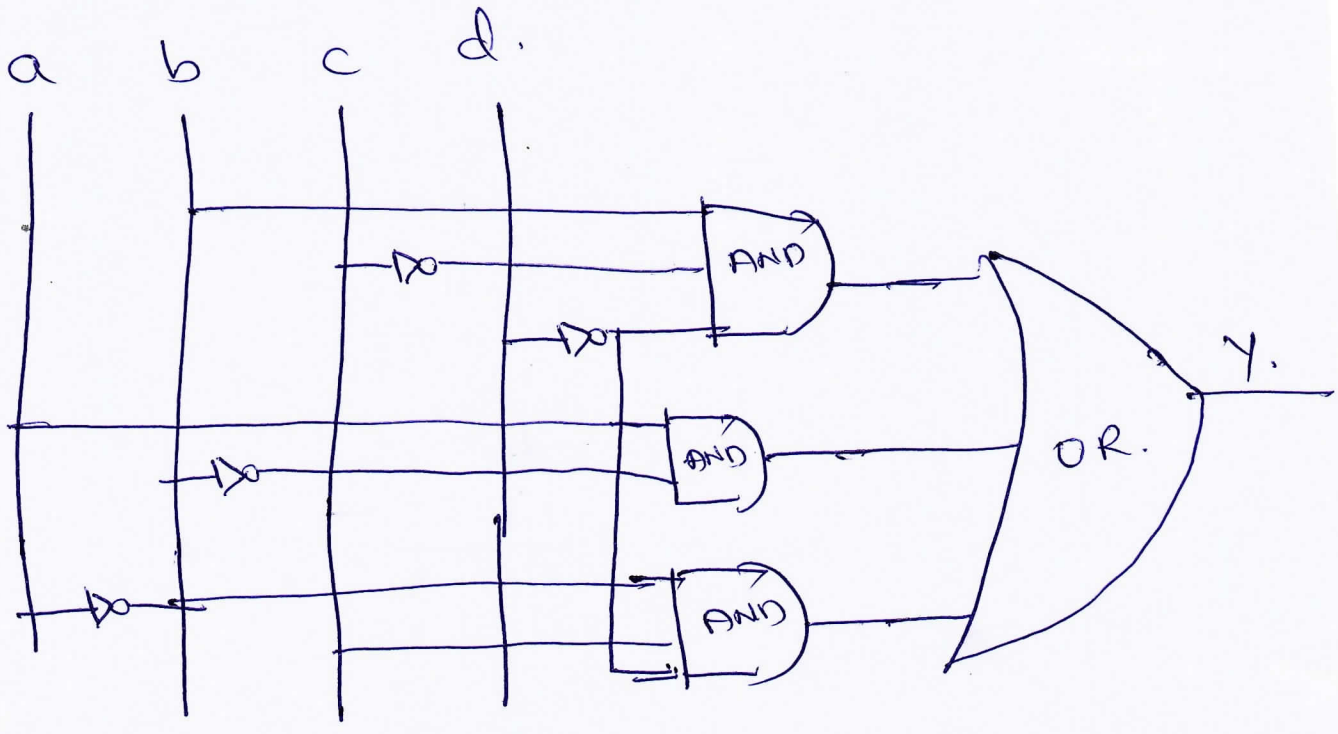
SOP expression

$= b\bar{c}\bar{d} + a\bar{b} + \bar{a}c\bar{d}$

Sop expression

$y = b\bar{c}\bar{d} + a\bar{b} + \bar{a}c\bar{d}$

Realize the circuit using basic gates.

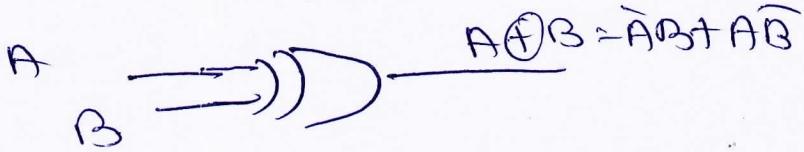


3b) Design the function EXOR using. i) NAND gates only. ii) NOR gates only. ? 06 marks

i) NAND gates only.

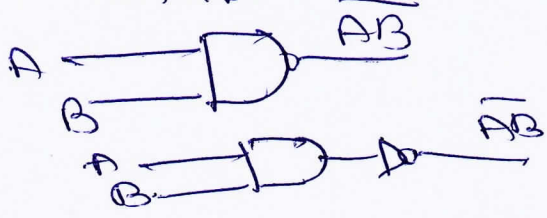
Required

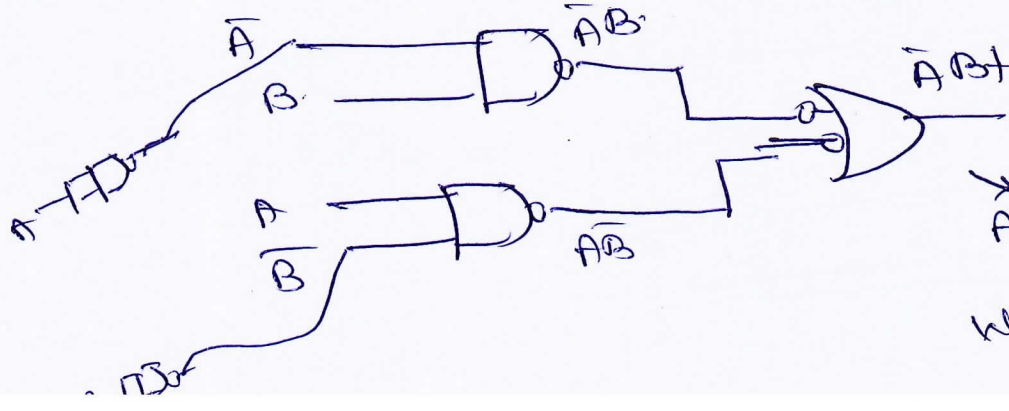
XOR -

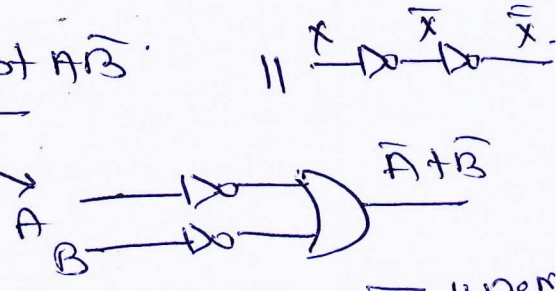


Available.

NAND.







W.K.T $\bar{A} + \bar{B} = \overline{AB}$ ||Den
(a

ii) XOR gate using NOR gate.

$$F = A\bar{B} + \bar{A}B$$

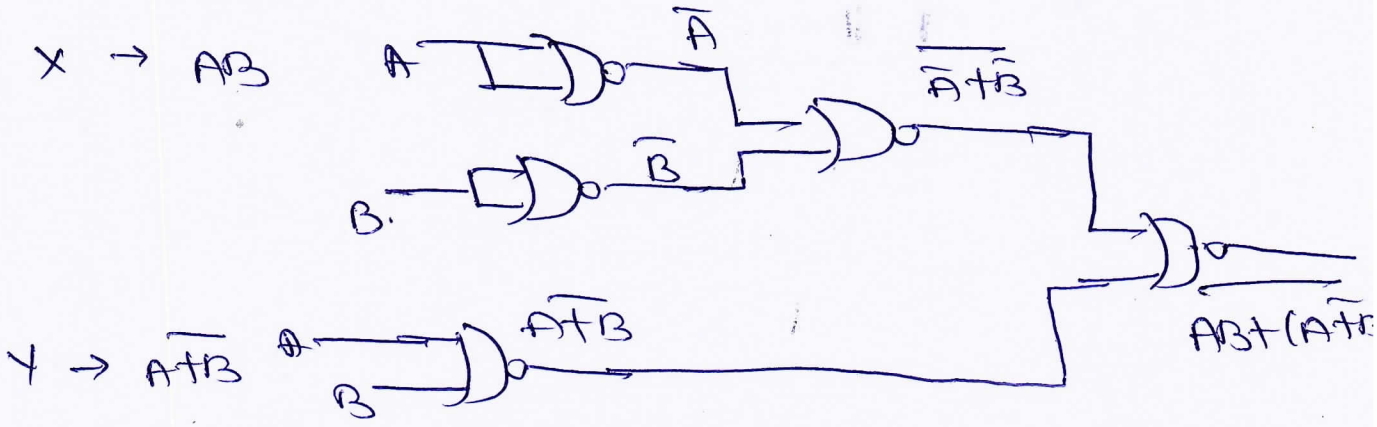
$$F = (A+B)(\bar{A}+\bar{B})$$

$$F = (A+B)(\overline{AB}) \quad \text{// De moggan law.}$$

$$\bar{F} = (A+B) + (AB)$$

$$F = \bar{\bar{F}} = \overline{AB + (A+B)}$$

X Y



$$F = \overline{AB + (A+B)}$$

$$= \overline{AB} \cdot (A+B) = (\bar{A}+\bar{B})(A+B)$$

$$= \bar{A}B + A\bar{B}$$

3c. A switching circuit has two control inputs (C_1 and C_2) two data inputs (X_1 and X_2) and one output Z. The circuits performs one of the logic functions such as OR, XOR, AND, EQV for control inputs combination C_1, C_2 as 00, 01, 10, 11 respectively. 04 marks.

i) Derive the truth table for Z.

ii) use a K-map to find minimum AND-OR g

i) Truth table for Z.

X_1	X_2	C_1	C_2	Z.	
0	0	0	0	0	
0	1	0	0	1	
1	0	0	0	1	} OR.
1	1	0	0	1	
0	0	0	0	0	
0	1	0	1	1	
1	0	0	0	1	} XOR.
1	1	0	1	0.	
0	0	0	0	0	
0	1	0	0	0	} AND.
1	0	1	0.	0	
1	1	1	0	1	
0	0	1	1	1	
0	1	1	1	0	} EQU.
1	0	1	1	0	
1	1	1	1	1	

Truth table:-

X_1	X_2	C_1	C_2	Z.
1	1	0	1	0
1	1	1	0.	1
1	1	1	1	1

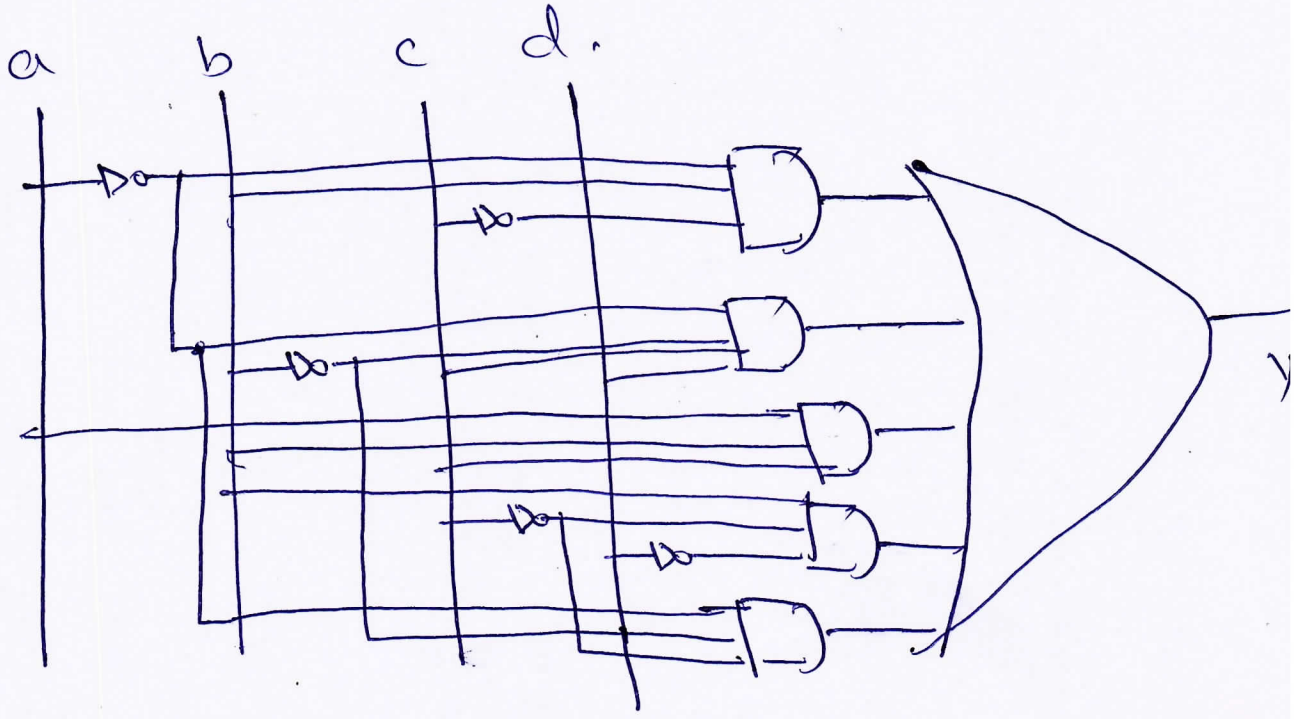
X_1	X_2	C_1	C_2	Z.
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0.	0
1	0	1	1	0
1	1	0	0.	1

ii) k-map.

ab \ cd	00	01	11	10
00	0	0	1	0
01	1	1	0	0
11	1	0	1	1
10	1	1	0	0

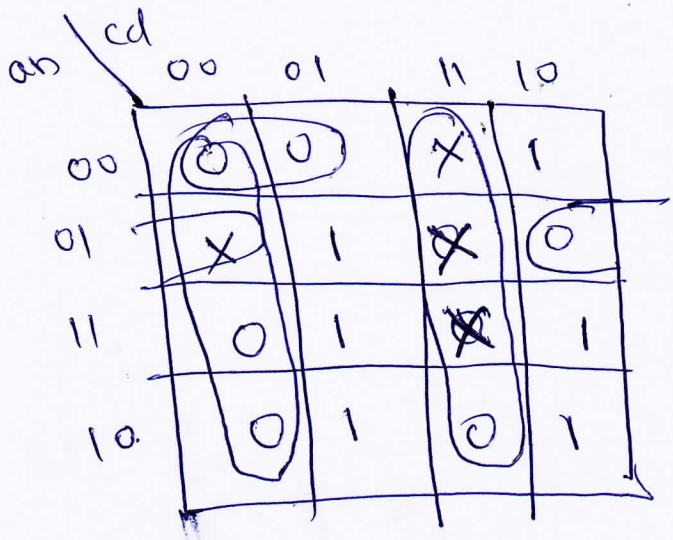
$Y = \bar{a}b\bar{c} + \bar{a}\bar{b}cd + abc + b\bar{c}\bar{d} + a\bar{b}\bar{c}$

Realize the given expression.



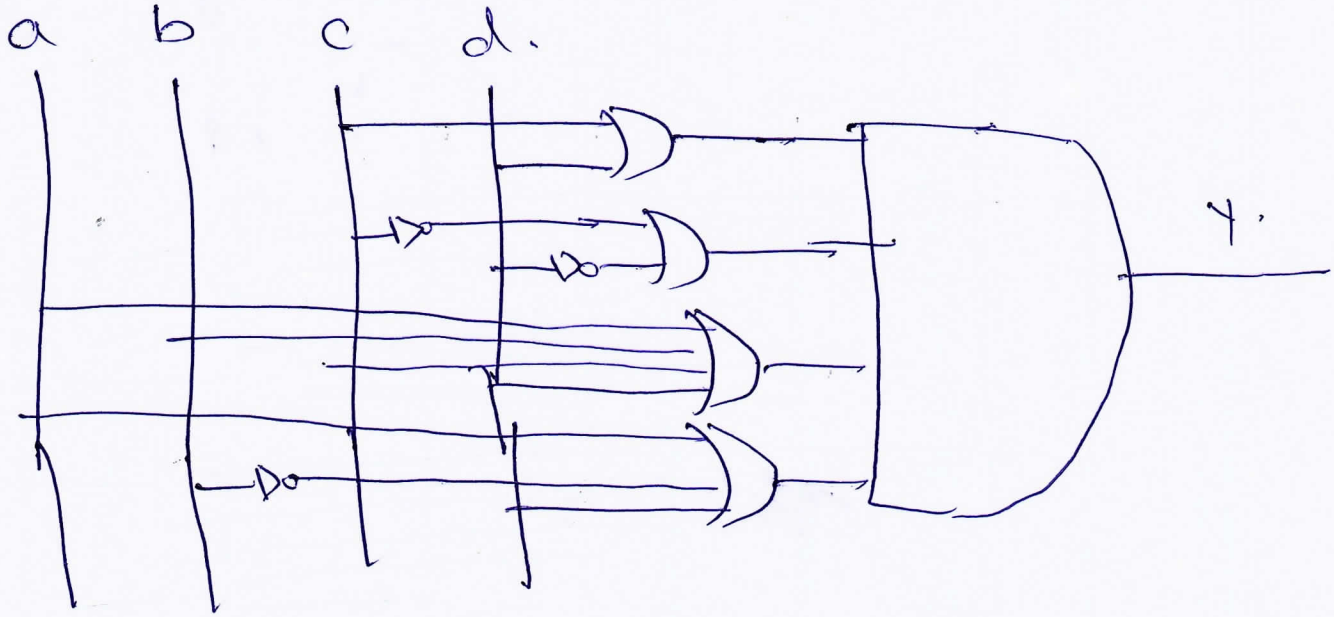
4a). Minimize the following function for POS using k-map. and realize it by using basic gates.

$f(a,b,c,d) = \Pi M(0,1,6,8,11,12) + d(3,7,14,15)$ (Or)



$Y = (c+d)(\bar{c}+\bar{d})(a+b+$
$(a+\bar{b}+d)$

Realize the expression Y.

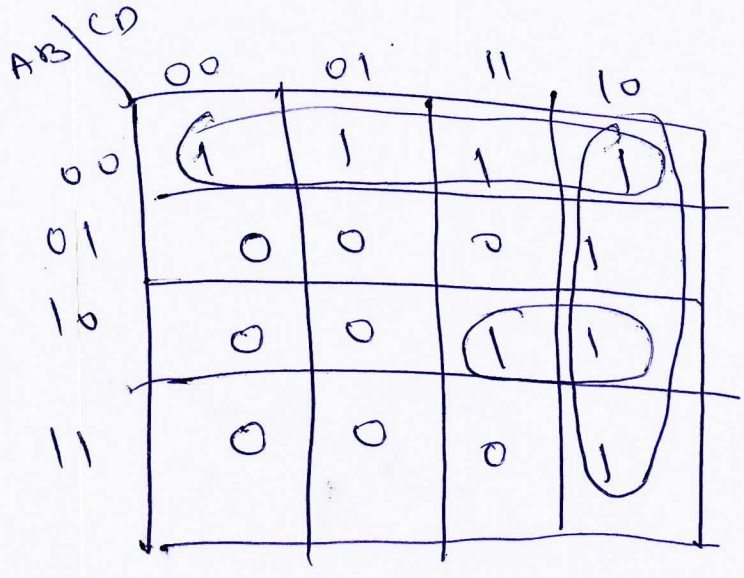


4b) Plot the following function on K-map (DO not expand to minterm before plotting):

$F(A,B,C,D) = \bar{A}\bar{B} + C\bar{D} + ABC + \bar{A}\bar{B}C\bar{D} + ABC$

find minimum sum of products. 06 marks

$F(A,B,C,D) = m_3 + m_2 + m_1 + m_0 + m_{14} + m_{10} + m_6 + m_{15}$



$Y = \bar{A}\bar{B} + C\bar{D} + \cancel{A}BC.$

4c. A digital system is to be designed in which the month of the year is given as I/P is four bit fro The month January is represented as '0000'. February as '0001' and so on, The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it i '0'. Consider the excess number in the i/p beyon '1011' as don't care condition.

i) Write truth table, SOP Σm and POS ΠM for

ii) Simplify for SOP using K-map. 08 marks

iii) Realize using basic gates.

i) Truth table.

Month	A	B	C	D	Output
Jan	0	0	0	0	1
Feb	0	0	0	1	0
March	0	0	1	0	1
April	0	0	1	1	0
May	0	1	0	0	1
June	0	1	0	1	0
July	0	1	1	0	1
Aug	0	1	1	1	1
Sep.	1	0	0	0	0
	1	0	0	1	1
Oct	1	0	1	0	0
Nov	1	0	1	1	1
Dec.	1	1	0	0	x
	1	1	0	1	x
	1	1	1	0	x
	1	1	1	1	x

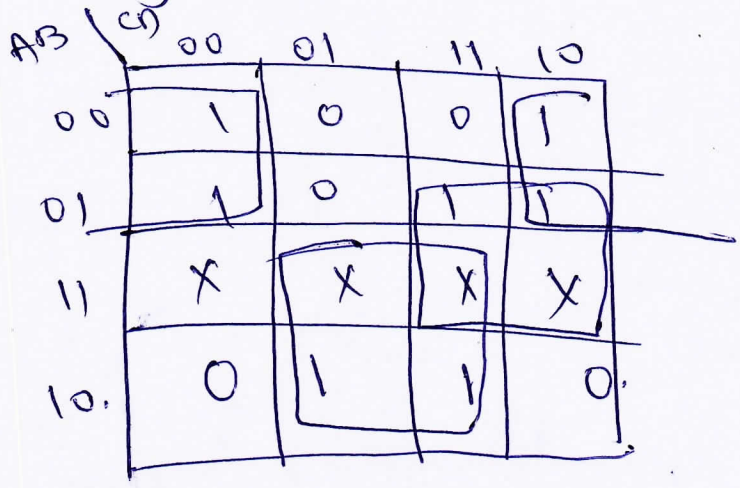
SOP form —

$$Y = \Sigma m(0,2,4,6,7,9) + d(12,13,14,15)$$

POS form —

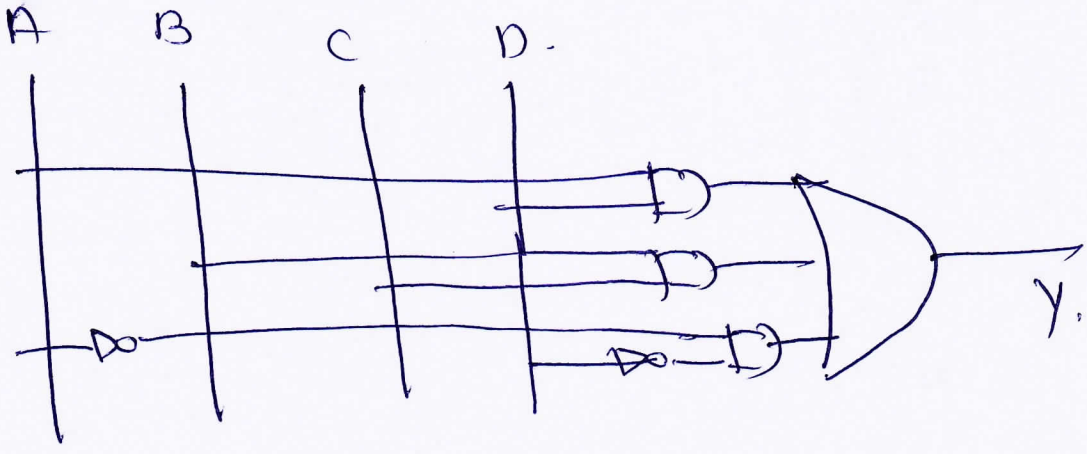
$$Y = \Pi M(1,3,5,8,10) \cdot D(12,13,14,15)$$

ii) SOP using K-map.



$Y = AD + BC + \bar{A}\bar{D}$.

iii) Realize the expression.

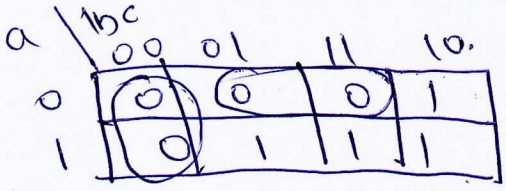


Module 03.

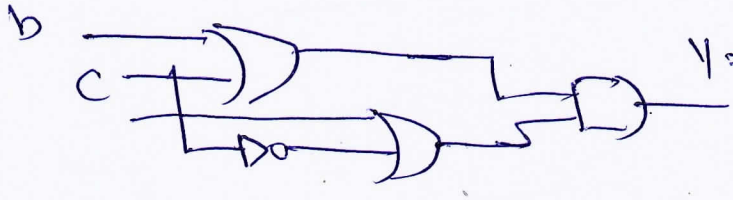
5a. Explain with neat diagram Static hazard 0 and its recover method? 06 marks.

Static 0 hazard — This type of hazard occurs for product of sum expression. It occurs for the situation $Y = A \cdot A'$.

Example: $Y = f(a,b,c) = \Pi M(0,1,3,4)$.



$Y = (b+c)(a+\bar{c})$.



Case 1: If $b=0$, $a=0$, $C=1$.

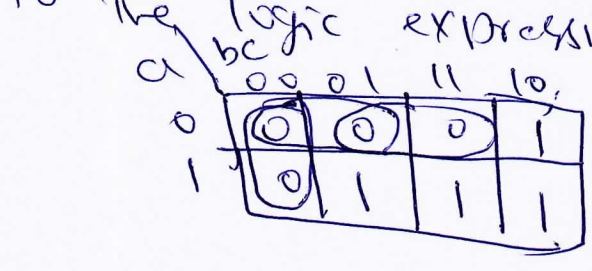
Due to not gate delay c' produces o/p as 1 and changes only after τ time.

$bc = 0 \cdot 1 = 1$.
$ac' = 0 \cdot 1 = 1$ $\Big\}$ $Y = 1$.

Case 2: If $b=0$, $a=0$, $C=0$, $Y=0$.

Hazard cover.

Hazard cover is adding extra maxterm to the logic expression.



$Y = (b+c)(a+\bar{c})(a+b)$.

$(a+b)$ term is independent of c.

5.b. Implement the following function using 3x4x2 PLA

$A(x,y,z) = \Sigma m(0,1,3,4)$; $B(x,y,z) = \Sigma m(1,2,3,4,5)$. 8 marks

$A(x,y,z) = \Sigma m(0,1,3,4)$

x \ yz	00	01	11	10
0	1	1	1	0
1	1	0	0	0

$A = \bar{x}z + \bar{y}\bar{z}$

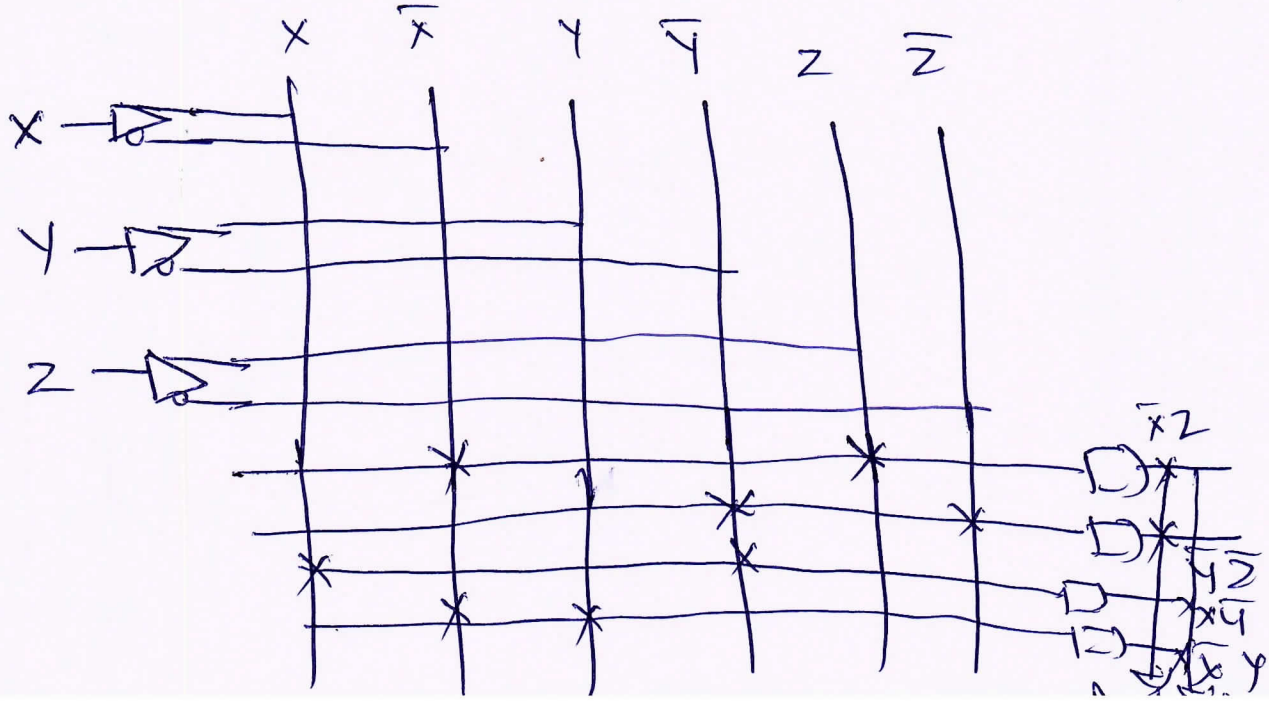
$B(x,y,z) = \Sigma m(1,2,3,4,5)$

x \ yz	00	01	11	10
0	0	1	1	1
1	1	1	0	0

$B = x\bar{y} + \bar{x}z + \bar{x}y$

PLA Table.

Product Terms	I/P's x	y	z	Outputs A	B
$\bar{x}z$	0	—	1	1	—
$\bar{y}\bar{z}$	—	0	0	1	—
$x\bar{y}$	1	0	—	—	1
$\bar{x}y$	0	1	—	—	1



5C. Using EVM method simplify the following function and implement it by using 8:1 MUX. 08 marks

$$F(a,b,c,d) = \Sigma m(0,1,2,4,5,6,9,10,12,13,14,15)$$

Truth table.

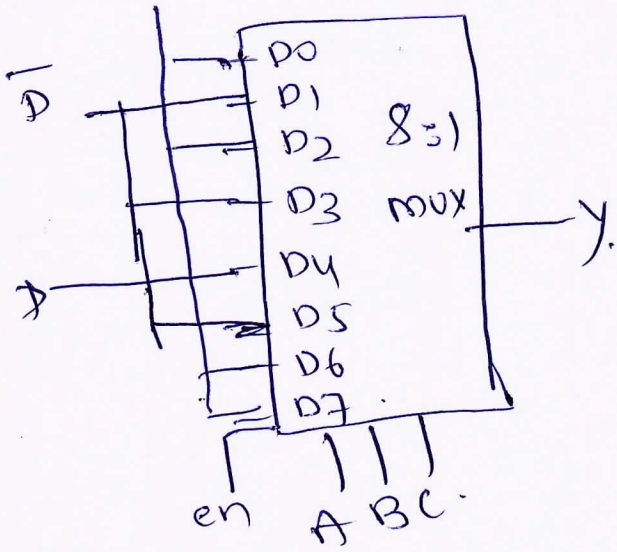
Assume D as MEV

A	B	C	D	y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

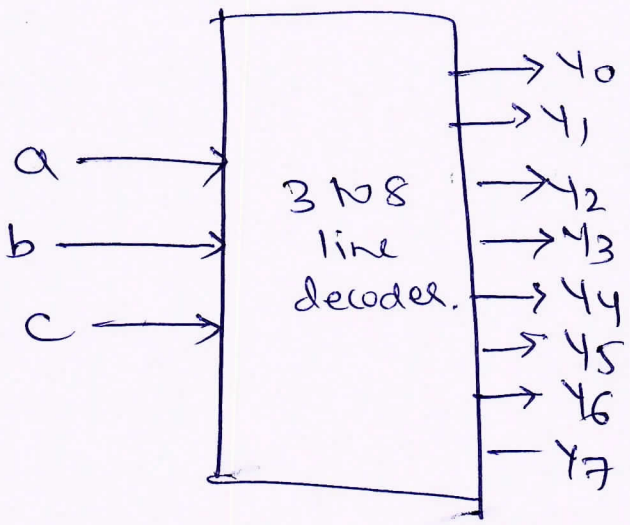
EVM table

A	B	C	y
0	0	0	1
0	0	1	$\overline{D}$
0	1	0	1
0	1	1	$\overline{D}$
1	0	0	D
1	0	1	$\overline{D}$
1	1	0	1
1	1	1	1

8:1 MUX

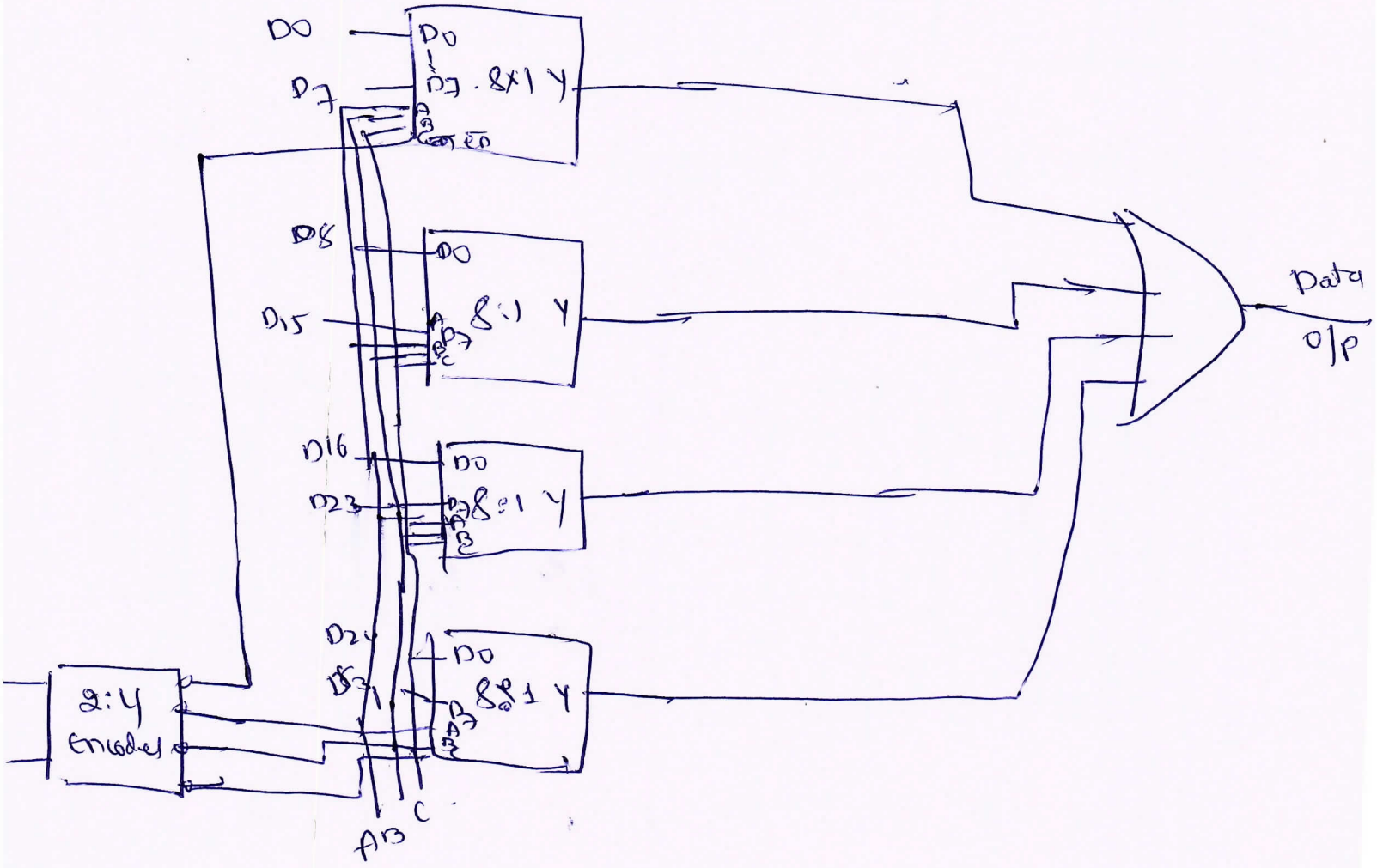


6a) With a neat diagram, explain 3 to 8 line decode



a	b	c	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5
0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0
0	1	1	0	0	0	1	0	0
1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

6b) Construct 32:1 mux using 8:1 mux and 2:4 dec



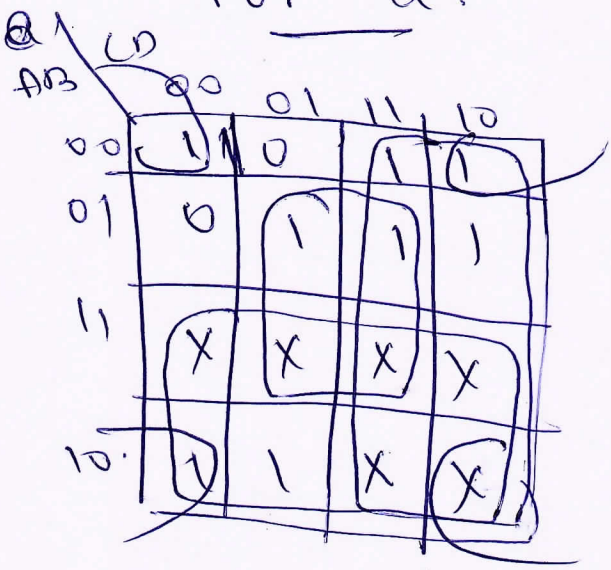
6c) Design 7-Segment decoder and realize using PLA. 08 marks.

Truth table for 7-segment decoder.

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

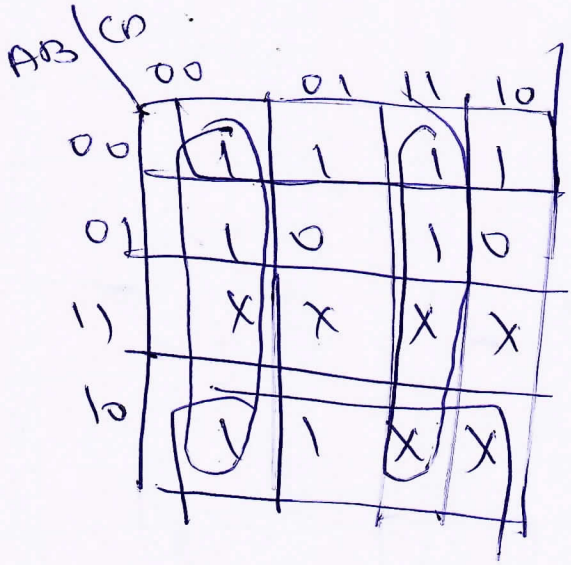
K-map Simplification

For a.



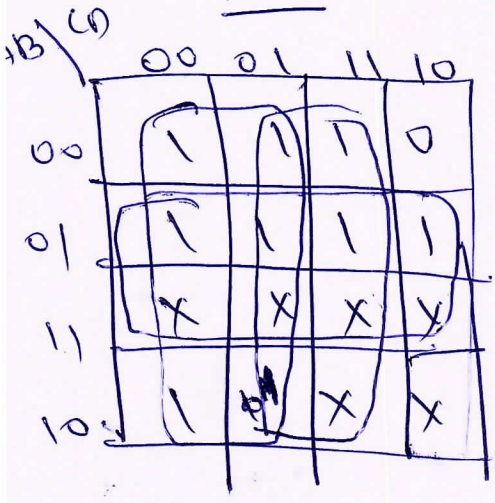
$a = A + C + B\bar{D} + \bar{B}\bar{D}$

For b



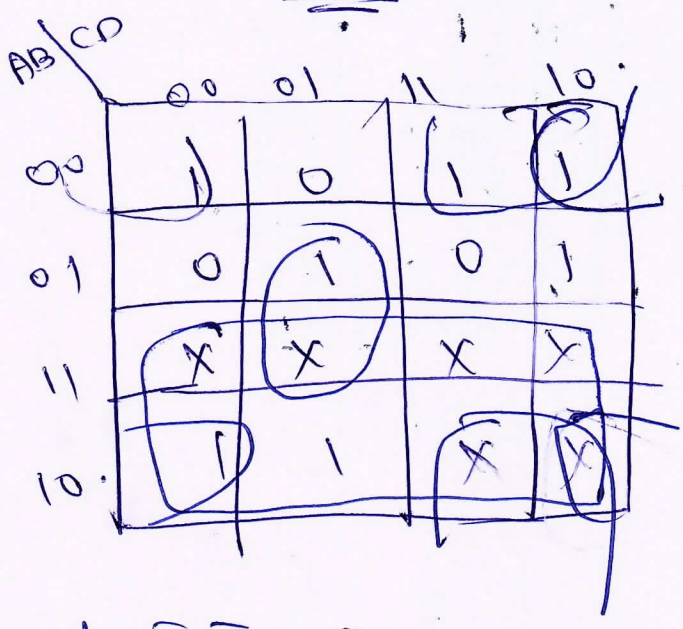
$b = \bar{B} + \bar{C}\bar{D} + CD.$

for C



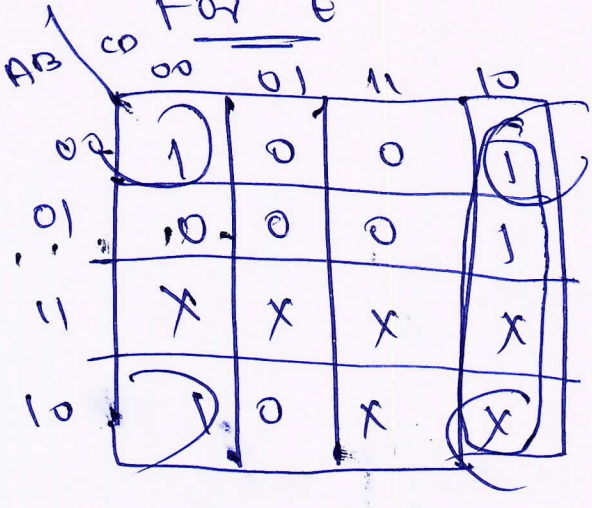
$C = B + \bar{C} + D.$

for D



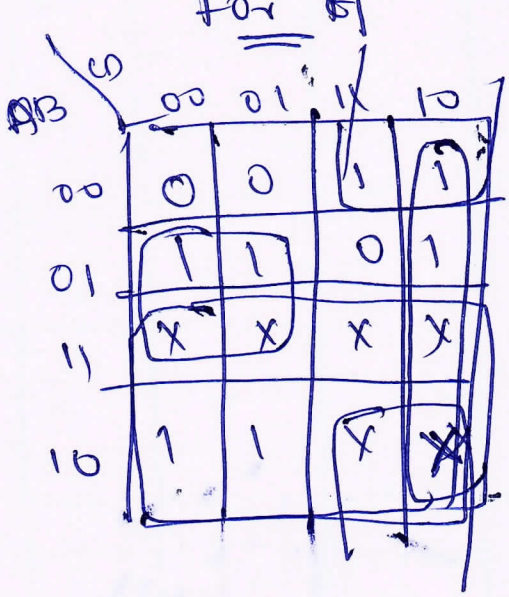
$d = \bar{B}\bar{D} + C\bar{D} + B\bar{C}D + \bar{B}C + A$

for E



$E = \bar{B}\bar{D} + C\bar{D}$

for G

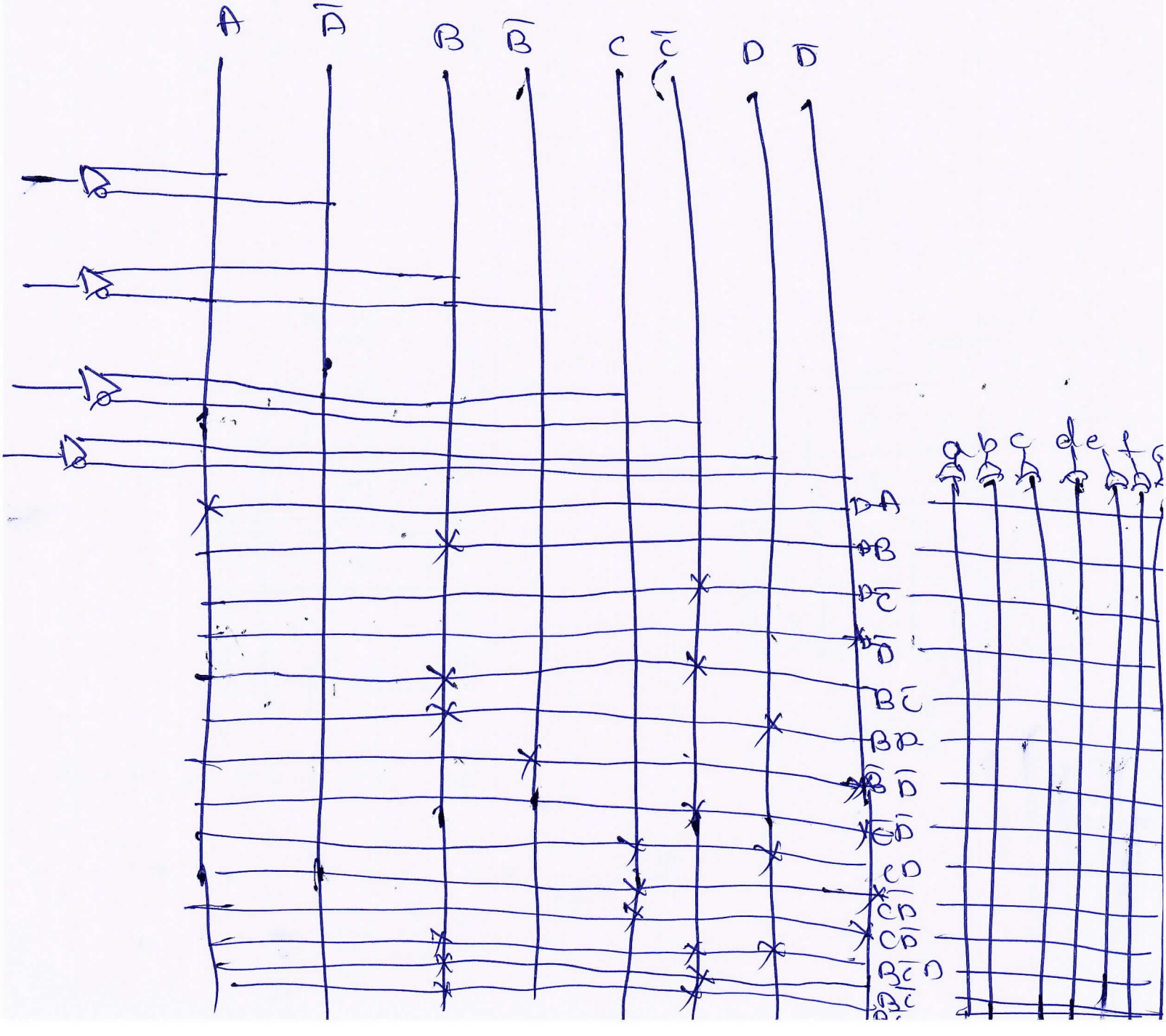


$G = A + B\bar{C} + \bar{B}C + C\bar{D}$

For F.

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

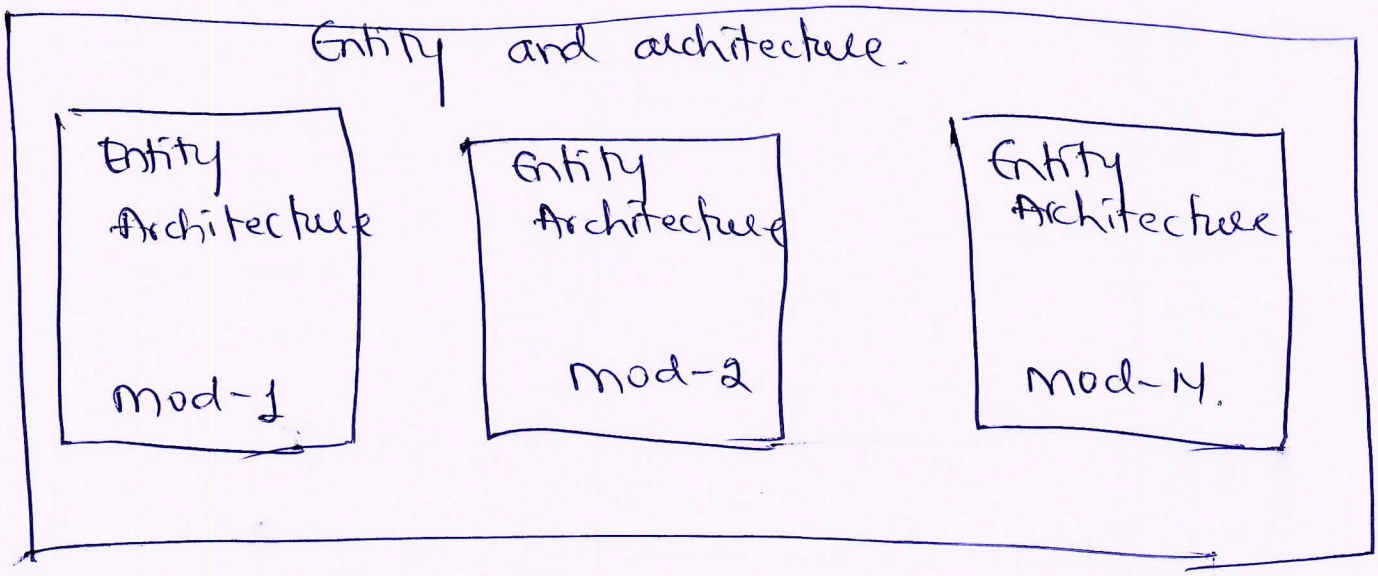
$F = A + \bar{C}\bar{D} + B\bar{C} + B\bar{D}$



Module 04.

7a) Explain with a neat diagram, VHDL program structure. 06marks

VHDL program structure.



When we describe a system in VHDL, we must specify an entity and an architecture at the top level and also specify an architecture for each component modules that as the part of the systems.

A VHDL module must have all inputs & outputs described in entity declaration & specifying the internal operation of the module using architecture declaration.

General format of entity declaration.

```
entity entity-name is
    [port (interface-signal-declaration);].
end [entity] [entity name];
```

General format for architecture.

architecture architecture_name of entityname is.

[declarations]

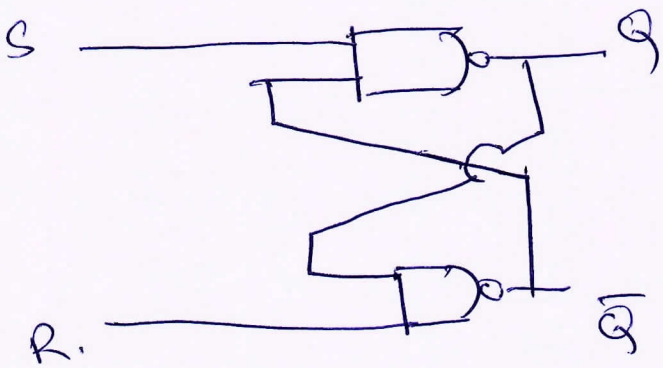
begin

architecture body.

end

[architecture] [architecture_name];

7b) Construct SR gates latch using NAND gates and derive the characteristics equation for the same? 05marks



case 1: $S=1, R=0, Q=0, \bar{Q}=1$

$S=1, R=1, Q=0, \bar{Q}=1$ memory.

case 2: $S=0, R=1, Q=1, \bar{Q}=0$

$S=1, R=1, Q=1, \bar{Q}=0$ memory.

Case 3: $S=0, R=0, Q=1, \bar{Q}=1$ Not used

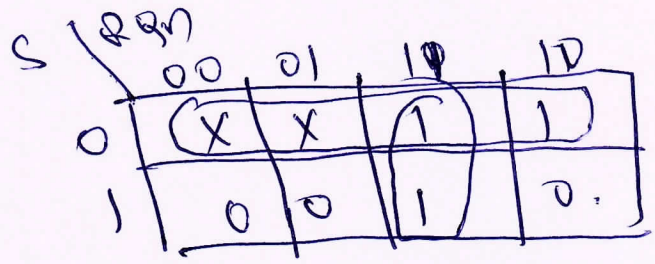
$S=1, R=1, Q=1, \bar{Q}=0$.

S	R	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	memory.	

Characteristic table

S	R	Qn	Qn+1
0	0	0	X
0	0	1	X
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

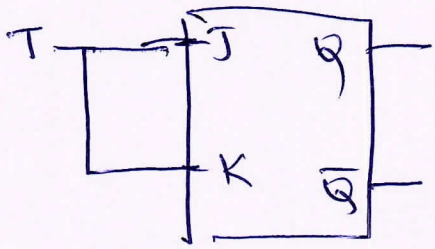
Characteristic Eqn



$Q_{n+1} = \bar{S} + RQ_n$

7.c Explain T-flip-flop with characteristics equation.

* T flip-flop is also known as 'Toggle flipf
* T flipflop is a modification of the JK flipflop
* It is obtained by connecting both inputs of J & K together.



Truth table for T-flip flop.

Clk	T	Qn+1
0	X	Qn
1	0	memory
↓	1	$\bar{Q_n}$

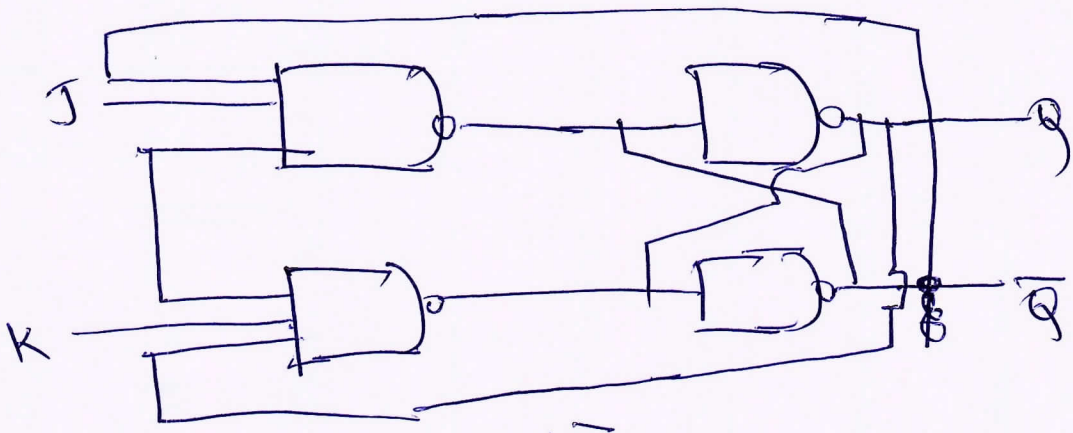
Characteristic Table.

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0.

Characteristic Equation

$Q_{n+1} = Q_n \oplus T$

8a. Explain with neat diagram, working of JK flip flop and delive its characteristic equation? 08 marks.



Q & $\bar{Q}$

clk = 0, memory

clk = 1, J = 1, K = 0, Q = 1, $\bar{Q}$ = 0.

clk = 1, J = 0, K = 1, Q = 0, $\bar{Q}$ = 1.

clk = 1, J = 1, K = 1, Q = 0, 1, 0, 1 .... $\bar{Q}$ = 1, 0, 1, 0 ....

Assume Q = 0, $\bar{Q}$ = 1.

Truth table

Clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
	0	1	0
	1	0	1
	1	1	toggle($\bar{Q}_n$)

Characteristic table.

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0.

Characteristic eqn

Q_n \ JK	00	01	10	11
0	0	0	1	1
1	1	0	0	1

$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}$

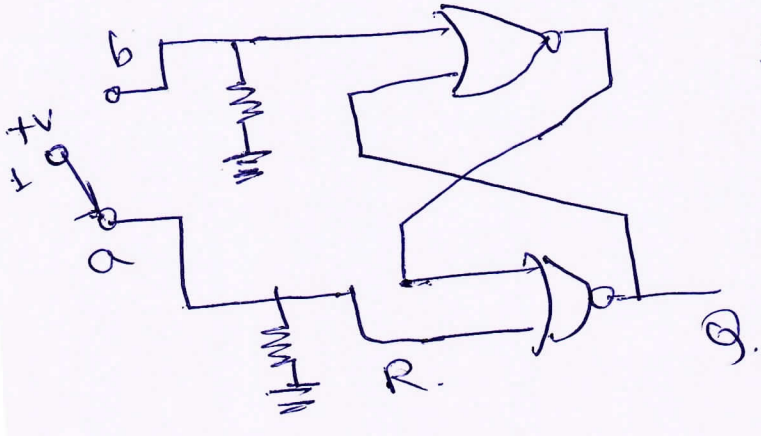
8b. Write VHDL code for 4 bit adder? 06 marks.

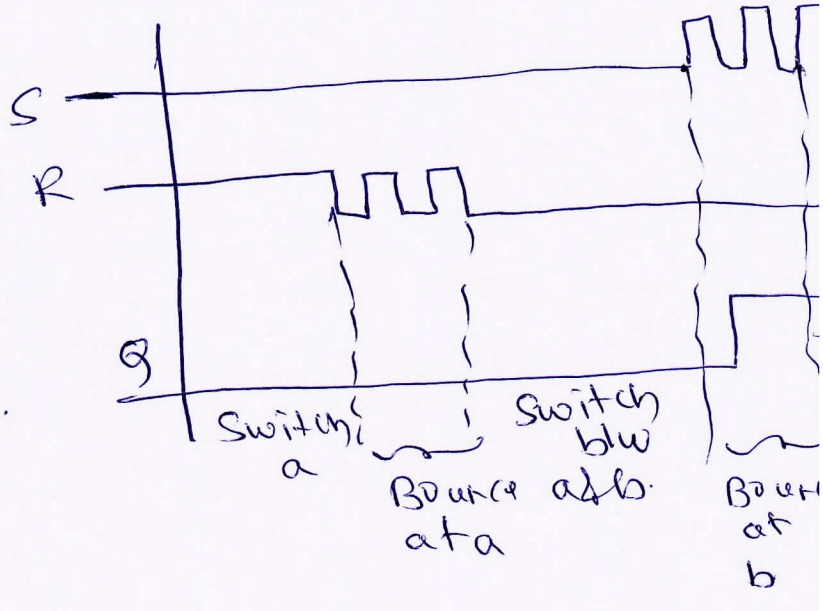
```
entity Adder4 is.
port (A,B : in bit_vector (3 downto 0);
      Ci : in bit
      S : out bit_vector(3 downto 0);
      Co : out bit):
end Adder4;
architecture Structure of Adder4 is.
component FullAdder.
  - port (x,y,Cin : in bit;
          cout, Sum : out bit)
end component.
Signal C : bit_vector( 3 downto 1);
begin
  - FA0 : Fulladder portmap (A(0), B(0), Ci, C(1), S(
  FA1 : Fulladder portmap (A(1), B(1), C(1), C(2), S(
  FA2 : Fulladder portmap (A(2), B(2), C(2), C(3), S(2)
  FA3 : Fulladder portmap (A(3), B(3), C(3), Co, S(3
end Structure;
```

C: Explain the application of SR latch in switch debouncing technique. 06 marks.

* useful application of the SR latch is for debouncing switches. When a mechanical switch is opened or closed, the switch contacts tend to vibrate or bounce open & closed several times before setting down to their final position. This produces a noisy transition, and this noise can interfere with the proper operation of a logic circuit.

The input of the switch in fig. below is connected to a logic 1 (+V). The pull down resistors connected to contacts a & b assure that when the switch is between a & b the latch inputs S & R will always be at logic 0, and the latch output will not change state.





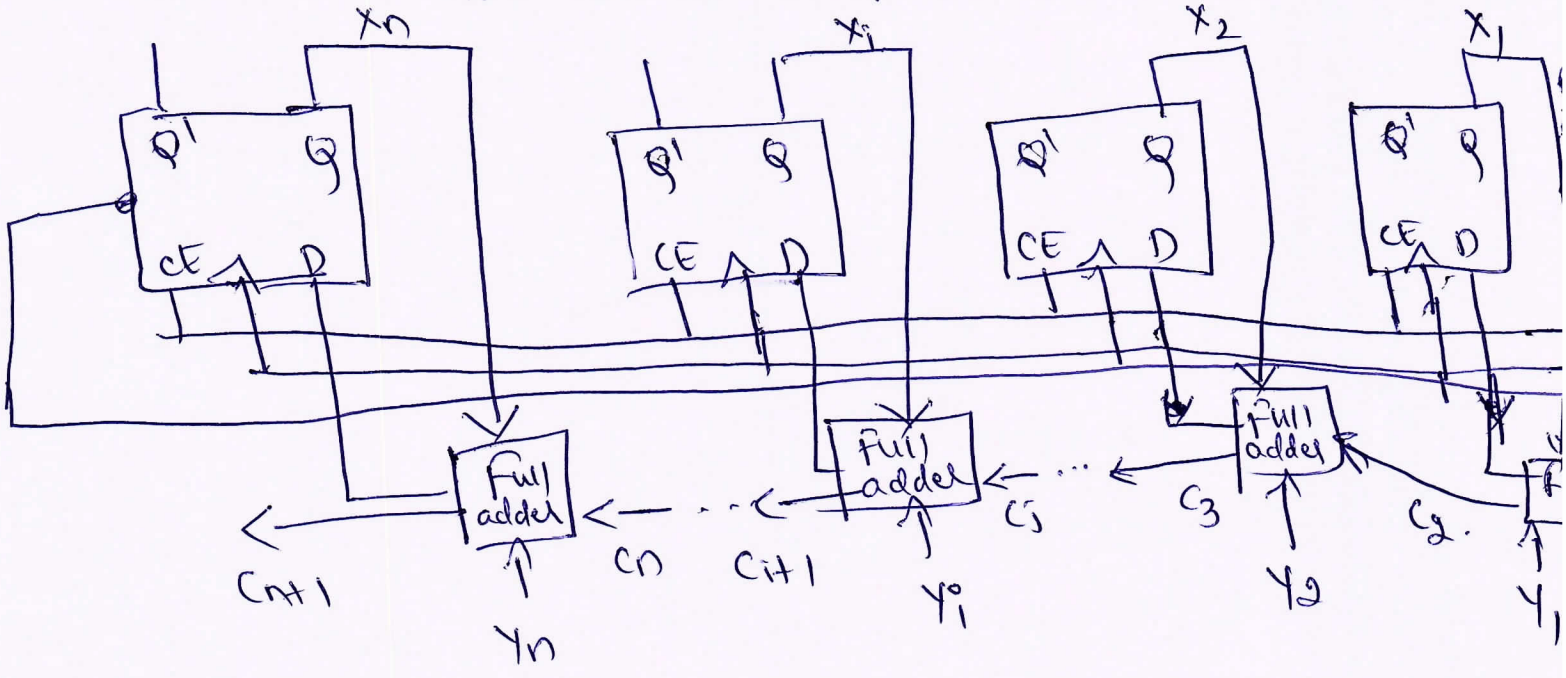
Module -05

9.a With neat diagram, explain 4 bit parallel adder with accumulator. 08 marks.

In computer circuits, it is frequently desirable to store one number in a register of flip-flops and add a second number to it, leaving the result stored in the accumulator.

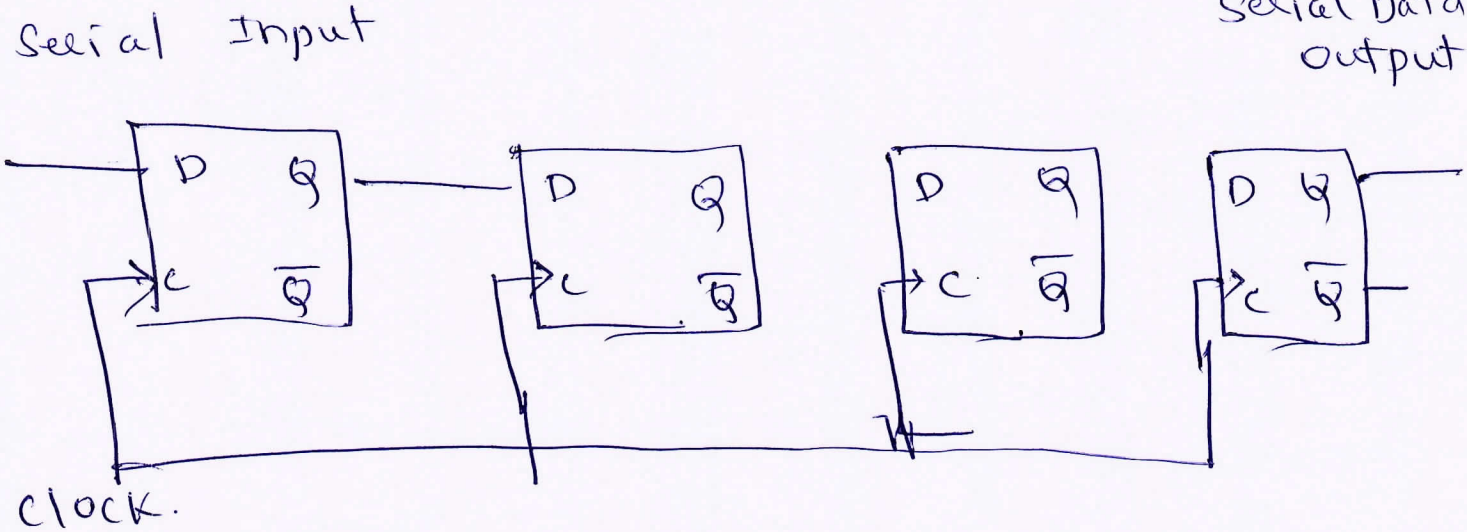
One way to build a parallel adder with an accumulator is as shown in fig. below.

Suppose that the number $X = X_n \ldots X_2 X_1$ is stored in the accumulator. Then the number $Y = Y_n \ldots Y_2 Y_1$ is applied to the full adder inputs and after the carry has propagated through the adders, the sum of X & Y appears at the adder outputs.



9b. With neat diagram explain 4 bit SISO register

SISO Register? 08marks



→ This register has four flip-flops (D) connected Serially where data is made input on one side and output appears on other side Serially.

→ The Q output of each flip-flop is connected to D input of next flip-flop.

→ The control input i.e., the clock input of each flip-flop is connected together to a common Synchronizing Signal called clock.

→ Thus, one of the +ve edge of the clock signal, the contents of each flip-flop is shifted one position to the right.

The output from the Shift register occurs at the right most flip-flop on the Serial data outline.

9c) Write a note on Johnson Tail counter? 04 marks

The Johnson Ring counter is another shift register with feedback exactly the same as a ring counter except here the inverted output $\bar{Q}$ of the last flip-flop is now connected back to the input D of the first flip-flop.

The main advantage of this type of ring counter is that it only needs half the number of flip-flops compared to the standard ring-counter then its number is halved. So a n-stage Johnson counter will circulate a single data bit giving sequence of 2n different states.

It can be considered as "mod-2n counter"

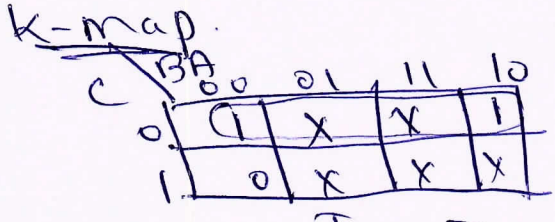
10a. Design Mod 5 counter using JK flipflops. 10 marks

State table.

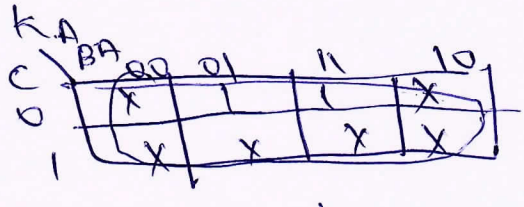
C	B	A	C+1	B+1	A+1	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

K-map.

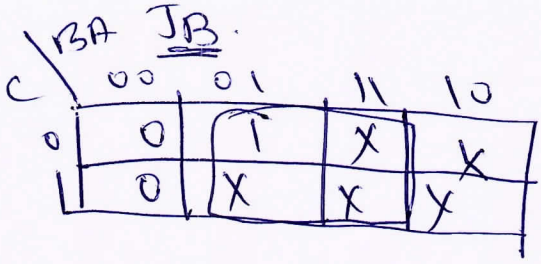
J_A



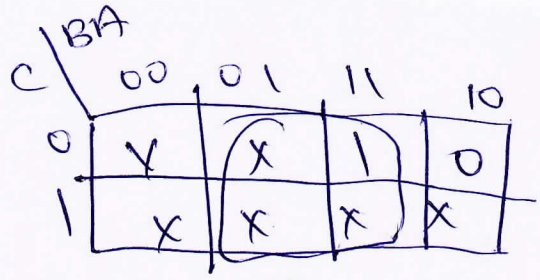
$J_A = \bar{C}$



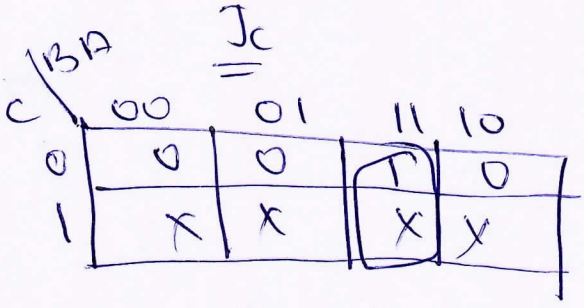
$K_A = 1$



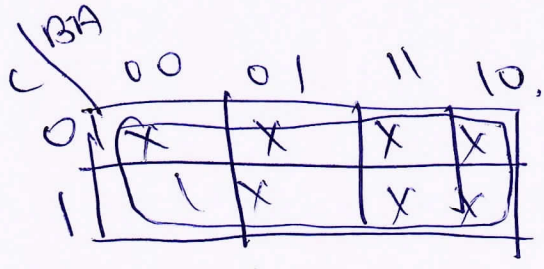
$J_B = A$



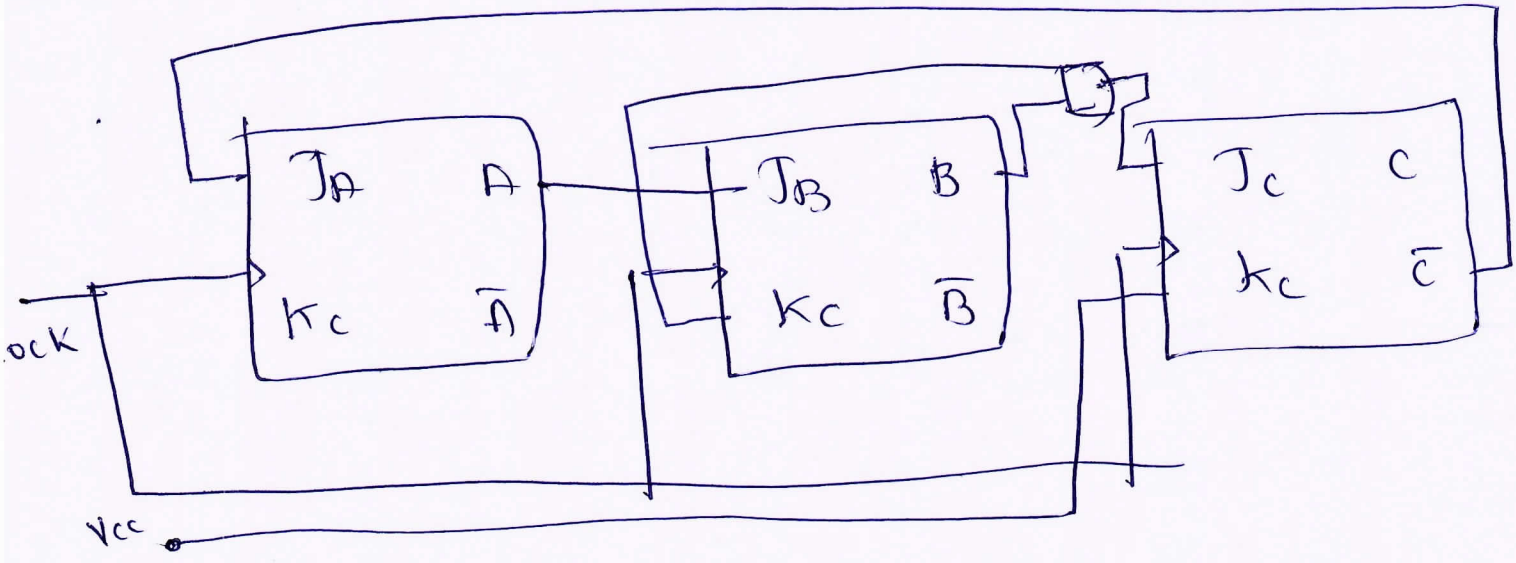
$K_B = A$.



$J_C = A \cdot B$

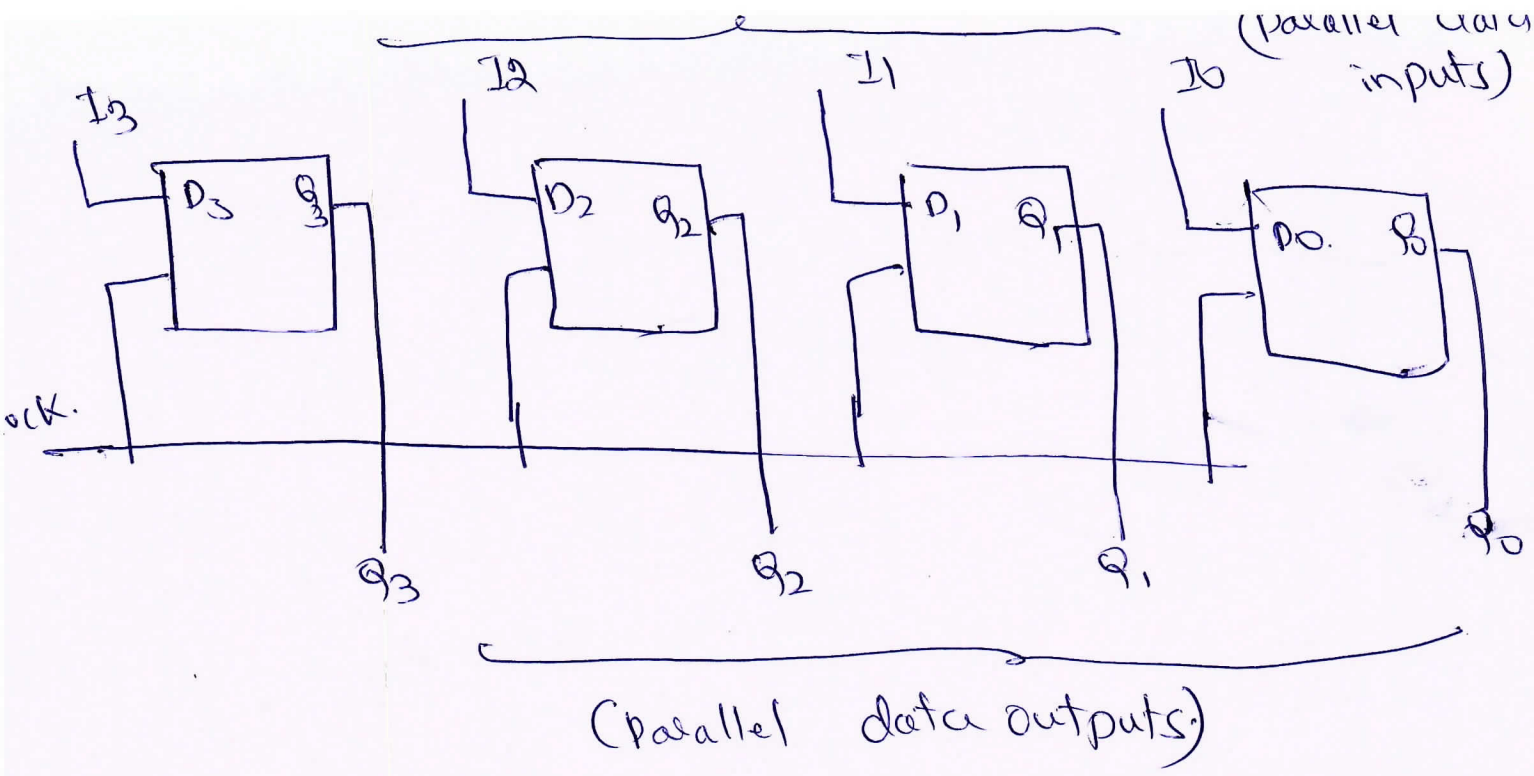


$K_C = 1$



b) Explain 4bit PIPO shift register with block diagram? 06marks

In parallel In parallel out there is simultaneous entry of all data bits and the bits appear on parallel outputs.

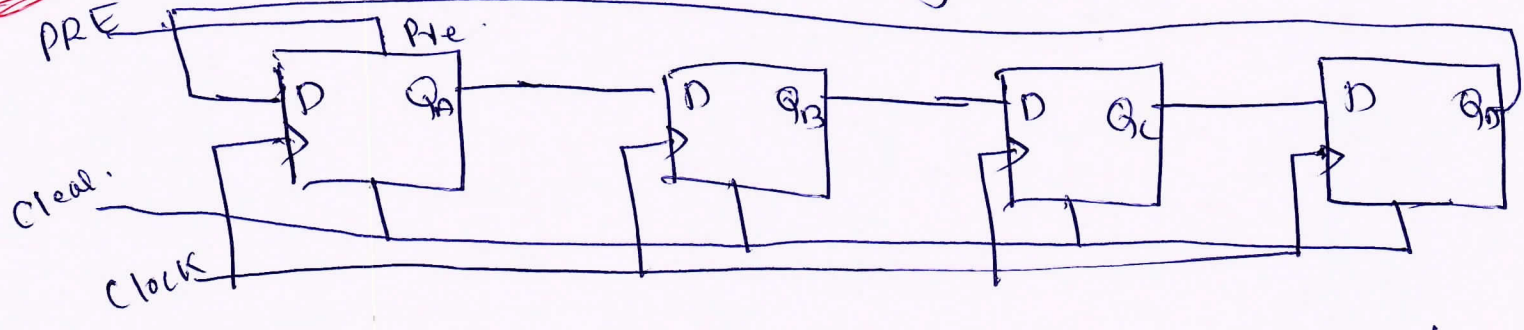


→ Inputs are applied simultaneously at I_3, I_2, I_1 & I_0

→ When inputs are loaded into flipflops it is reflected back in outputs Q_3, Q_2, Q_1, Q_0 at the same time.

→ Clock pulse is applied to each flip-flop to make it positive or negative or edge triggering.

10c) Write a note on Ring counter? 04 marks.



→ Here the Q of each flip-flop is connected to the D input of the next flip-flop & the output of the last flipflop is ~~feed~~fed back to the input of first flip-flop.

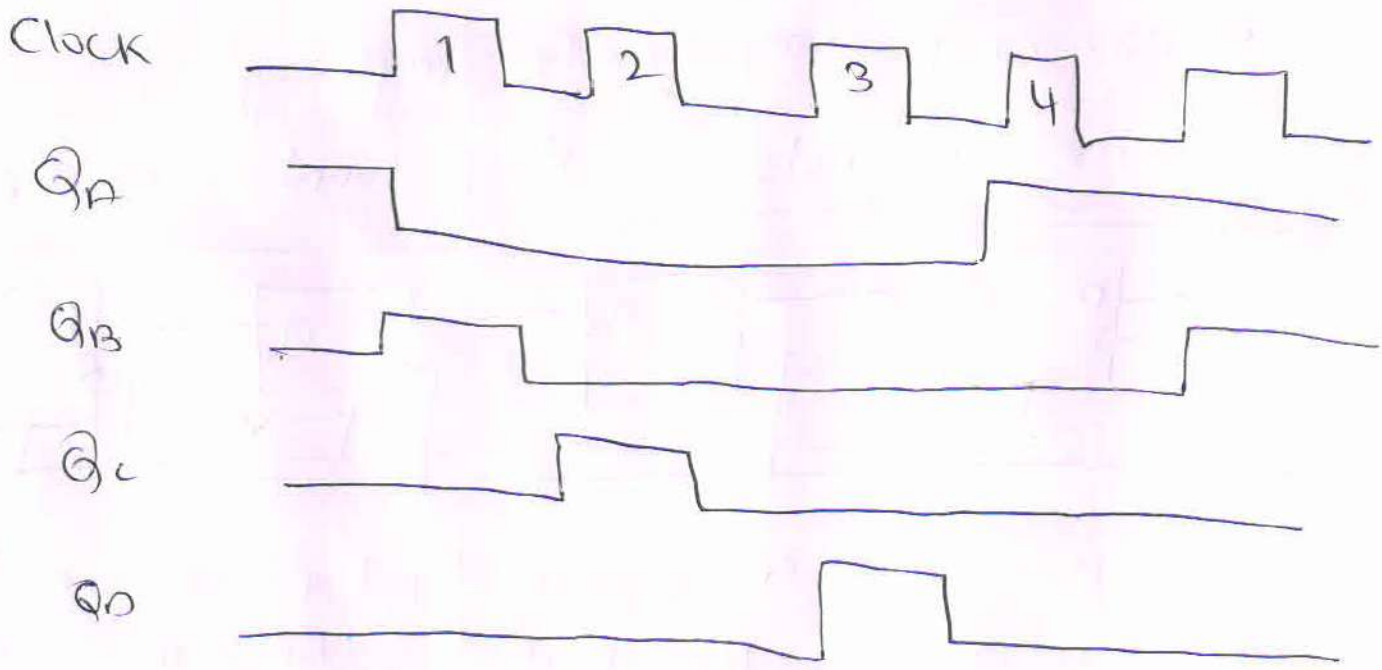
The clr & PRE pins make the output of first flip-flop to '1' and remaining o/p as zero.

i.e. Q_A is 1 and Q_B, Q_C & Q_D are '0'

Truth table

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3.	0	0	0	1

Waveforms



Sandeep. Pelkal. R.

P. Raikar