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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Solution & Scheme for the Model Question Paper Set-1 of 21ELN14/24 (Basic Electronics & Communication Engineering) is prepared by

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Model Question Paper - I with effect from 2021 (CBCS Scheme)

USN | | | | | | | | | | |

First/Second Semester B.E Degree Examination

Basic Electronics & Communication Engineering

TIME: 03 Hours Max. **Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**

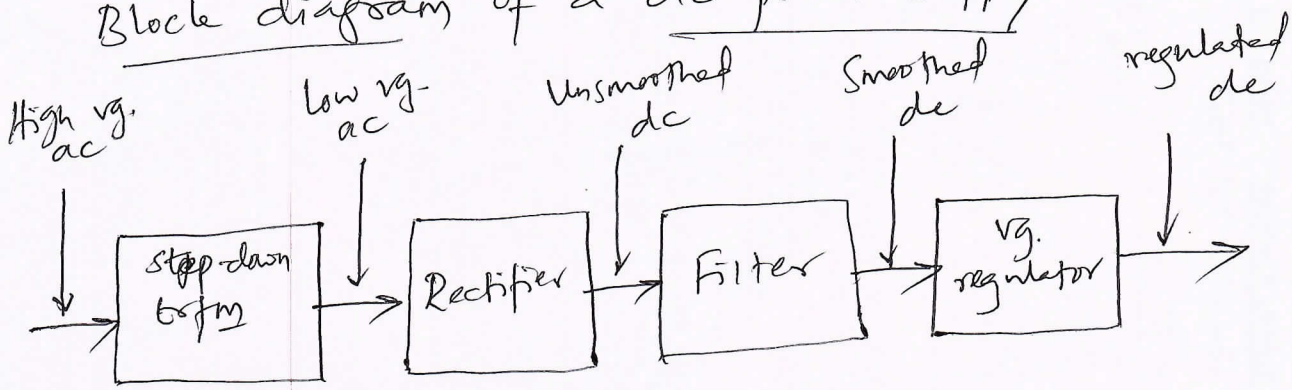
		Module-1 (Power Supplies, Amplifiers, Operational amplifiers, Oscillators)	**Marks**
Q.01	a	With neat block diagram explain the working of a DC power supply. Also mention the principal components used in each block.	7
	b	Mention advantages of negative feedback in amplifiers circuits. With relevant equations and diagram explain the concept of negative feedback.	7
	c	With circuit diagram and waveform show how operational amplifier can work as a comparator.	6
		OR	
Q.02	a	With neat circuit diagram and waveforms explain the working of bridge rectifier.	8
	b	Write a note on frequency response characteristics of an amplifier circuit, clearly mentioning the half power frequencies.	6
	c	List and explain conditions for sustained oscillations. Determine the frequency of oscillation of a three-stage ladder network in which C=10 ηF and R=10 kΩ.	6
		Module-2 (Logic Circuits, Data representation, Shift registers, Counters)	
Q. 03	a	Discuss the design of a 3-bit asynchronous up-counter.	6
	b	With a neat block diagram show how typical input and output blocks are connected to a microcontroller unit.	7
	c	With the help of a timing diagram explain how D-type bistable circuit works.	7
		OR	
Q.04	a	Design a full adder using two half adders and an OR-gate.	8
	b	Design a 4-stage shift register using J-K bistables.	7
	c	Write a note on different data types mentioning the bit size and range of values supported.	5
		Module-3 (Embedded Systems, Sensors and Interfacing, Actuators, Communication Interface)	
Q. 05	a	Explain the working, principle of operation and applications of stepper motor.	8
	b	Write a note on classification of embedded systems.	6
	c	Bring out the main features of UART and USB.	6

		OR	
Q. 06	a	Give the classification of transducers with examples.	6
	b	Bring out the differences between RISC and CISC, Harvard & Von-Neumann.	6
	c	Define 'Actuator' and briefly describe the following actuators - relay, Piezo-buzzer	8
		Module-4 (Analog and Digital Communication)	
Q. 07	a	Describe the blocks of the basic communication system.	6
	b	Define the following terms: (i) Modulation (ii) Carrier communication system (iii) Baseband communication system with neat and suitable waveforms.	6
	c	Explain the following with the help of waveforms. (i) PAM (ii)PWM (iii)PPM (iv) PCM	8
		OR	
Q. 08	a	Define sampling theorem and explain when aliasing can happen. Also mention the different ways in which aliasing can be avoided.	6
	b	Define the following terms: Multipath, Constructive and destructive interference, Coherence time, Coherence bandwidth, Delay spread	10
	c	Define an antenna and discuss different types of antennas.	4
		Module-5 (Cellular Wireless Networks, Wireless Network Topologies, Satellite Communication, Optical Fiber Communication, Microwave Communication)	
Q. 09	a	Draw the schematic diagram of a cellular telephone system and define its basic components.	6
	b	Explain the optical fiber communication system with a block diagram.	6
	c	With the help of diagrams, discuss the following types of network topologies: Ad-Hoc Network Topology, Infrastructure Network Topology	8
		OR	
Q. 10	a	With the help of architecture figures explain the evolution from GSM to LTE.	8
	b	List the requirements identified for the 4G technology.	4
	c	Draw the block diagram showing the basic elements of a satellite communication system and briefly explain them.	8

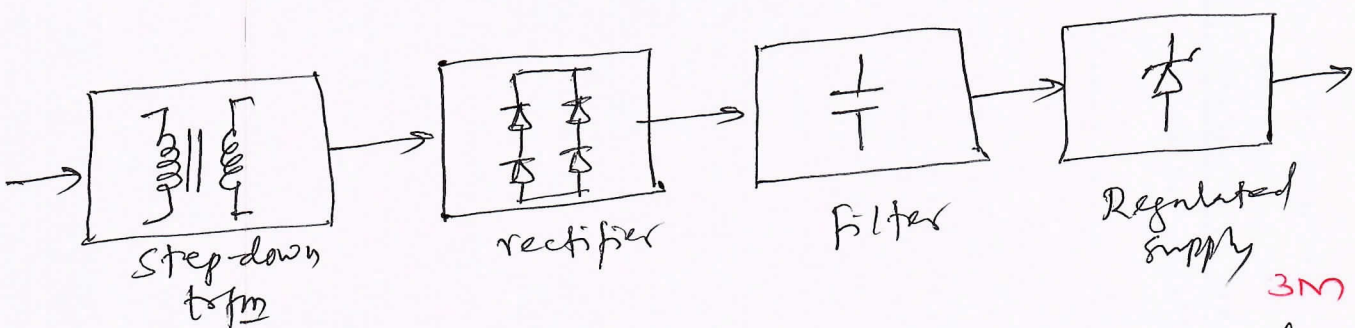
Module - 1

Q.1) a) With a neat block diagram explain the working of a dc power supply. Also mention the principal components used in each block.

Soln: Block diagram of a dc power supply -



Below figure shows the principal components used in each block :-



3M

The mains input is at a relatively high vg., a step down transformer of appropriate turns ratio is used to convert this to a low vg.

The iron cored step down transformer feeds a rectifier arrangement. The output of the rectifier is then applied to a capacitor filter. This capacitor stores a considerable amount of energy (charge) and is being constantly ~~top-up~~ topped-up by the rectifier arrangement. The capacitor also helps ~~out~~ to smooth out the vg. pulses produced by the rectifier. Finally, a stabilizing ~~ckt~~ circuit consisting of zener diode as a vg. regulator provides a constant output vg.

-4M

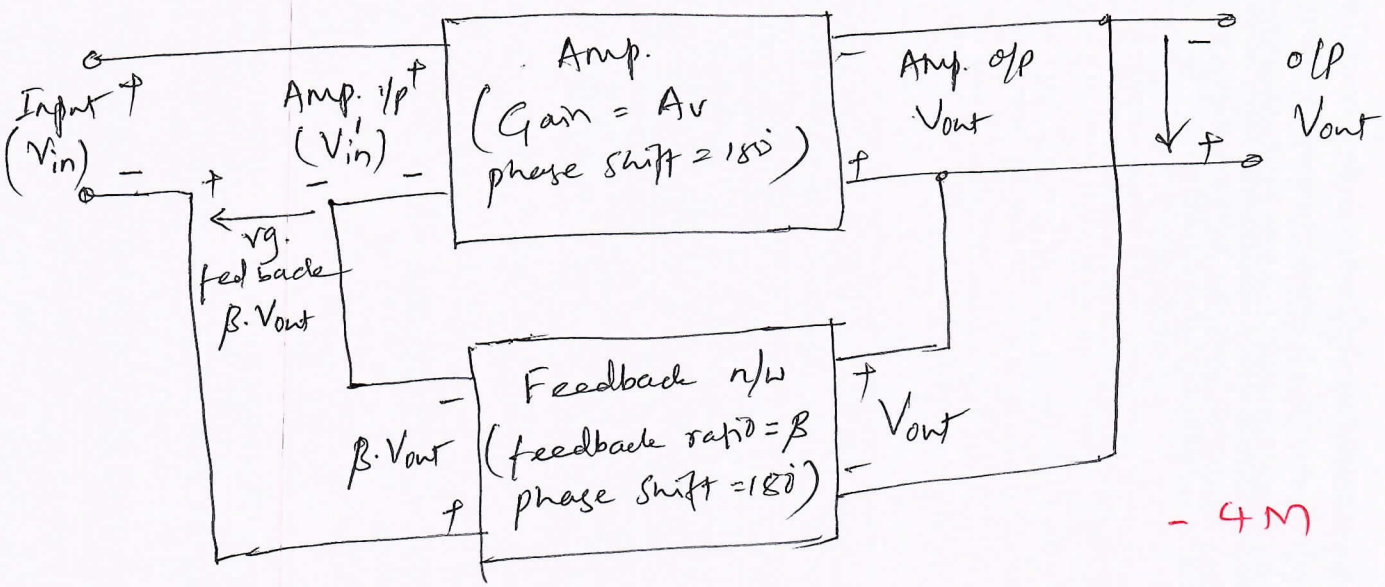
b) Mention advantages of negative feedback in amplifier circuits. With relevant equations and diagram explain the concept of negative feedback.

Sol:- Advantages of negative feedback are:

1) it stabilizes amplifier gain
2) it reduces non-linear distortion
3) it increases circuit stability
4) it increases input impedance
5) it decreases output impedance
6) it improves frequency response & bandwidth

- 3M

concept of negative feedback -



- 4M

Many practical amplifiers use negative feedback in order to precisely control the gain, reduce distortion and improve bandwidth.

Negative feedback has the effect of reducing the overall gain of the circuit.

In the figure shown above, the portion of the output vg. fed back to the input is given by β and the overall vg. gain will be given by

$$G = \frac{V_{out}}{V_{in}}$$

By applying KVL $\rightarrow$ $V_{in}' = V_{in} - \beta V_{out}$

$\therefore$ $V_{in} = V_{in}' + \beta V_{out}$

and $V_{out} = A_v \times V_{in}$, where A_v is the internal gain of the amplifier

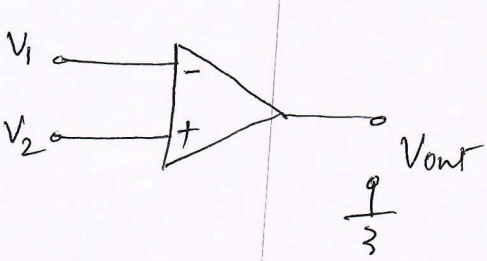
$\therefore$ Overall gain, $G = \dfrac{A_v \times V_{in}'}{V_{in}' + \beta V_{out}} = \dfrac{A_v \times V_{in}'}{V_{in}' + \beta (A + V_{in}')}$

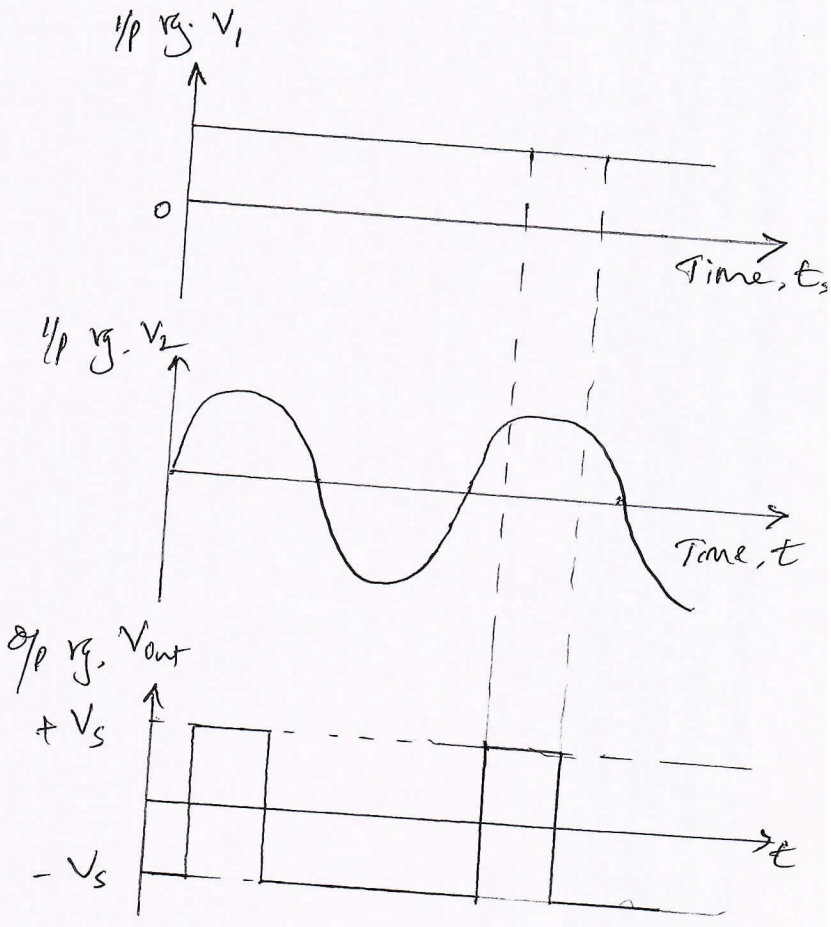
Thus, $G = \dfrac{A_v}{1 + \beta A_v}$

Hence, the overall gain with negative feedback applied will be less than the gain without feedback.

c) With circuit diagram and waveform show how operational amplifier can work as comparator.

Soln. Op-amp as a comparator.





3M

- Since no feedback has been applied, comparator circuit uses the max. gain of the op-amp.

The o/p vg. produced by the op-amp will thus rise to the max. possible value whenever the vg. present at the non-inverting input exceeds that present at the inverting input.

Conversely, the o/p vg. produced by the op-amp will fall to the minimum possible value whenever the vg. present at the inverting input exceeds that present at the non-inverting input.

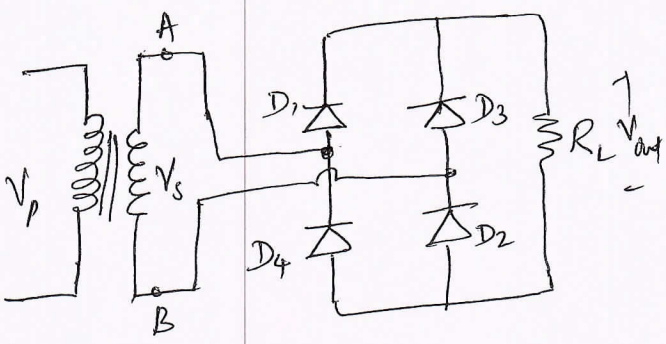
A typical application for a comparator is that of comparing a signal voltage with a reference vg. The o/p will go high (or low) in order to signal the result of the comparison.

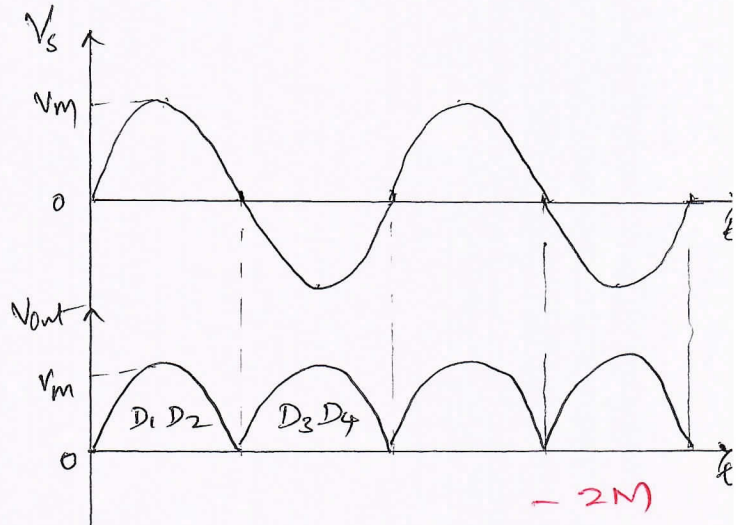
3M

Q.2) a) With a neat circuit diagram and waveforms explain the working of bridge rectifier

Soln:

Bridge rectifier





– 2M

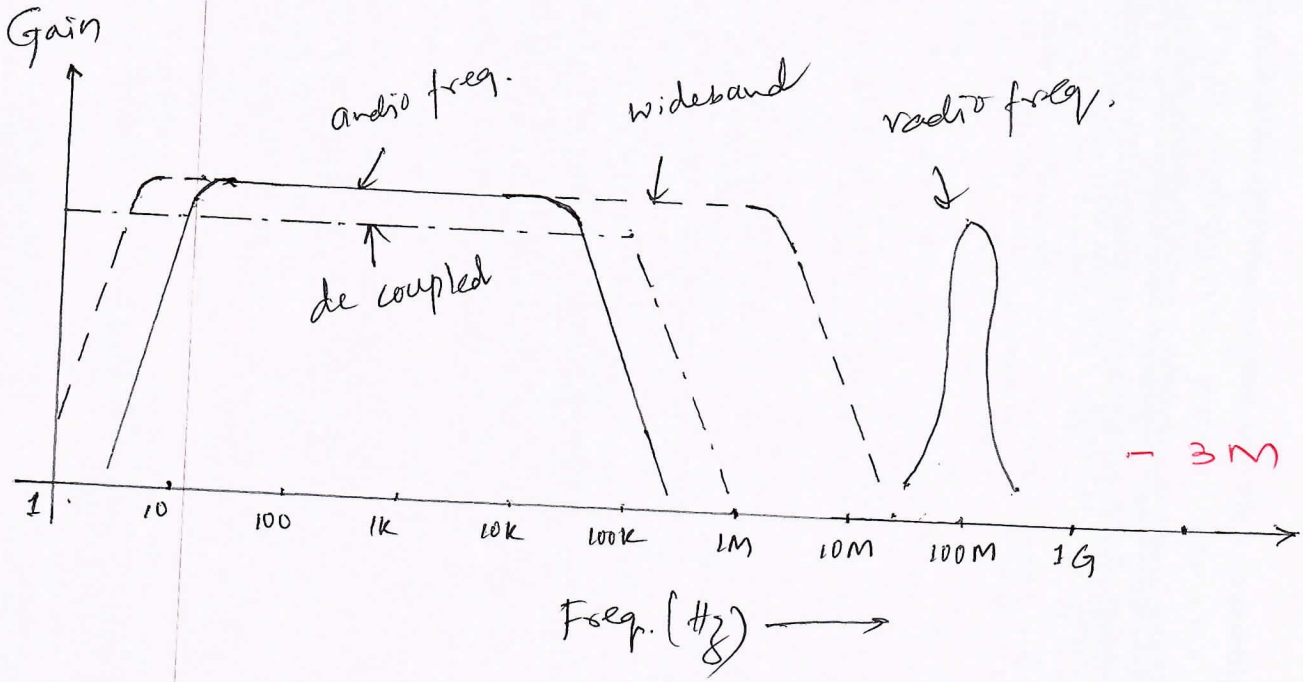
– 2M

– In a full-wave bridge rectifier opposite pairs of diodes conduct on alternate half-cycle ($D_1 D_2$ and $D_3 D_4$).
– on the secondary windings of the transformer, when point 'A' is positive w.r.t. point 'B' diodes D_1 & D_2 will conduct and load rg. will appear across R_L as V_{out} as shown in figure. – 2M

When point 'B' is positive w.r.t. point 'A', diodes D_3 & D_4 will conduct and load rg. will appear across R_L.
In both the half cycles current is routed thro' the load in the same direction. – 2M

b) Write a note on frequency response characteristics of an amplifier circuit, clearly mentioning the half power frequencies.

Soln: The freq. response characteristics for various types of amplifier are shown as below:



- 3M

The freq. response of an amplifier is usually specified in terms of the upper and lower cut-off frequencies of the amp. These frequencies are those at which the output power has dropped to 50% (otherwise known as the -3dB points) or where the voltage gain has dropped to 70.7% of its mid-band value.

- 3M

c) List and explain conditions for sustained oscillations. Determine the frequency of oscillation of a three-stage ladder n/w in which C = 10nF and R = 10 kΩ

Sol:- Conditions for sustained oscillations are :

1) The feedback must be positive ie, the signal fed back must arrive back in-phase with the signal at the input

2) The overall loop voltage gain must be greater than 1. ie, The amplifiers gain must be sufficient to overcome the losses associated with any frequency selective feedback n/w.

– 3M

Hence to create an oscillator, an amp. is required with sufficient gain to overcome the losses of the n/w that provide positive feedback. Assuming that the amp. provides 180° phase shift, the freq. of oscillation will be that at which there is 180° phase shift in the feedback n/w.

Given C = 10nF & R = 10kΩ

Frequency of oscillation is given by,

$$f = \frac{1}{2\pi \times \sqrt{6} RC}$$

$$= \frac{1}{2 \times \pi \times \sqrt{6} \times 10 \times 10^{3} \times 10 \times 10^{-9}}$$

$$= \frac{1}{6.28 \times 2.45 \times 10^{-4}}$$

– 3M

$$= \underline{649 \text{ Hz}}$$

Q.No | Module-2

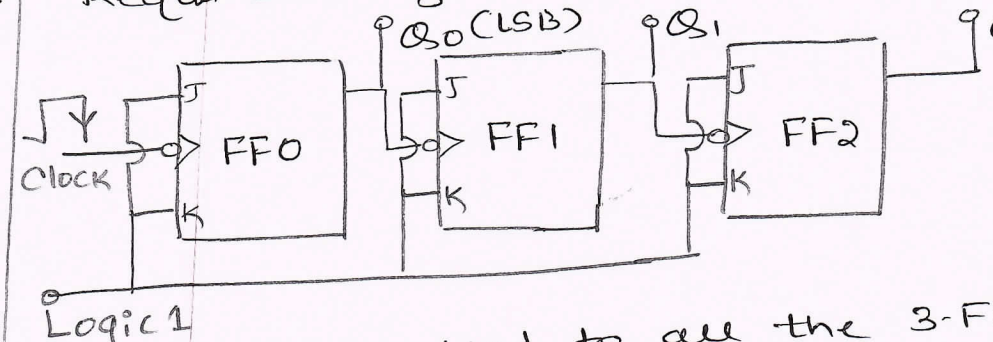
3a) Discuss the design of a 3-bit asynchronous up counter

→ Counter is a logic ckt, which counts the number of events either in ascending or descending order, In case of 3 bit up counter it can count from 0 to 7 i.e 000 to 111

→ For a 1 bit counter, we need one Flip-Flop, hence for 3 bit counter we need 3 Flip-Flops for the design

→ Preferably J-K Flip Flops are selected for counter operation.

→ Required logic ckt is shown below



– 3M

→ Logic 1 is applied to all the 3-FF for toggling at negative transition of the applied clock.

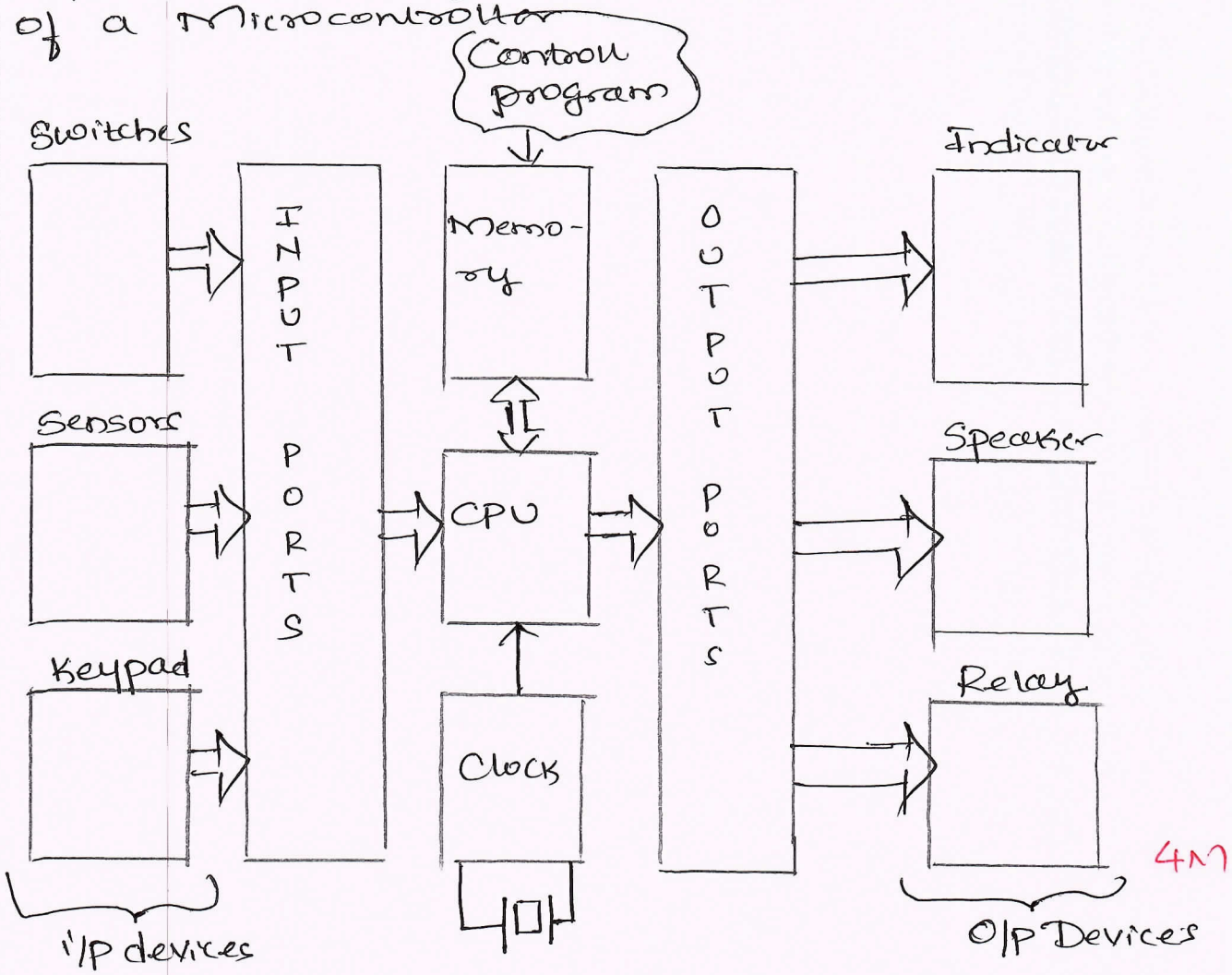
→ As it is an Asynchronous counter, the clock of the 2nd FF onwards is activated/controlled by the O/P of previous FF, Hence here FF1 and FF2 clocks are controlled and triggered by O/P of FF0 and FF1 (Q1) respectively.
(Q0)

→ Truth Table

Clock pulse No.	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

– 3M

3b) Typical Blocks diagram to show the i/p & o/p blocks of a Microcontroller



4M

* Microcontroller (MC) is a programmable device, consists of CPU, Memory units (RAM, ROM) and other peripheral embedded on a single chip.

* CPU: CPU is the main part of MC, having ALU and control unit within it. It is responsible for accepting, processing and controlling the necessary actions as per the user program or predefined program

* Control program: These are the sequence of software instructions, which will be monitoring the i/p and o/p devices continuously.

3M

* I/p and o/p devices: Any device or component can communicate to the MC, through the i/p ports which are then processed by CPU and results are obtained by o/p devices through o/p ports of microcontroller

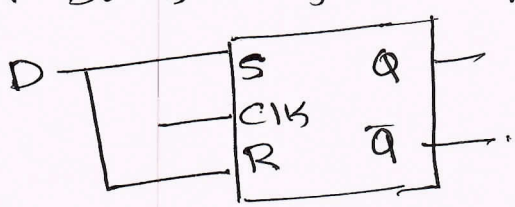
Q.no | Module-2

3c

D-Type Bistable

* The D-Type Bistable has two inputs, D (Data) and clock (CLK). The Data i/p which can be 0 or 1 is clocked in to Bistable such that o/p state only changes when clock changes the state.

* Block Diagram of D Type Bistable.



Truth Table

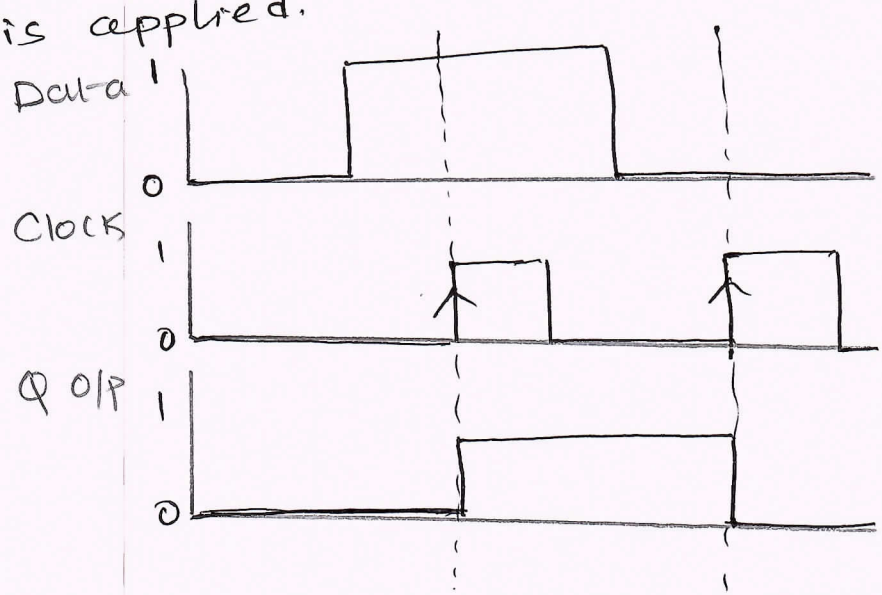
Clock	D	Q	$\bar{Q}$	comments
↓ 0	X	Q	$\bar{Q}$	No-change
↑ 1	0	0	1	Reset
↑ 1	1	1	0	Set

– 3M

* Timing Diagram Analysis.

Whenever the CLK signal is LOW, the i/p is never going to affect the o/p state. Any Logic State of the input (D) will appear at o/p Q only if the rising edge of the clock is applied.

– 3M



– 1M

Q.No Module-2

4a) Design a Full adder using two half adders and OR gate

Consider the Truth table of Full-Adder

input			output	
Cin	B	A	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

– 2M

$SUM = A\bar{B}\bar{C}in + \bar{A}B\bar{C}in + \bar{A}\bar{B}Cin + ABC$ } 2M

$SUM = A \oplus B \oplus Cin$ – (1)

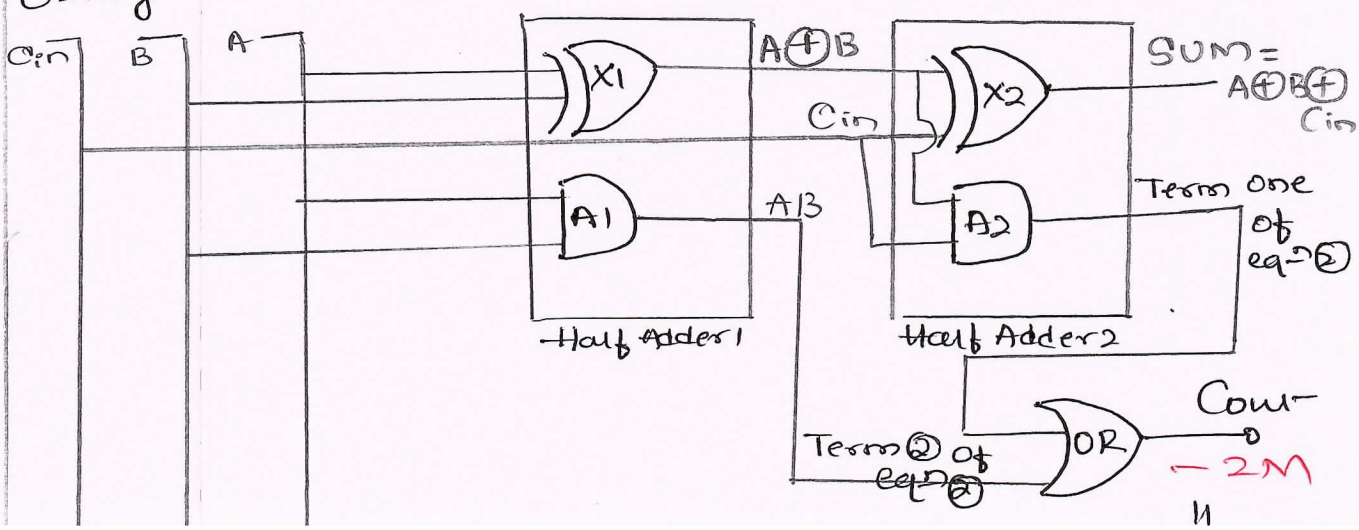
$Cout = A\bar{B}\bar{C}in + \bar{A}\bar{B}Cin + \bar{A}BCin + AB\bar{C}$

$= \bar{C}in[A\bar{B} + \bar{A}B] + AB[\bar{C}in + Cin]$

$= Cin[A \oplus B] + AB[1]$

$Cout = Cin[A \oplus B] + AB$ – (2) } 2M

From eqn (1) and (2) we can implement Full Adder using two Half adders and OR gate

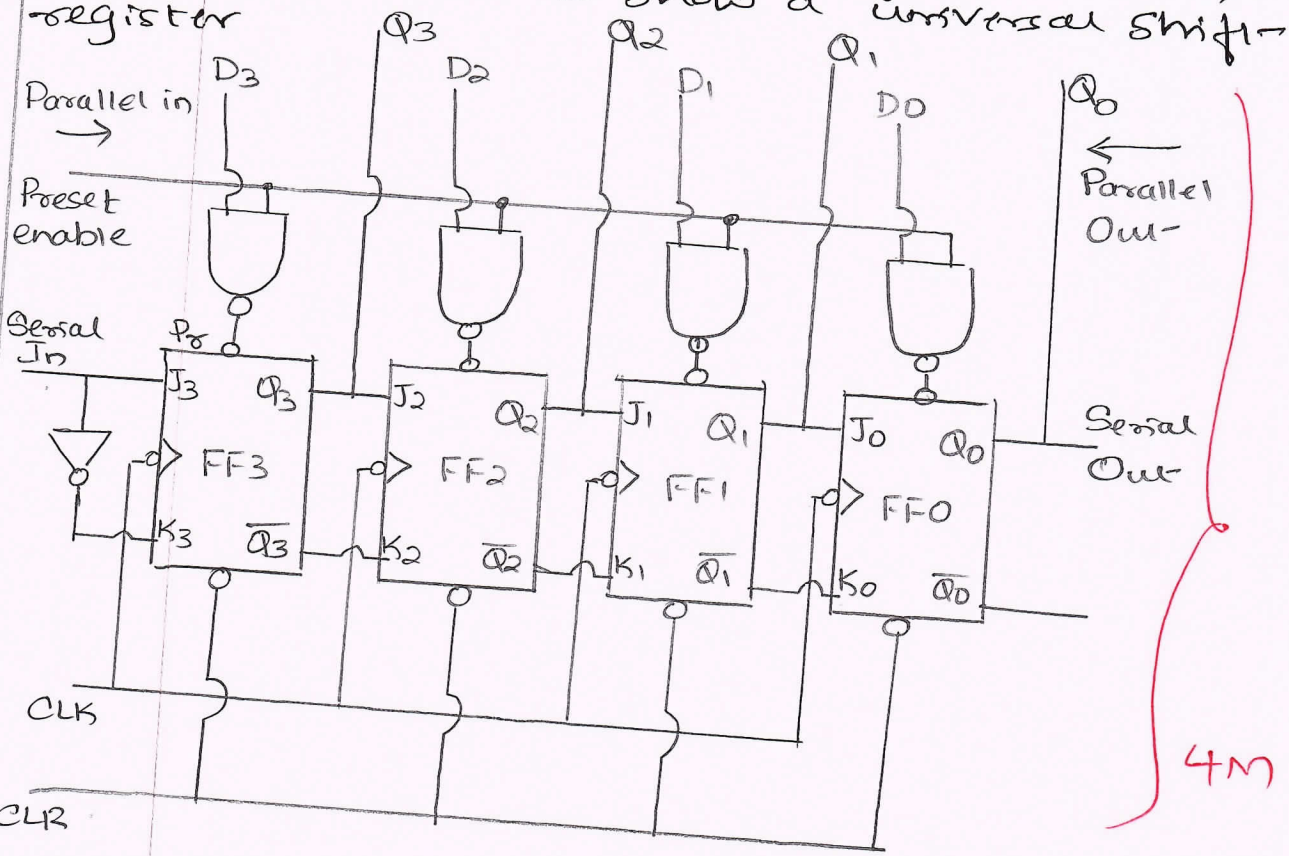


Q.No

Module-2

4b Design a 4-stage Shift Register using JK-Flip

As it is not mentioned to Design SIPO, PISO, SIS or PIPO, we need to show a universal shift-register



→ SIPO Shift Register: Upon each clock pulse, i/p data is entered serially (at first LSB entered in FF3) directly o/p is collected from Q_3-Q_0 of flipflop FF3-FF0,

→ PISO and PIPO: All FF are cleared, by making CLR=0. During normal operation, CLR=1. Also make preset- Pr=0. All FF are triggered by common clock pulse (CK). Parallel in line is enabled as i/p.

3M

→ effect of D_i

case(i): If $D_i=0$, Pr=1 and $Q_i=0$

case(ii): If $D_i=1$, Pr=0 and $Q_i=1$.

→ For PIPO operation: Data is entered through Preset enable (Pr=1). In this case o/p is independent of clock.

Ex: Data = 0110, applied through preset i/p.

Since clock is not involved, Q_3, Q_2, Q_1, Q_0 = 0110

Q.No | Module-2

4C **Data Types:** Data can be from one bit- length to n bit- length, It indicates the capacity of a processor/ controller can handle.

Typical Data Types are

→ Bit: It represents a binary bit- 1 or 0 2M

→ Byte: It represents the group of 8 binary bits
example: 10101010

→ Double Byte / word: Represents 16 bit- data

→ Different- Data types are listed in the below

Table

Decimal number	Hexadecimal number	Binary number (2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 = 128 64 32 16 8 4 2 1)
0	0	0 0 0 0
1	1	0 0 0 1
2	2	0 0 1 0
3	3	0 0 1 1
4	4	0 1 0 0
5	5	0 1 0 1
6	6	0 1 1 0
7	7	0 1 1 1
8	8	1 0 0 0
9	9	1 0 0 1
10	A	1 0 1 0
11	B	1 0 1 1
12	C	1 1 0 0
13	D	1 1 0 1
14	E	1 1 1 0
15	F	1 1 1 0
16	10	1 0000

2M

→ Table-2

Data Types	Bits	Range of values	Binary range 1M
Unsigned Byte	8	0 to 255 = (2^8)	0000 0000 - 1111 1111
Signed Byte	8	-128 to +127	10000000 - 01111111
Unsigned word	16	0 to 65,535 (2^{16})	0000 0000 0000 0000 to 1111 1111 1111 1111
Signed word	16	-32,768 to 32,767	1000 0000 0000 0000 to 0111 1111 1111 1111

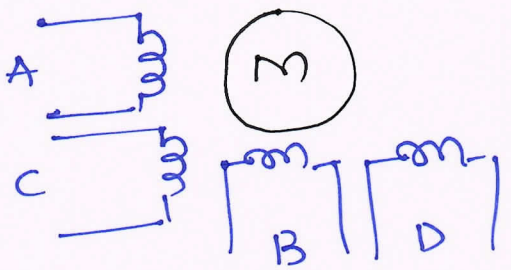
Q.No	Module-3

5a) Working, principle of operation and application of Stepper motor.

→ A stepper motor is an electro-mechanical device which generates discrete displacement (motion) in response to dc electrical signals

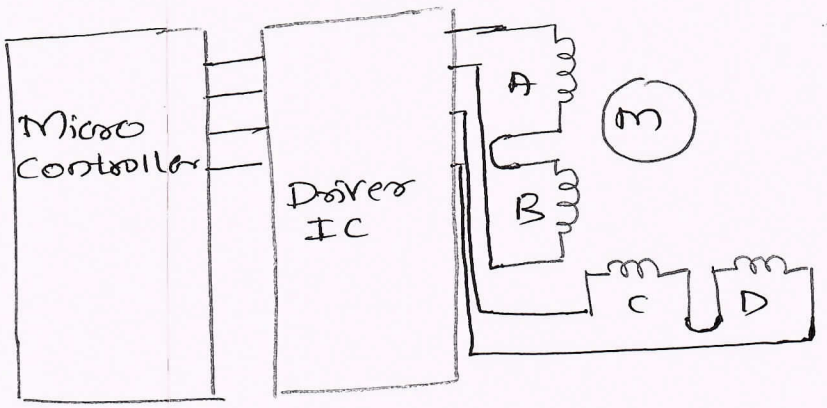
→ Based on the type of coil winding, a two phase stepper motor is classified as
a) Unipolar b) Bipolar — 2M

→ a) Unipolar: It contains two windings per phase. The direction of rotation of the motor is controlled by changing the direction of current flow. The coils are named as A, B, C and D. Coil A & C carry current in opposite direction for phase1, where as coil B & D carry current in opposite phase. It is shown below



— 3M

→ The rotation of Stepper motor can be controlled by Interfacing it with the microcontroller through a driver IC called ULN2803, which can boost the signal level from 5V to 24V. Each coil can be programmed by using 4 pins of a port of a microcontroller by method called wave step shown below



Wave Step Sequence

Step	Coil A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

— 3M

Q.No	Module-3

5b] Classification of Embedded System

Embedded Systems are classified as

i) Based on Generation.
ii) Based on Complexity and Performance
iii) Based on Deterministic behaviour
iv) Based on Triggering.

[i] Based on Generation: — 2M

* First Generation: These were designed based on 8bit µp and 4bit µc, Ex: Digital Telephone Keypad.
* Second Generation: These were designed based on 16bit µp and 8bit µc, Ex: SCADA
* Third Generation: These are based on 32 bit µp and 16 bit µc, Ex: Robotics
* Fourth Generation: These are based on 64 bit µp and µc, ex: Digital camera

[ii] Based on Complexity and Performance — 2M

* Small Scale: These are built with a single 8or 16 bit µp/µc, The main programming tool used are an editor, ex: An electronic toy
* Medium Scale: These are built with a single 16 bit or 32 bit µp/µc, The main programming tools used are C, C++, Java, etc. Ex: Smart watch
* Large Scale: These are built on single 32 bit or 64 bits µp/µc. used in larger appliance like washing machine

[iii] Based on Deterministics behaviour: It is applicable for 'Real Time' Systems. The behaviour can be either deterministic or non-deterministic. — 1M

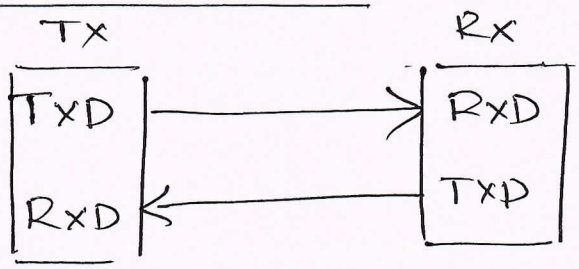
[iv] Based on Triggering: These embedded systems are based on a particular event for which an appropriate action is initiated.
Ex: In a smoke sensor alarm system, Alarm is activated immediately after smoke is sensed. — 1M

Q.No | Module-3

5c) Main Features of UART and USB.

UART Features are

3M



1. It needs only two wires b/w Transmitter and Receiver for data transfer
2. No clock signal is required during the communication
3. Typical baudrate required are 9600 b/sec
4. Parity bit can be used for better communication

USB Features

3M

1. It uses less power and does not have any fragile moving parts
2. Data Storage on these devices are impervious to mechanical shock, magnetic field and dust
3. It supports Data speed from 1.5 Mbps to 40 Gbps.

6a) Classification of Transducers with example.

* Transducers are the devices which can convert a physical form of value like (sound, light etc) to an equivalent electrical form. Such operation is normally seen at i/p side of embedded system and are called "Sensors", and the reverse operation is called "Actuator".

* These are classified as

3M

a) Input (Sensor) transducers

b) Output (Actuator) transducers

Q.No | Module - 3

6a) Continued

Example	Type of Transducer	Function
① Microphone	Input	Converts audio to electrical signal
② Thermocouple	Input	Converts temperature to equivalent voltage
③ Loud speaker	Output	Converts electrical signal to sound/audio signal

3M

6b) Difference between RISC & CISC, Harvard & Von-neuman

	RISC	CISC
①	Supports Less number of Instructions	Supports More number of Instructions
②	Supports Instruction pipelining	Does not support Instruction Pipelining
③	Instructions are orthogonally designed	Does not support orthogonal Instructions.
④	Large number of Instructions are related to registers	Limited number of registers
⑤	Instructions are of Single and fixed length	Variable length.

3M

	Harvard Architecture	Von-Neuman Architecture
①	Uses seperate bus for Instruction and Data fetching	Single shared bus for Instruction and data fetching
②	Corruption of program memory are very less	More chances of corruption of Program memory
③	High Cost	Low cost

3M

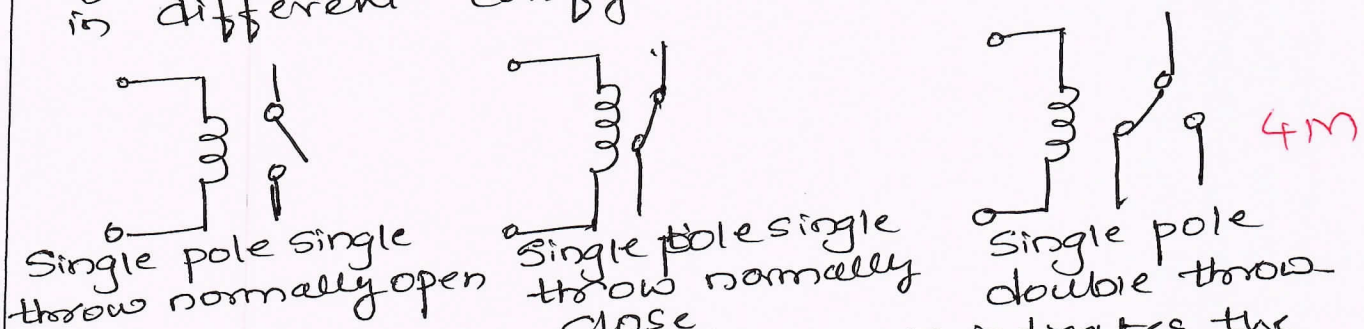
Q.No | Module-3

6C) Actuator is a transducer. which converts electrical signal to corresponding physical parameter like sound, switching etc. — 1M

Relay:

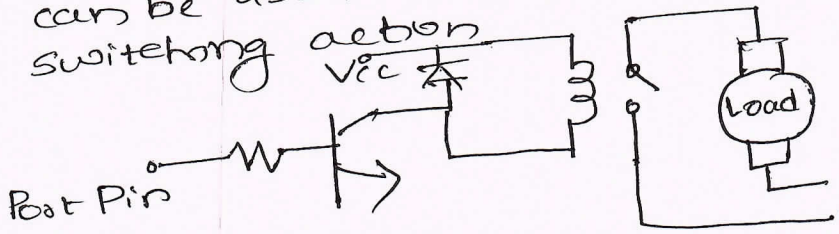
It is a electromechanical switch, It contains relay coil made up of insulated wire on a metal core and a metal armature with one or more contacts

When voltage is applied to the relay coil current flows through the coil, which intern generates a magnetic field. Relay are available in different configurations.



4M

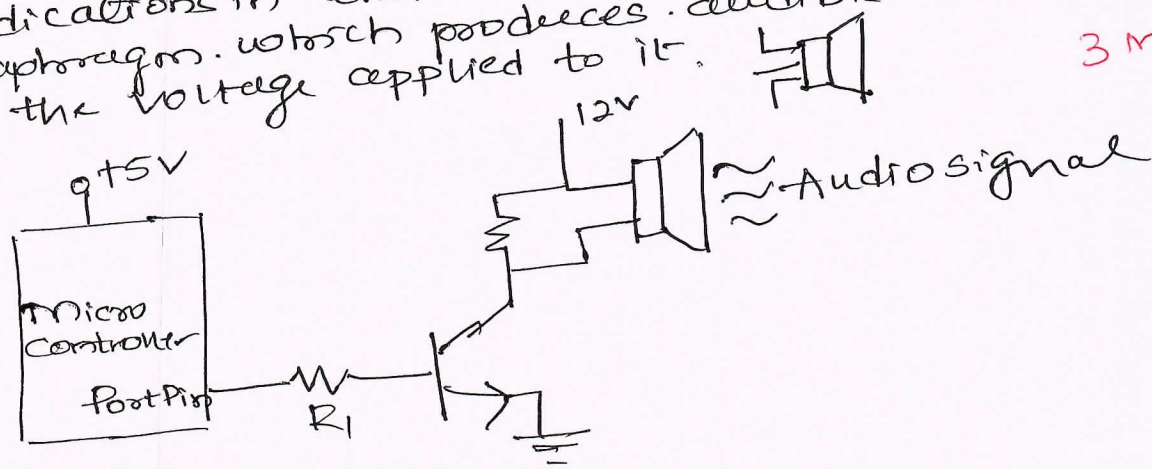
In the above configurations, pole indicates the switch and it can be closed/open, this action can be used in an embedded application involving switching action



Piezo Buzzer

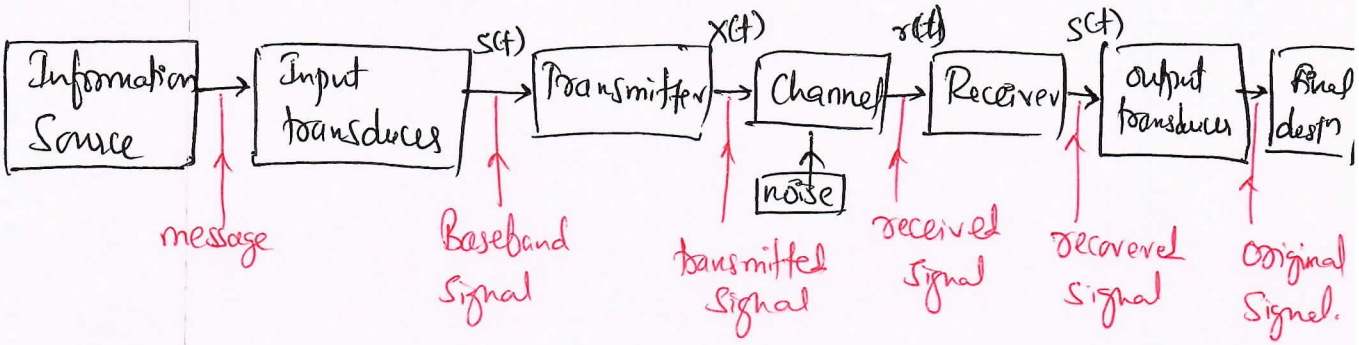
It is a Piezo electric device for generating audio indications in embedded applications. It contains a Diaphragm. which produces audible sound in response to the voltage applied to it.

3M



Q. 7. a Describe the blocks of the basic communication system - 6M

Solution Figure 7.a shows the block diagram of a basic comm system.



2M

The main constituents of basic communication system are

Information Source - A communication system transmits ~~infor~~ information from information source to a destination

- Information is transmitted in the form of electrical signals.

Input transducer - If the information produced by the information source is not in the electrical form then we make use of a transducer which converts non-electrical energy to electrical energy.

2M

The transducer produces the electrical signal known as base band signal. s(t)

Transmitter - Transmitter consists of a modulator, voltage amplifier stage & power amplifier stage. The modulator translates the baseband signal from low frequency to high frequency. The amplifiers amplify their levels & is then transmitted.

Channel – The transmission medium between transmitter & receiver is known as channel.

Depending on physical implementation there are hardware channels & software channels — 1M

hardware channels are – transmission lines
- twisted pair cables
- coaxial cables

– waveguides
– optical cables

Software channels are open space, sea water, air.

Noise – Random & unpredictable energy present in system — 1M

Receiver – Receiver seperates the noise from the received signal & then recovers the original baseband signal.

6.b Bring out the differences between RISC & CISC, Harvard & Von-Neumann — 6M

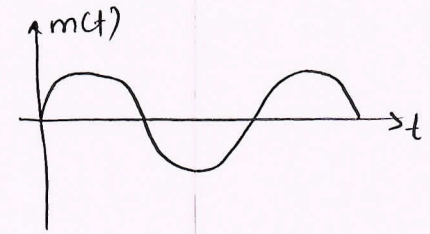
Repeated the question

RISC	CISC
① Instruction pipelining & increased execution speed	① No instruction pipelining
② Orthogonal instruction set	② Non-orthogonal
③ Operations are performed on registers only	③ Operations are performed on both memory & reg
④ With Harvard architecture	④ Either harvard or von neumann

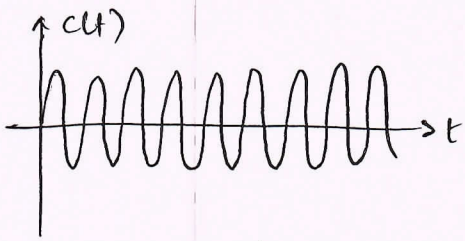
Harvard	Von-Neumann
① Seperate bus for instruction & data	① Shared bus
② No memory alignment problems	② allows self modifying codes
③ High cost	③ low cost
④ Data & memory are stored in diffent location	④ Data/memory stored in same location

7.b Define the following terms (i) modulation (ii) Carrier Communication system (iii) Baseband Communication system with neat & suitable waveform 6M

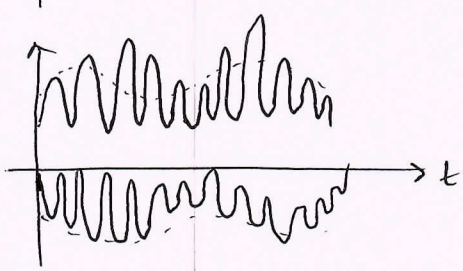
(i) Modulation - Modulation is a process of changing the characteristics (amplitude, frequency and phase) of a carrier wave with respect to message signal. 1M



message signal

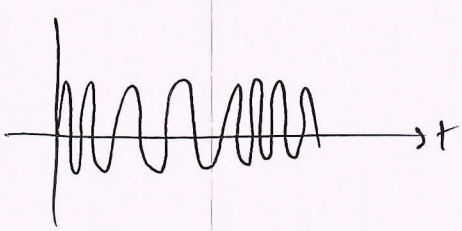


Carrier signal

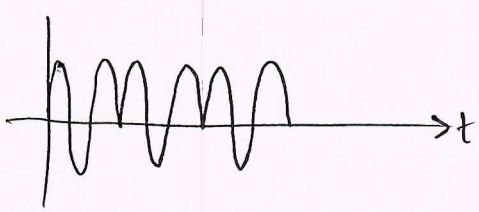


amplitude modulation

3M



Frequency modulation



Phase modulation

(ii) Carrier communication system

Carrier Communication system involves transmission of information by modulating the carrier signal.

2M

(iii) Baseband Communication System

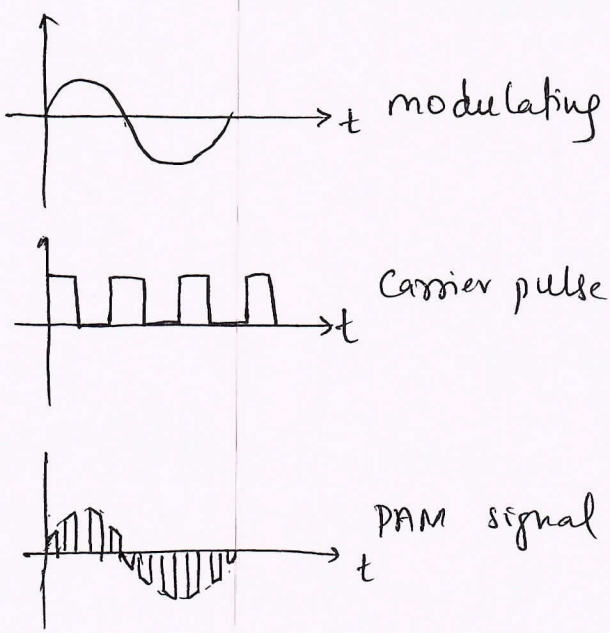
It involves transmission of information without modulation

7.c Explain the following with the help of waveforms
(i) PAM (ii) PWM (iii) PPM (iv) PCM 8M

(i) PAM - Pulse Amplitude Modulation

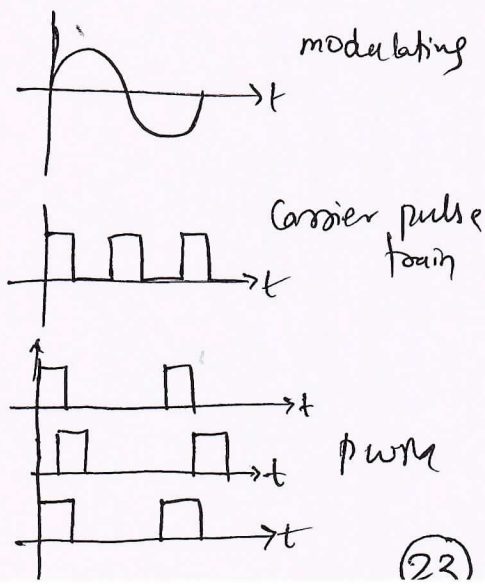
- PAM is ~~defined~~ an analog modulation scheme in which the amplitude of the pulse carrier varies proportional to the instantaneous amplitude of modulating signal.
- Here the signal is sampled at regular intervals & each sample is made proportional to amplitude of the signal. ~~at the~~

2M



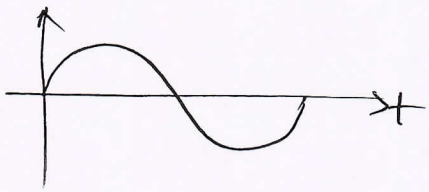
(ii) Pulse width modulation (PWM) 2M

Also known as pulse duration modulation or pulse time modulation.
It is an analog modulation scheme in which width or duration or time of the pulse train is varied w.r.t instantaneous amplitude of baseband signal

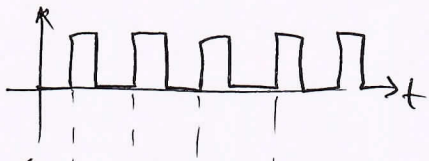


(iii) PPM - Pulse position modulation

- Here amplitude & width of the pulses are kept constant while the position of each pulse w.r.t reference pulse is varied
- Here the transmitters o/p power is constant

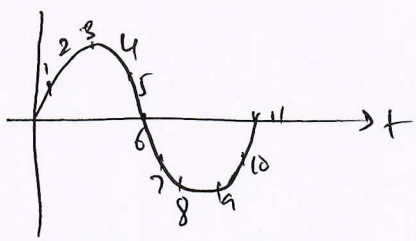


2M

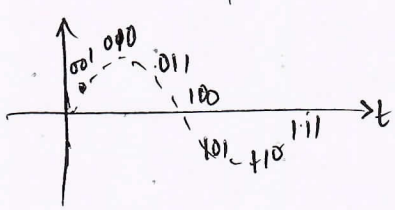


(iv) PCM - Pulse code modulation

It is a digital modulation in which the message signal is sampled & rounded off to the nearest value of the finite set of allowable values & the rounded values are coded.



2M



8.a Define Sampling theorem & explain when aliasing can happen. Also mention the different ways in which aliasing can be avoided 6M

Sol^n Sampling theorem :- A continuous time signal may be completely represented in its samples & recovered back, if the sampling frequency is twice the max frequency of the signal $f_s \gg 2f_m$ 1M

- When sampling rate becomes exactly equal to $2f_m$ S/s then it is called ~~neq~~ nyquist rate.
- A low pass filter is used to recover the original signal samples.
- The process of reconstructing the continuous time signal samples is known as interpolation. 3M
- When the sampling frequency is less than the nyquist rate, then aliasing problem is said to occur
- Aliasing is the phenomenon in which high frequency component in the frequency spectrum takes the identity of a lower frequency component.

To avoid aliasing

(1) Nyquist rate must be met properly i.e $f_s \gg 2f_m$

(2) Pre alias filter must be used to limit the band of frequencies of the signal to f_m Hz // 2M

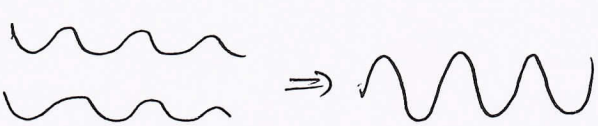
8.b Define the following terms: Multipath, Constructive & destructive interference, coherence time, coherence b/w. delay spread 10M

Sol^n **Multipath** - Propagation loss & noise are not the only problem in the communication system. As a result of reflections, rays can take several different paths from transmitter to the receiver. This phenomenon is known as multipath. 2M

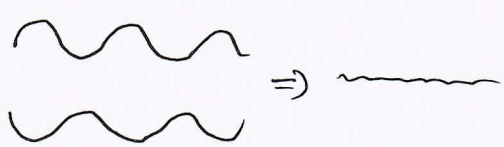
Constructive & Destructive interference:-

At the receiver side, if the incoming rays add together in different ways as shown in figure below, then the rays add & the peaks of the incoming rays coincide ~~so they~~ then ~~they~~ it is known as constructive interference.

However if the peaks of one ray coincide with the troughs of another, then the result is destructive interference. in which the rays cancel each other. 2M



Constructive interference



Destructive interference

Coherence time:- Due to destructive interference, the power of the received signal drops to a greater level. 2M

Also, if the mobile moves from one place to another, then the ray geometry changes, so does the interference pattern. Changes ~~form~~ between constructive & destructive.

In this scenario, the amplitude & phase of the received signal vary over a timescale known as coherence time (T_c)

$$T_c = \frac{1}{f_D} \quad \text{where } f_D = \frac{v}{c} f_c$$

f_D - doppler frequency
f_c - carrier "

(OR)

8.b continued ...

Coherence bandwidth :- 2M

If the ~~for~~ carrier frequency changes, then the wavelength & the radio ~~wa~~ signal changes. This also makes the interference pattern change ~~from~~ between constructive & destructive. In this scenario the amplitude & phase & the received signal vary over a frequency scale called coherence Bandwidth (B_c).

$$B_c = \frac{1}{\tau}$$ τ – delay spread & channel

Delay spread :- Represented by τ is the difference between the arrival times & the earliest & latest rays.

$$\tau = \frac{\Delta L}{c}$$ ΔL – difference between path lengths & longest & shortest rays. 2M

c – speed & light.

8.c Define an antenna & discuss different types & antennas.

Soln An antenna is a device for converting 4M electromagnetic radiation in space into electrical currents in conductors or vice-versa.

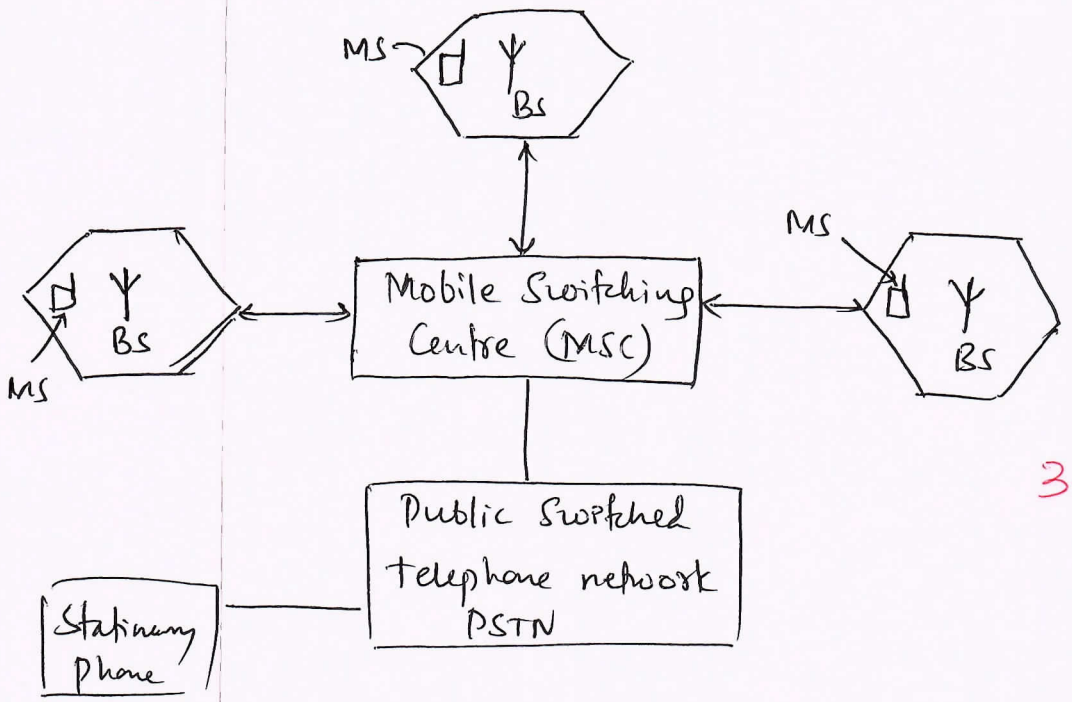
Types & antennas

1) Omnidirectional antennas
2) Dipole antennas
3) Collinear Omni antennas
4) Directional antennas
5) ~~Path~~ Patch antenna
6) ~~Path array~~ Patch array antennas
7) Yagi antennas

MODULE - 05

Cellular, Wireless networks, Wireless n/w topologies, Satellite Communication, Optical fibre Comm, microwave Communication

9.a Draw the schematic diagram of a cellular telephone system & define its basic components. 6M



3M

Mobile station (MS) :- It is a mobile handset used by the user to communicate with another user

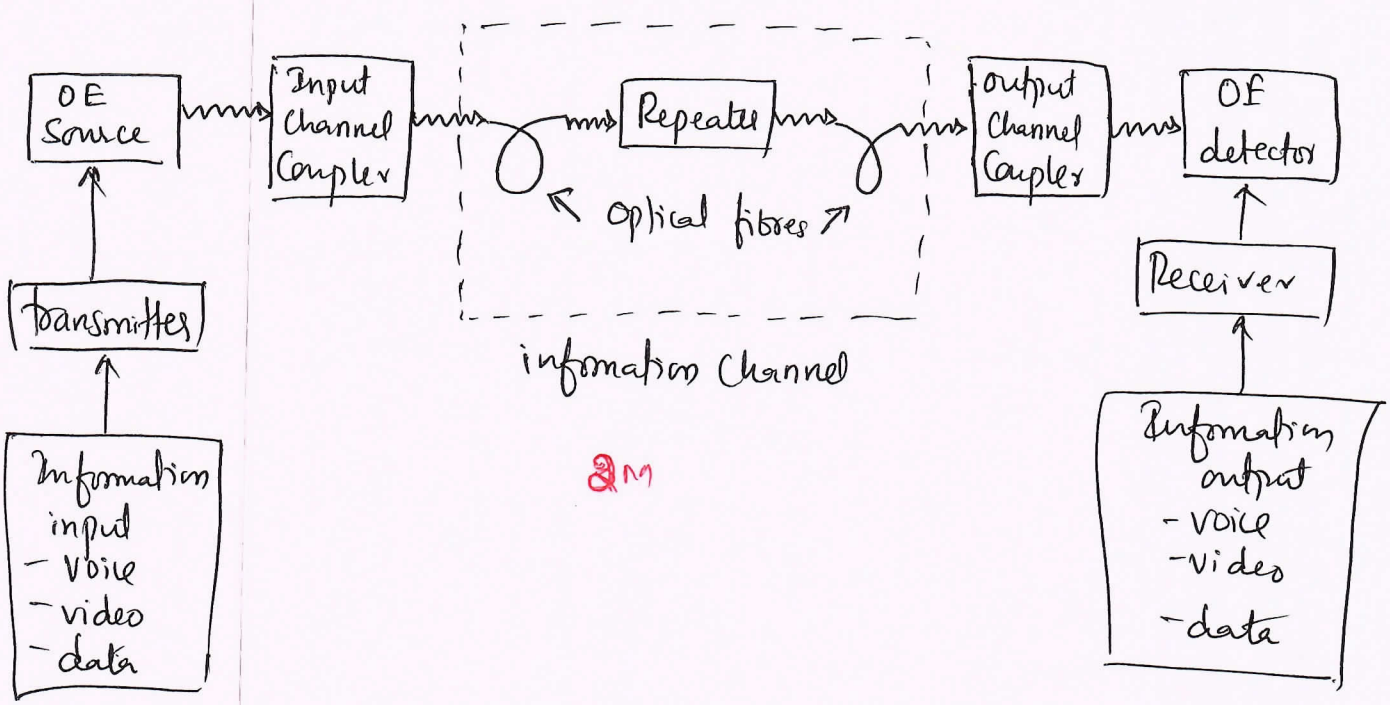
Cell :- a small hexagonal service area of range (5 km to 20km)

Base station (BS) :- Each cell contains an antenna, which is known as BS controlled by a small office 3M

Mobile Switching Centre (MSC) :- It is an office which controls the Base station //

Q.6 Explain the optical fibre communication system with a block diagram 6M

Soln



2M

Information Input :- Information input maybe in any of the several physical forms like voice, video, data. Transducers are used to convert non electrical signal to electrical. 1M

Transmitter :- It comprises of electronic stage which converts electric signal into proper form & impresses this signal onto electromagnetic wave (Carrier) for onward transmission 1M

Optoelectronic Source (OE) :- Optoelectronic (OE) source generates an electromagnetic wave in the optical range which acts as information carrier. 1M

Channel Couplers :- The channel coupler is an antenna, which collects the signal from transmitter & directs this to atmospheric channel. 1M

At the receiver end, again the antenna collects the signal & routes it to the receiver.

9.b Continued ...

Fiber optic information Channel :- This is the path between the transmitter & receiver. In optical Communication optical fibers act as channel.

Repeater :- As the signal propagates along the length of the fibre, they get attenuated due to absorption, Scattering etc. This makes the signal weak. Before signal become weak, its strength & shape are restored using repeater.

Optoelectronic Detector :- It re-converts the optical signal into an electrical signal.

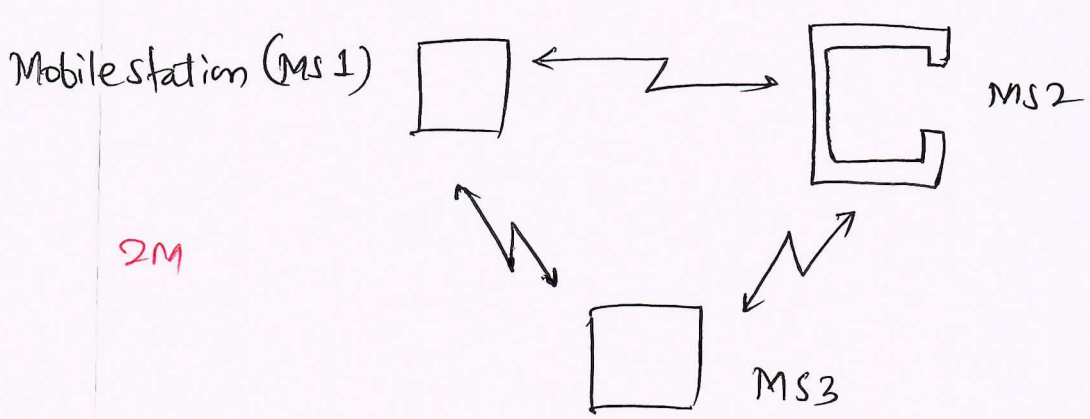
Receiver :- It receives the information signal in its electrical form.

Information output :- Using output transducers the required information o/p is presented to user. //

9.c With the help of diagrams, discuss the following types of network topologies: Adhoc n/w topology, infrastructure n/w topology. 8M

Soln

Adhoc network topology



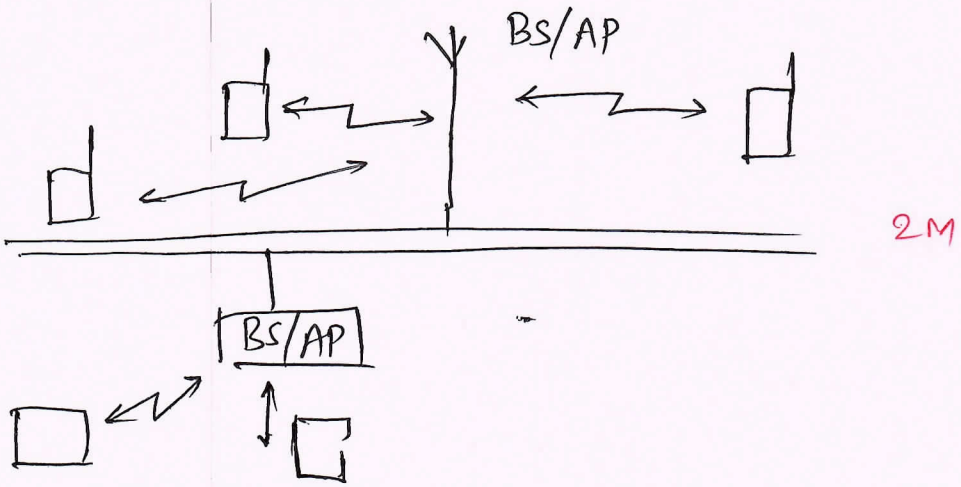
2M

9.c Continued...

Adhoc wireless n/w do not need any infrastructure to work. Each node can communicate directly with other nodes, so no base station is necessary.

- There are primarily used by military & in few commercial applications
- This topology is suitable for rapid deployment in a mobile or fixed environment 4M
- Nodes within an adhoc n/w can only communicate if they reach each other physically
- In some n/w applications, users may be distributed & may reach only a portion of the other users due to power limitations.
- Under such circumstances, we go for multiple adhoc n/w topology

Infrastructure network topology :-

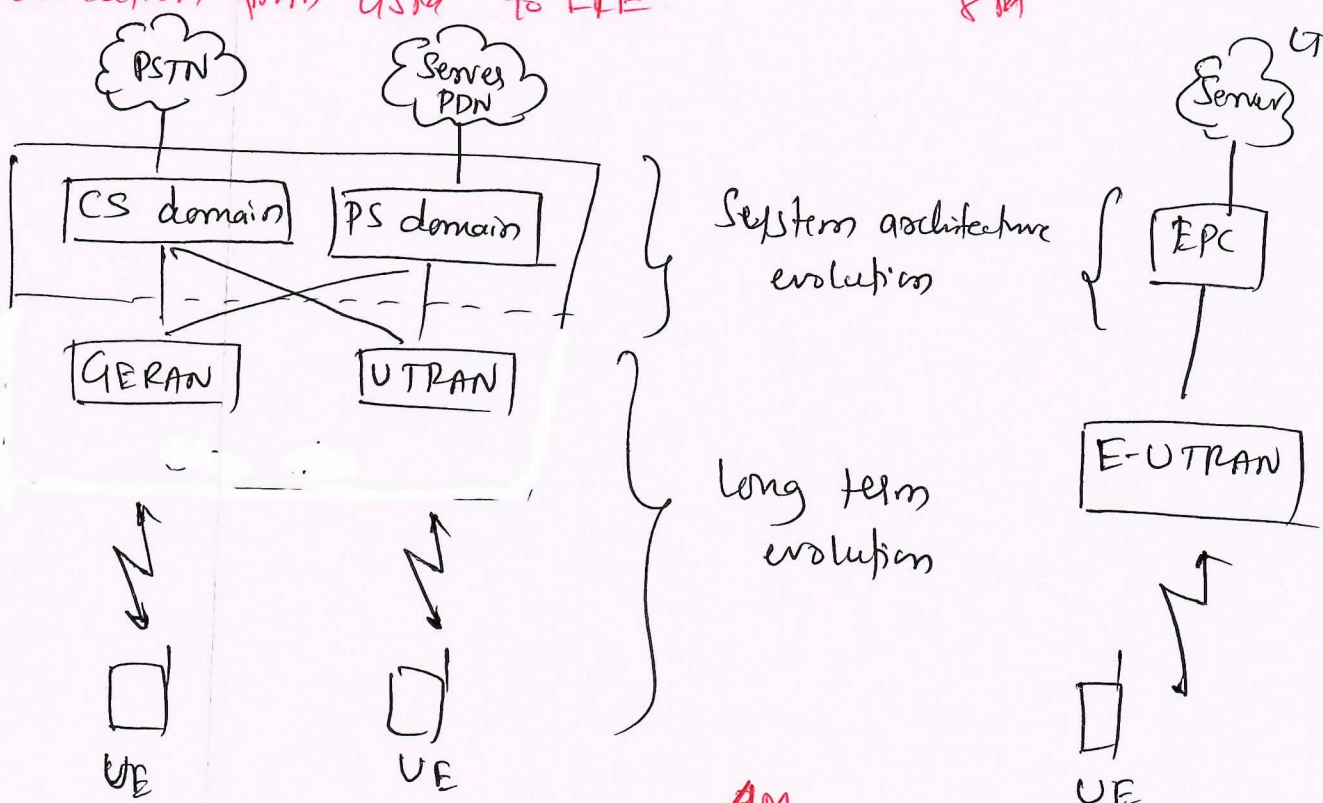


2M

9.c Continued ...

- In this topology, there is a fixed infrastructure that supports the communication between ~~them~~ mobile terminals & bet^n mobile & fixed terminals.
- designed for large coverage area. & multiple base stations (BS) or access points (AP) operations
- BS serves as hub of the n/w & mobile terminals are located at different positions at the ends & spokes
- Any communications happens through BS

10.a With the help of architecture figures explain the evolution from GSM to LTE. 8M



4M

10.a Continued...

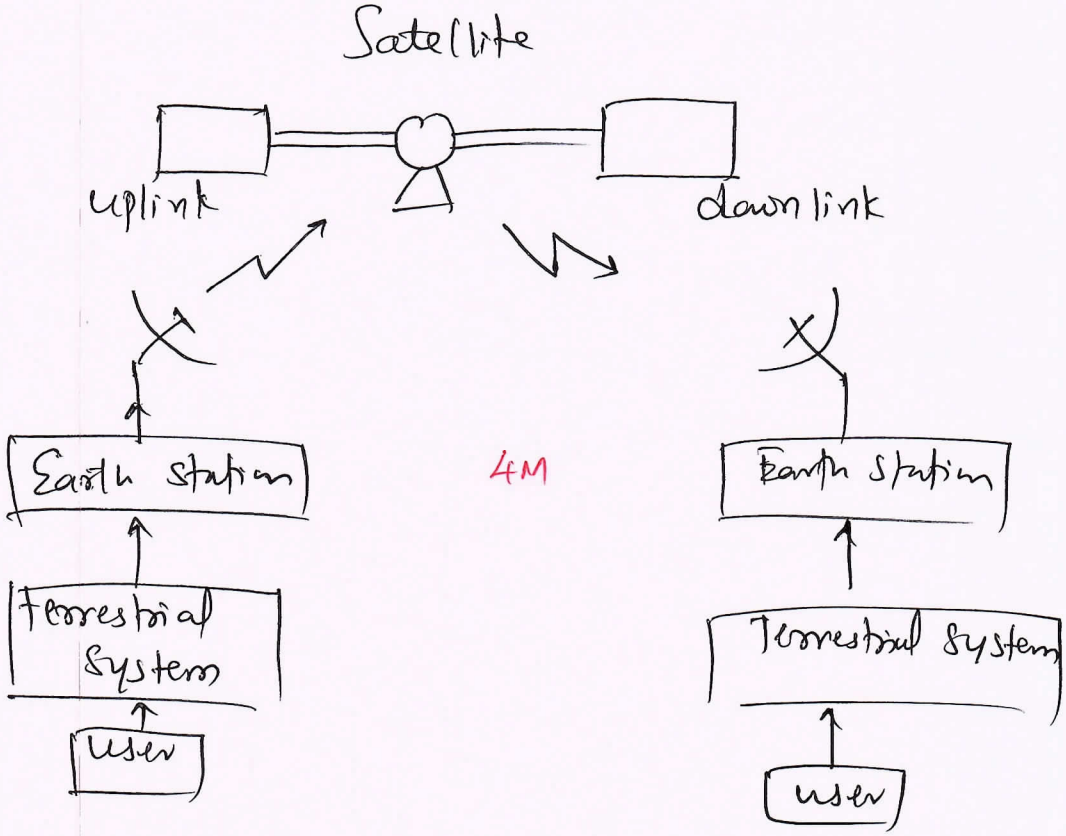
- In the new architecture Evolved packet core (EPC) is a direct replacement of the packet switched domain of UMTS - (Universal mobile telecommunication System.) & GSM.
- It distributes all types of information to the user
- The new architecture was designed as part of two 3GPP work items namely system architecture evolution (SAE) which covered core network & long term evolution (LTE) which covered the radio access n/w, air interface & mobile. 4M
- Officially the whole system is known as Evolved packet System (EPS), while the acronym LTE refers to only the evolution of air interface //

10.b List the requirements for the 4G technology. 4M

- Higher spectral efficiency
- Reduced cost per bit
- Increased service provisioning by lowering the cost & increasing the efficiency
- Open interfaces as against closed technologies of past
- Power consumption efficiency
- Scalable & flexible usage of frequency band //

10.c Draw the block diagram showing the basic elements of a satellite communication system & briefly explain them 8M

Sol:



4M

User - generates the baseband signal that proceeds through a terrestrial n/w & transmitted to a satellite at the earth station 1M

Satellite - Consists of large no. of repeaters that perform reception of modulated RF carrier in its uplink from all earth stations & retransmits them back to earth station in down link frequency 1M

Terrestrial n/w - This is a n/w on ground which carries the signal from user to earth station 1M

Earth station - It a radio station located on earth & used for relaying signals from satellites 1M