CBCS SCHEME

USN 18EE34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronics Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. (10 Marks)

b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero. (10 Marks)

OR

2 a. Derive the expression for stability factors S' and S'' for fixed bias circuit. (08 Marks)

b. A voltage divider biased circuit has $R_1 = 39K\Omega$, $R_2 = 82K\Omega$, $R_C = 3.3K\Omega$, $R_E = 1K\Omega$ and $V_{CC} = 18V$. The silicon transistor used has $\beta = 120$. Find Q-point and stability factor. (07 Marks)

c. Explain the operation of transistor as switch with suitable circuit and necessary waveforms. (05 Marks)

Module-2

3 a. State and prove Millers theorem. (06 Marks)

b. Compare the characteristics of CB, CE and CC configurations. (06 Marks)

c. For the collector feedback configuration having $R_F = 180K\Omega$, $R_C = 2.7K\Omega$, $C_1 = 10\mu F$, $C_2 = 10\mu F$, $\beta = 200$, $r_o = \infty\Omega$ and $V_{CC} = 9$volts. Determine the following parameters:
i) re ii) z_i iii) z_o iv) A_v (08 Marks)

OR

4 a. Derive suitable expression to explain the effect of cascading of amplifiers on lower and upper cut off frequencies. (08 Marks)

b. Derive equations for miller input capacitance and miller output capacitance. (08 Marks)

c. A transistor in CE mode has h-parameters $h_{ie} = 1.1K\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. (04 Marks)

Module-3

5 a. Derive expression for Zi and Ai for a Darlington Emitter follower circuit. (10 Marks)

b. Explain the need of a cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. (06 Marks)

c. Write a note on cascade amplifier. (04 Marks)

OR

6 a. List the general characteristics of negative feedback amplifier. (04 Marks)

b. A given amplifier arrangement has the following voltage gain $AV_1 = 10$, $AV_2 = 20$ and $AV_3 = 40$. Calculate the overall voltage gain and determine the total voltage gain in dB. (04 Marks)

c. For the voltage series feedback amplifier. Derive an expression for output impedance (Resistance). (08 Marks)

Module-4

7 a. Show that maximum efficiency of class-B push pull amplifier (power amplifier) circuit is 78.54%. (08 Marks)

b. Explain the classification of power amplifier with a neat circuit diagram and waveforms. (07 Marks)

c. A class-B push pull amplifier operating with $V_{CC} = 25V$ provides a 22V peak signal to 8Ω load. Calculate the circuit efficiency and power dissipated per transistor. (05 Marks)

OR

8 a. Draw the circuit of wein bridge oscillator and explain its operation. (10 Marks)

b. With a neat circuit diagram and waveform, explain the working principal of crystal oscillator operating in series resonant mode. A crystal has the following parameters L = 0.3341H, C = 0.065pF and R = 5.5KΩ. Calculate its resonant frequency. (10 Marks)

Module-5

9 a. With the help of neat diagram, explain the working and characteristics of N-channel JFET. (10 Marks)

b. For a self bias JFET circuit, $V_{DD} = +12V$, $R_D = 2.2K\Omega$, $R_G = 1M\Omega$, $R_S = 1K\Omega$, $I_{DSS} = 8mA$, $V_P = -4$ Volts. Determine the following parameters: i)V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_G vi) V_D (10 Marks)

OR

10 a. With neat sketches, explain the operation and characteristics of n-channel depletion type MOSFET. (10 Marks)

b. Derive expression for V_{GS}, I_D, V_{DS}, V_D and V_S for a voltage divider bias circuit using FET. (10 Marks)

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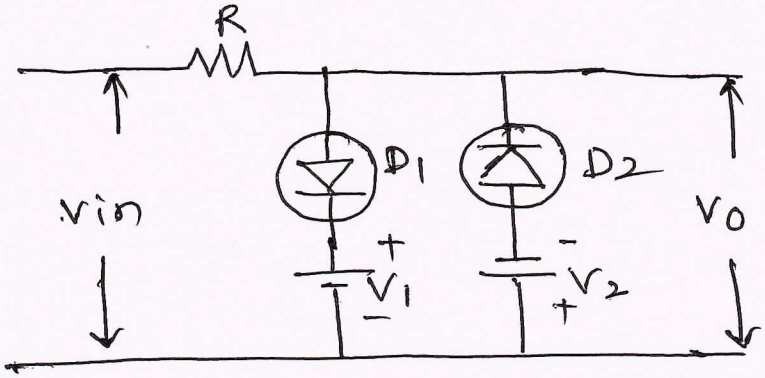
Analog Electronics Circuits 18EE34
Jan 2020

1a Double ended clipper Circuit

Clip off the portions of both positive and Neg half cycles of the i/p. Two way parallel Clipp shown in fig



$V_{in} = V_m \sin \omega t$

The diode D_1 and D_2 are ideal diodes.

— 2M

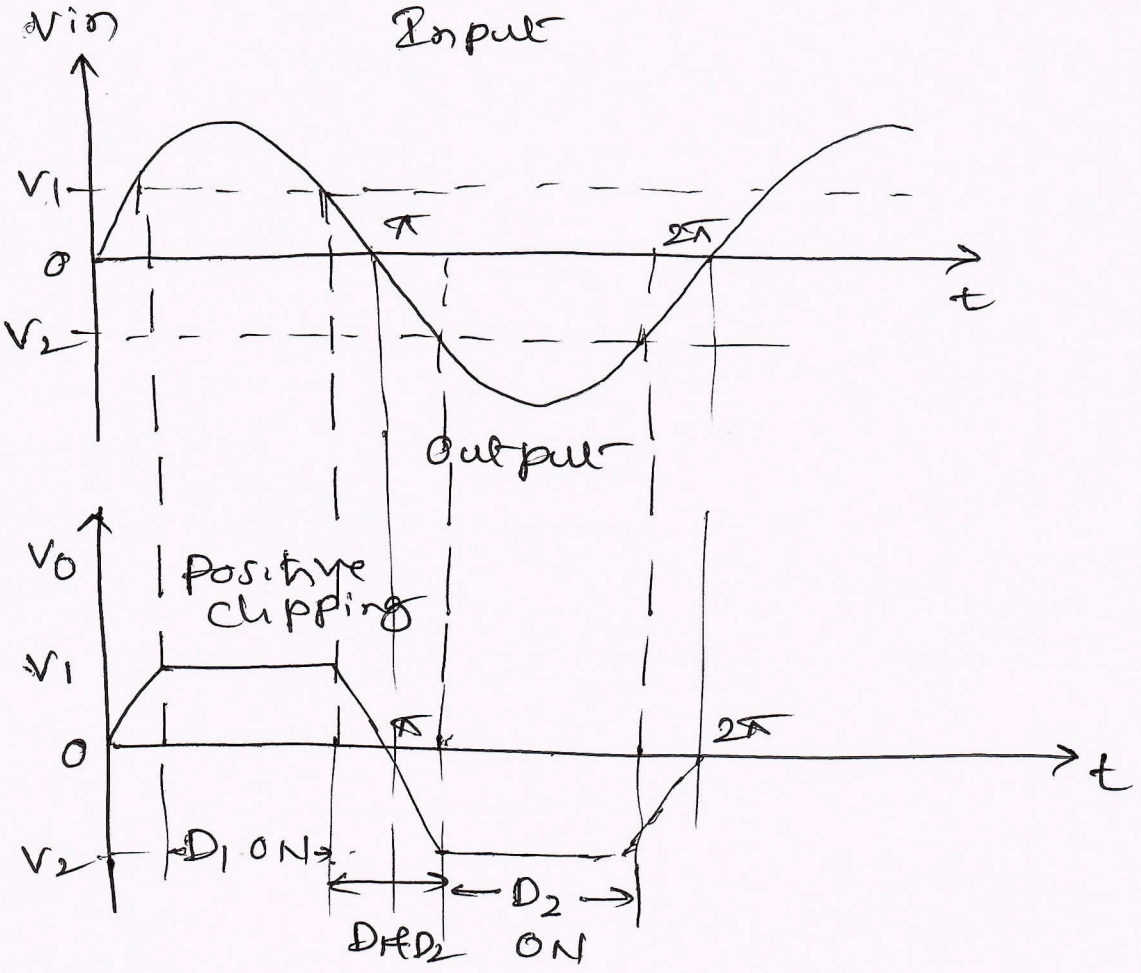
Positive half cycle of input: $V_{in} > V_1$ then dio D_1 becomes forward biased and Conducts. whil D_2 reverse biased for the entire positive ha cycle of the i/p

when $V_{in} < V_1$, D_1 and D_2 are off, & $V_o = V_{in}$

$V_{in} > V_1$ D_1 is ON, D_2 is OFF & $V_o = V_1$

Negative half cycle of the input: As long as V_{in} is greater than V_2, the diode D_2 remains reverse biased. D_1 remains OFF for t entire negative half cycle of the i/p $\therefore V_o = V_i$ when V_{in} becomes less than V_2. The dio D_2 becomes forward biased and Conducts. Th diode D_1 is OFF $V_o = V_2$. The O/P is negativ as V_2 are opposite to that of V_1 — 4m

35



— 2M

Wave form for two way clippers.

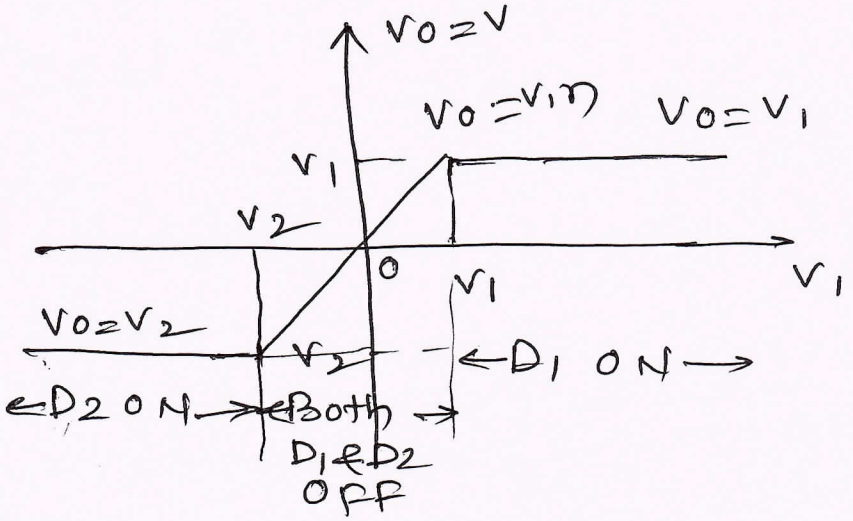
Transfer characteristics for the two way clippers

$V_o = V_{in}$ for $V_{in} < V_1$ } Positive cycle

$V_o = V_1$ for $V_{in} > V_1$ }

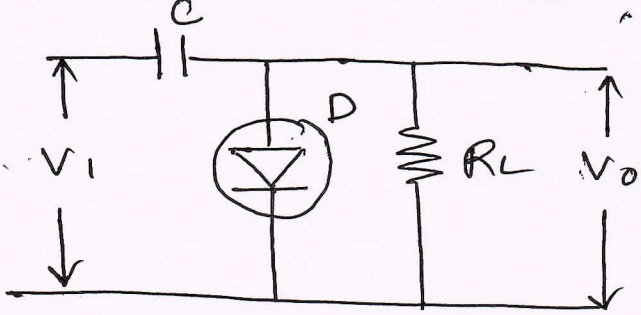
$V_o = V_{in}$ for $V_{in} > V_2$ } Negative cycle.

$V_o = V_2$ for $V_{in} < V_2$ }



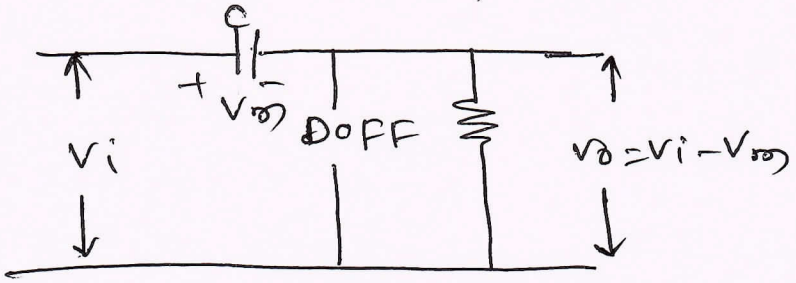
— 2M

1b Clamper Circuit - positive peak signal to zero is Negative Clamper - which add the negative levels to the ac o/p.
It consists of capacitor C, Ideal diode D a load resistance R_L, as shown in fig



Assume
D is ideal diode
$\tau = R_C$ to be very large. — 2M

During first quarter of positive cycle of input voltage V_i, the capacitor gets charged through the forward biased diode D, up to the maximum value of V_m of the i/p signal. The capacitor charging is almost instantaneous by selecting the proper value of C and R_C in the circuit. Capacitor once charged to V_m acts as a battery of voltage V_m



— 4M

When D is on the o/p voltage V_o is zero. As i/p voltage decreases after attaining the maximum value V_m the capacitor charged to V_m the diode becomes reverse biased.

The capacitor holds entire charge as $V_c = V_m$ the o/p voltage $V_o = V_i - V_c = V_i - V_m$

During the negative half cycle of V_i, the diode will remains reverse biased. The capacitor starts discharging through the resistance R_L. As the time constant $R_L C$ is very large it can be approximated the capacitor holds all its charge and remains charged to V_m. Hence it can be written

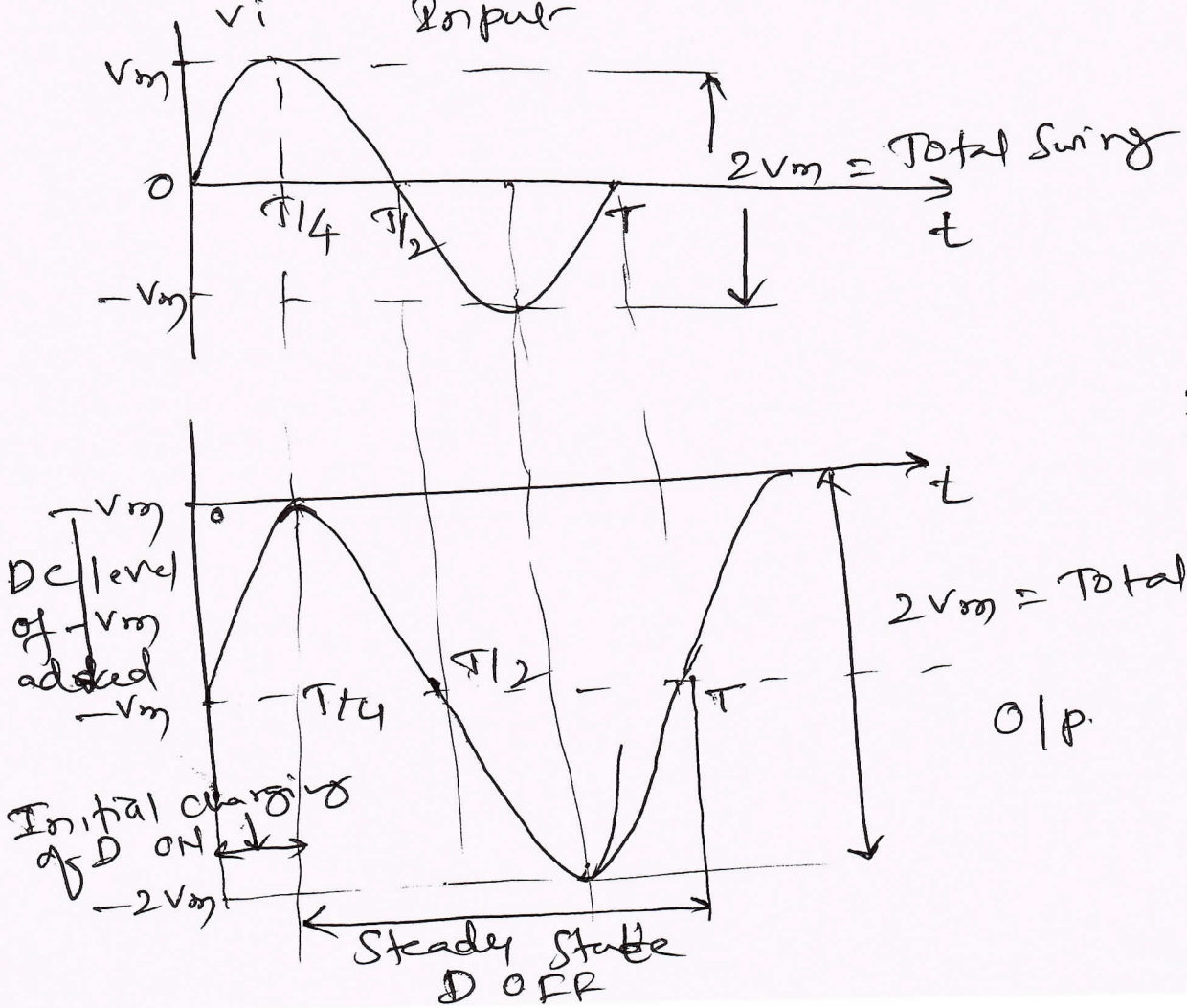
$V_o = V_i - V_c = V_i - V_m$ for negative half cycle

$V_o = -V_m$ for $V_i \geq 0$

$V_o = 0$ for $V_i = V_m$

$V_o = -2V_m$ for $V_i = -V_m$ — 2M

The i/p and o/p waveform are shown in fig



2a Expression for Stability factor S' and S'' for Fixed bias Circuit.

Biasing provides the stability on I_C against the variation of I_{CO}, β and V_{BE}

Stability factor provides the change in operating point due to variation in temperature.

(i) $S' = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\beta \text{ constant}} = S_{ICO}$ (ii) $S(V_{BE}) = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO}, \text{Con}}$

Fixed bias Stability factor $S(I_{CO})$

$\therefore I_B = \frac{V_{CC}}{R_B}$, when I_B changes by ΔI_B, V_{CC} and V_{BE} are unaffected

$\therefore$ $S(I_{CO})$ for Common emitter Configuration

$I_C = \beta I_B + I_{CEO} = \beta I_B + (1+\beta) I_{CBO}$ —(1)

I_{CBO} changes by ΔI_{CBO}, I_B changes by ΔI_B and I_C changes by ΔI_C. The above eqn (1) becomes

$$\Delta I_C = \beta \Delta I_B + (1+\beta)\Delta I_{CBO}$$

$$1 = \frac{\beta \Delta I_B}{\Delta I_C} + \frac{(1+\beta)\Delta I_{CBO}}{\Delta I_C}$$

$$1 - \frac{\beta \Delta I_B}{\Delta I_C} = (1+\beta)\frac{\Delta I_{CBO}}{\Delta I_C}$$

$$\therefore \frac{\Delta I_{CBO}}{\Delta I_C} = \frac{1-\beta(\Delta I_B/\Delta I_C)}{(1+\beta)}$$

$$S_{ICO} = \frac{\Delta I_C}{\Delta I_{CBO}} = \frac{(1+\beta)}{1-\beta(\Delta I_B/\Delta I_C)} \quad \text{— (2)}$$

$\therefore S_{ICO} = \frac{1+\beta}{1-\beta(\Delta I_B/\Delta I_C)} = \frac{1+\beta}{1}$ $\left(\frac{\Delta I_B}{\Delta I_C} \approx 0\right)$ —(3)

Stability factor $S(I_{BE}) = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\beta \text{ Constant}}$

We know that $I_C = \beta I_B + (\beta+1) I_{CBO}$

represent I_B in terms of V_{BE} we get

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B} + (\beta+1) I_{CBO} = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CBO}$$

$$\therefore \frac{\Delta I_C}{\Delta V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = \frac{-\beta}{R_B} = S(V_{BE}) = S''$$

Relation between $S(I_{CO})$ and $S(V_{BE})$

we know that $S_{I_{CO}} = 1+\beta$ & $S_{V_{BE}} = -\frac{\beta}{R_B}$

multiplying numerator and denominator by $(1+\beta)$ we get

$$S(V_{BE}) = \frac{-\beta(1+\beta)}{R_B(1+\beta)}$$

$$S(V_{BE}) = \frac{-\beta S(I_{CO})}{R_B(1+\beta)} \quad \left[\because S_{I_{CO}} = (1+\beta)\right]$$

— 4m

Stability factor S_β. $S_\beta = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{V_{BE}, I_{CO} \text{ Constant}}$

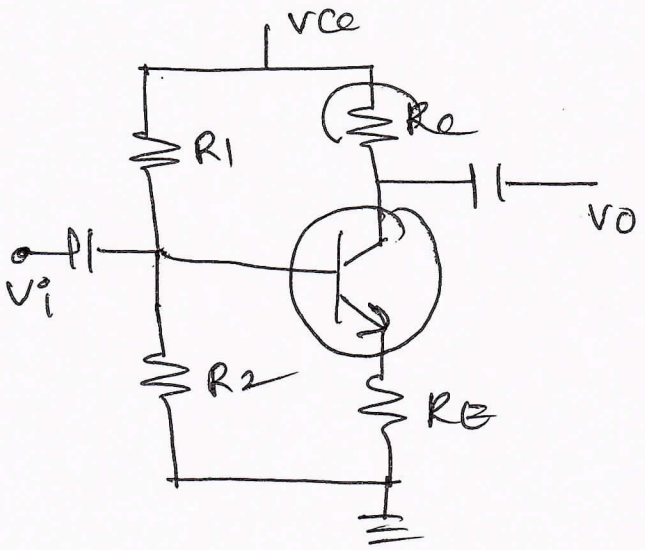
$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CBO}$$

$$\frac{\Delta I_C}{\Delta \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta}$$

$$\therefore S_\beta = \frac{\Delta I_C}{\Delta \beta} = \frac{I_C}{\beta} \quad \therefore I_B = \frac{I_C}{\beta} \text{ & } I_B >> I_{CBO}$$

2b Voltage divider bias $R_1 = 39k\Omega$, $R_2 = 82k\Omega$, $R_C = 3.3k\Omega$, $R_E = 1k\Omega$ and $V_{CC} = 18V$, $\beta = 120$

Q Point and Stability factors.



$$R_{Th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{3198}{121} = 26.43k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{1476}{121}$$

$$= 12.19V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta+1)\cdot R_E} \quad \text{— 4m}$$

$$= \frac{12.19 - 0.7}{26.43k + (121)\,1k}$$

$$= 77.79\mu A$$

$$I_E = \beta \cdot I_B = 0.938mA$$

$$V_{CE} = V_{CC} - I_E(R_C + R_E) = 18 - (0.938)(3.3+1)$$

$$= 18 - 0.938(4.3) = 13.967V$$

Q Point $= (V_{CE}, I_C) = (13.967,\ 0.938)$

$$S(V_{BE}) = \frac{-\beta \| R_E}{\beta + R_{Th} \| R_E} = \frac{-120 \| 1k\Omega}{120 + 26.4k\Omega \| 1k\Omega}$$

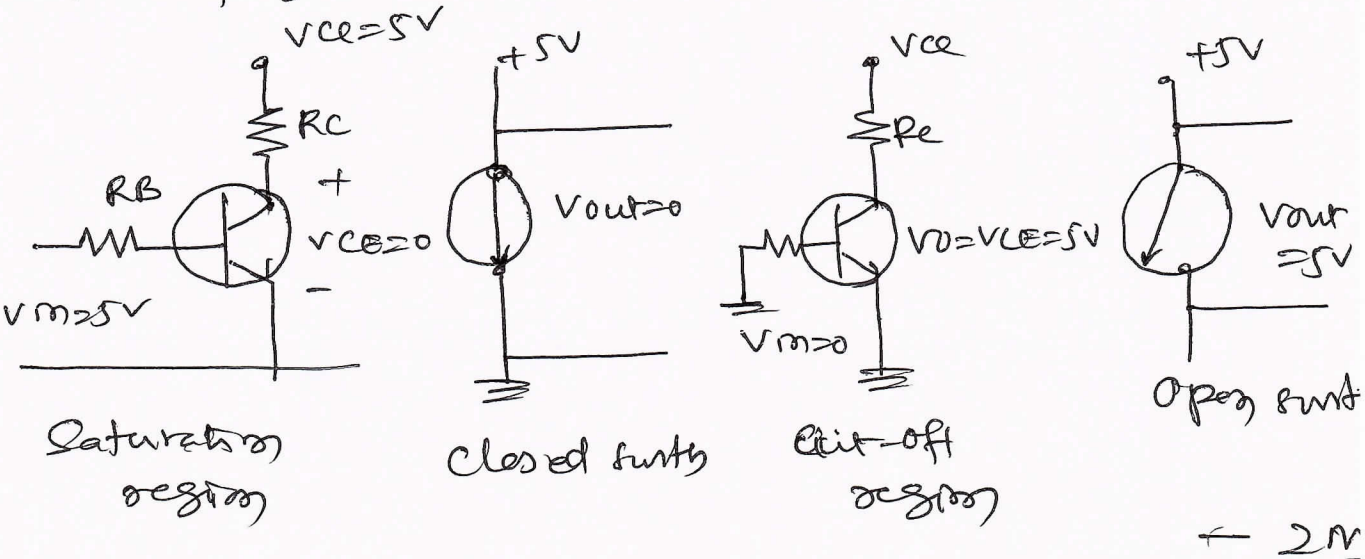
$$= -0.82 \times 10^{-3} \quad \text{— 03m}$$

2c Transistor as a Switch.

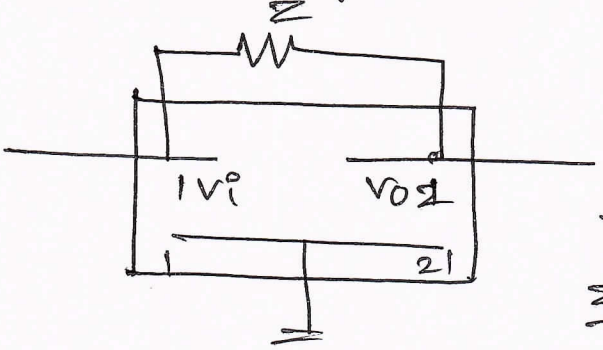
BJT as a Switch it operates in two regions
① Cut-off ② Saturation

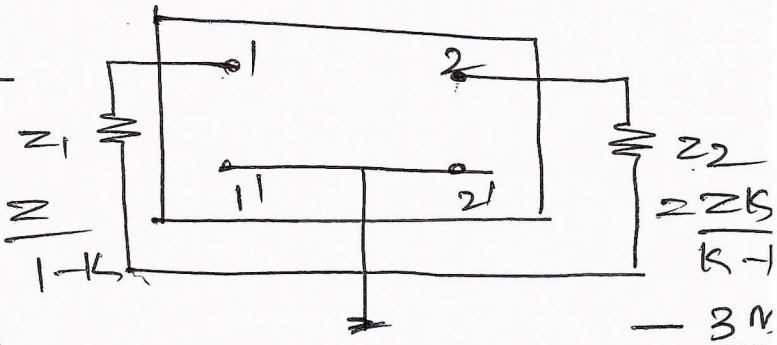
For Cut-off region both the junctions of transistors are reverse biased. only reverse Current flows. No Current flows through the transistor in Cut off region. It acts as open Switch

In Saturation region both junctions are forward biased it o VCE(Sat). Collector Current is large and is Controlled by external resistance Connected in Collector Circuit. VCE Sat- in the range 0.2 to 0.3 V and Can be neglected to supplied Voltage, VCE for CE configuration o Zero in Saturation region. Thus it acts as a Closed Switch. It is shown in below fig



3g Millers theorem : Millers theorem is used for converting any circuit having the configuration of common impedence betn i/p and o/p to another configuration of seperater impedence for input and output. Millers theorem simplifies the circuit for analysis of input impedence and output impedence





— 3M

Z. is the impedence connected between i/p and output node 1 and node 2 it is replaced by two seperate impedences Z_1 & Z_2

Z_1 is connected between node 1 and ground .. Z_2 is connected between node 2 and ground, V_1 and V_2 are voltages at node and node 2 respectively. The Z_1 and Z_2 are derived from the ratio of Vo and Vi ($\frac{V_o}{V_i}$) is gain denoted by K

$$I = \frac{V_i}{Z}, \quad I = \frac{V_i - V_o}{Z} = \frac{V_i\left[1 - \frac{V_o}{V_i}\right]}{Z}$$

$$= \frac{V_i}{Z}[1-K] \quad \therefore Z_1 \Rightarrow \frac{Z}{1-K}$$

3M

$$Z_2 = \frac{V_o}{I}$$

where $I = \dfrac{V_o - V_i}{Z} = \dfrac{V_o\left[1 - \dfrac{V_i}{V_o}\right]}{Z}$

$$= \frac{V_o\left[1 - \dfrac{1}{A_V}\right]}{Z}$$

$$= \frac{V_o\left[\dfrac{K-1}{K}\right]}{Z}$$

$$\therefore Z_2 = \frac{V_o}{I} = \frac{Z}{\dfrac{(K-1)}{K}} \quad - 3M$$

$$= \frac{ZK}{K-1} \quad \left[\frac{V_o}{V_i} = A_V = K\right]$$

11/c

3b Characteristics of CB, CE and CC Configuration.

	CB	CE	CC
① Input resistance	Very low $\leq 20\,\Omega$	Low (KΩ)	High 500k
② output resistance	Very high (MΩ)	High (40KΩ)	Low 50Ω
③ Input Current	I_E	I_B	I_B
④ Output Current	I_C	I_e	I_E
⑤ input voltage applied between	Emitter & Base	Base & Emitter	Base & Collector
⑥ output voltage taken between	Collector & Base	Collector & Emitter	Emitter & Collector
⑦ Current amplification factor	$\alpha dc = \frac{I_e}{I_E}$	$\beta dc = \frac{I_e}{I_B}$	$\frac{I_E}{I_B}$
⑧ Current gain	Less than unity	High (20 to few Hundreds)	High 20 to few Hund
⑨ Voltage gain	Medium	medium	Low
⑩ Applications	Input of multi stage amplifier	Audio signal Amplification	Impedance matching

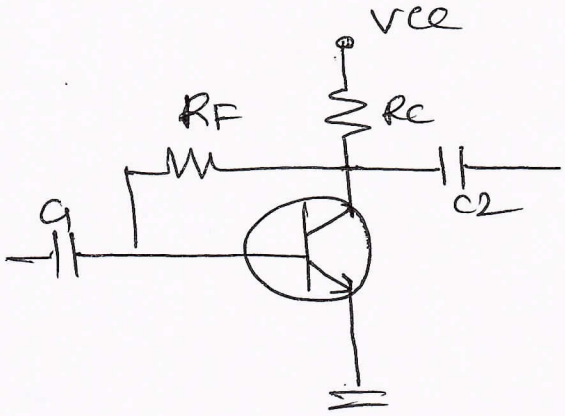
6X1M
= 6

3c for a Collector feedback configuration R_F = ?

$R_C = 2.7\,k\Omega$ $C_1 = 10\,\mu F$, $C_2 = 10\,\mu F$, $\beta = 200$

$r_o = \infty\,\Omega$ V_{CE} = given, (i) r_e = ? (ii) Z_i = ?

(iii) Z_o and (iv) A_V = ?



Collector feed back Configuration

$$I_B = \frac{V_{CE} - V_{BE}}{R_F + \beta R_C}$$

$$= \frac{9 - 0.7}{200k * 2.7 * 180k}$$

$$= 11.53\,\mu A \quad -3m$$

$$I_E = (\beta + 1) I_B = 2.32\,mA$$

$$r_e = \frac{26\,mV}{I_E} = \frac{26\,mV}{2.32\,mA} = 11.21\,\Omega \quad -2M$$

$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_e}{R_C + R_F}} = \frac{11.21}{\frac{1}{180} + \frac{2.7k}{2.7k + 200}} = 566.16\,\Omega$$

$$Z_o = R_C \,||\, R_F = \frac{2.7k \times 180k}{2.7k + 18k} = 2.66\,k\Omega$$

$$A_V = -\frac{R_C}{r_e} = \frac{-2.7\,k\Omega}{11.21\,\Omega} = -240.86$$

$-03m$

4a Expression for explaining the effect of cascading of amplifiers on lower and upper cutoff frequencies

Frequency response of the multi-stage amplifier is always less than that of the bandwidth of single stage amplifier.

Low cut-off frequency. The overall voltage gain at lower cut-off frequency

$$A_{V\text{-}Low} = A_{V1} \times A_{V2} \cdots \times A_{Vn} = (A_{V\text{-}low})^n$$

$n \rightarrow$ number of cascaded stages.

$$\left[\frac{A_{V\text{-}low}}{A_{V\text{-}mid}}\right]_{overall} = \left[\frac{A_{V\text{-}low}}{A_{V\text{-}mid}}\right]^n = \frac{1}{1 - j\left(\frac{f_1}{f}\right)^n}$$

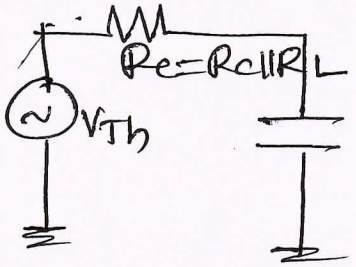
$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{[1+(f_1/f_{c\text{-}low})^2]^n}}, \quad f_{c\text{-}low} = \frac{f_1}{\sqrt{2^{1/n}-1}}$$

— 04M

High Cut-off frequency

$$A_V = \frac{V_{out}}{V_{in}} \qquad \left[V_0 = \frac{-jX_C}{R-jX_C} V_{in}\right]$$

$$= \frac{1}{1+j(RW_C)}$$



$$A_V = \frac{1}{1+j(2\pi f_C R)} = \frac{1}{1+j(f/f_2)} \quad \left(A_V = \frac{1}{\sqrt{1+(f/f_2)^2}}\right.$$

$$f_2 = \frac{1}{2\pi R_e}$$

$$\Rightarrow A_{V\text{-}high}/A_{V\,mid} = 1/\sqrt{2} = \frac{1}{\sqrt{[1+(f_{c\text{-}high}/f_2)^2]^n}}$$

$$\Rightarrow f_{c\text{-}high} = f_2\sqrt{2^{1/n}-1}$$

The cut-off frequencies for cascaded Do
from f_{c1} and f_{c2}

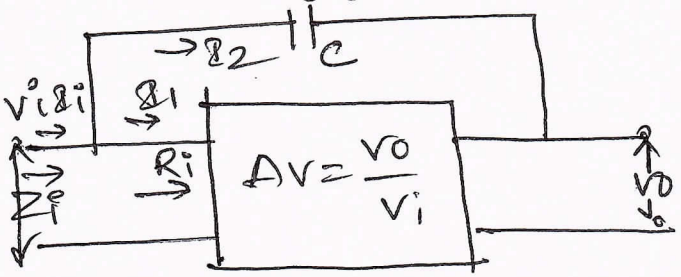
$$f_{c\text{-}low} = \frac{f_{c1}}{\sqrt{2^{1/n}-1}}, \quad f_{c\text{-}high} = f_{c2}\sqrt{2^{1/n}-1}$$

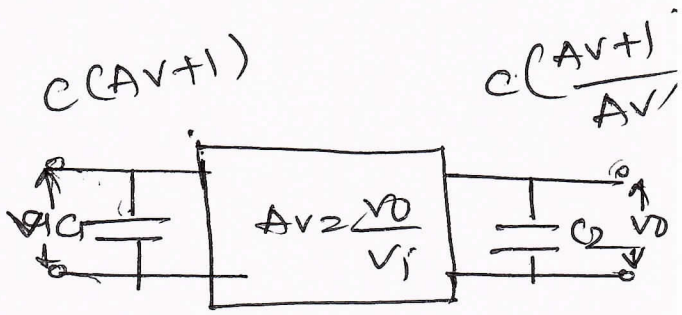
$$B.W = f_{c\,high} - f_{c\,low}$$

Each stage has different lower and upper
Critical frequencies.

Lower Critical frequency f_{cL}, upper crit
frequency f_{cu} — 04m

4b In the high frequency analysis of transistor split the capacitance between input (base or gate) and output (collector or drain). This is achived using miller theorem as shown in the fig





Av represents the voltage gain of the amplifier
C represents either C_{be} or C_{gd}

Applying KCL for ① $I_i = I_1 + I_2$ — ①

where $I_i = \frac{V_i}{Z_i}$ and $I_1 = \frac{V_1}{R_i}$

& $I_2 = \frac{V_1 - V_0}{X_C} = \frac{V_1 - A_V \cdot V_i}{X_C} = \frac{(1 - A_V)\, V_1}{X_C}$

Substituting value of I_2

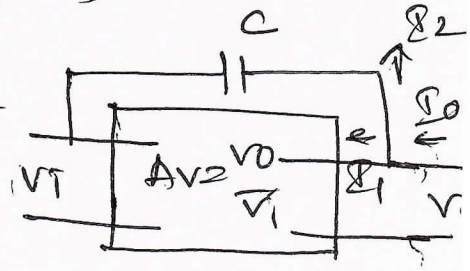
$$I_1 = \frac{V_1}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_V)\, V_i}{X_C} \Rightarrow \frac{1}{Z_i} = \frac{1}{R_i} + \frac{(1 - A_V)}{X_C}$$

$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{CM}}$ where $X_{CM} = \frac{X_C}{(1 - A_V)}$

$$X_{CM} = \frac{X_C}{(1 - A_V)} \Rightarrow \frac{1}{2\pi f_{CM}} = \frac{1}{(1 - A_V)(2\pi f C)}$$

$$\frac{1}{C_M} = \frac{1}{(1 - A_V) \cdot C}$$

Let us consider the circuit



Apply KCL

$I_0 = I_1 + I_2$ — 04M

$I_1 = \frac{V_0}{R_0}$ and $I_2 = \frac{V_0 - V_i}{X_C}$ 25

$R_0 \rightarrow$ sufficiently large ignore the first

$\therefore I_0 = \frac{V_0 - V_i}{X_C} = \frac{V_0 - \frac{V_0}{A_V}}{X_C}$

$= \frac{V_0(1 - 1/A_V)}{X_C}$

$\frac{I_0}{V_0} = \frac{1 - 1/A_V}{X_C}$

$\frac{V_0}{I_0} = \frac{X_C}{1 - 1/A_V} \Rightarrow X_{CMO} = \frac{X_C}{1 - 1/A_V}$

$\frac{1}{2\pi f C_{MO}} = \frac{1}{2\pi f C(1 - 1/A_V)}$

Usually $A_V >> 1$ $\therefore C_{MO} = C$ 04m

4c A transistor CE model has h-parameter $h_{ie} = 1.1\,k\Omega$ $h_{re} = 2\times10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\,\mu A/V$

CB mode h-parameters

$$h_{ib} = r_e = \frac{26\,mV}{I_e}$$

$$h_{fb} = -\alpha \cong -1$$

$$\therefore h_{rb} = \frac{h_{ie}}{1+h_{fe}} = \frac{1100}{1+100} = 10.89\,\Omega$$

$$h_{rb} = \frac{h_{ie}\cdot h_{oe}}{1+h_{fe}} = \frac{1100\times25\times10^{-6}}{1+100} = 2.22\times10^{-5}$$

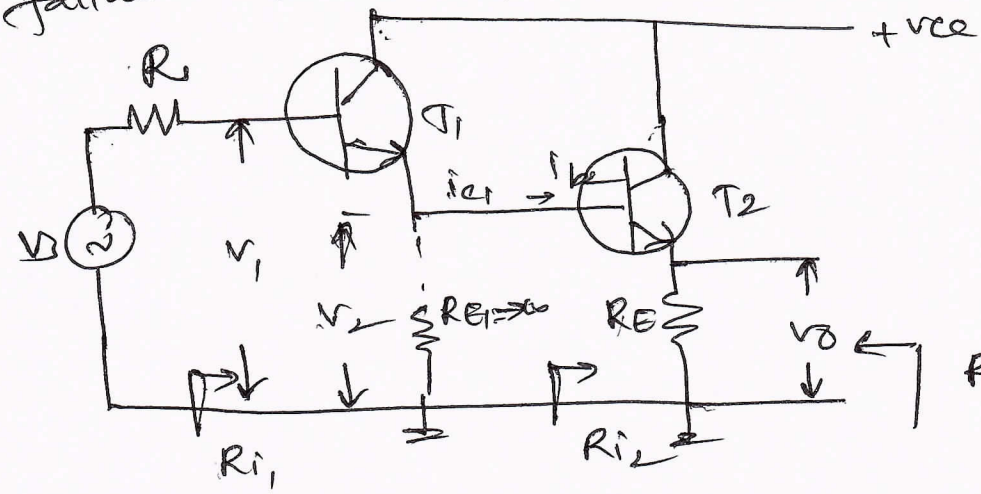
$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}} = \frac{-100}{1+100} = -0.99$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}} = \frac{25\times10^{-6}}{1+100} = 0.24\times10^{-6}$$

$4\times1m = 4m$

Sq Expression for Z_i and A_i for Darlington emitter follower.

The direct coupling of two stage emitter follower amplifier. The cascade connection of two emitter follower is called Darlington Connection

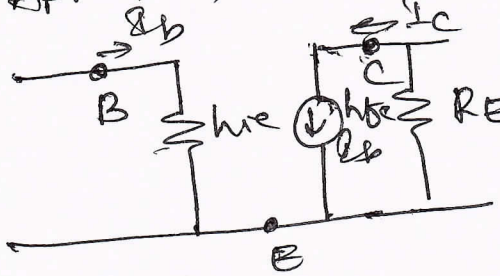


Darlington emitter follower Circuit

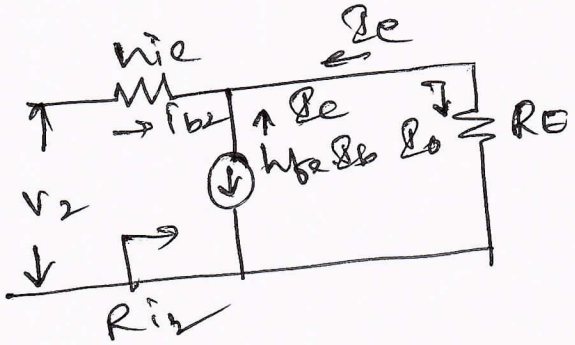
— 2M

Assume Load resistance R_L such that $R_L \cdot h_{oe} < 0$.

Approximate analysis of second stage.



The same circuit is redrawn making the Collector Common, i.e. h-equivalent Common Collector Configuration



Analysis of 2nd stage

Current gain $A_{i2} = \frac{I_o}{I_{b_2}} = \frac{I_e}{I_{b_2}}$

$= \frac{I_b + h_{fe} I_b}{I_b} = \frac{I_b(1+h_{fe})}{I_b}$

$A_{i2} = 1 + h_{fe}$

I/p resistance $Z_{i2}(R_{i2}) = \frac{V_2}{I_{b_2}}$

Applying KVL to outer loop

$V_2 - I_{b_2} \cdot h_{ie} - I_o \cdot R_E = 0$

$V_2 = I_{b_2} h_{ie} + I_o \cdot R_E$ — 02M

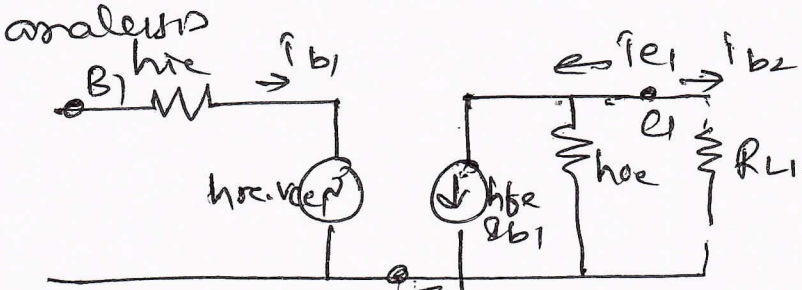
$$\frac{V_2}{I_{b2}} = R_{i_2} = h_{ie} + A_{i2} \cdot R_E \qquad \left(\frac{I_o}{I_{b2}} = A_{i2}\right) \quad (2)$$

$$\therefore R_{i2} = (1+h_{ie})\, R_E \quad (h_{ie} << (1+h_{fe}).R_E) \quad (3)$$

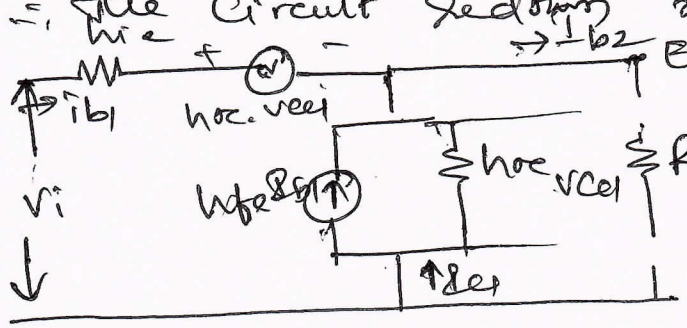
Analysis of first stage

i/p resistance of second stage R_{i2} is high

$\therefore h_{ie} \cdot R_{i2} < 0.1$ does not occur. Hence exact analysis



$\therefore$ The circuit redrawn making Collector Common



$$\therefore A_{i1} = \frac{I_{b2}}{I_{b1}} = \frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{e1})$$

$$\therefore I_{e1} = -h_{fe}.I_{b1} + h_{oe}.V_{ce1}.$$

$$= -h_{fe} I_{b1} + h_{oe}(-I_{b2}.R_{L1})$$

$$= h_{fe}.I_{b1} + h_{oe} I_{e1} . R_{L1}$$

Substitute I_{e1} in eq^n (4), we get

$$\therefore I_{e1} = -(I_{b1} + h_{fe}.I_{b1} + h_{oe}.I_{e2}.R_{L1}) = -I_{b1} - h_{fe}.I_{b1} - h_{oe}.I_{e1}.R_{L1}$$

$$-\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}.R_{L1}} \qquad (R_{L1} = (1+h_{fe})\, R_E)$$

$$\therefore A_{i1} = \frac{-I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe}).R_E} \qquad (5)$$

— 03 m

Input resistance $R_i = Z_i$

Applying KVL to the outer loop

$$V_i - I_{b1}.h_{ie} - h_{re}.V_{ce1} + V_{ce1} = 0$$

$$V_i = I_{b1} h_{ie} + h_{re}.V_{ce1} - V_{ce1}$$

The term $h_{re}.V_{ce1}$ is negligible

$$= I_{b1} h_{ie} - (-I_{b2}.R_{L1})$$

$= I_{b1} \cdot h_{ie} + I_{b2} \cdot R_4$

33

$\therefore R_{i1} = h_{ie} + A_{i1}(1+h_{fe}) R_E$ — (6)

$\therefore R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{(1+h_{fe})(1+h_{fe}) \cdot R_E}{1+h_{oe} \cdot h_{fe} R_E}$ — (7)

$\therefore R_{i1} = \frac{(1+h_{fe})^2 \cdot R_E}{1+h_{oe} h_{fe} \cdot R_E}$ $\left(\because h_{ie} < \frac{(1+h_{fe})^2 R_E}{1+h_{oe} \cdot h_{fe} \cdot R_E}\right)$

Current gain $A_i = A_{i1} \times A_{i2} = \frac{(1+h_{fe})}{1+h_{oe}(1+h_{fe})R_E} \times (1+h_{fe})$

$A_i = \frac{(1+h_{fe})^2}{1+h_{oe}(1+h_{fe}) \cdot R_E}$ — (10)

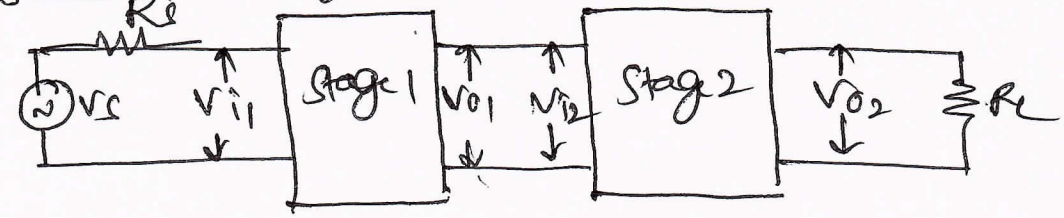
— 03

5b Need of Cascading

For faithfull amplification amplifier should have desired voltage gain, current gain. It should match the source and output impedance with the load. This amplification cannot be achieved with the single stage. In such situation one stage are cascaded with another stage, such that input and output stages provides impedance matching requirements. middle stage provides the amplification

— 03M

Two stage Cascade Amplifier: The output of the first stage is connected to the i/p of the second stage



V_{i_1} → the input of the first stage, V_{o_2} the output of the second stage. ∴ V_{o_2}/V_{o_1} the overall voltage gain of the two stage amplifier

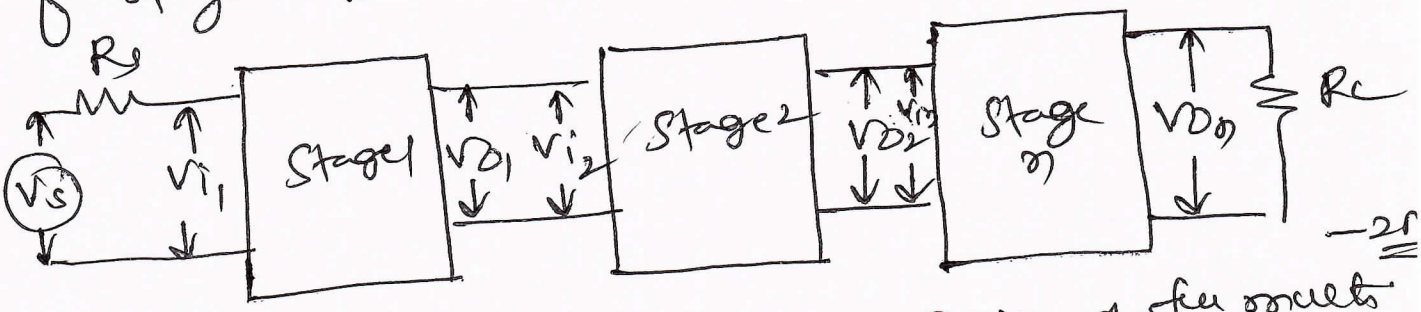
$$A_V = V_{o_2}/V_{i_1} = \frac{V_{o_2}}{V_{i_2}} \times \frac{V_{i_2}}{V_{i_1}} \Rightarrow V_{o_1} = V_{i_2}$$

$$\therefore A_V = \frac{V_{o_2}}{V_{i_2}} \times \frac{V_{o_1}}{V_{i_1}} = A_{V_2} \cdot A_{V_1} \quad \text{—(1)}$$

— 03M

voltage gain of the amplifier is the product of the voltage gain of two individual gain

5c. Cascade Amplifier: The gain of the amplifier is increased by connecting more number of stages in cascade



— 2M

The resultant voltage gain of the multi stage amplifier is the product of voltage gain of the various stages

$$\therefore A_V = A_{V_1} \cdot A_{V_2} \cdots A_{V_n} \quad \text{—(2)}$$

The voltage gain of the k^{th} stage is given by

$$A_{V_k} = \frac{A_{i_k} \cdot R_{L_k}}{R_{i_k}}$$

R_{Lk} is the effective load resistance of the k^{th} stage and R_{ik} is the i/p impedance of the k^{th} stage

— 2M

39 General characteristics of Negative feedback amplifier

A → used to represent the transfer gain without feedback

Af → used to represent transfer gain with feedback

$A = \frac{X_o}{X_i}$ and $A_f = \frac{X_o}{X_s}$

X_o → output voltage or output current

X_i → Input voltage or Input current

X_s → Source voltage or source current

The negative feedback relation between X_i and X_s

$X_i = X_s + (-X_f)$, where X_f = feedback voltage or feedback current, $A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$

Dividing by X_i to numerator and denominator

$A_f = \frac{X_o/X_i}{(X_i + X_f)/X_i} = \frac{A}{1 + X_f/X_i}$ $\left(\because A = \frac{X_o}{X_i}\right)$

$= \frac{A}{1 + (X_f/X_o)(X_o/X_i)}$

$A_f = \frac{A}{1 + \beta A}$ $\left(\because \beta = \frac{X_f}{X_o}\right)$ — 02M

β → feedback factor

The voltage amplifier, gain with Negative feedback is

$A_{vf} = \frac{A_v}{1 + A_v} \times \frac{X_f}{\beta X_o}$

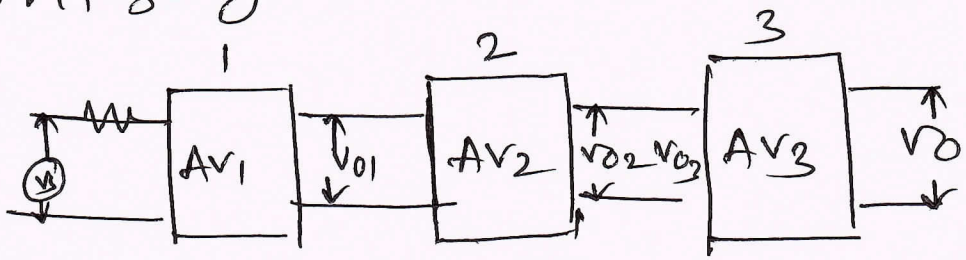
A_v → Open loop gain or gain without feedback

β → feedback factor. 02M

6b $A_{V_1} = 10$, $A_{V_2} = 20$, $A_{V_3} = 40$

Overall voltage gain

voltage gain in dB



— 02M

$$\therefore A_V = \frac{V_0}{V_{03}} \times \frac{V_{02}}{V_{01}} \times \frac{V_{01}}{V_i} \quad \begin{bmatrix} V_{02} = V_{i3} \\ V_{01} = V_{i2} \\ V_{01} = V_i \end{bmatrix} \text{—2M}$$

$$= A_{V_3} \times A_{V_2} \times A_{V_1}$$

$$= 40 \times 20 \times 10$$

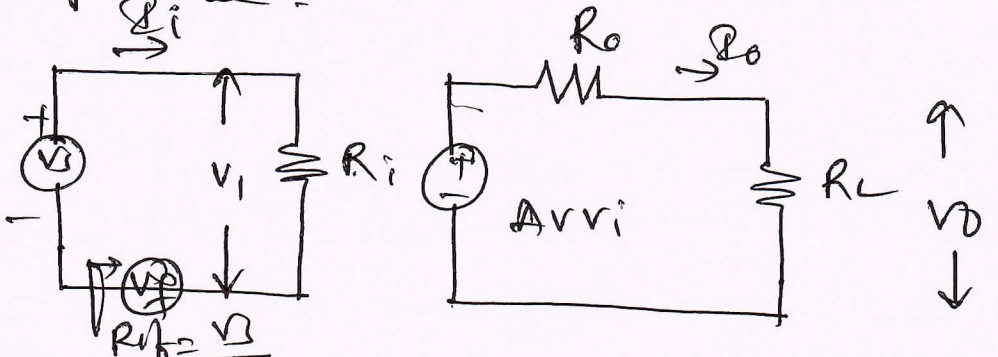
$$A_V = 8000 \quad \text{—2M}$$

$$dB = 20 \log 8000$$

$$= 20 \times 3.9$$

$$= 78.06 \text{ dB} \quad \text{—2M}$$

6c Voltage series feedback expression for outp
impedance:



— 2M

Voltage series topology with amplifier o/p ref
ced by Thevenins model Av represents the
open circuit voltage gain taking Ro into acco
The i/p resistance with feed-back given by

$$R_{if} = \frac{V_s}{I_i} \quad \ldots (1)$$

— 02M

Applying KVL to the input side, we get

$$V_s = I_i \cdot R_i - V_f = 0$$

$$\therefore V_s = I_i R_i + V_f = I_i R_i + \beta V_o$$

The o/p voltage Vo is given by

$$V_o = \frac{A_{V_o} \cdot V_i \cdot R_L}{R_o + R_L} = A_v I_i R_i = A_v \cdot V_i$$

— 2M

$$\& A_v = \frac{V_o}{V_i} = \frac{A_{V_o} \cdot R_L}{R_o + R_L}$$

$$\therefore V_s = I_i \cdot R_i + \beta A_v I_i \cdot R_i$$

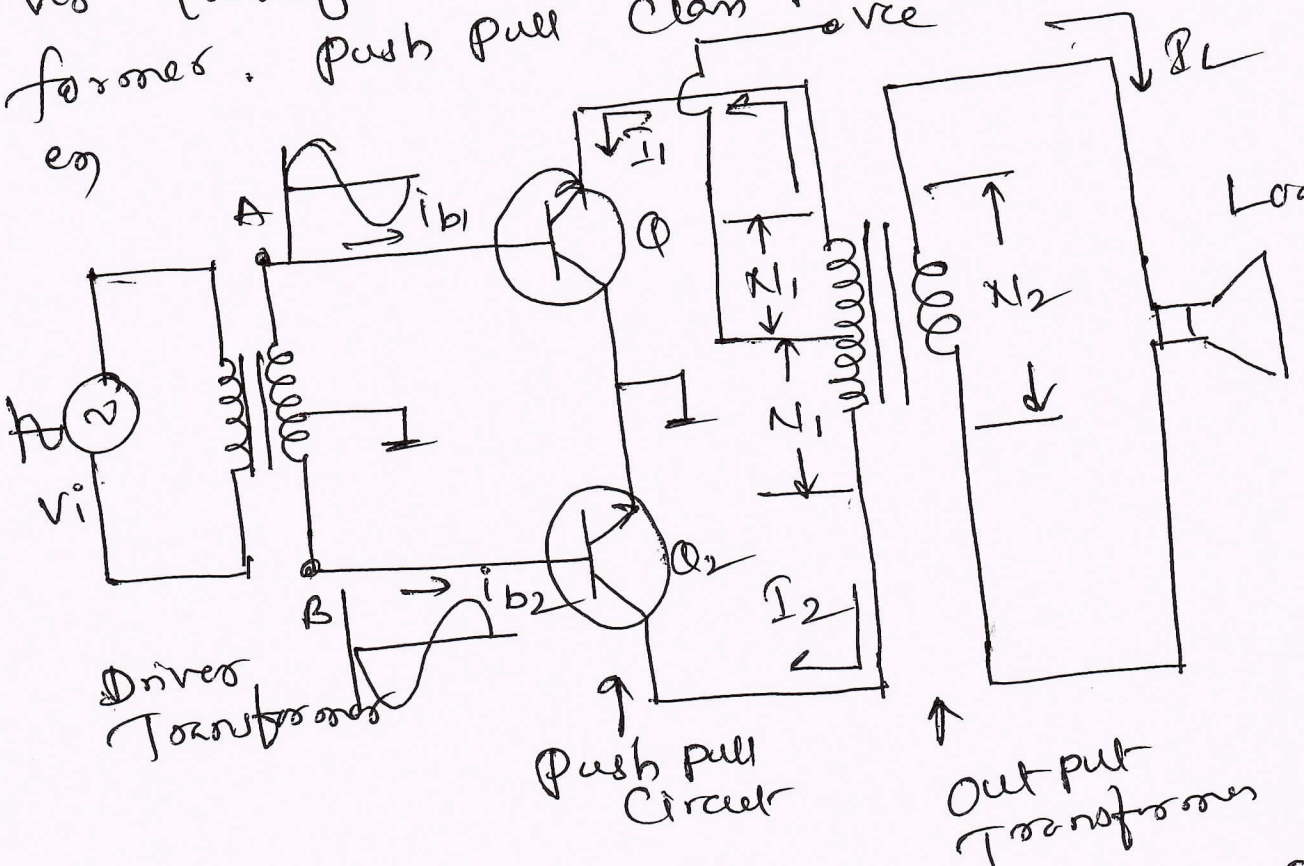
$$\frac{V_i}{I_i} = R_i + \beta A_v \cdot R_i$$

$$R_{if} = R_i + (1 + \beta A_v)$$

— 2M

Class B push pull Amplifier

push pull requires two transformers one as I/
transformer called driven transformer and ano
Connect to the load called as o/p transformer
The i/p signal is applied to the primary of dri
ver transformer. Both are centre tapped trans
former. Push pull Class B amplifier circuit is gi
en



— 03m

Q_1 and Q_2 are n-p-n transistor. Both t
transistor are Common Emitter Configuratio
The driver transformer drives the Circu
i/p applied to the primary transformer
centre tap of the secondary transformer
is grounded. Centre tap of the primary of
output transformer is connected to the supp

Voltage V_{CE}

Q_1 conducts for positive half cycle and produce positive half cycle across the load. Q_2 conducts for the Negative half cycle producing Negative half cycle across the load

DC power I/P $\rightarrow$ $P_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$

$\therefore P_{DC} = V_{CE} \times I_{dc} = \frac{2I_m}{\pi} \times V_{CE}$ — 2N

AC power output $V_{rms} = \frac{V_m}{\sqrt{2}}$, $I_{rms} = \frac{I_m}{\sqrt{2}}$

$P_{ac} = V_{rms} \cdot I_{rms} = I^2_{rms} \times R_L' = \frac{V^2_{rms}}{R_L'}$

using the peak value $\therefore P_{ac} = \frac{I_m \cdot V_m}{\sqrt{2} \cdot \sqrt{2}} = \frac{I_m}{2}$

$P_{ac} = \frac{I_m^2 R_L'}{2} = \frac{V_m^2}{2R_L'}$ — 2N

Efficiency $\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\frac{I_m V_m}{2}}{\frac{2}{\pi} \cdot V_{CE} I_m} \times 100$

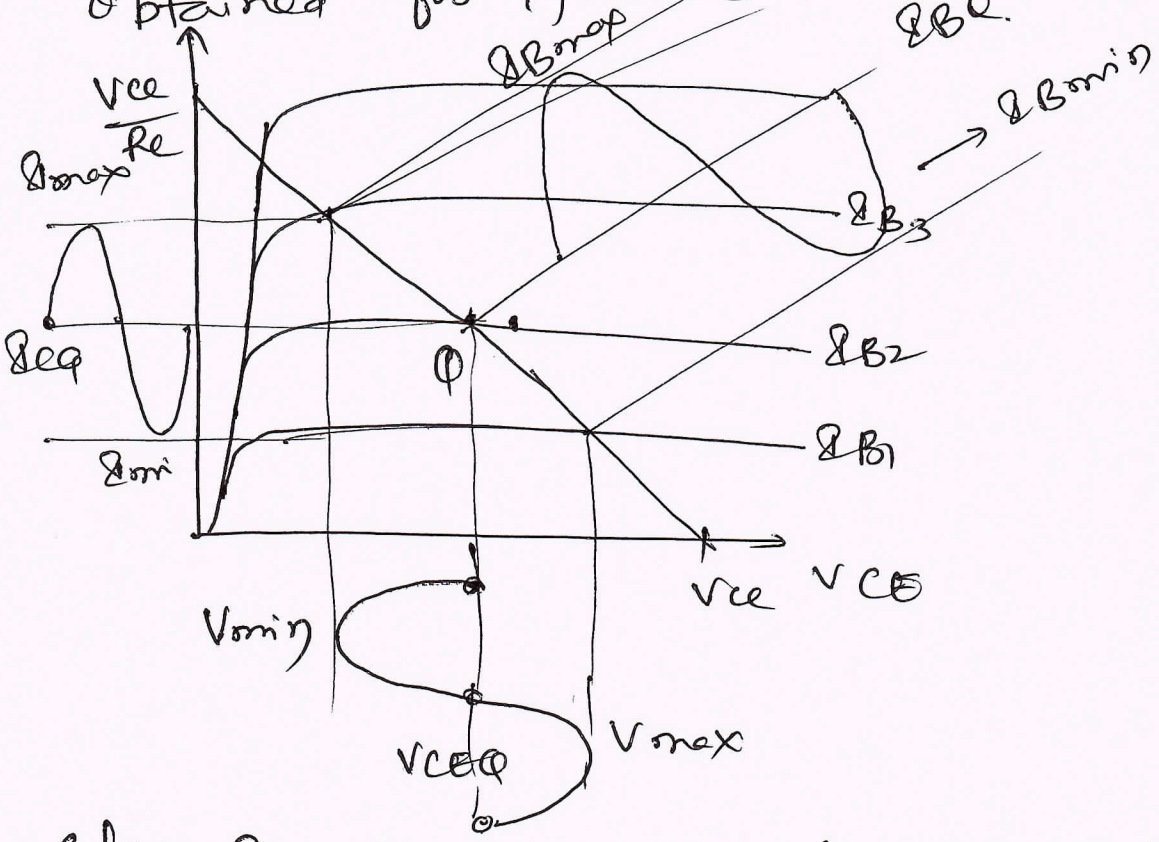
$\therefore \% \eta = \frac{\pi}{4} \cdot \frac{V_m}{V_{CE}} \times 100$ — 1m

maximum efficiency : $V_m = V_{CE}$ for maximum η $\therefore \% \eta = \frac{\pi}{4} \times \frac{V_{CE}}{V_{CC}} \times 100 = 78.5\%$

The maximum possible value of push pull Class B amplifier is 78.5%.

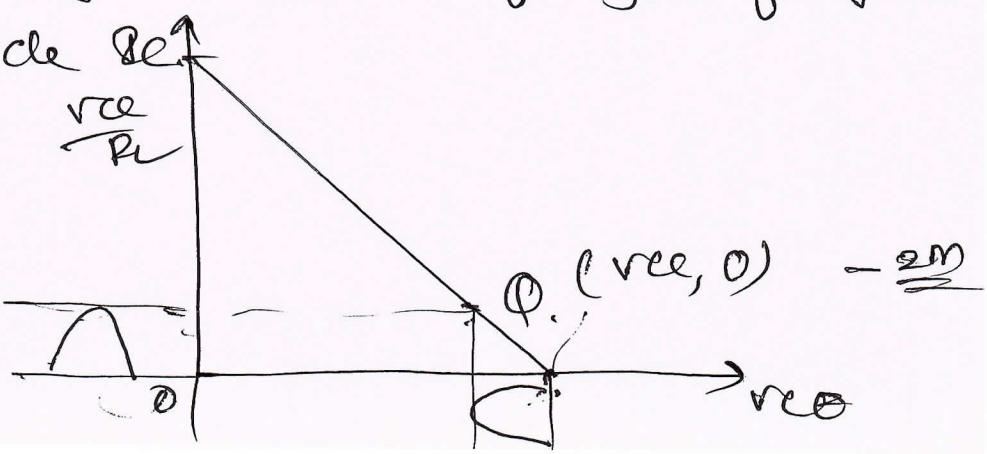
7b Classification of power Amplifiers.

Class A : The power amplifier is said to be class A amplifier if the Q point and i/p signal are selected such that output signal is obtained for full cycle



— 2M

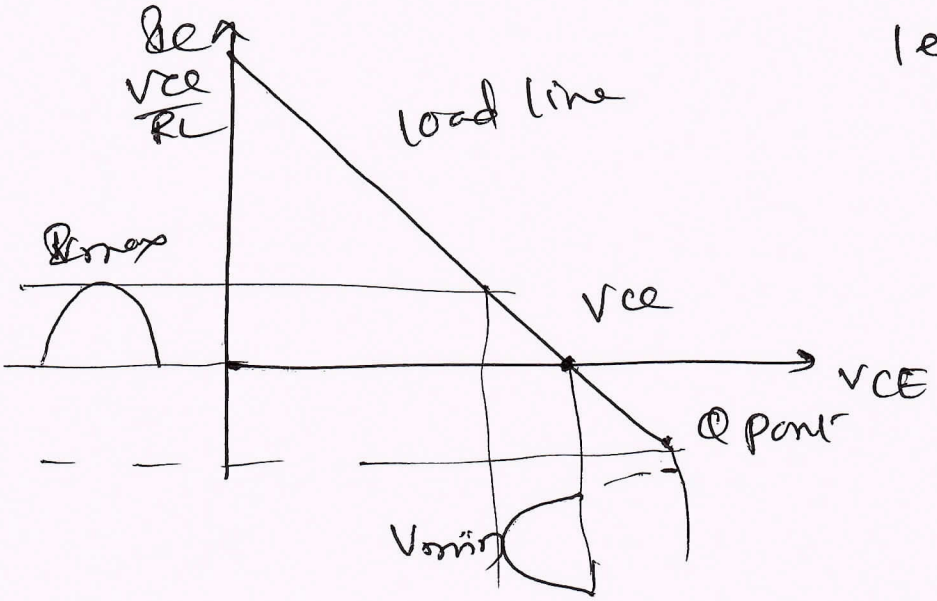
Class B : Power amplifier is said to be class B amplifier. If the Q point and i/p signal are selected. such that o/p is obtained only for the one half cycle for the full input cycle



— 2M

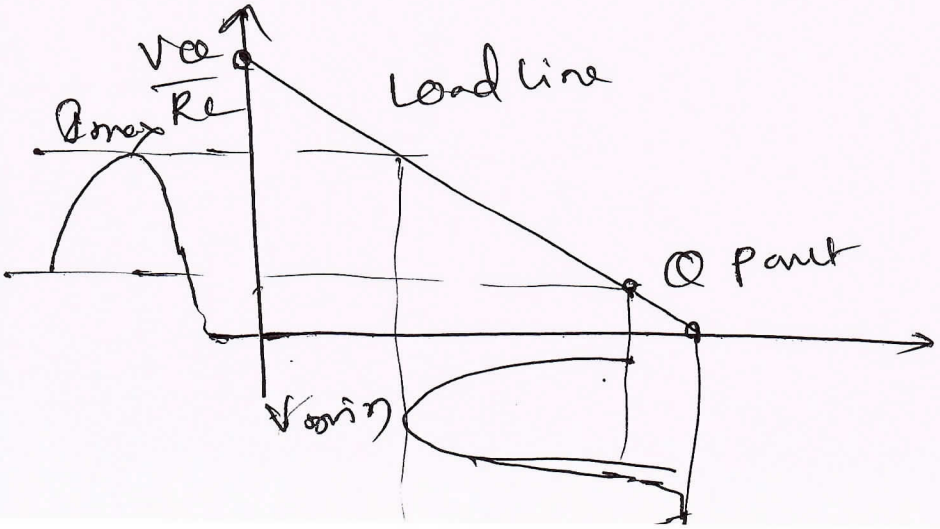
Class C amplifier : The power amplifier is said to be class C amplifier. If the Q point and i/p signals are selected such that o/p signals is obtained for less than half cycle for full input cycle.

Collector current flow less than 180°



— 2M

Class AB : The power amplifier is said to be class AB amplifier. If the Q point and i/p signals are selected such that the o/p signal obtained more than 180° but less than 360° for full i/p cycle



2M

7C A Class AB - push pull amplifier $V_{CC} = 25V$, provid 22V peak signal, to 8Ω load. Calculate. Circuit efficiency and power dissipation

$V_m = 22V$, $V_{CC} = 25V$, $R_L = 8\Omega$

$$P_{ac} = \frac{V_m \times V_{CC}}{\pi} = \frac{V_m^2}{2R_L'} = \frac{(22)^2}{2\times 8} = 30.25$$

$$P_{DC} = \frac{2}{\pi} \cdot V_{CC} \cdot V_m \quad -2m$$

$$\therefore \%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{30.25}{\frac{2}{\pi} \times V_{CC} \times \frac{V_m}{R_L}}$$

$$= \frac{30.25}{\frac{2}{\pi} \times 25 \times \frac{22}{8}} = \frac{30.25}{43.767} \times 100$$

$$\%\eta = 0.6911 \times 100 = 69.11\%$$

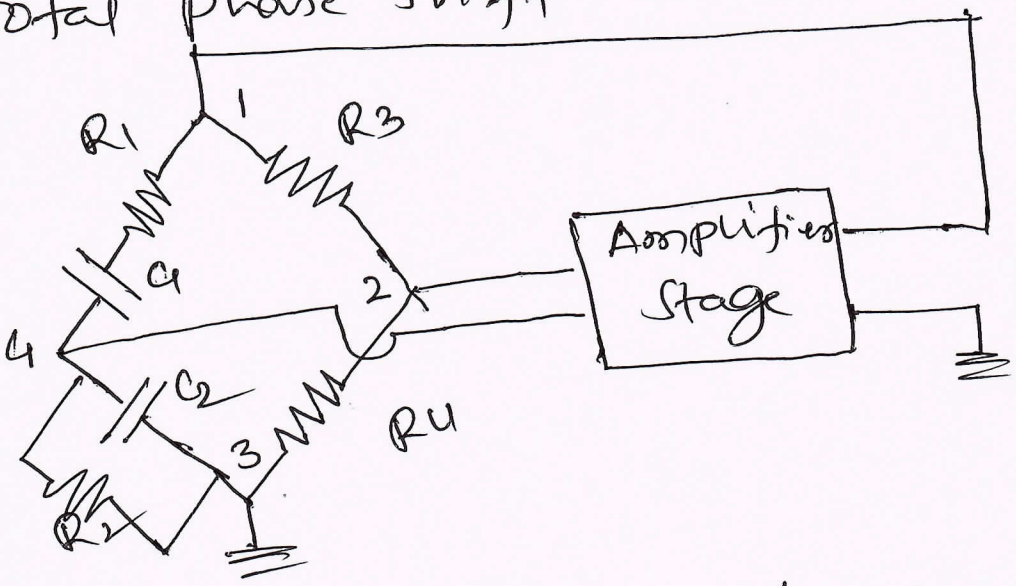
power dissipation P_d

$$P_d = P_{DC} - P_{ac} = 43.767 - 30.25$$

$$= 13.512 \quad -3m$$

Q9 Wein Bridge Oscillator : Generally amplifier stage introduces the 180° phase shift and feed back introduces 180° additional phase shift obtain the phase shift of 360° (2π radians around loop.

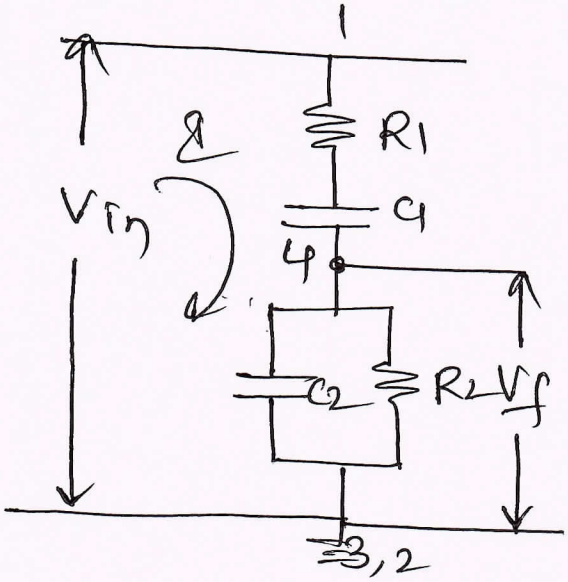
Wein Bridge oscillator uses non inverting amplifier does not provide the phase shift the total phase shift is zero or 2π. The total phase shift around the loop is zero



The o/p of amplifier is applied between the terminal 1 & 3 which is the i/p to the feed back N/W & the terminal 2 and 4 are the o/p of feed back N/W

Two arm of the bridge R_1, C_1 in series and R_2, C_2 in parallel are called freque

Sensitive qoom. These two decides the freq of the oscillator. feed back n/w is called Lead-lag n/w.



$$\therefore Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1+j\omega R_1 C_1}{j\omega C_1}$$

$$Z_2 = R_2 \| \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$= \frac{R_2}{1+j\omega R_2 C_2} \quad \text{---(1)}$$

Replacing $j\omega = s$

$$Z_1 = \frac{1+sR_1C_1}{sC_1}, \quad Z_2 = \frac{R_2}{1+sR_2C_2}$$

$$\therefore I = \frac{V_{in}}{Z_1+Z_2} \quad \& \quad V_f = I \cdot Z_2 = \frac{V_{in} Z_2}{Z_1+Z_2}$$

$$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1+Z_2} \quad \text{---(2)}$$

$$\beta = \frac{\left[\frac{R_2}{1+sR_2C_2}\right]}{\left[\frac{1+sR_1C_1}{sC_1}\right] + \left[\frac{R_2}{1+sR_2C_2}\right]} = \frac{sC_1R_1}{1+s(R_1C_1+R_2C_2+C_1R_2) + s^2R_1R_2C_1C_2}$$

Replacing s by $j\omega$, $s^2 = -\omega^2$

$$\beta = \frac{j\omega C_1 R_2}{(1-\omega^2 R_1R_2C_1C_2) + j\omega(R_1C_1+R_2C_2+C_1R_2)}$$

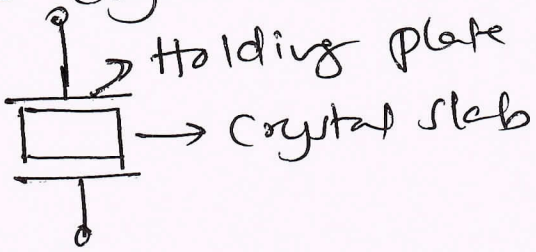
Rationalizing and imaginary part zero

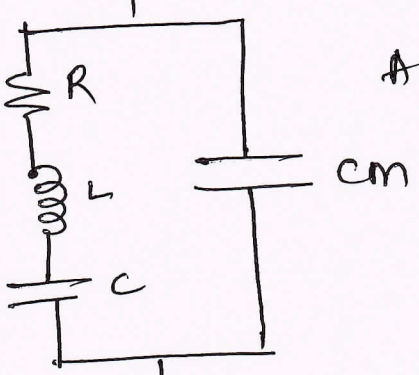
$$\omega^2 = \frac{1}{R_1R_2C_1C_2} \Rightarrow \omega = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$f_2 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi RC} \quad \text{---4M}$$

8b Crystal oscillator

Crystal oscillators are synthetically manufactured exhibiting piezoelectric effect. Under the influence of mechanical pressure the voltage generated across the opposite faces of the crystal by the applied mechanical force. The crystal to vibrate. The ac voltage gets generated across it. Every crystals has its own resonating frequency. Crystal generates electrical signal of very Constant frequency. A crystal oscillator is basically tuned Circuit oscillators using Piezoelectric Crystal as its resonant tank Circuit





AC equivalent Circuit

— 04m

Capacitance existing due to the metal plates separated by a dielectric crystal slab. Called mounting Capacitance denoted by Cm or C
Internal frictional losses denoted by R.
Inertia represented by an inductance L
In vibration Condition, the Stiffness represented by the capacitor C. The overall equivalent Circuit is shown in above fig

∴ The RLC form resonating circuit

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}$$

Q → Quality factor of Crystal

$$Q = \frac{\omega L}{R}$$

Q is high – 20,000

$\therefore \sqrt{\frac{Q^2}{1+Q^2}}$ approaches to unity

$$\therefore f_r = \frac{1}{2\pi\sqrt{LC}}$$ — 4M

The crystal frequency inversely proportional to the thickness of the crystal

$f \propto \frac{1}{t}$, for high frequency thickness is small. Crystal oscillator used upto 200 to 300 kHz

L = 0.334 H, C = 0.065 PF and R = 5.5 kΩ

$$\therefore f_r = \frac{1}{2\pi}$$

$$Q = \frac{\omega L}{R} = \frac{2\pi f \cdot L}{R}$$

for $\sqrt{\frac{Q^2}{1+Q^2}} = 1$

$$\therefore f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.334 \times 0.065\,pF}}$$

$$= \frac{1}{3.142\sqrt{0.04 \times 10^{-12}\,F}}$$

$$= 795.67\ kHz$$ — 2M

9a N- Channel JFET

JFET of low frequency small signal. Drain to source current of JFET is controlled by gate to source voltage. The change in the drain current due to change in gate to source voltage

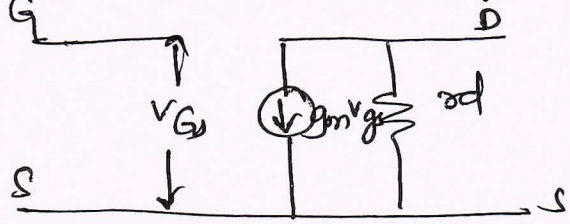
$\therefore \Delta I_d = g_m \Delta V_{GS}$ —①

The relation between output and input is β in case of BJT and g_m in case FET

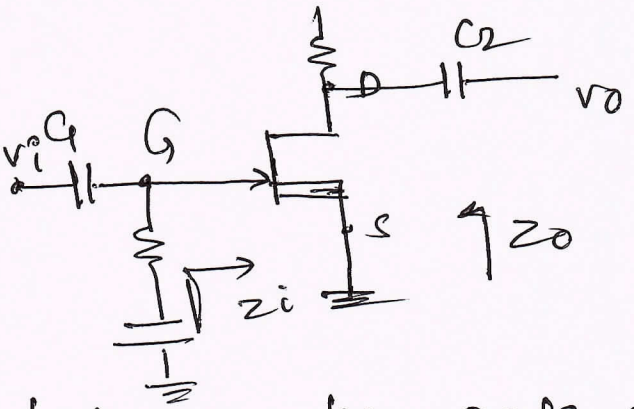
The another important parameter of drain resistance r_d

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{Constant}} \quad —②$$

The output impedance Z_o



CS Common source



— 04m

Input is applied between the gate and source and output is taken from the drain and source the Common source fixed bias is shown in fig. Coupling capacitor C_1 and C_2 are used to isolate the dc from the applied ac sig. ac acts as a short circuit for the ac analysis.

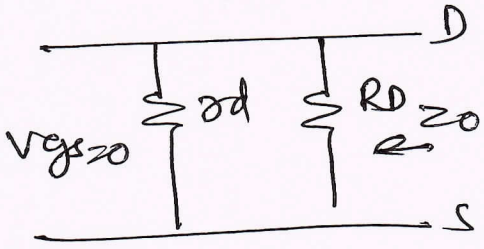
All Capacitors and dc supply voltages are to be Short Circuits and JFET with its low frequency equivelent Circuit

The i/p impedence and the o/p impedence and voltage gain of the above

Input impedence $Z_i = R_G$

output impedence $Z_o =$, Set $V_i = 0$, $V_{gs} = 0$

hence $g_m V_{gs} = 0$



$g_m \cdot V_{gs} = 0$, the Current source to be replaced by an open Circuit. The output impedence

$Z_o = R_D \| r_d$, resistance r_d is sufficiently larger Compared to R_D ($r_d >> R_D$)

$\therefore Z_o = R_D$

voltage gain $A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

From the Circuit $V_o = -g_m V_{gs} \cdot (r_d \| R_D)$

$V_i = V_{gs}$ $\therefore V_o = -g_m \cdot V_i (r_d \| R_D)$

$\therefore A_V = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$

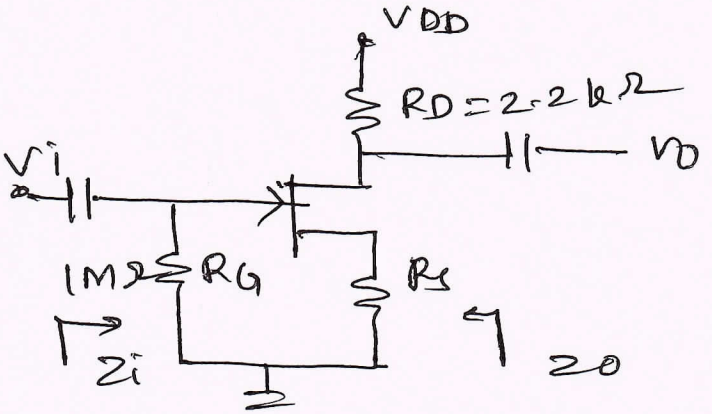
if $r_d >> R_D$ $\therefore A_V = -g_m \cdot R_D$

Negative sign indicates there is Phase shift of 180° between input and output

06 m

9b - Self bias FET $V_{DD} = 12V$, $R_D = 2.2k\Omega$
$R_G = 1M\Omega$, $R_S = 1k\Omega$ $I_{DSS} = 8mA$, $V_p = -4$

(i) $V_{GS} = ?$ (ii) $I_D = ?$ (iii) $V_{DS} = ?$ (iv) $V_S = ?$ (v) $V_G = ?$
(vi) $V_D = ?$



(i) g_m

$\therefore g_{mo} = \frac{2I_{DSS}}{|V_p|} = \frac{2 \times 8}{4}$

$= 4 \times 10^{-3} = 4m$

$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_p}\right)$

$= 4 \times 10^{-3}\left(1 - \left(\frac{-8}{-4}\right)\right)$

$= 4 \times 10^{-3} \times 3$ [$V_{gs} = -8$

$= 12 \times 10^{-3}$ $= -8 \times$

$= -8$

— 4m

$V_i =$

(ii) $I_D = I_{DSS}\left(1 + \frac{I_D \cdot R_S}{V_p}\right)^2$

$= 8 \times 10^{-3}\left(1 + \frac{I_D \cdot R_S}{V_p}\right)^2$

$I_D = 8 \times 10^{-3} - 4I_D + 500 I_D^2$

$\therefore 500 I_D^2 - 5I_D + 8 \times 10^{-3} = 0$

$\therefore I_D = 8mA$ or $2mA$

I_D can not have I_{DSS}, $\therefore I_D = 2mA$

$V_{GSQ} = -I_D R_S = -2 \times 10^{-3} \times 1 \times 10^3 = -2V$

(iv) $\therefore V_{GS} = V_S = I_D \cdot R_S = -2 \times 10^{-3} \times 1 \times 10^3 = 2V$

(iii) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 12 - 2 \times 10^{-3}(2.2 \times 10^3 + 1 \times 10^3) = 12 - 6.4 = 5.6V$

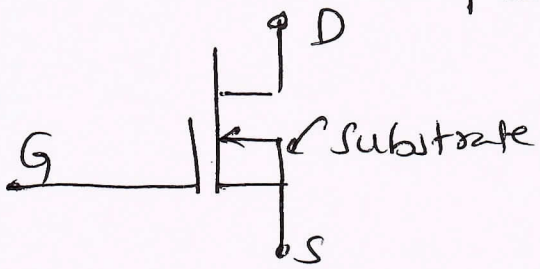
$\therefore V_D = V_{DS} + V_S = 5.6 + 2 = 7.6V$ — 6m

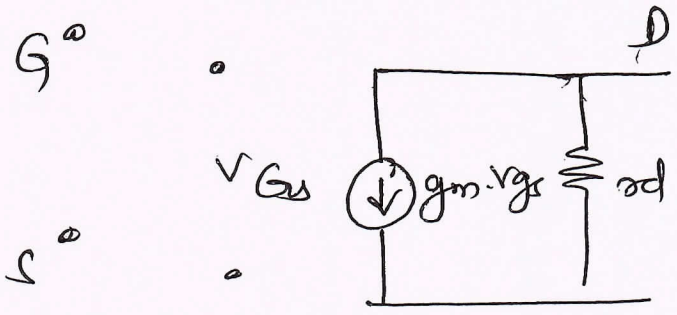
$V_G = 0$

$\therefore V_{GS} = -2$, $I_D = 2mA$, $V_{DS} = 5.6V$, $V_S = 2V$

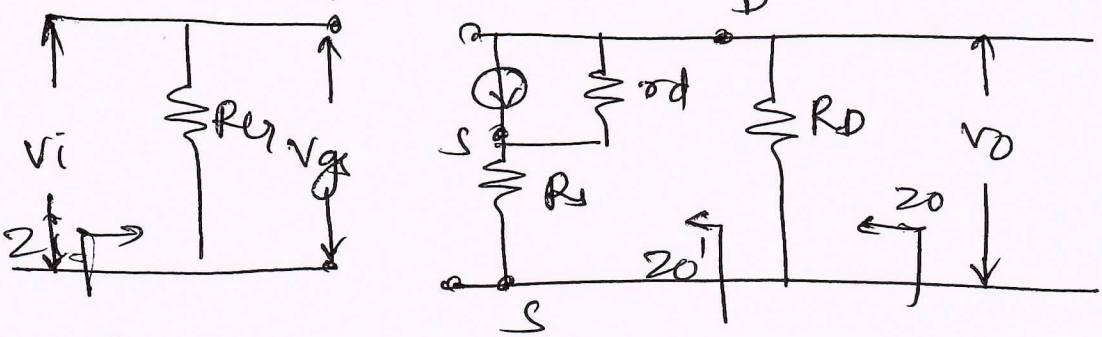
$V_G = 0$, $V_D = 7.6V$

10a n-channel depletion layer MOSFET





It is exactly similar to the JFET. The only difference is that the depletion layer MOSFET V_{GS} is positive for n-channel and Negative for P channel MOSFET



— 04m

∴ Input impedance $Z_i = R_G$

output impedance $Z_o = Z_o' \| R_D$

$\therefore Z_o' = \frac{V_O}{I_d} \Big|_{V_i=0}$

Apply KVL to the o/p Circuit

$V_O = (I_d - g_m \cdot V_{gs}) r_d + I_d \cdot R_S$

Applying KVL to the i/p Circuit

$V_{gs} = V_m - I_d \cdot R_S \quad , \quad V_m = 0$

$\therefore V_{gs} = -I_d \cdot R_S$

Substitute the value of V_{gs}

$V_O = ([(I_d - g_m(-I_d \cdot R_S)] r_d) + (I_d \cdot R_S) = I_d(r_d + g_m R_S r_d + R_S)$

$Z_o' = \frac{V_O}{I_d} = r_d + g_m R_S \cdot r_d + R_S$

— 02m

$\mu = g_m r_d$

$\therefore Z_o' = r_d + R_s(\mu+1)$

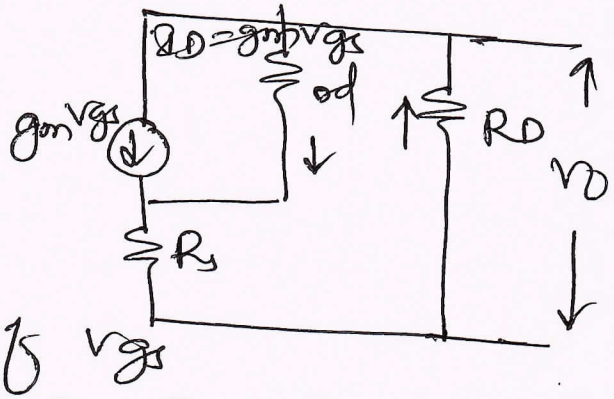
$\therefore Z_o = Z_o' \| R_D = ([r_d + R_s(\mu+1)]) \| R_D$

Voltage gain $A_v = \frac{v_o}{v_i}$, $v_o = -I_d \cdot R_D$

Apply the KVL to the output circuit

$(I_d - g_m v_{gs}) r_d + I_d \cdot R_s + I_d \cdot R_D = 0$

$v_{gs} = v_{in} - I_d \cdot R_s$



Substituting value of v_{gs}

$\therefore I_d (r_d + R_s + R_D + g_m R_s \cdot r_d) = g_m v_i r_d$

$\therefore I_d = \frac{g_m v_i r_d}{r_d + R_s + R_D + g_m R_s \cdot r_d}$,

$\therefore v_o = \frac{-g_m v_i r_d}{r_d + R_s + R_D + g_m R_s \cdot r_d}$

$A_v = \frac{v_o}{v_i} = \frac{-g_m R_D}{1 + g_m \cdot R_s + \frac{R_s + R_D}{r_d}}$

$r > R_s + R_D$

$\therefore A_v = \frac{v_o}{v_i} = \frac{-g_m R_D}{1 + g_m \cdot R_s}$ — 04m

10 b Expression for the V_{GS}, I_D, V_{DS} and V_S for voltage divider

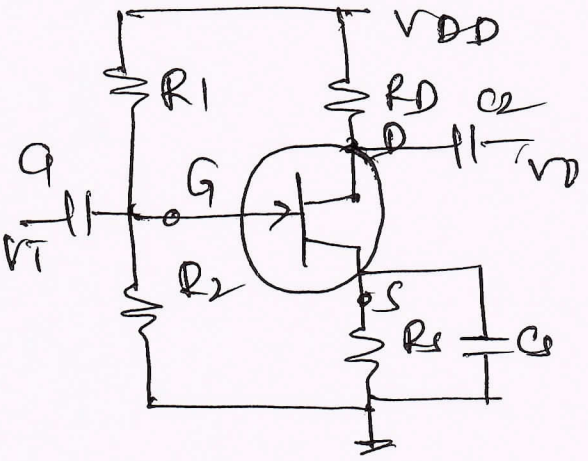
n- Channel JFET with voltage divider bias

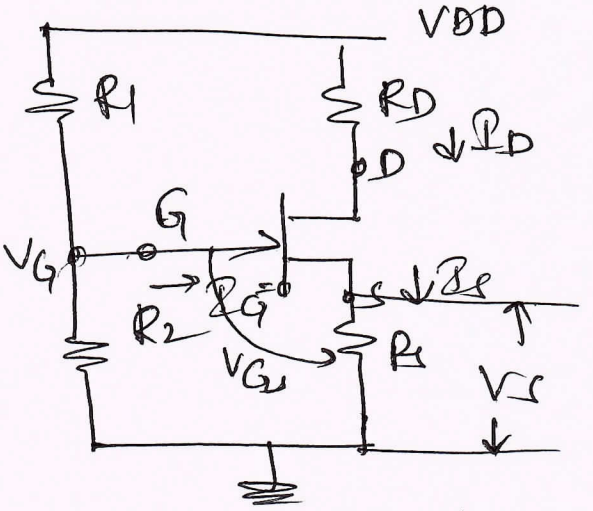
Voltage at the source of JFET is more positive than the voltage at the gate in order to keep the gate source junction reverse biased

The source voltage is $V_S = I_D \cdot R_S$

The gate voltage is set by R_1 and R_2 as expressing the voltage divider formula.

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) \cdot V_{DD} \quad \because I_G = 0$$





03

DC analysis: Apply the KVL to the i/p Circuit

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S \cdot R_S = V_G - I_D \cdot R_S \quad (I_D = I_S)$$

$$\therefore V_{GS} = V_G - I_D R_S$$

Apply the KVL to the output Circuit

$$V_{DS} + I_D \cdot R_D + V_S - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D \cdot R_S \quad \text{— 03}$$

$= V_{DD} - I_D(R_D + R_S)$

Q. point of the JFET amplifier using the voltage divider is given by

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and $V_{DSQ} = V_{DD} - I_D \cdot (R_D + R_S)$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$V_S = I_D \cdot R_S$ —— 4m

For valid I_D V_{DS} must be positive

12-03-2022
(K.M. Wadekhaft)

15/03/2022

15/3/22
Dean, Academics.