CBCS SCHEME

USN | | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, July/August 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Define combinational logic circuit and place the following equation into the proper canonical form:
$P = f(a, b, c) = ab' + ac' + bc$ **(04 Marks)**

b. Obtain minimal expression using k-map for the following incompletely specified function:
$F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw the circuit diagram using basic gates. **(06 Marks)**

c. Minimize the expression using Quine Mecluskey method.
$Y = \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}\overline{D} + AB\overline{C}D + A\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D}$ **(10 Marks)**

2 a. Place the following equations into the proper canonical form:
i) $G = f(w, x, y, z) = \overline{w}x + y\overline{z}$
ii) $T = f(a, b, c) = (a + \overline{b})(\overline{b} + c)$ **(04 Marks)**

b. Obtain minimal logical expression for the given maxterm expression using K-map $f(a, b, c, d) = \pi M(0, 1, 4, 5, 6, 7, 9, 14) \cdot \pi d(13, 15)$. **(06 Marks)**

c. Obtain all the prime implicants of the following Boolean function using Quine-Meckluskey method
$f(a, b, c, d) = \sum(0, 2, 3, 5, 8, 10, 11)$. Verify the result using K map technique. **(10 Marks)**

3 a. Draw the circuit for 3 to 8 decoder and explain. **(08 Marks)**

b. Implement the following Boolean function using 4:1 multiplexer.
$F[A, B, C, D] = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. **(06 Marks)**

c. A combinational circuit is defined by the functions $F_1 = \sum m(3, 5, 7)$, $F_2 = \sum m(4, 5, 7)$. Implement the circuit with a programmable logic array having 3 inputs, 3 product terms and two outputs. **(06 Marks)**

4 a. Draw the key pad interfacing diagram to a digital system using 10-line decimal to BCD encoder and explain. **(06 Marks)**

b. Explain Look-Ahead carry adder with neat diagram and relevant expression. **(06 Marks)**

c. Design 2-bit comparator using gates. **(08 Marks)**

5 a. Explain the operation of a switch debouncer using S-R. Latch with the help of circuit and waveforms. **(06 Marks)**

b. Find characteristic equations for S-R and T. Flip flops with the help of function tables and explain. **(06 Marks)**

c. Explain the working principle of 4-bit synchronous binary counts. **(08 Marks)**

6 a. Draw the logic diagram, functional table and timing diagram of master-slave JK flip flop and explain briefly. **(10 Marks)**

b. Explain four bit binary ripple counter with logic and timing diagram. **(10 Marks)**

7 a. Design mod-6 synchronous counter by using JK flip-flop, with excitation table. **(10 Marks)**

b. Draw and explain Mealy and Moore sequential circuit model and compare mealy and Moore circuit models. **(10 Marks)**

8 a. Design a Mod-6 synchronous counter using clocked T Flip-Flop. **(10 Marks)**

b. Construct the transition table, state table and state diagram for the sequential circuit shown in Fig.Q.8(b). **(10 Marks)**

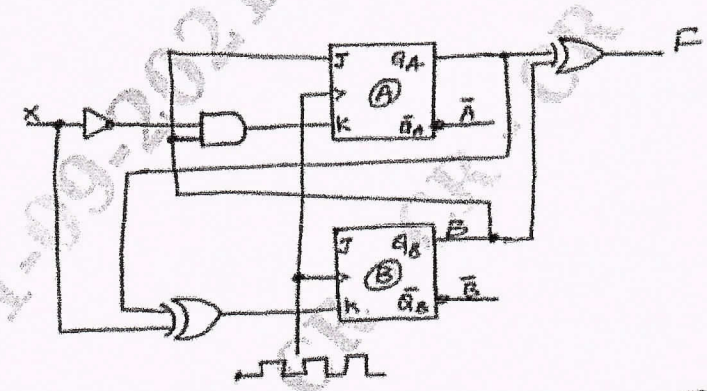

Fig.Q.8(b)

9 a. Design and draw Mealy model of sequential detector circuit to detect the pattern 101. **(10 Marks)**

b. Draw the block diagram of serial adder with accumulator and explain its working operation. **(10 Marks)**

10 a. State the guidelines for construction of state graph. **(06 Marks)**

b. Draw the block diagram of binary multiplier and explain its working principle. **(08 Marks)**

c. Draw and explain the operation of FPGA implementation of a parallel adder with accumulator. **(06 Marks)**

* * * * *

Subject Name:- DSD

Subject Code:- 18EC34.

June / August - 2021

Scheme & Solution.

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15.03.2022
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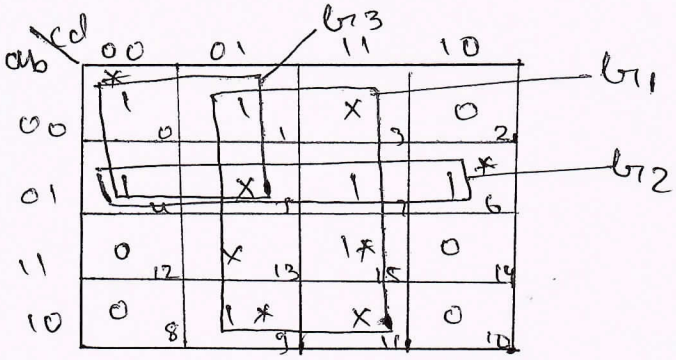
1) a) Define combinational logic circuit and place the following equation into the proper canonical form. $P = (a\bar{b} + a\bar{c} + bc)$

→ Combinational circuit is a circuit whose output at anytime is purely determined by inputs at that time.

$$P = f(a,b,c) = a\bar{b} + a\bar{c} + bc$$
$$= a\bar{b}(c+\bar{c}) + a\bar{c}(b+\bar{b}) + (a+\bar{a})bc$$
$$= a\bar{b}c + a\bar{b}\bar{c} + ab\bar{c} + a\bar{b}\bar{c} + abc + \bar{a}bc$$

4M

b) Obtain minimal expression using k-map for the following incompletely specified function $F(a,b,c,d) = \sum m(0,1,4,6,7,9,15) + \sum d(3,5,11,13)$ & draw circuit diagram using basic gates.

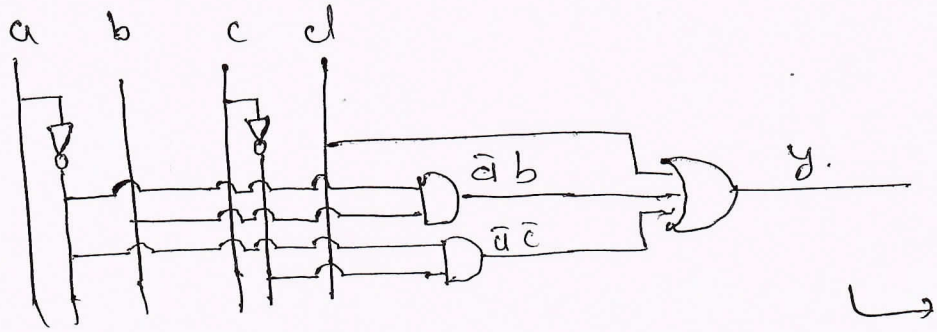


→ 2M

Group no.	prime implicant	essential P.I	epi cell no.
b_1	d	d	{9, 15}
b_2	$\bar{a}b$	$\bar{a}b$	{6}
b_3	$\bar{a}\bar{c}$	$\bar{a}\bar{c}$	{0}.

→ 2M

$$y = d + \bar{a}b + \bar{a}\bar{c}.$$



→ 2M

6M

c) minimize the exp^n using Quine Mccluskey method.

$Y = A\bar{B}C\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D}$

$= 0100, 0101, 1100, 1101, 1001, 0010.$

$= 4_{(4)}, 5_{(4)}, 12_{(4)}, 13_{(4)}, 9_{(4)}, 2_{(4)}$

$= \Sigma m(2, 4, 5, 9, 12, 13).$

Group	minterm	variables A B C D
1	2	0 0 1 0
	4	0 1 0 0 ✓
2	5	0 1 0 1 ✓
	9	1 0 0 1 ✓
	12	1 1 0 0 ✓
3	13	1 1 0 1 ✓
1	(4, 5)	0 1 0 –
	(4, 12)	– 1 0 0 ✓
2	(5, 13)	– 1 0 1 ✓
	(9, 13)	1 – 0 1
1	(4, 12, 9, 13)	– 1 0 –

6m

10m

Prime implicants	decimal	minterm 2 4 5 9 12 13
$B\bar{C}$	(4, 5, 12, 13)	x x Ⓧ x
$A\bar{C}D$	(9, 13)	Ⓧ x → 3m
$\bar{A}B\bar{C}$	(4, 5)	x x
$\bar{A}BC\bar{D}$	(2)	Ⓧ

$Y = B\bar{C} + A\bar{C}D + \bar{A}\bar{B}C\bar{D}.$ → 1m

2) a) Place the fllwng equations into proper canonical form

i) $f = f(w,x,y,z) = \bar{w}x + y\bar{z}$

$= \bar{w}x(y+\bar{y})(z+\bar{z}) + y\bar{z}(w+\bar{w})(x+\bar{x})$

$= (\bar{w}xy + \bar{w}x\bar{y})(z+\bar{z}) + (y\bar{z}w + y\bar{z}\bar{w})(x+\bar{x})$

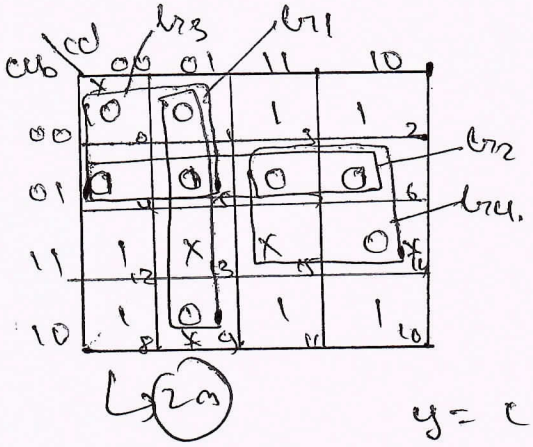
$= \bar{w}xyz + \bar{w}xy\bar{z} + \bar{w}x\bar{y}z + \bar{w}x\bar{y}\bar{z} + wxy\bar{z} + w\bar{x}y\bar{z} + \bar{w}\bar{x}y\bar{z} + \bar{w}xy\bar{z}$ → (2m)

ii) $T = f(a,b,c) = (a+\bar{b})(\bar{b}+c)$

$= ((a+\bar{b})+c\bar{c})((\bar{b}+c)+a\bar{a})$ (4m)

$= (a+\bar{b}+c)(a+\bar{b}+\bar{c})(a+\bar{b}+c)(\bar{a}+\bar{b}+c)$. → (2m)

b). Obtain minimal logical exp^n for the given maxterm exp^n using k-map $f(a,b,c,d) = \prod M(0,1,4,5,6,7,9,14) * \prod d(13,15)$.



→ (2m)

group no.	Prime Implicates	epi	epi cell no.
gr1	$c+\bar{d}$	$c+\bar{d}$	{0,4}
gr2	$a+\bar{b}$		
gr3	$a+c$	$a+c$	{5,7}
gr4	$\bar{b}+\bar{c}$	$\bar{b}+\bar{c}$	{14}

→ (2m)

$y = (c+\bar{d})(a+c)(\bar{b}+\bar{c})$ → (2m)

c) obtain all prime implicants of the fllwng Boolean function using Quine-McCluskey method.

$f(a,b,c,d) = \Sigma(0,2,3,5,8,10,11)$ verify using k map technique.

group	minterm	variables a b c d.
0	0	0 0 0 0 ✓
1	2	0 0 1 0 ✓
	8	1 0 0 0 ✓
2	3	0 0 1 1 ✓
	5	0 1 0 1
	10	1 0 1 0 ✓
3	11	1 0 1 1 ✓

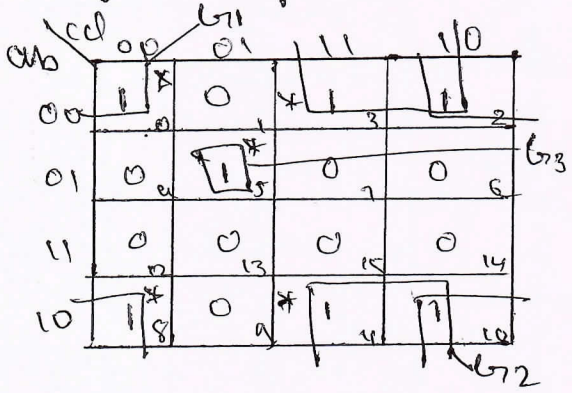
0	(0, 2) (0, 8)	0 0 — 0 — 0 0 0
1	(2, 3) (2, 10) (8, 10)	0 0 1 — — 0 1 0 + 0 — 0
2	(3, 11) (10, 11)	— 0 1 1 1 0 1 —
0	(0, 2, 8, 10) (0, 8, 2, 10)	— 0 — 0 — 0 — 0
1	(2, 3, 10, 11) (2, 3, 10, 11)	— 0 1 — ~~0~~ 0 1 —

→ 4m

PI terms (Prime implicants)	decimal	minterms. 0 2 3 5 8 10 11
$\bar{a}b\bar{c}d$	(5)	(X)
$\bar{b}\bar{d}$	(0, 2, 8, 10)	(X) x (X) x → 3m
$\bar{b}\bar{c}$	(2, 3, 10, 11)	x (X) x (X)

$\therefore y = \bar{a}b\bar{c}d + \bar{b}\bar{d} + \bar{b}\bar{c}$. → 1m

using k map.



Group no.	P.I	epi	epi cell no
G1	$\bar{b}\bar{d}$	$\bar{b}\bar{d}$	{0, 8}
G2	$\bar{b}\bar{c}$	$\bar{b}\bar{c}$	{3, 11}
G3	$\bar{a}b\bar{c}d$	$\bar{a}b\bar{c}d$	{5}

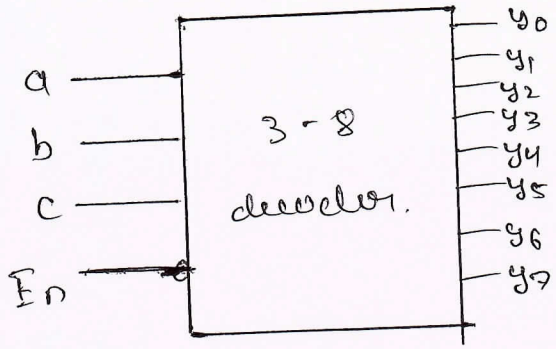
$y = \bar{a}b\bar{c}d + \bar{b}\bar{d} + \bar{b}\bar{c}$.

→ 2m

→ 10m

3) Draw the input circuit for 3-8 decoder and explain.

3-8 line decoder gives 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of the eight outputs.



→ (1m)

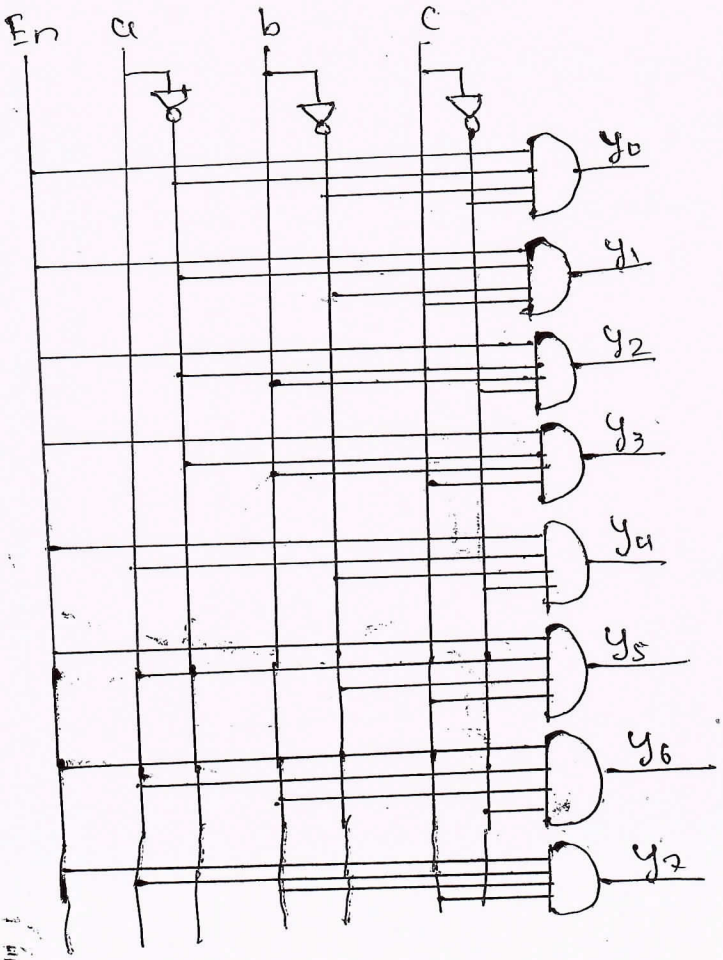
Truth table.

En	a	b	c	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

$y_0 = En\,\bar{a}\,\bar{b}\,\bar{c}$
$y_1 = En\,\bar{a}\,\bar{b}\,c$
$y_2 = En\,\bar{a}\,b\,\bar{c}$
$y_3 = En\,\bar{a}\,b\,c$
$y_4 = En\,a\,\bar{b}\,\bar{c}$
$y_5 = En\,a\,\bar{b}\,c$
$y_6 = En\,a\,b\,\bar{c}$
$y_7 = En\,a\,b\,c.$

(8m)

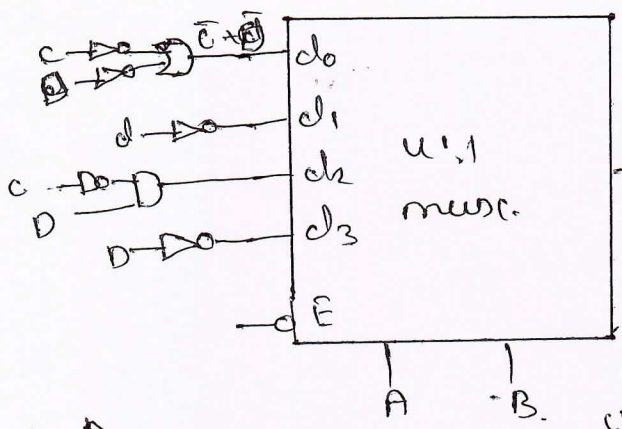
→ (3m)



→ (4m)

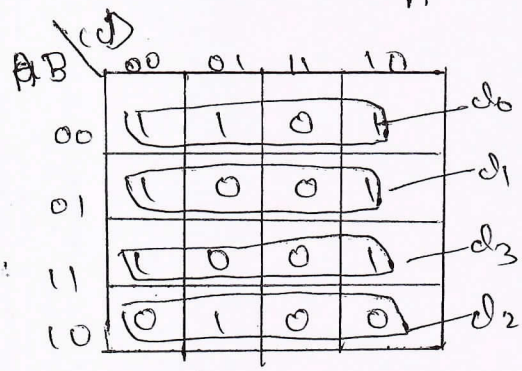
An known in the truth table, only one output is at logic 1 for each of the input combination, the input combinations can be regarded as binary numbers.

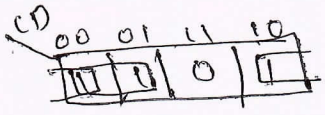
3 b) Implement the following boolean fun^n using 4:1 mux
$F(A,B,C,D) = \Sigma m(0,1,2,4,6,9,12,14)$.



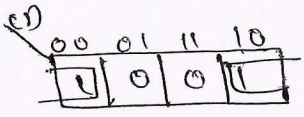
A	B	y
0	0	d_0
0	1	d_1
1	0	d_2
1	1	d_3.

3m

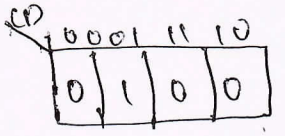




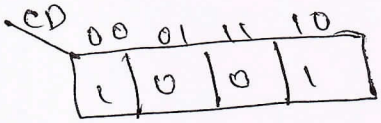
$d_0 = \bar{C} + \bar{D}$



$d_1 = \bar{D}$



$d_2 = \bar{C}D$



$d_3 = \bar{D}$.

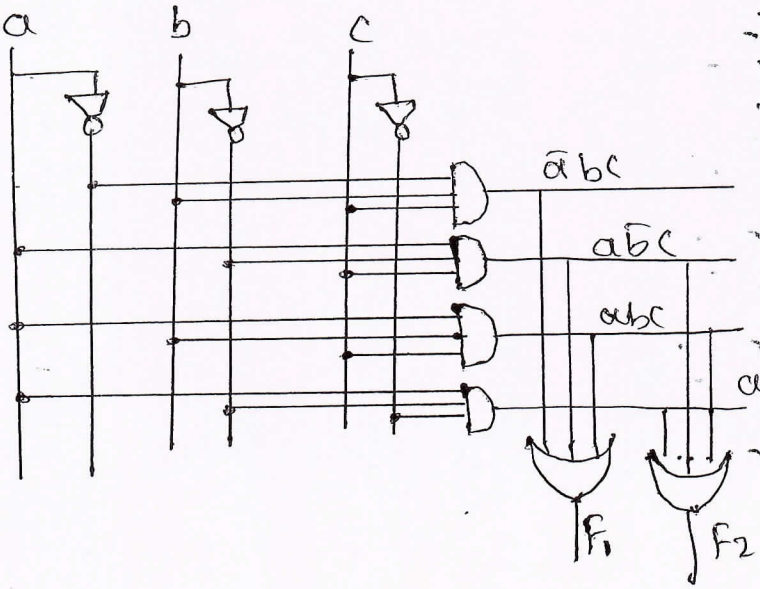
6m

3 c) A combinational circuit is defined by the fun^n $F_1 = \Sigma m(3,5,7)$, $F_2 = \Sigma m(4,5,7)$. Implement the circuit with a PLA having 3 I/P, 3 product terms and two O/P.

$F_1 = \Sigma m(3,5,7)$
$= \bar{a}bc + a\bar{b}c + abc$

$F_2 = \Sigma m(4,5,7)$
$= a\bar{b}\bar{c} + a\bar{b}c + abc$.

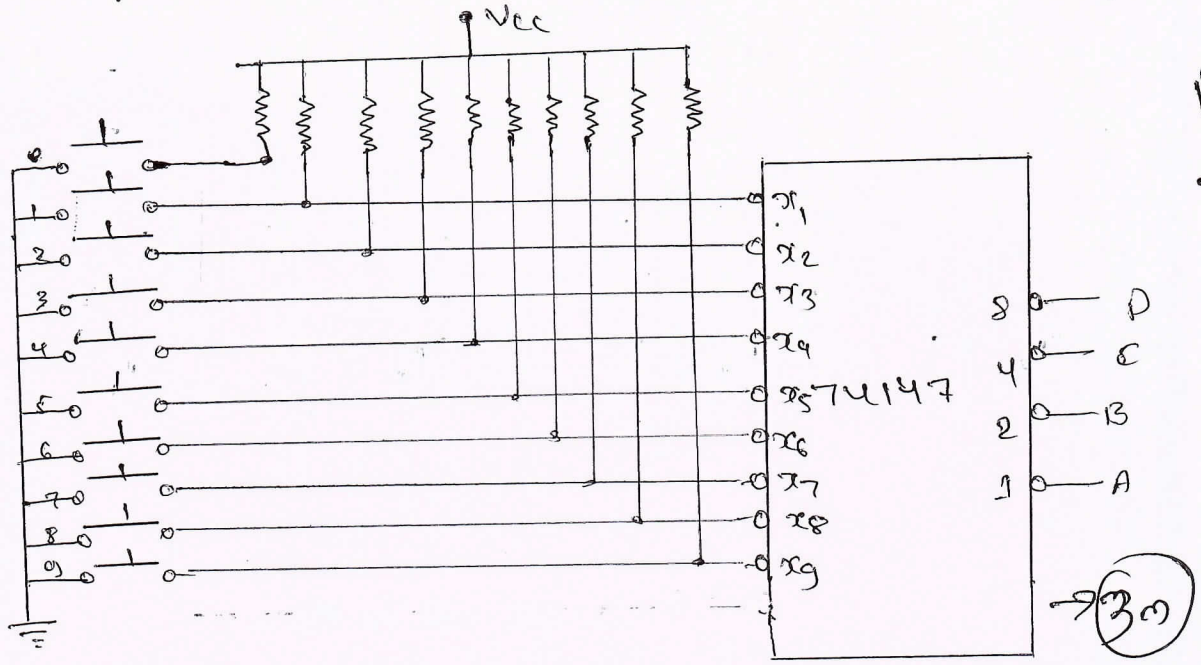
2m



4m

6m

4) a) Draw the keypad interfacing diagram to digital system using 10-line decimal to BCD encoder and explain.



6M

3M

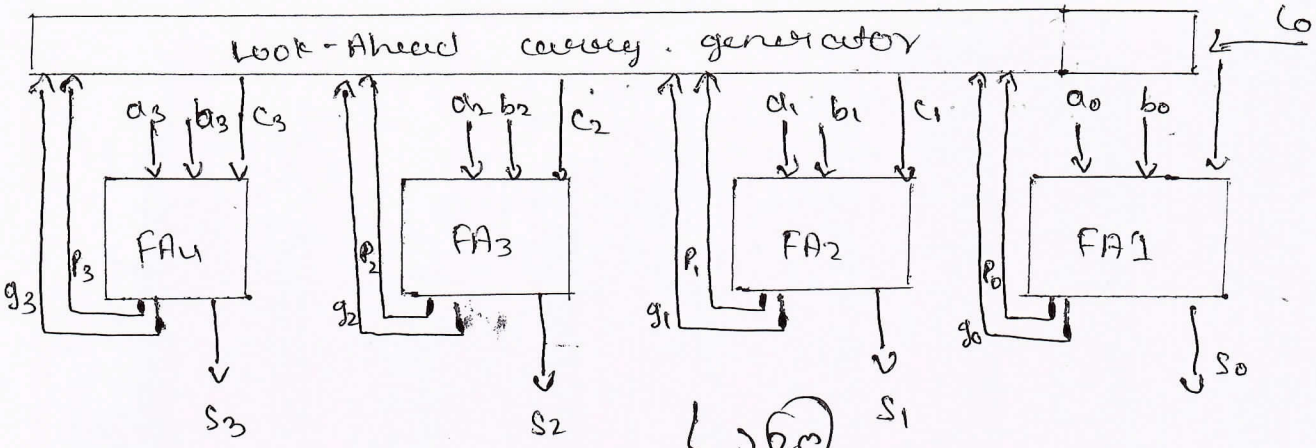
It encodes nine data lines to four line BCD. the implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level, when the keys are open. all the I/P are at 1 and all the O/P's are at 1. when any key is pressed the corresponding active low code appears at the O/P. → 1M

Incidentally, the 74147 is also referred to as a priority encoder this is because the device awards priority to the highest order I/P

Decimal	Input.									output			
	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	D	C	B	A
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	X	0	1	1	1	1	1	1	1	1	1	0	1
3	X	X	0	1	1	1	1	1	1	1	1	0	0
4	X	X	X	0	1	1	1	1	1	1	0	1	1
5	X	X	X	X	0	1	1	1	1	1	0	1	0
6	X	X	X	X	X	0	1	1	1	1	0	0	1
7	X	X	X	X	X	X	0	1	1	1	0	0	0
8	X	X	X	X	X	X	X	0	1	0	1	1	1
9	X	X	X	X	X	X	X	X	0	0	1	1	0

2M

4. b) Explain Look-ahead carry adder with neat diagram and relevant exp^n.



2m

* the parallel adder and subtractor are essentially ripple configuration.
* the parallel adder and subtractor are essentially
* the carry at any given stage would be available only after carry of previous stage has been generated.
* the effect of propagation delay could be more and more permanent as no. of bits increases.
* In order to remove carry dependency at each stage we go for carry look ahead adder.

6M

wkt, $C_{i+1} = a_i c_i + a_i b_i + b_i c_i$

$\therefore C_{i+1} = a_i b_i + (i(a_i + b_i)$ — (1).

$g_i = (a_i * b_i)$ → carry generate function

$P_i = a_i + b_i$ → carry propagate function.

$C_{i+1} = g_i + P_i c_i$ — (2).

at $i=0$ $C_1 = g_0 + P_0 C_0$ — (3)

→ 4m

Now $C_2 = g_1 + P_1 C_1$ — (4)

now substitute (3) in (4).

$C_2 = g_1 + P_1 (g_0 + P_0 C_0)$

$= g_1 + P_1 g_0 + P_1 P_0 C_0$ — (5)

Now $C_3 = g_2 + P_2 C_2$

$= g_2 + P_2 g_1 + P_2 P_1 g_0 + P_2 P_1 P_0 C_0$ — (6).

$C_4 = g_3 + P_3 C_3$

$= g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0 + P_3 P_2 P_1 P_0 C_0$ — (7)

eq^n (5), (6) & (7) indicate that C_2, C_3, C_4 are function of only parallel inputs.

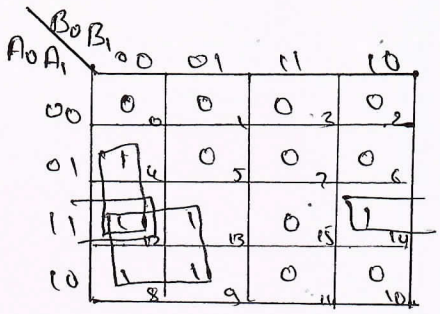
2. c) Design 2-bit comparator using gates.

Inputs				outputs		
A		B				
A_0	A_1	B_0	B_1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

$(A>B) = \sum m(4, 8, 9, 12, 13, 14)$

$(A=B) = \sum m(0, 5, 10, 15)$

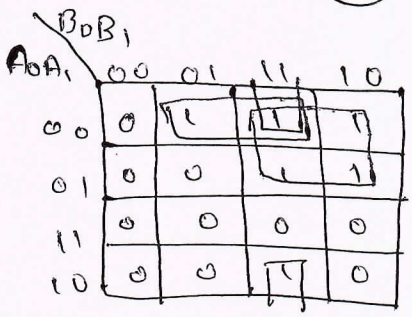
$(A<B) = \sum m(1, 2, 3, 6, 7, 11)$



1m

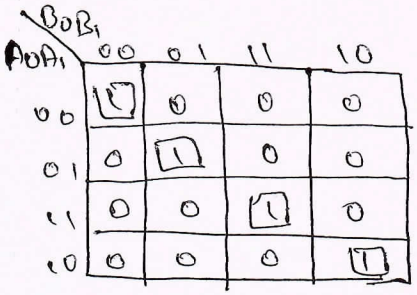
$A>B = A_0\bar{B_0} + A_1\bar{B_0}\bar{B_1} + A_0A_1\bar{B_1}$

2m



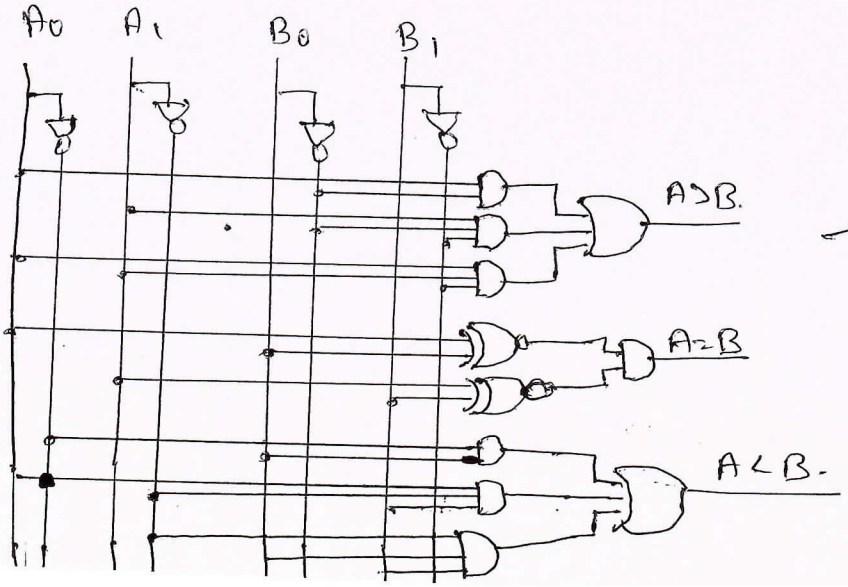
$A<B = \bar{A_0}B_0 + \bar{A_0}\bar{A_1}B_1 + \bar{A_1}B_0B_1$

2m



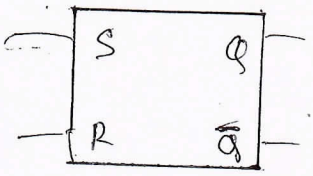
$(A=B) = \bar{A_0}\bar{A_1}\bar{B_0}\bar{B_1} + \bar{A_0}A_1\bar{B_0}B_1 + A_0A_1B_0\bar{B_1} + A_0\bar{A_1}B_0\bar{B_1}$

$= (\overline{A_0 \oplus B_0}) \cdot (\overline{A_1 \oplus B_1})$

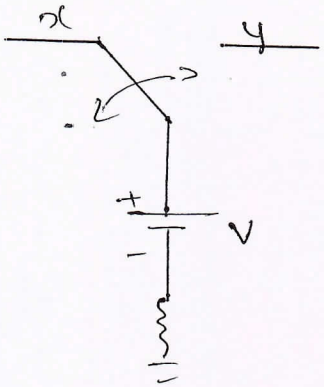


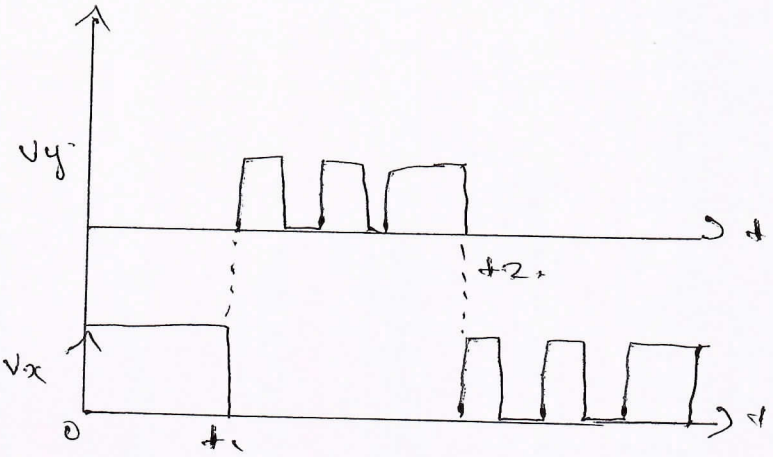
1m

5) a) Explain the operation of a switch debouncer using S-R latch with the help of circuit and waveforms.



SR latch.



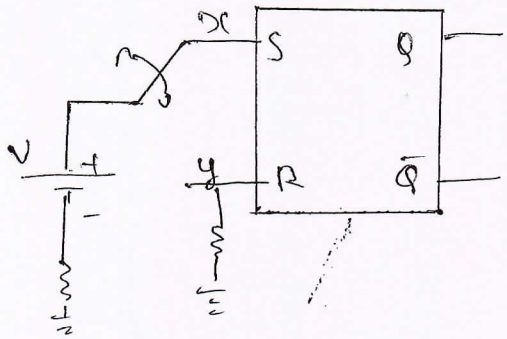


↳ (2m)

* mechanical switches such as toggle switches or push button when switched from one position to another does several make and break operation, this is called switch bounce.
* when center tap is moved from x to y at time t_1 we can see several make and break operation takes place.
* Similar operation is seen at time t_2 when center contact is made to y to x.
* In order to avoid this we go for SR latch.

↳ (2m)

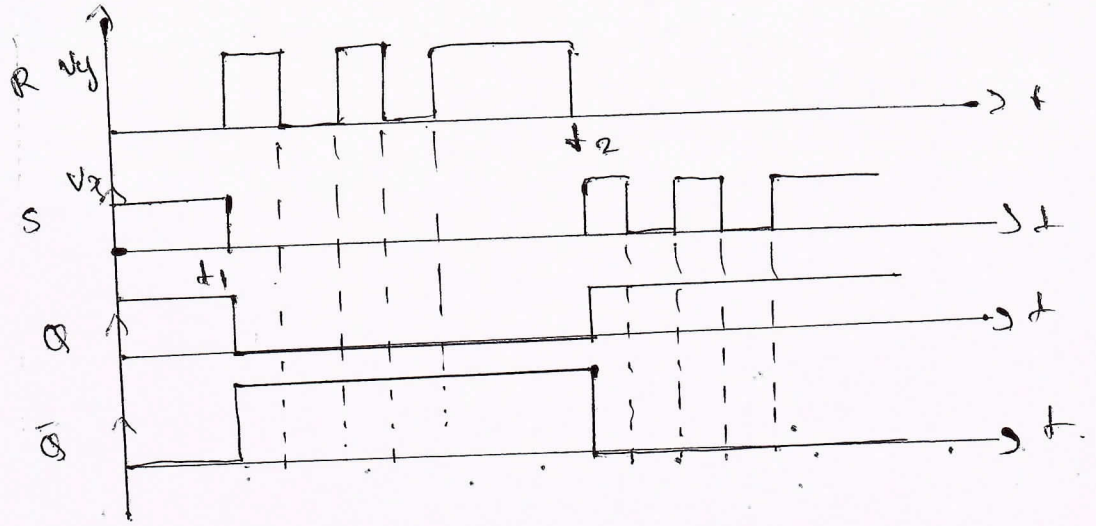
(6m)



S	R	Q_+	$\bar{Q}_+$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	Invalid	

Stable.

↳ (2m)



7 b) Find characteristics equations for S-R and T flip flop with the help of function tables and explain.

The algebraic discription of the next state table of a flip-flop is called the characteristic equation of the flip-flop. This discription is easily obtained by constructing the K-map for Q^+ in terms of the present state and inform^n I/P variables. The characteric eqn's specify only the functional behaviour of the flip-flops.

(2m)

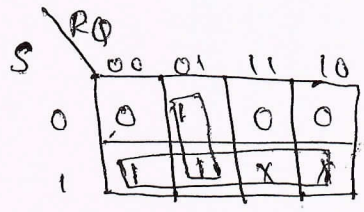
S-R

S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	—

function table.

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

for Q^+



$Q^+ = S + \bar{R}Q$.

is the equ characteristic eq^n of SR f-f.

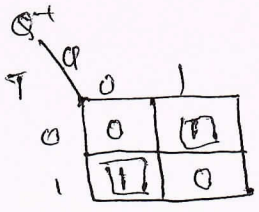
(3m)

T flip flop.

T	Q
0	Q
1	$\bar{Q}$

Function table.

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0



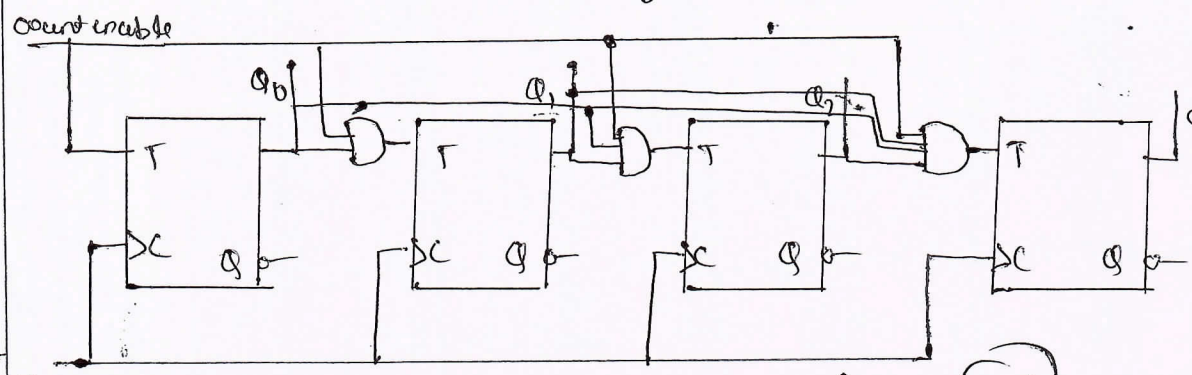
(1m)

$Q^+ = T\bar{Q} + \bar{T}Q$

$= T \oplus Q$.

C) Explain the working principle of 4-bit synchronous binary counter.

If the clock pulses to be counted are applied simultaneously to the control input of all the flip-flops in the cascade, such counters are called as synchronous counters.



8M

3M

count	Q_3	Q_2	Q_1	Q_0	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
3	0	0	1	1	1	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	1
11	1	0	1	1	0	1	0	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0
14	1	1	1	0	0	0	0	1
15	1	1	1	1	0	0	0	0

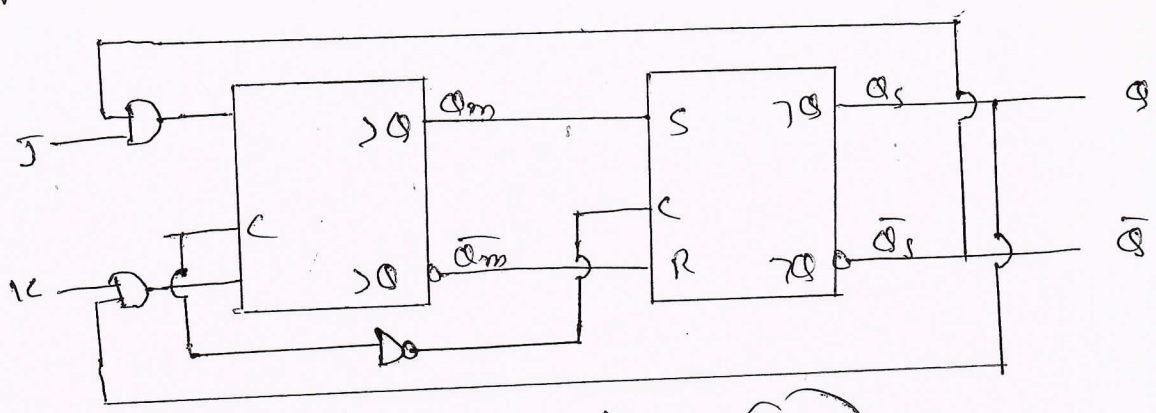
observe that Q_0 toggles with every clock pulse. the other o/p toggles whenever all the lower order f-f are at 1.

when count enable line is at logic 1. the AND gate o/p place at the T i/ps. when all the previous flip-flops o/p are at 1. the flip-flop whose T input is at logic 1 toggles at the next clock pulse. as the no. of stages increases the no. of i/p to the AND gate also increases.

making use of the fact that ANDed output of all previous flip-flops are available at the output of each AND gate. the gating can be modified to keep the no. of input to the AND gates constant.

5M

5) a) Draw the logic diagram, functional table and timing diagram of master-slave JK flip-flop and explain briefly.



→ (3m)

truth table.

clk	J	K	Q^+	$\bar{Q}^+$
0	x	x	Q	$\bar{Q}$
⎍	0	0	Q	$\bar{Q}$
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	$\bar{Q}$	Q

→ (7M)

case 1: when clock is 1 & J, K are equal to logical 0 and 1, then we assume the Q = 1 & $\bar{Q}$ = 0. The S=0 & R=0, clock=1 then Qm & $\bar{Q}m$ will be previous value which is nothing but Qm = 1 & $\bar{Q}m$ =

case 2:

when clock is 1 & J, K are equal to logical 1 & 0 then assume Q=1 & $\bar{Q}$ =0. the S=0 & R=0 then Qm & $\bar{Q}m$ will be in its previous state only i.e, Qm =1 & $\bar{Q}m$ =0.

case 3:

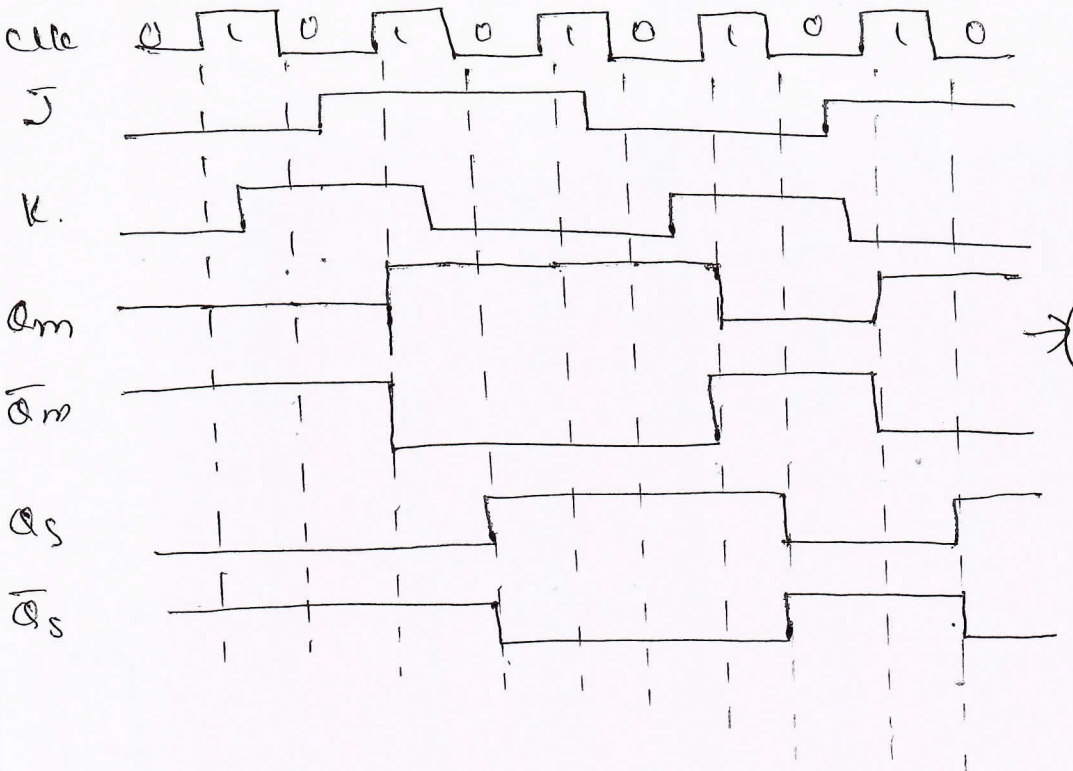
when c=1, J=0 & K=0 then for AND gate any one i/p is 0 then o will be 0, ∴ S=0 & R=0 then Qm & $\bar{Q}m$ take the previous value & the same is passes to Qs and $\bar{Q}s$.

case 4:

when c=1, J=1 & K=1, assuming Q=1 & $\bar{Q}$ =0 then S=0 & R=1 then Qm & $\bar{Q}m$ =1 the same is passes to Qs & $\bar{Q}s$ ∴ $Q^+ = \bar{Q}$ & $\bar{Q}^+ = Q$.

case 5:

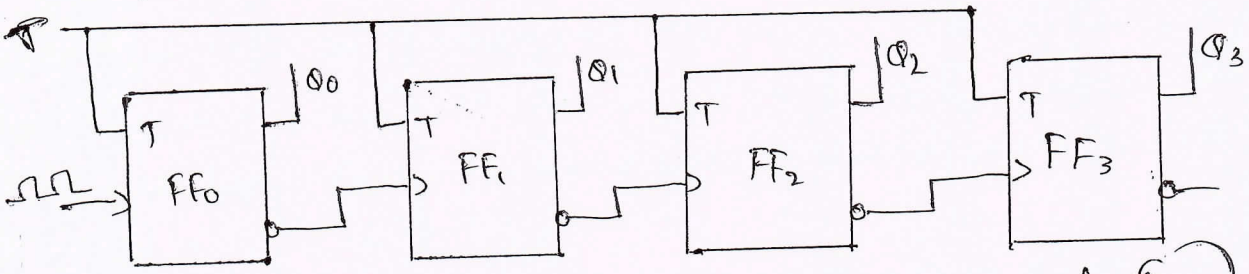
when c=0, the whatever may be the value of J and K then Q^+ & $\bar{Q}^+$ will take previous value.



5m

10M

6 b) Explain 4 bit binary ripple counter with logic and timing diagram.

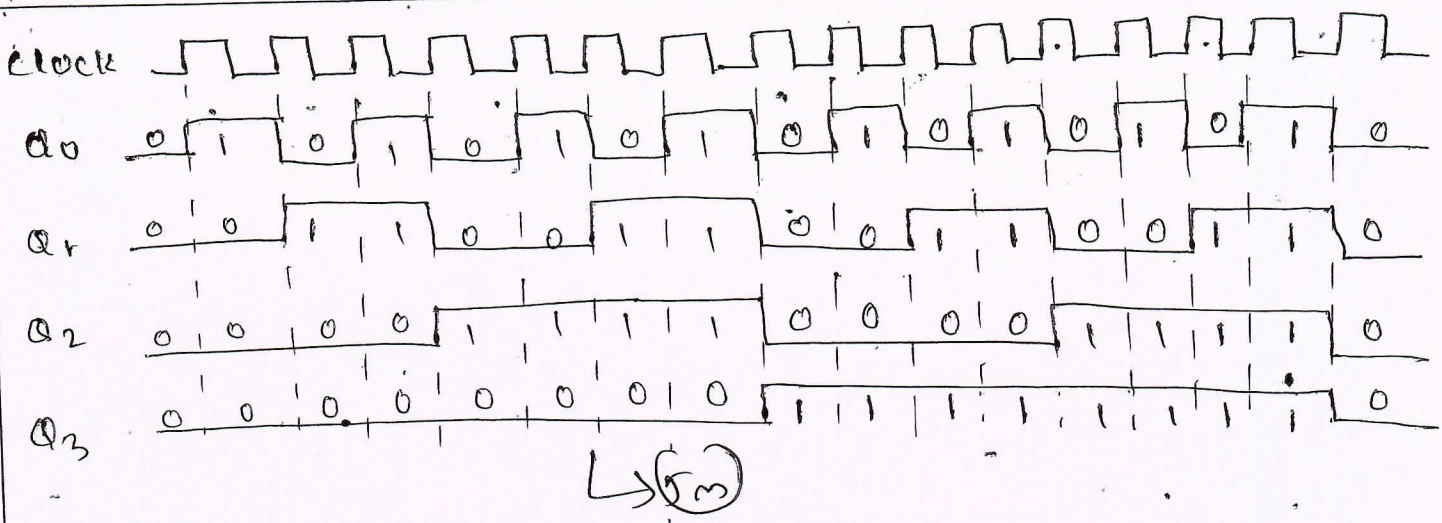


5m

Binary counters o/p the binary number sequence. when the count enable or T i/p are at logic 1, the output of each flip-flop toggles for every 0 to 1 transition of its clock input or at every positive edge of its clock input. The clock inputs of flip-flops FF_0, FF_2, FF_3 are connected to $\bar{Q}$ of the previous flip-flops. These flip-flops changes states on the 1 to 0 transition of the Q outputs which corresponds to 0 to 1 transition of the $\bar{Q}$ outputs.

2m

10M



↳ (5m)

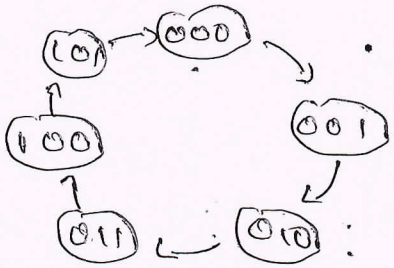
7) a). Design mod-6 synchronous counter by using JK flip-flop, with excitation table.

counting sequence.

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

0 0 0 - repeat

state diagram.



↳ (2m)

10M

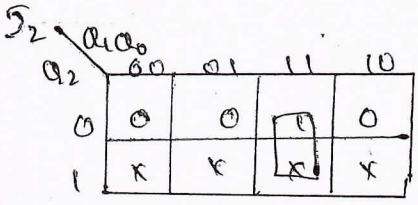
application table of J-K flip flop.

Q	Q^+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

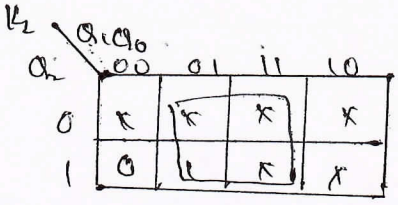
Excitation table.

Present state			next state			Inputs.					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

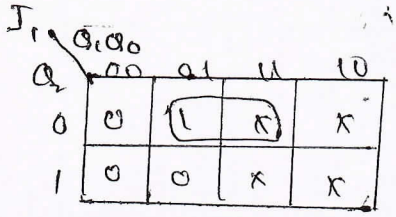
↳ (2m)



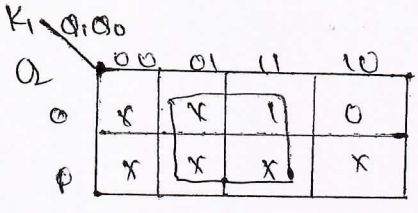
$J_2 = Q_1Q_0$



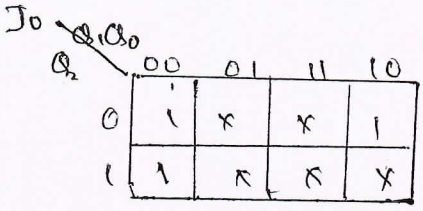
$K_2 = Q_0$



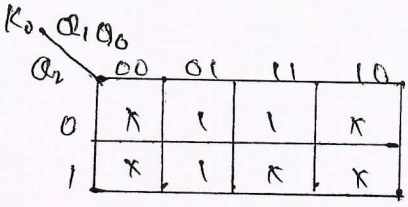
$J_1 = \overline{Q_2}Q_0$



$K_1 = Q_0$

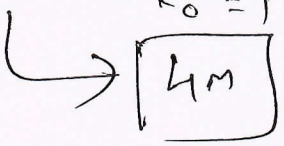


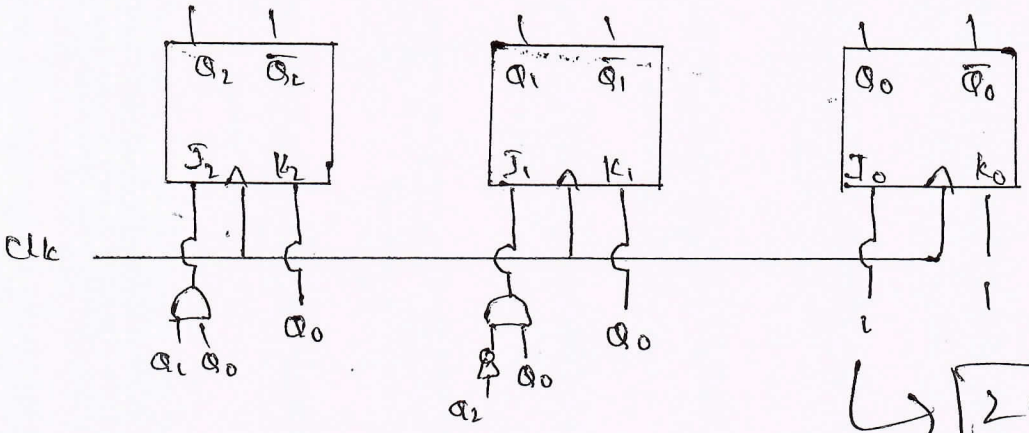
$J_0 = 1$.

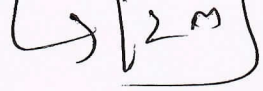


$K_0 = 1$

state machine.

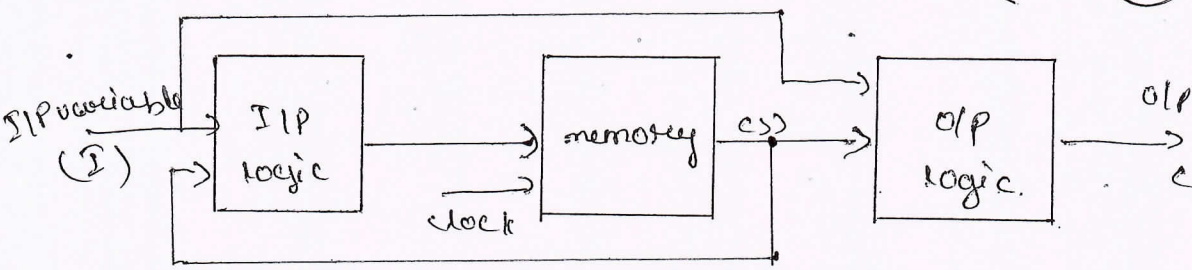






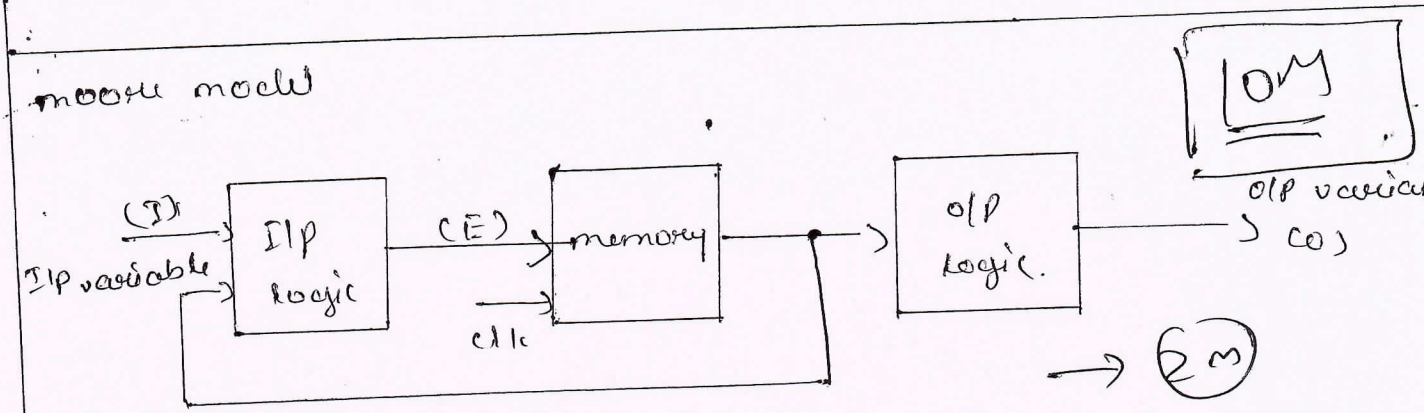
7 b) Draw and explain Mealy and Moore sequential circuit model and compare mealy and moore circuit model.

Mealy model.



* when the O/P of the sequential circuit depends on both present state and inputs of the flip-flops. then that sequential circuit is referred to as mealy model.
* It is in contrast to a moore machine, whose o/p values are determined solely by its current state.
* It is for each state & i/p, atmost one transition is possible in mealy machine.

moore model



→ (2M)

* when the o/p of a sequential circuit depends only on the present state of the flip-flop, then that sequential circuit is referred to as a moore model.
* In this the o/p is derived using only present states of the flipflops or combination of it. → (3M)
* It has more states than a mealy machine;

Mealy model	moore model
* output depends on present state and external input.	* o/p depends only on the present state of flipflop.
* change in input effects the output.	* change in input dosnot effect the output.
* It requires less no. of states for implementing a function.	* It requires more no. of states for implementing a function.

→ (3M)

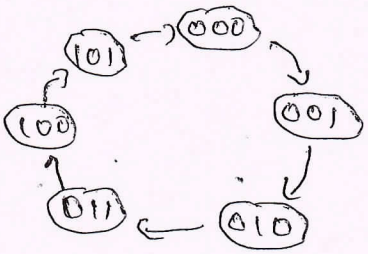
8) a) Design a mod-6 synchronous counter using clocked T-flip-flop.

counting sequence.

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

0 0 0 - repeat

State diagram.



application table.
(T F-F).

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

→ (2M)

Excitation table.

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

10M

2M

T_2

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	0	1	x	x

$T_2 = Q_2Q_0 + Q_1Q_0$

T_1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	1	0
1	0	0	x	x

$T_1 = \bar{Q}_2Q_0$

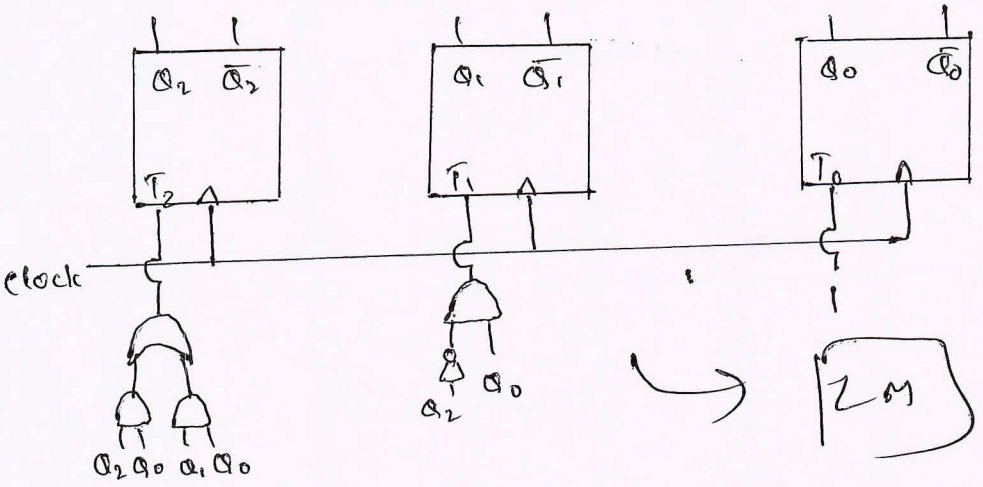
T_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	1	1	1
1	1	1	x	x

$T_0 = 1$

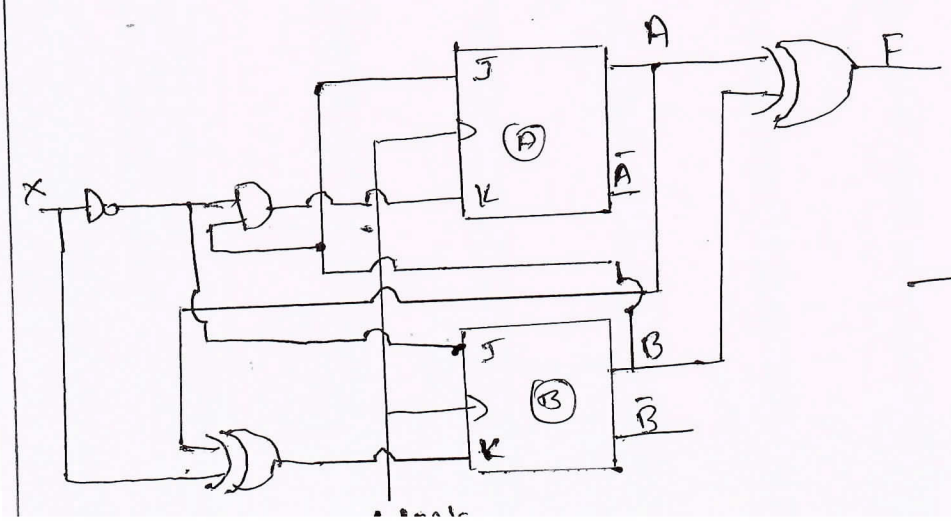
4M

State machine.



2M

b) construct the transition table, state table and state diagram for the sequential circuit shown.



1M

From figure.

$J_A = B$ $\quad K_A = \bar{x}B$.

$J_B = \bar{x}$ $\quad K_B = A \oplus x$

$F = A \oplus B$.

A	B	x
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

J_A	J_B	K_A	K_B	F
0	1	0	0	0
0	0	0	1	0
1	1	1	0	1
1	0	0	1	1
0	1	0	1	1
0	0	0	0	1
1	1	1	1	0
1	0	0	0	0

→ 2M

Excitation table

P, S	n, S x				O/P F	
A B	x=0		x=1		x=0	x=1
	$J_A K_A$	$J_B K_B$	$J_A K_A$	$J_B K_B$		
0 0	0 0	1 0	0 0	0 1	0	0
0 1	1 1	1 0	1 0	0 1	1	1
1 0	0 0	1 1	0 0	0 0	1	1
1 1	1 1	1 1	1 0	0 0	0	0

transition table.

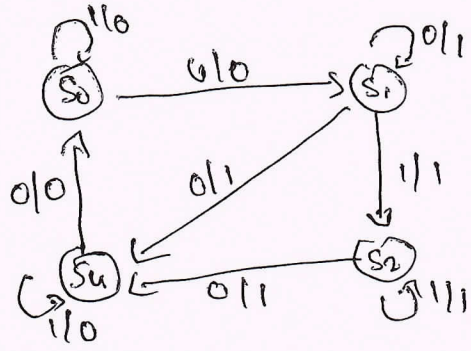
P, S	n S		O/P F	
A B	x=0	x=1	x=0	x=1
0 0	0 1	0 0	0	0
0 1	1 1	1 0	1	1
1 0	1 1	1 0	1	1
1 1	0 0	1 1	0	0

→ 2M

State table. → 2M

state	x=0	x=1
S_0(00)	S_1	S_0
S_1(01)	S_3	S_2
S_2(10)	S_3	S_2
S_3(11)	S_0	S_3

→ 2M

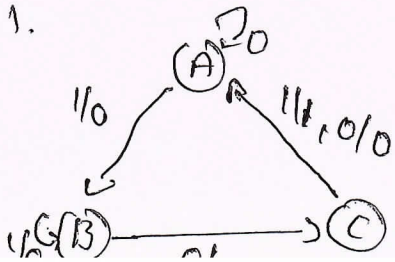


→ 2M

→ 10M

9) a) design & draw mealy model of sequential detector circuit to detect the pattern 101.

Form on, ~~overlap~~ overlapping.



State table.

P.S	N.S x/z			
	x=0	z	x=1	z
A	A	0	B	0
B	C	0	B	0
C	A	0	A	1

→ (2M)

State assignment table.

A	B	C
00	01	10

transition table.

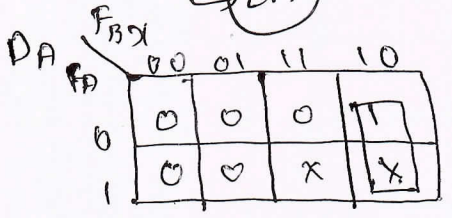
P.S	N.S x/z			
	x=0	z	x=1	z
00	00	0	01	0
01	10	0	01	0
10	00	0	00	1
11	xx	x	xx	x

(2M)

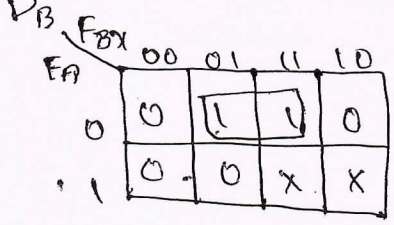
Excitation table.

P.S		N.S x/z			
		x=0	z	x=1	z
F_A	F_B				
0	0	00	0	01	0
0	1	10	0	01	0
1	0	00	0	00	1
1	1	xx	x	xx	x

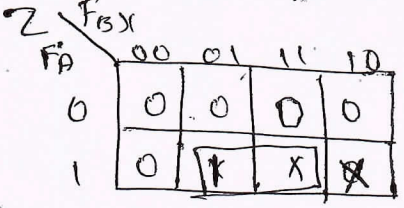
→ (2M)



$D_A = F_B \bar{x}$

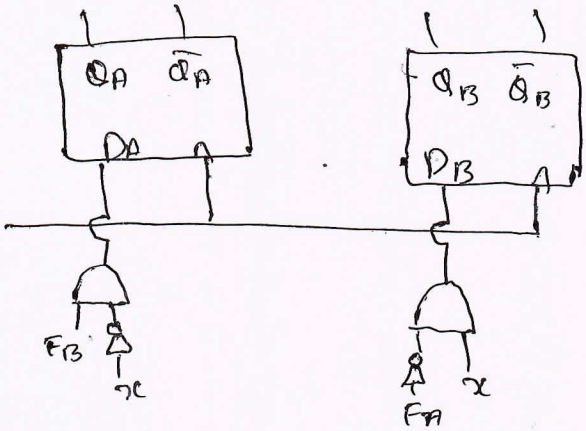


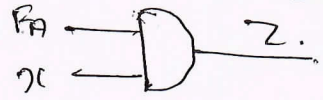
$D_B = F_A \bar{x}$.



$z = F_A x$

→ (4M)

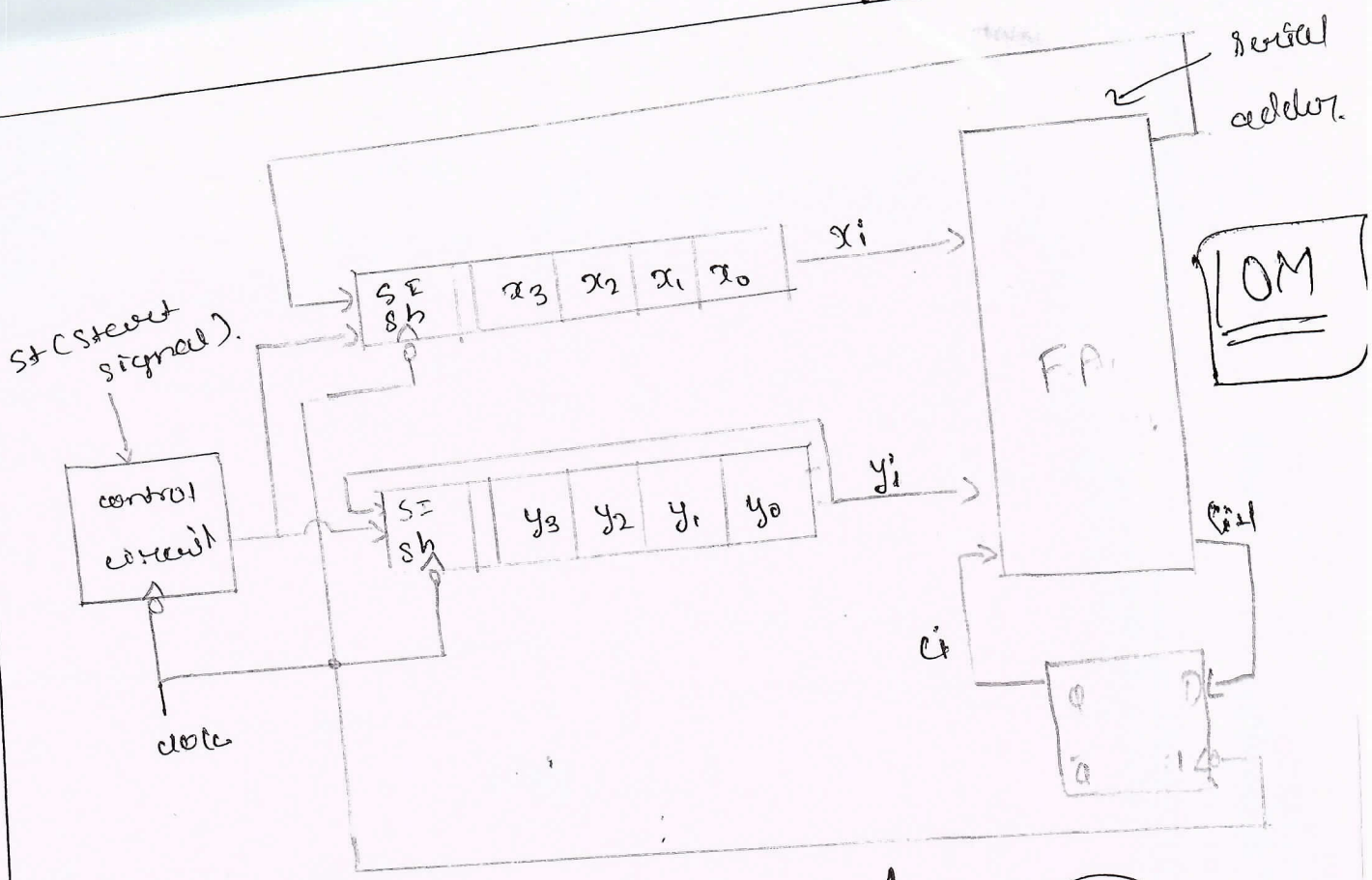




10M

b) Draw the block diagram of serial adder with accumulator & explain its working oprn.

* shift registers x & y are used to hold 4-bit number to be added.
* the x register is called as accumulator & the y register is called as addend register.



operation of serial adder.

3M

T	x	y	C_i	S_i	C_{i+1}
t_0	0101	0111	0	0	1
t_1	0010	1011	1	0	1
t_2	0001	1101	1	1	1
t_3	1000	1110	1	1	0
t_4	1100	0111	0	(1)	(0).

5M

* when Shift = 1 & for rising edge of the clock serial i/p is fed into & q_3 and contents of register are shifted once.
* at each clock time a pair of bits is added.
* when sh = 1 & for falling edge of clock sum bit is shifted into accumulator. C_{i+1} is shifted into D flipflop & content of addend register shifted once and after 4 clock we get Sum = $S_3 S_2 S_1 S_0$ & Carry = C_4

10) a). State the guidelines for const^n of state graph.

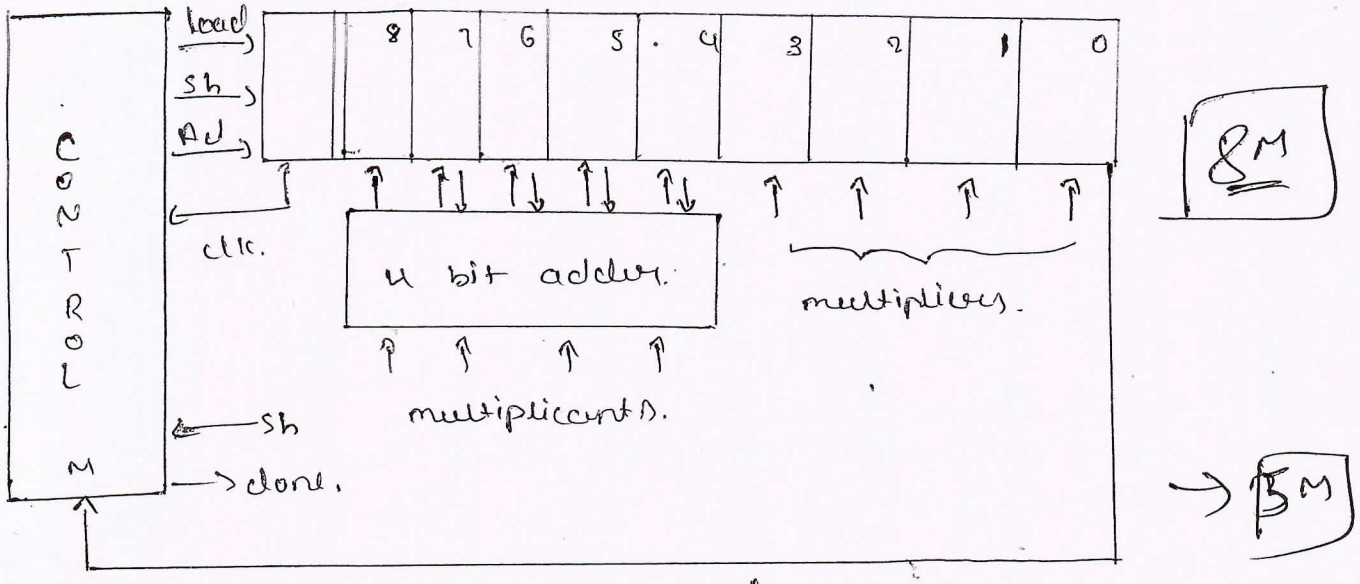
* First, construct the some sample i/p and o/p sequence to understand the problem statement.
* determine under what cond^{n}s, if any circuit should reset to initial state.
* If only one or 2 sequences lead to a nonzero o/p a must go

Start is to construct a partial state graph for these sequences.

* another way to get started is to determine what sequences or groups of sequences must be remembered by circuit and set up states accordingly.
* Each time add an arrow to the state graph. determine whether it can goto one of the previously defined states or whether a new state must be added.
* check your graph to make sure there is one and only one path leaving each state for each combinat" values of the i/p variables.
* when graph is completed test it by applying the i/p sequences formulated in part and making sure the o/p sequences are correct.

↳ BM

b) Draw the blk diagram of binary multiplier and explain its working principle.



If LSB(M) m=0 only sh → acc → right one
m=1 acc + multiplicand = acc.
sh → acc → right once.

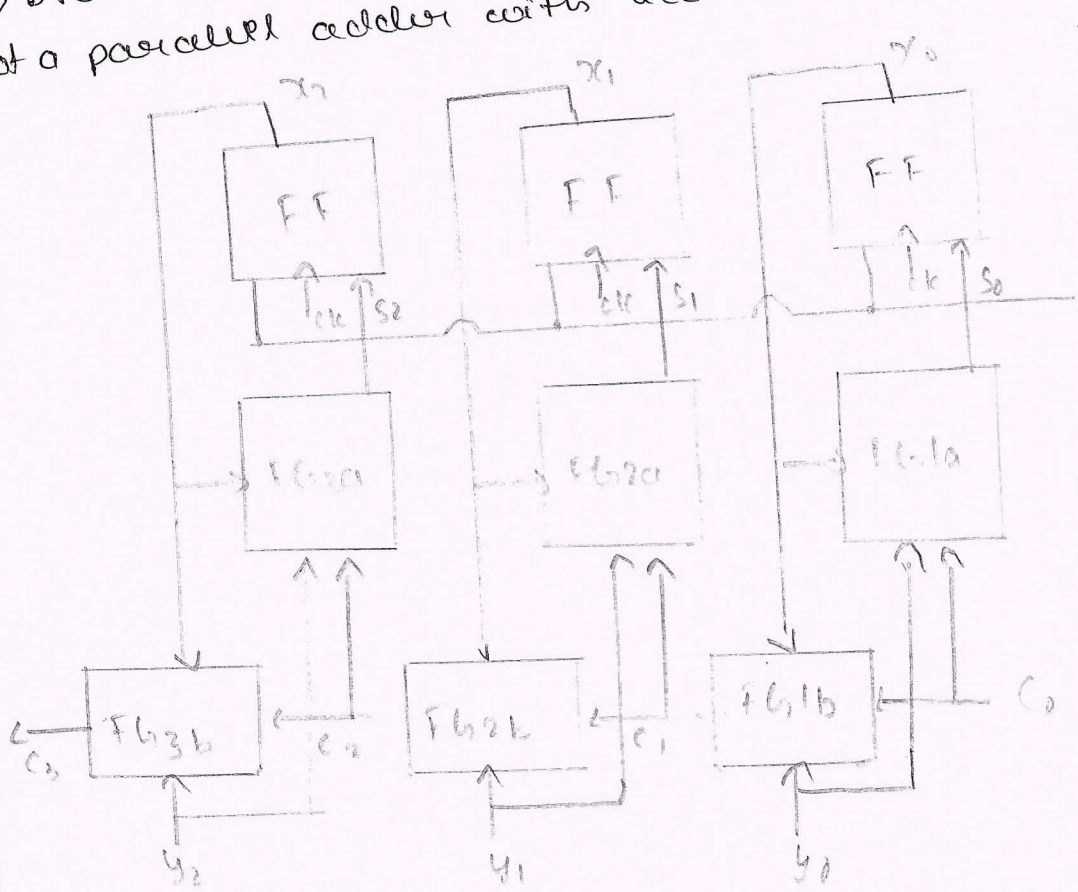
* Initially when start signal is given to control the control circuit loads multiplier into accumulator during rising edge of clock lower level of accumulator & three 5 highest bits.
* 4 bit adder adds multiplicand with contents of accumulator & result is stored back into accumulator during rising edge of clock.
* If m=0 we get Ad=1 multiplicand is added to the accumulator register & result is stored in accumulator. then contents of accumulator is

↳ 27

* If M=0, addn will not be carried out & contents of accumulator are shifted right once.
* after 4 shift circuit will be available in product register.
* after complete multiplication control unit makes done = 1.

c) Draw and explain the operation of FPGA implementation of a parallel adder with accumulator.

6M



3M

* Each bit of the adder can be implemented with two 3-V -able function generators. one for the sum and one for the -ry. The add signal is connected to the CE i/p of each flip-flop, so that the sum is loaded by the rising clock edg when Ad = 1, the arrangement for generating the carries is sl slow, because the carry signal must propagate through a function generator & its external interconnects for each bit Because adders are frequently used in FPGAs, most FPGAs h built-in fast carry logic in addition to the function genera If the fast carry logic is used, the bottom row of functio generators of the fig above is not needed. A parallel ad with an accumulator can be implemented using only one fun generator for each bit.

3M