CBCS SCHEME

USN | 2 | U | D | 1 | 8 | E | C | 0 | 6 | 9 |

18EC72

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With necessary circuit diagram, explain the operation of tristate inverter. Also realize a 2 : 1 multiplexer using tristate inverter. **(08 Marks)**

b. Implement a D flipflop using transmission gates and explain its operation with necessary tining diagram. **(08 Marks)**

c. Realize CMOS compound gate for the function $Y = \overline{A(B+C)+DE}$. **(04 Marks)**

OR

2 a. Explain the operation of MOSFET with necessary diagrams. Also derive the equation for drain current in linear and saturation region of operation. **(10 Marks)**

b. Draw the circuit of CMOS inverter and explain its DC transfer characteristics. **(06 Marks)**

c. Explain the following non-ideal effects channel length modulation, mobility degradation. **(04 Marks)**

Module-2

3 a. Explain CMOS n-well fabrication process with necessary diagrams. **(12 Marks)**

b. What is scaling. Compute drain current, power, current density and power density for constant field and constant voltage scaling. **(08 Marks)**

OR

4 a. Draw the layout of $Y = \overline{(A+B+C)D}$ and estimate the area. **(08 Marks)**

b. Mention different types of MOSFET capacitances and explain with necessary diagrams and equations. **(06 Marks)**

c. With neat diagram, explain lambda based design rules for wires and contacts. **(06 Marks)**

Module-3

5 a. Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit inverter. **(08 Marks)**

b. Explain Cascode Voltage Switch Logic (CVSL). Also realize two input AND/NAND using CVSL. **(06 Marks)**

c. Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagrams :
i) 2-input NAND gate ii) 3-input NOR gate. **(06Marks)**

OR

6 a. Explain : i) pseudo nMOS ii) ganged CMOS with necessary circuit examples. **(06 Marks)**

b. Estimate t_{pdf} and t_{pdr} of a 3-input NAND gate if the output is loaded with h identical gates. Use Elmore delay model. **(08 Marks)**

c. Explain skewed gates with an example. **(06 Marks)**

Module-4

7 a. With necessary circuit diagrams, explain resettable latches with
i) synchronous reset
ii) asynchronous reset. (08 Marks)

b. Compute the output voltage V_{out} in the following pass transistor circuits. Assume $V_t = 0.7$. (Ref. Fig.Q7(b)).

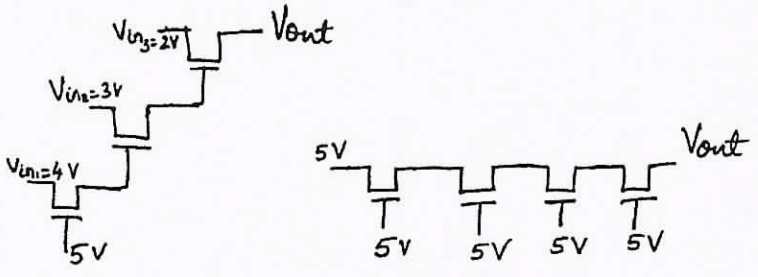

Fig.Q7(b) (06 Marks)

c. With necessary diagram, explain a D flipflop with two-phase non-overlapping clocks. (06 Marks)

OR

8 a. With necessary circuit diagram explain 3-bit dynamic shift register with depletion load. (08 Marks)

b. Realize $F = \overline{A_1A_2A_3 + B_1B_2}$ using dynamic CMOS logic. Also explain the cascading problem in dynamic logic with necessary example. (08 Marks)

c. Explain the general structure of ratioless synchronous dynamic logic with relevant diagram. (04 Marks)

Module-5

9 a. With necessary circuit diagram, explain the operation of three transistor DRAM cell. (08 Marks)

b. Explain full CMOS SRAM cell with necessary circuit topology. (08 Marks)

c. Explain the terms :
i) Observability
ii) Controllability
iii) Fault coverage. (04 Marks)

OR

10 a. What is a fault model? Explain stuck-at model with examples. (07 Marks)

b. Mention the approaches used in design for testability. Explain scan based testing using necessary diagrams. (07 Marks)

c. Draw the circuit of 3-bit BIST register and explain. (06 Marks)

* * * * *

18EC72 (VLSI Design)

Scheme & Solution prepared by

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2.) Prof. Deepak Sharma

28.05.2022

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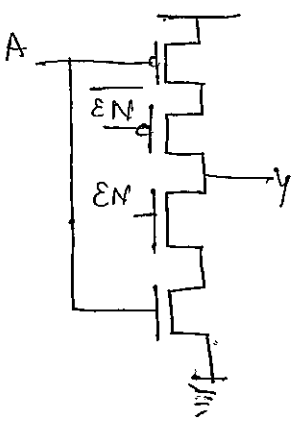
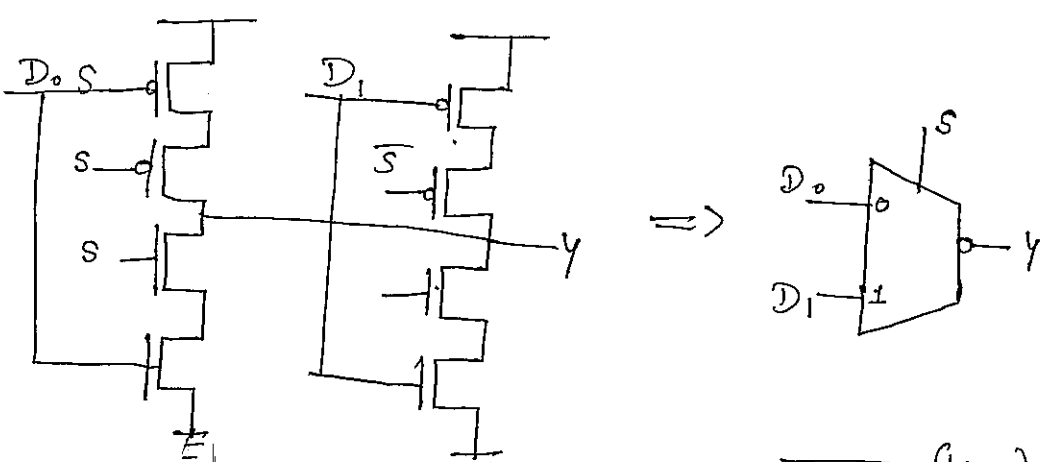
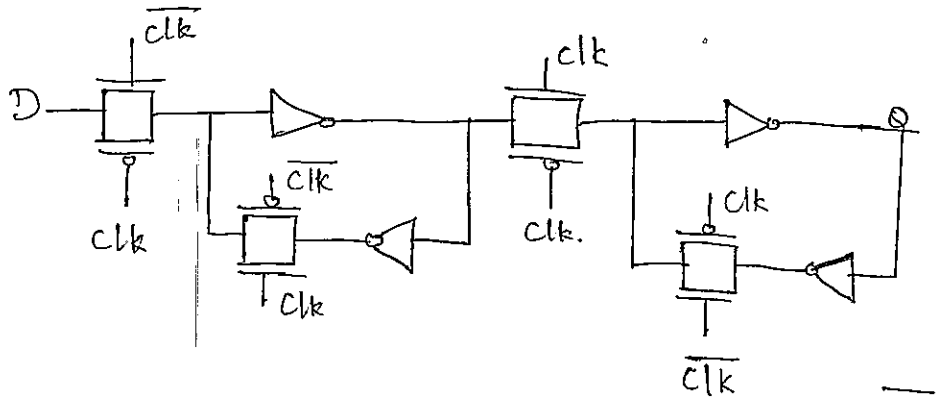
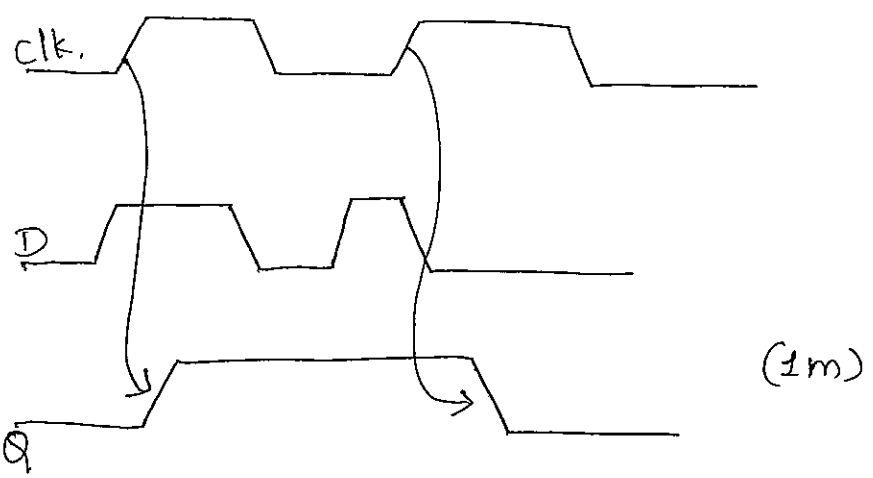
Department: E&C
Subject with Sub. Code: VLSI Design - 18EC72 **Semester / Division: 7 /A&B**
Name of Faculty: Dr. Vikas Balikai, Prof. Deepak Sharma

Q.No.	Solution and Scheme	Marks
1 a)	Module - 1 Tristate Inverter  Truth Table EN | A | Y 1 | 0 | 1 1 | 1 | 0 0 | 0 | z 0 | 1 | z —— (4m) 2:1 Multiplexer using tristate inverter  —— (4m)	08

Q.No.	Solution and Scheme	Marks
b)	D flipflop using transmission gate.  — (3M)  (1m) Explanation with Truth table — (4m)	08

Clk	D	Q^+
0	X	Q
1	X	Q
↓	0	0
↑	1	1

Explanation.

Q.No.	Solution and Scheme	Marks
1C)	Realization of CMOS gate for $Y = \overline{A(B+C)+D\varepsilon}$	

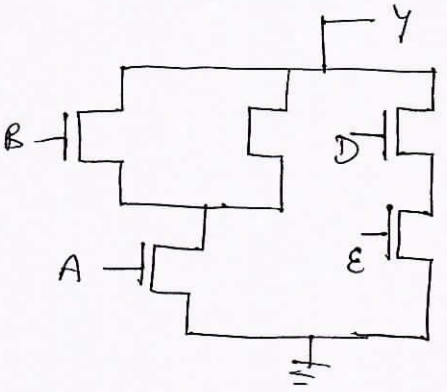
Pulldown network

$A(B+C)+D\varepsilon$

OR (parallel)

AND AND (series)

OR (parallel)



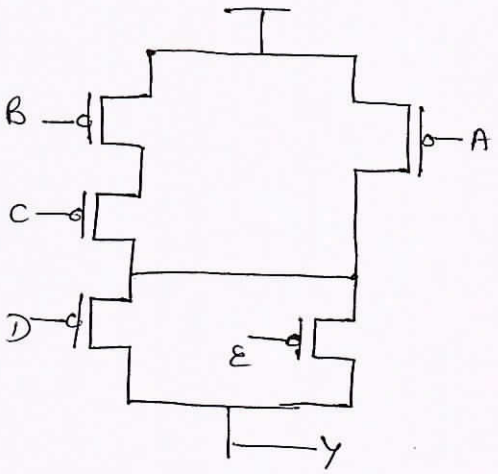
Pull up network

$A(B+C)+D\varepsilon$

AND

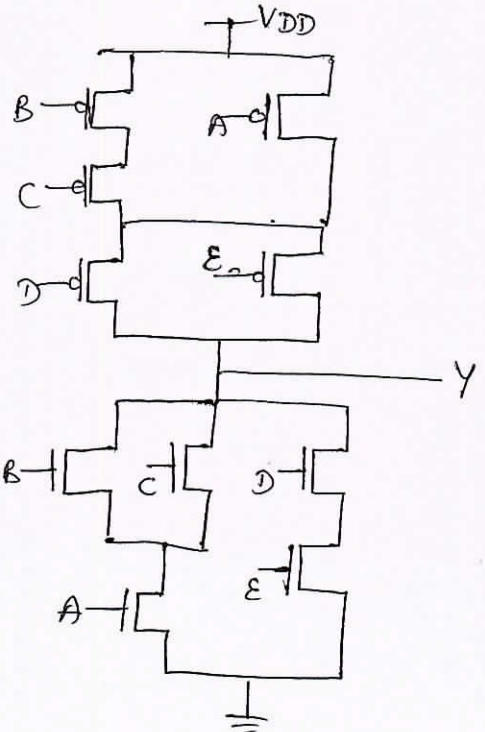
OR OR

AND



04

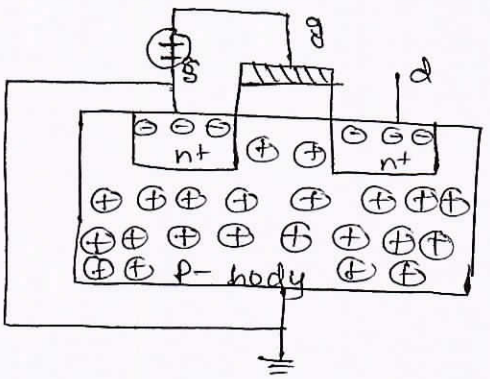
CMOS Gate



OR

Q.No.	Solution and Scheme	Marks

2a) Case (i) Cut off region, $V_{gs} < V_t$.

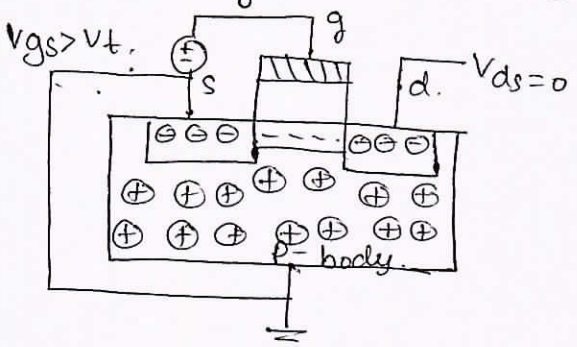


Explanation

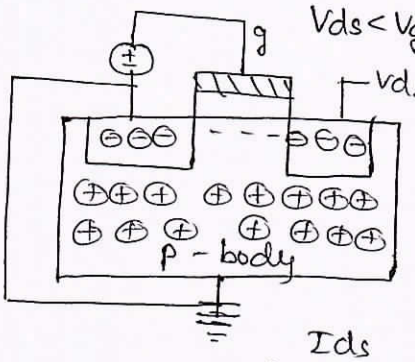
No channel

$I_{ds} = 0$.

Case (ii): $V_{gs} > V_t$ and $V_{ds} = 0$

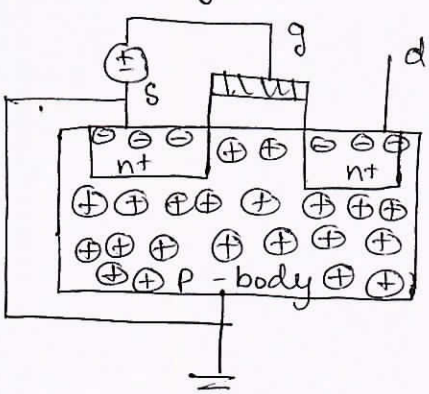


case(iii) $V_{gs} > V_t$ and $V_{ds} < V_{gs} - V_t$.



Ids increases with Vds.

Case(iv) $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$.



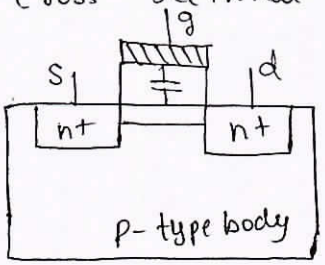
channel pinches off

Ids independent of V_{ds}

——(04m)

Q.No.	Solution and Scheme	Marks

Cross sectional view of nmos.

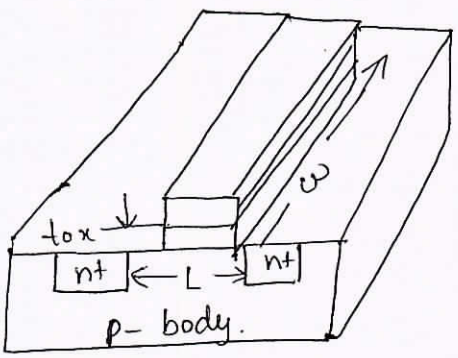


Non-saturated region

$$Q = CV = C_g V_{gc}$$

$$Q_{channel} = C_g\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)$$

$$C_g = \frac{\varepsilon_{ox} WL}{t_{ox}} = C_{ox} WL.$$



where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.

$$V = \mu\varepsilon.$$

$$\varepsilon = \frac{V_{ds}}{L} \quad \text{and} \quad \tau = \frac{L}{\mu \frac{V_{ds}}{L}}.$$

$$I_{ds} = \frac{Q_{channel}}{\tau} = \frac{C_g\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)}{\frac{L}{\mu \frac{V_{ds}}{L}}}$$

$$I_{ds} = \frac{\mu C_{ox} W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds} \longrightarrow \text{Current in linear region}$$

Saturation region: Substitute $V_{ds} = V_{gs} - V_t$

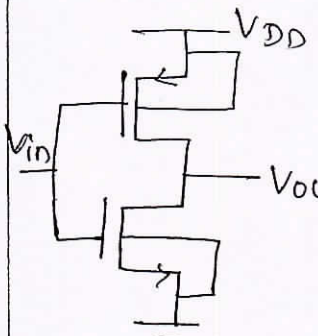
$$I_{ds} = \frac{\mu C_{ox} W}{L}\left[V_{gs} - V_t - \frac{(V_{gs} - V_t)}{2}\right](V_{gs} - V_t)$$

$$= \frac{\mu C_{ox} W}{L}\left(\frac{V_{gs} - V_t}{2}\right)^2 = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 \longrightarrow \text{saturation current}$$

(06 M)

Q.No.	Solution and Scheme	Marks

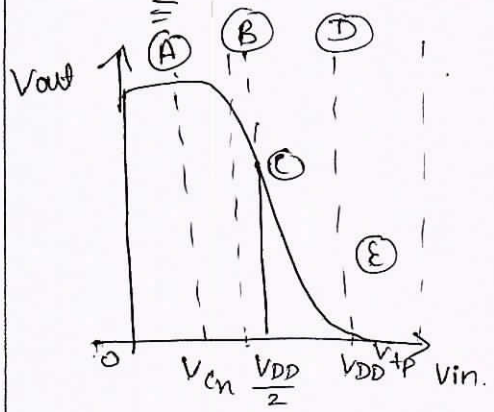
b) CMOS inverter



$V_{gsn} = V_{in}$, $V_{gsp} = -(V_{DD} - V_{in})$

$V_{dsn} = V_{out}$, $V_{dsp} = -(V_{DD} - V_{out})$

Explanation — (3m)



V_{TC} — (3m)

(2c) channel length modulation — Explanation with equations for $L_{eff} = L - L_d$.

$$I_{ds} = \frac{\beta}{2} V_{ST}^2 \left(1 + \frac{V_{ds}}{V_n}\right)$$ — (02M)

Mobility degradation — Explanation with equations

$$\mu_{eff-n} = \frac{540 \ \frac{cm^2}{V-s}}{1 + \left(\frac{V_{gs} + V_t}{0.54 \ \frac{V}{nm} \ t_{ox}}\right)^{1.55}} \quad \& \quad \mu_{eff-p} = \frac{185 \ \frac{cm^2}{V-s}}{1 + \frac{|V_{gs}| + 1.5|V_t|}{0.388 \ \frac{V}{nm} \ t_{ox}}}$$

— (02M)

Q.No.	Solution and Scheme	Marks

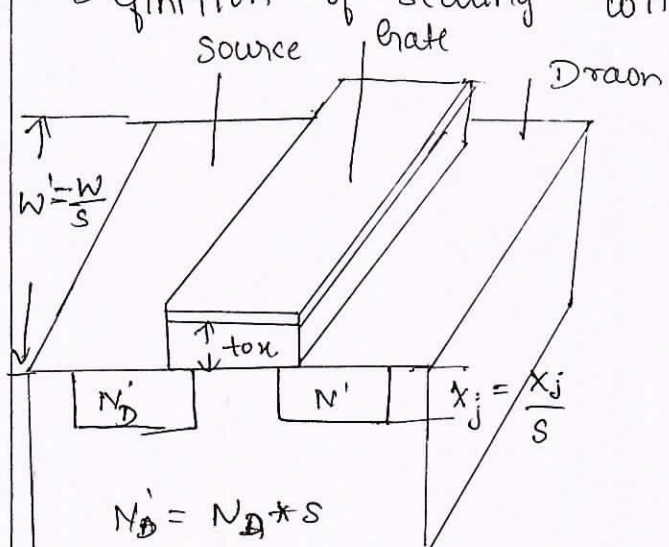
Module - 2.

3a) Explanation of CMOS n-well process with necessary diagrams and masks for the following steps. —

* n - well formation (n - well mask)
* Gate formation (polysilicon mask)
* n+ diffussion regions (n+ diffusion mask)
* Definition of p+ regions (p+ diffusion mask)
* Contact cut definition (Contact mask)
* Metallization (metal mask) — 06 x 02 m each.

b)

Definition of scaling with diagram — (02 m)



$$t_{ox}' = \frac{t_{ox}}{S}$$

$$N_D' = N_D * S$$

Q.No.	Solution and Scheme	Marks

Constant field scaling

Current

$$I_D' = \frac{kn'}{2}\left[2\left(V_{GS}' - V_{T_0}'\right)V_{DS}' - V_{DS}'^2\right] = \frac{Skn}{2}\frac{1}{S^2}\left[2(V_{GS}-V_{T_0})V_{ds} - V_{DS}^2\right]$$

$$I_{D(lin)}' = \frac{kn}{S.2}\left[2(V_{GS}-V_{T_0})V_{DS} - V_{DS}^2\right] = \boxed{\frac{I_{D(lin)}}{S}}$$

Power : $P = I_D . V_{DS}$

$$P' = I_D' . V_{DS}' = \frac{I_D}{S} \cdot \frac{V_{DS}}{S}$$

$$\boxed{P' = \frac{P}{S^2}}$$

$$\text{Current density} = \frac{I_D}{\text{Area}} = \frac{I_D'}{\text{Area}'} = \frac{\frac{I_D}{S}}{\frac{W}{S}\cdot\frac{L}{S}} = \frac{I_D \times S}{\text{Area}}$$

$$\boxed{J' = J.S}$$

Power density $= \frac{P'}{\text{Area}} = \frac{\frac{P}{S^2}}{\frac{\text{Area}}{S^2}} = \boxed{\frac{P}{\text{Area}}}$ —(3M)

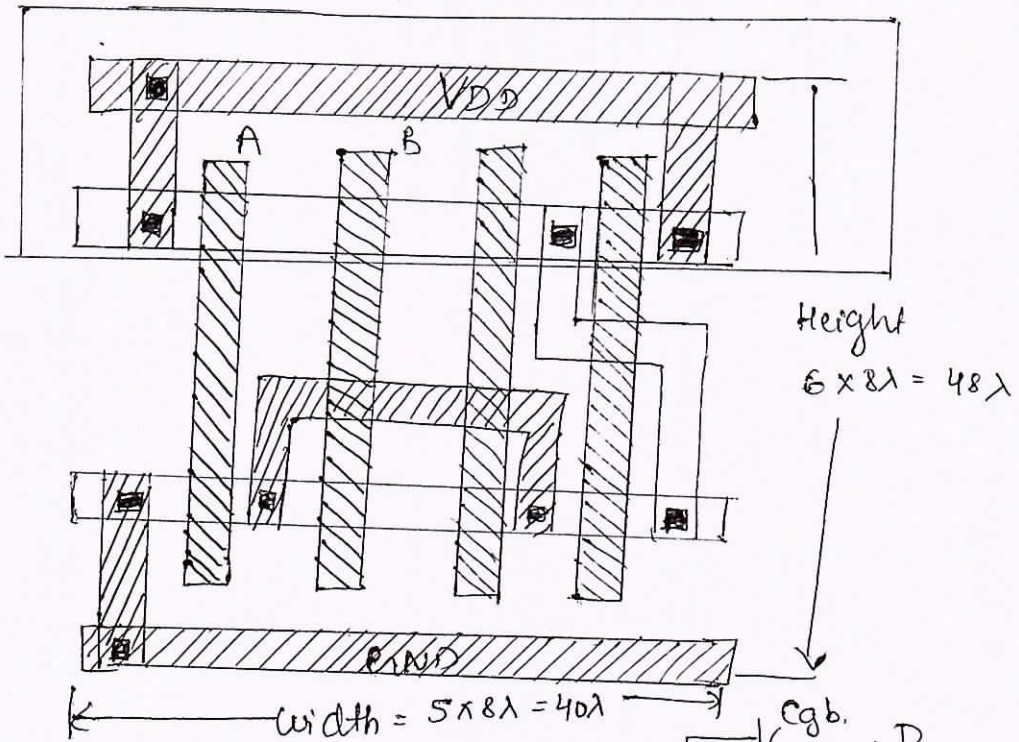
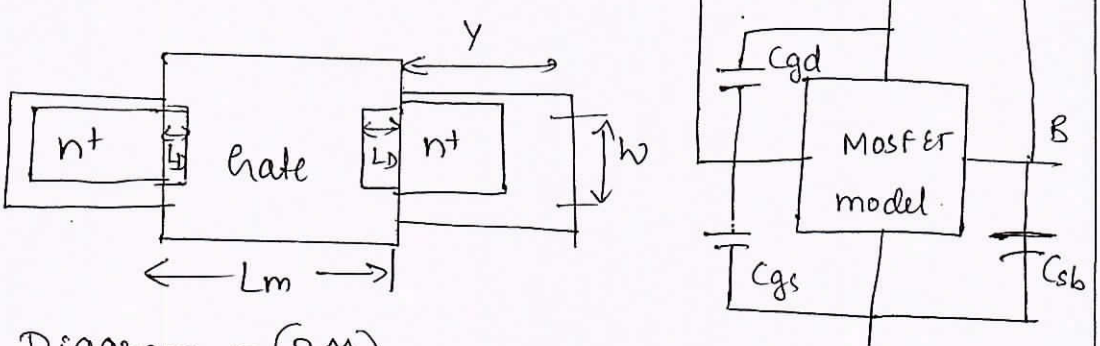
Constant Voltage scaling

Current $= I_{D(lin)}' = \frac{kn'}{2}\left[2(V_{GS}' - V_{T_0}')V_{DS}' - V_{DS}'^2\right]$

$$I_D' = \frac{S.kn}{2}\left[2[V_{GS} - V_{T_0}]V_{DS} - V_{DS}^2\right] = \boxed{S\, I_{D(lin)}}$$

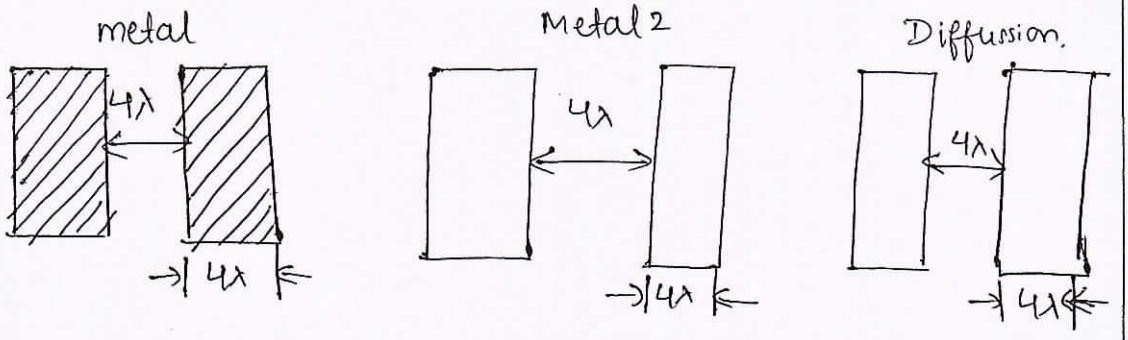
$$\text{Current density} = \frac{I_D'}{\text{Area}} = \frac{S.I_D}{\frac{\text{Area}}{S^2}} = \boxed{\frac{S^3 . I_D}{\text{Area}}}$$

$$\text{Power density} = \frac{P'}{\text{Area}} = \frac{I_D' V_{DS}'}{\text{Area}'} = \frac{S.I_D.V_{DS}}{\text{Area}/S^2} = \boxed{\frac{S^3.P}{\text{Area}}}$$ —(3M)

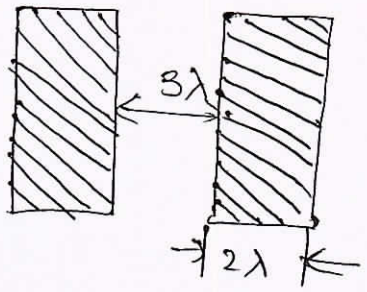
Q.No.	Solution and Scheme	Marks
4a)	Layout diagram of $Y = \overline{(A+B+C)D}$ — (5M) Area estimation — (2M) Schematic — (1m) 	08
4b)	 Diagram — (2M) Explanation of oxide related capacitances with Cgb, Cgs & Cgs equations — (02 M). Explanation of junction capacitance with five junction capacitance indication — (02 M)	

Q.No.	Solution and Scheme	Marks

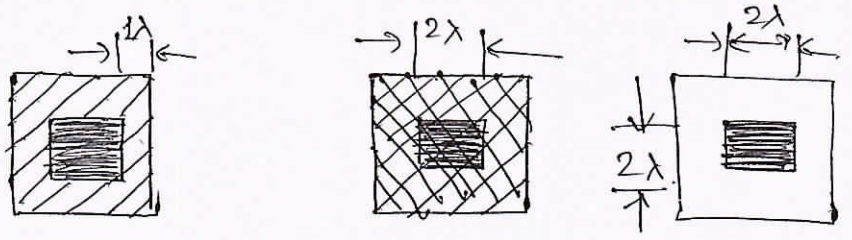
4C) Explanation of design rules for wires —— 4m



Polysilicon.



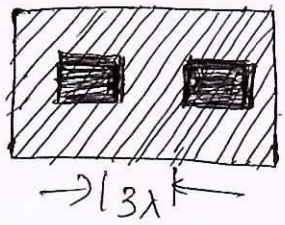
Explanation of design rules for contacts —(2M)



Metal 1 to diffusion

Metal to polysilicon.

Metal 1 to Metal 2.



02

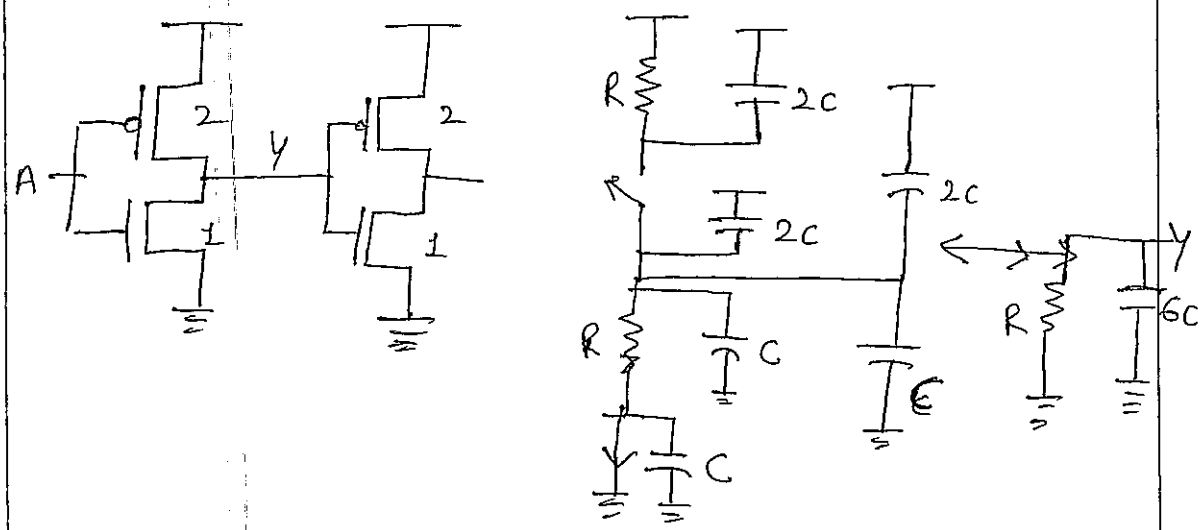
Q.No.	Solution and Scheme	Marks

Module – 3.

5a) Explanation of effective resistance capacitance with necessary notations — (02 M)

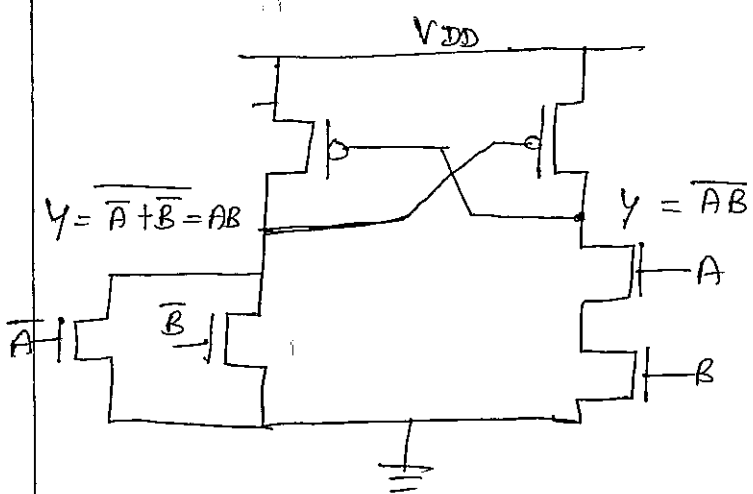
Explanation of gate and diffusion capacitance with necessary notations — (02m)

equivalent circuit ——— (04m). 05



5b) Explanation of cascade voltage switch logic —(03 M).

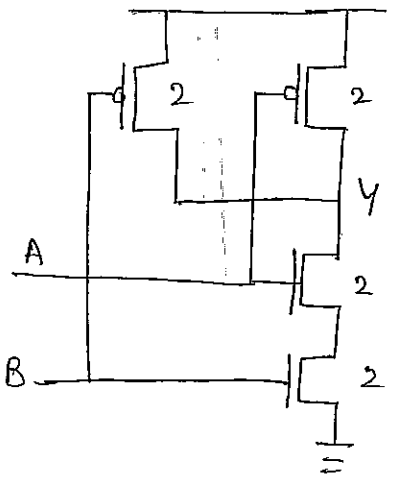
Two input AND / NAND using CVSL — (03 M). 06



Q.No.	Solution and Scheme	Marks
5C)	Explanation of linear delay model with the equation $d = f + p$ ——— (02M).	06

Logical effort computation

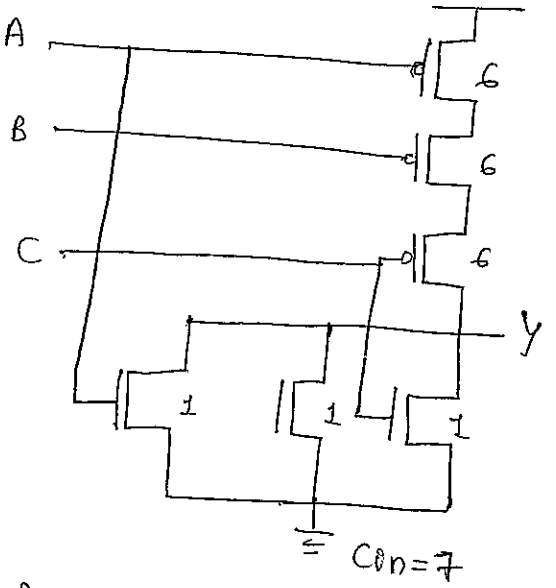
2 i/p NAND



$C_{in} = 4$

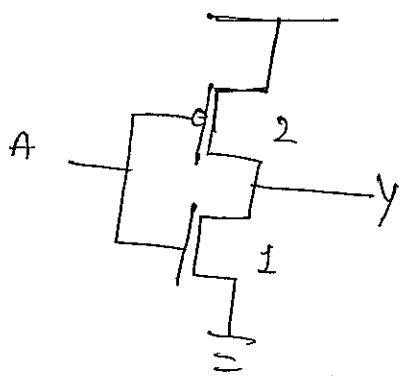
Logical effort $g = \frac{4}{3}$ (02M)

3 i/p NOR



$g = \frac{7}{3}$ ——— (02M)

Unit sized inverter



$C_{in} = 3$

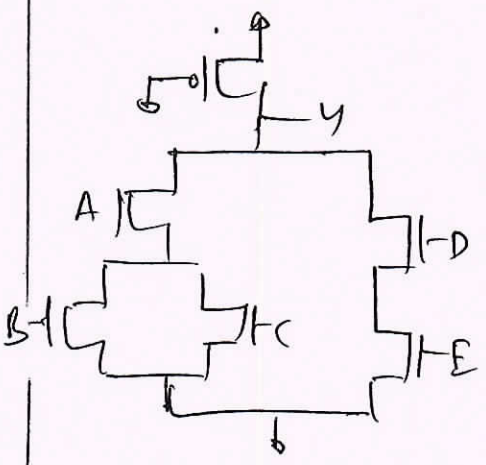
6. a Explain i) pseudo-nmos ii) ganged CMOS with necessary circuit examples 6M

Sol:

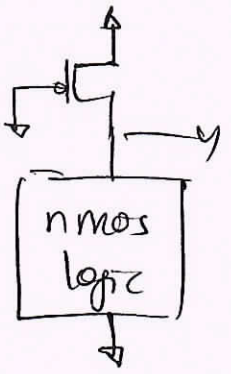
Pseudo nmos

A modified version of CMOS technology is known as pseudo nmos., in which Pmos is used as load instead of depletion nmosfet.

Ex $Y = \overline{A(B+C)+DE}$



General form



2M

This is a ratioed logic where adequate ratio for $\frac{\beta_{driver}}{\beta_{load}}$ is selected. It has only n+1 transistors.

In addition the capacitive load on each i/p is one unit as one transistor is used for each i/p.

Pseudo nmos has higher speed & low area. 3M

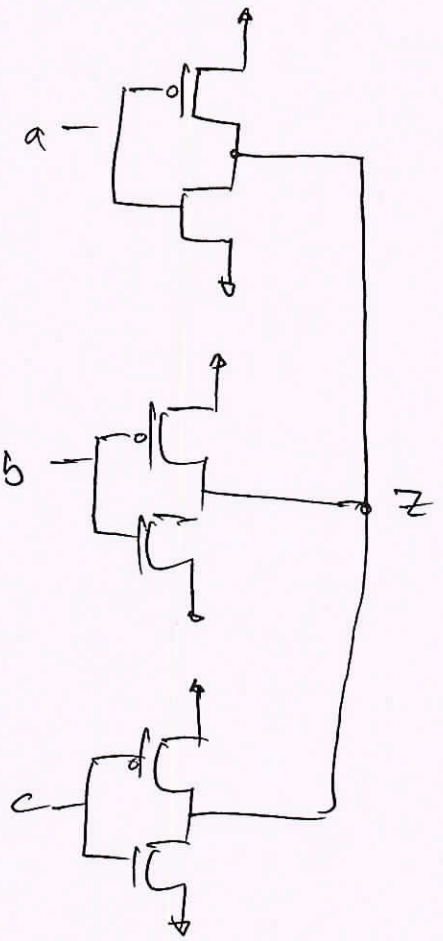
Ganged CMOS

In this type of circuit when $\beta_{driver}/\beta_{load}$ is equal to unity, then the circuit becomes destructive in nature. The o/p is '1' when i/p is 000 & o/p is '0' when i/p is 111. But for any other combinations V_{DD} gets shorted to V_{ss} hence $\beta_{driver}/\beta_{load} \neq 1$.

6. a
Continued

When the ratio is greater than unity the pull down transistor will have higher sinking ability thus ckt works as NOR

When ratio is greater than unity, then pull down has lesser sinking ability, then ckt behaves as Nand



$\frac{\beta_{driven}}{\beta_{load}} > 1 \quad Z = \overline{a+b+c}$

$\frac{\beta_{driven}}{\beta_{load}} < 1 \quad Z = \overline{a.b.c}$

im

//

6. b. Estimate t_{pdf} & t_{pdr} of a 3:1p Nand gate if the o/p is loaded with h identical gates. Use Elmore model — 8M

Soln

Each nand gate load presents 5 units of Cap capacitance on a given i/p.

Figure below shows the equivalent ckt including load for the falling transition.

Node n_1 has 3C Capacitance & Resistance of $R/3$ — 3M

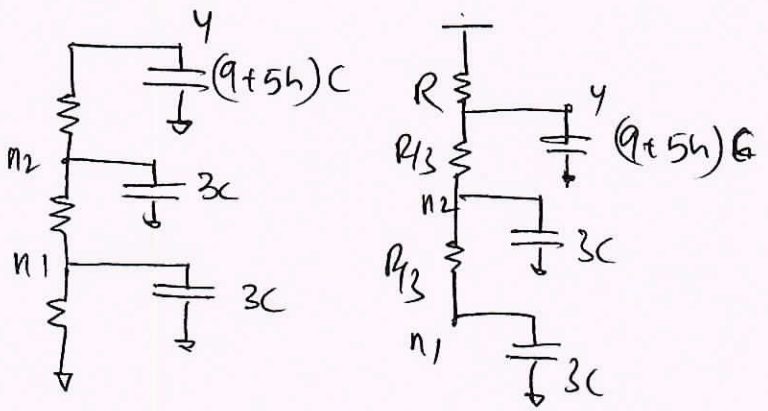
Node n_2 = 3C $R = R/3 + R/3$

node y $\Rightarrow (9+5h)C$ $R = R/3 + R/3 + R/3$

∴ Elmore delay model for falling o/p is sum of three RC products

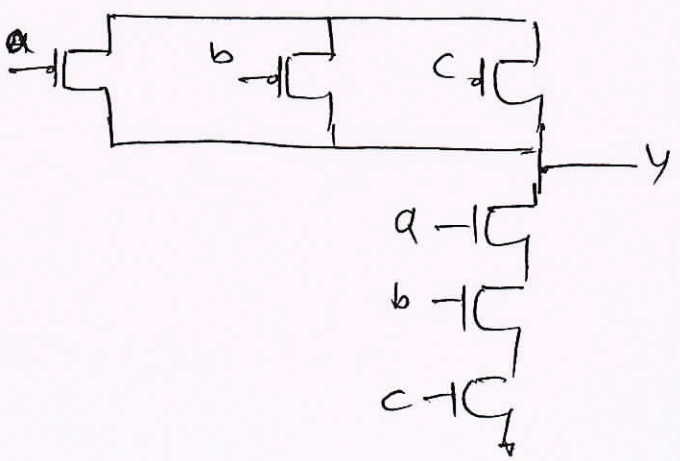
$$t_{pdf} = 3C\left[R/3\right] + 3C\left[R/3 + R/3\right] + (9+5h)C\left[R/3 + R/3 + R/3\right]$$

$$\boxed{t_{pdf} = (12+5h)RC}$$



3M

3:1p nand gate =>



6c. Explain Skewed gates with an example. 6M

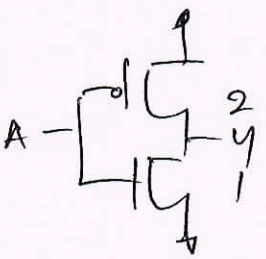
Sol:) If one of the i/p transition is more than the other, it results into a phenomenon known as skewing.

Hi skew = gates favor the rising o/p transition

Lo-skew gates favor falling o/p transition

Example

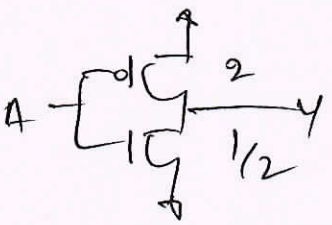
inverter unskewed



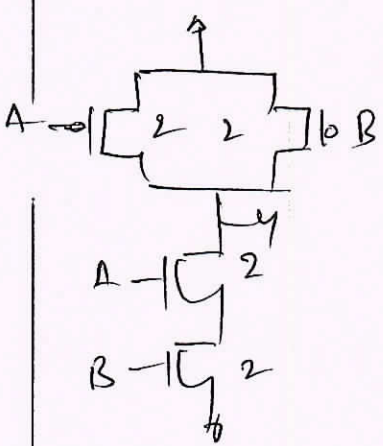
3M

Lo skew

Hi skew

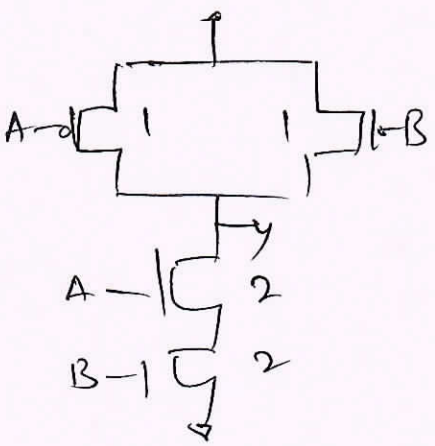


nand gate

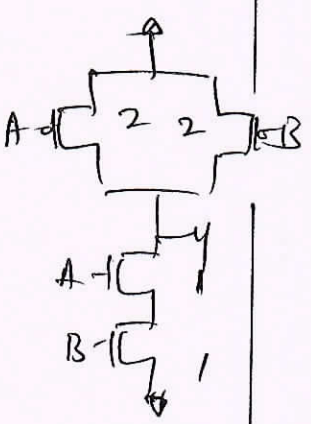


unskewed

Lo skew



Hi skew

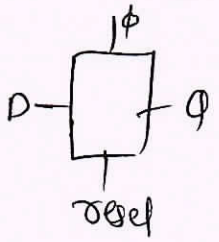


3M

7-a. With necessary circuit diagrams, explain resettable latches with i) Synchronous reset ii) asynchronous reset — 8M

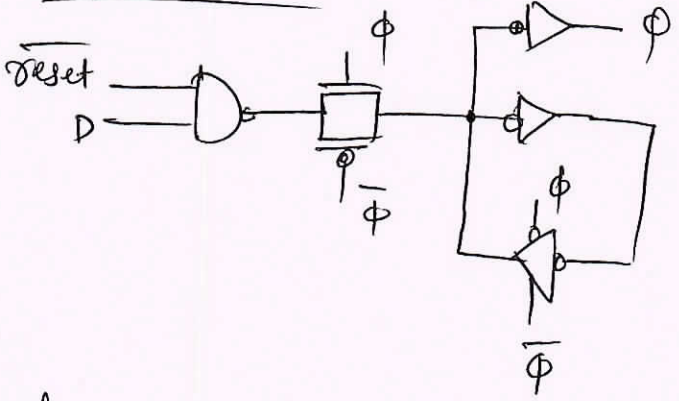
Sol:

Symbol



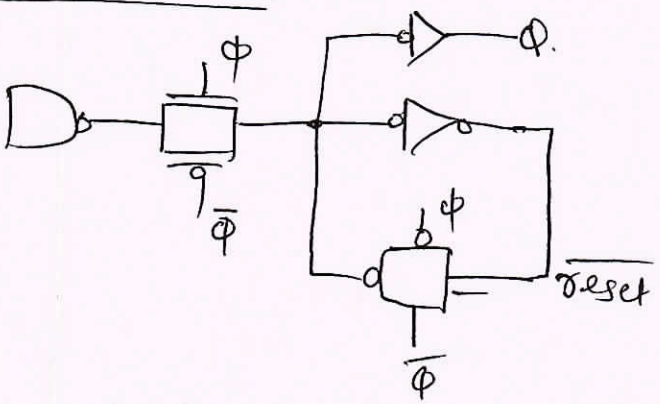
1M

Synchronous reset



2M

Asynchronous reset



2M

Most practical sequencing elements require a reset signal to enter a known initial state on startup. There are two types of reset mechanism Synchronous & asynchronous.

3M

Asynchronous forces Q low immediately while synchronous reset waits for the clock.

7.a Continued

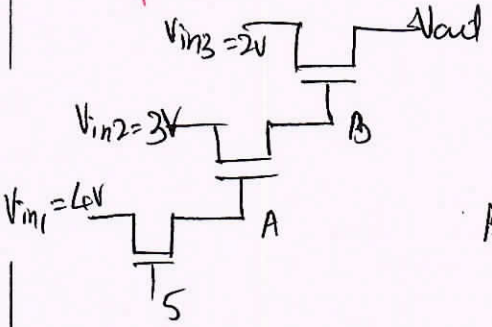
Synchronous ~~rest~~ reset must be stable for a setup & hold time, while the asynchronous reset is characterized by propagation delay

Synchronous reset is simply requires ANDing the D i/p with $\overline{reset}$.

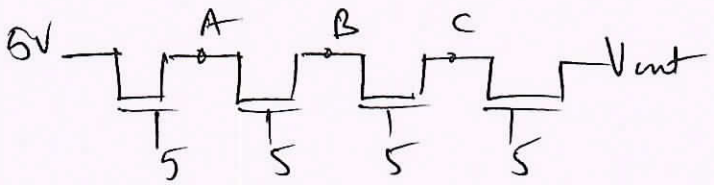
Asynchronous reset requires gating both the data & the feedback to force the reset independent of Clock.

7.b Compute the o/p in the following pass transistor. Assume $V_t = 0.7\,V$. 6M

Soln:



A = 4 B = 3 $V_{out} = 2V$ // 3M



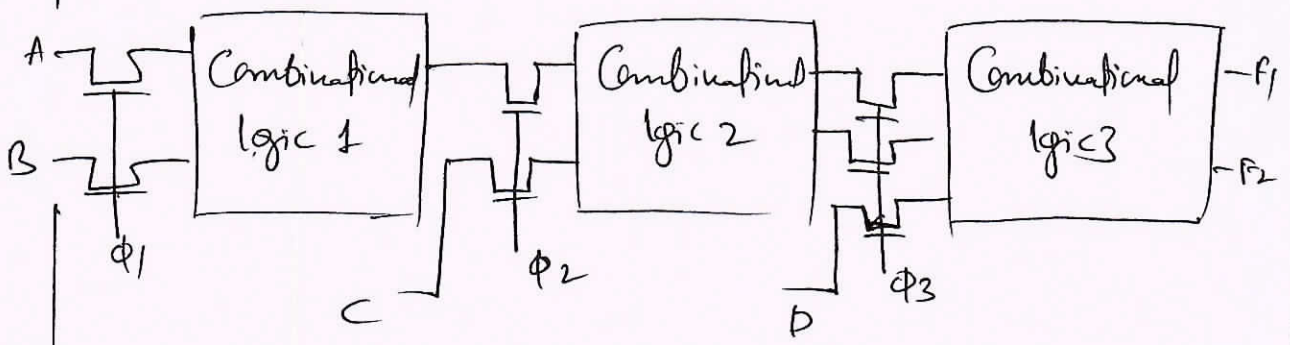
3M

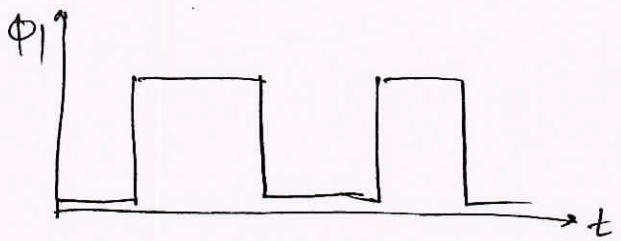
A = 4.3 B = 4.3 C = 4.3 ~~Vout~~

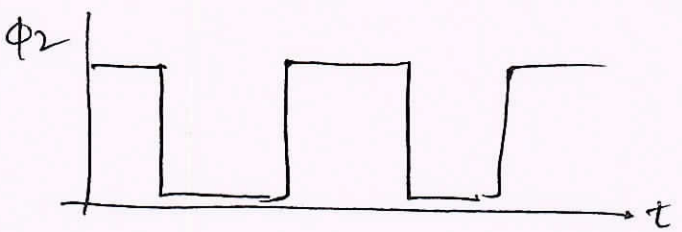
$V_{out} = 4.3V$ //

7.c With necessary diagram, explain D flip flop with two phase overlapping clocks. 6M

Sol^n The non overlapping property of the 2 clock signals guarantees that at any given time, only one of the two clock signals can be active.







When clock 0 is active, the i/p levels of stage 1 & stage 3 are applied through the pass transistors while the i/p capacitances of stage 2 retain their previous values.

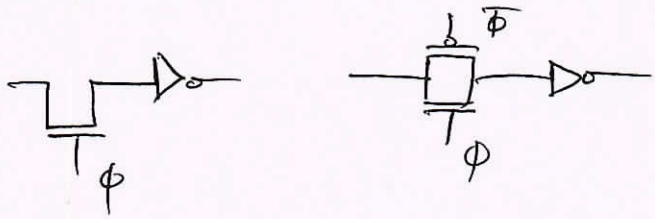
This allows us to incorporate the dynamic memory

Ex 3 stage depletion load nmos dynamic shift register.

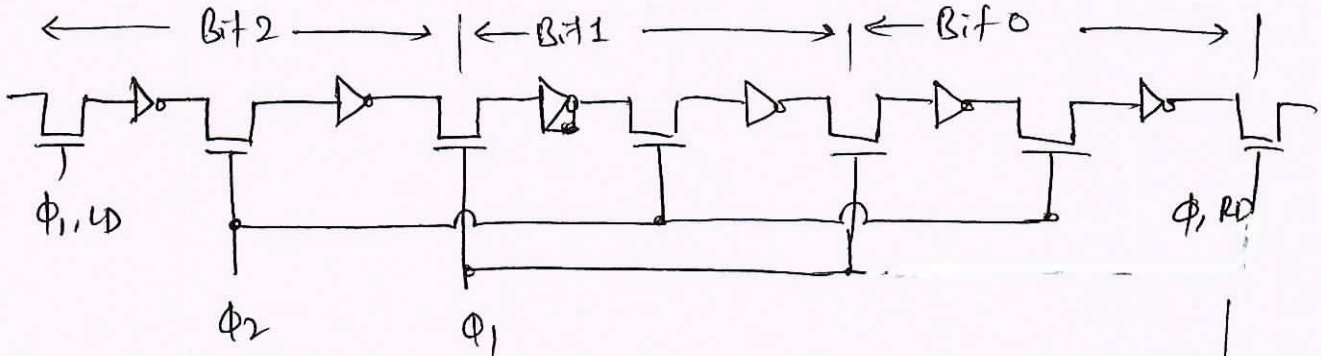
//

8.a With necessary diagram explain 3 bit shift register (dynamic) 8M

Soln Figure shows a simple ~~dynamic~~ register element in both nmos & cmos versions



using the dynamic register elements, a dynamic shift register can be constructed. A three bit shift register is as shown below.



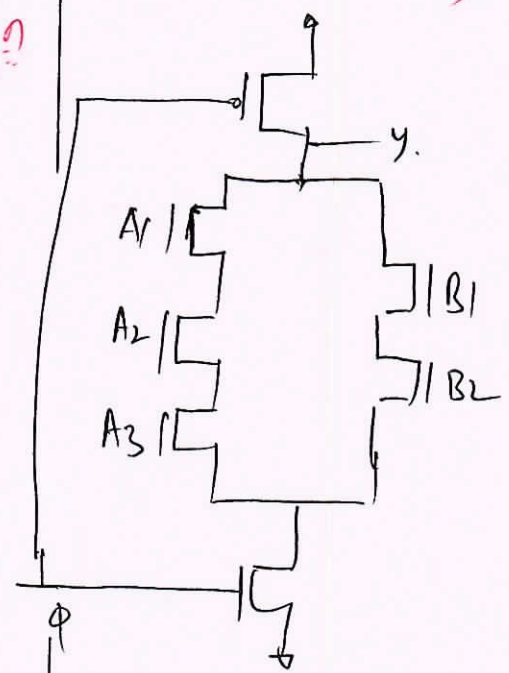
Here LD. = Load and RD = Read. The cmos version uses transmission gate:

When ϕ_1 = high the i/p bit gets transmitted to inverting buffer when ϕ_2 = high then the bits are stored & thus the 3-bit shift register behaves as memory.

Upon subsequent non-overlapping clocks ϕ_1 & ϕ_2 the data can be shifted out at the o/p side.

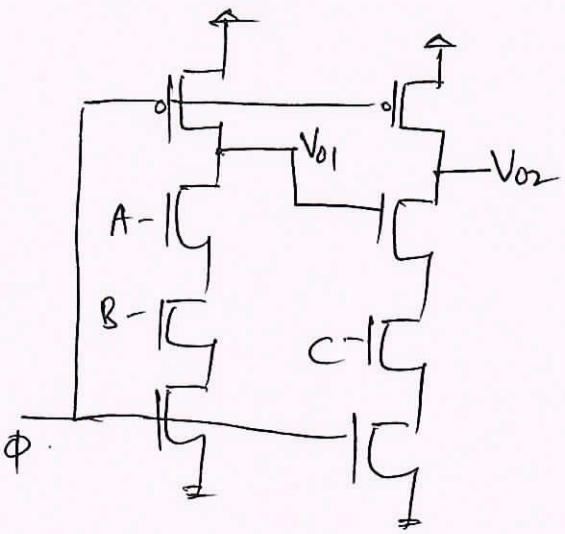
8.b Realize $F = \overline{A_1A_2A_3 + B_1B_2}$ using dynamic CMOS logic. Also explain the cascading problem in dynamic logic with necessary example. 8M

Sol:



Cascading problem

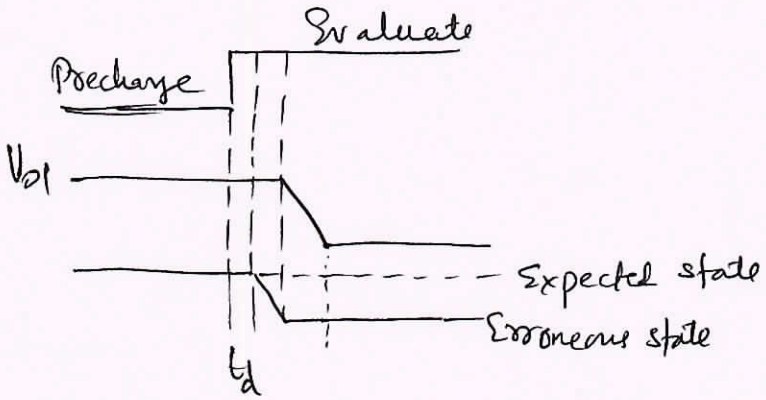
Consider a two i/p nand gates being cascading one after the other using the dynamic logic 2M



2M

Let A = B = C = 1

When the i/p are all '1' the waveforms & the above ckt looks like.



2M

According to the given i/p $V_{O1} = 0$ & $V_{O2} = 1$. But here the second o/p will not be in the expected state. The reason is V_{O1} will not go low until its Capacitance is discharged completely

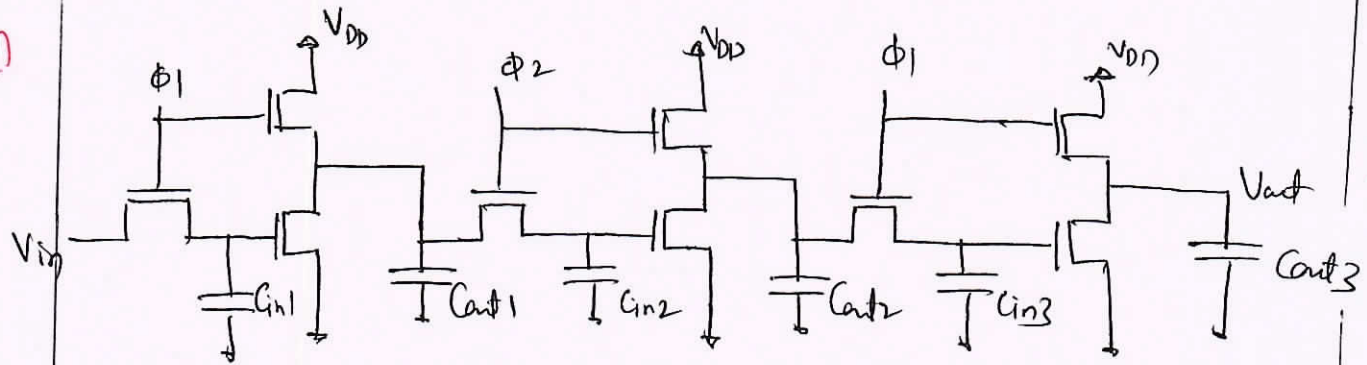
8.b Continued

Hence there will be a small propagation delay But as C=1, V_{O2} will go low. It will not go high until next precharge phase. Thus we have an erroneous o/p. 2M

This problem is solved by adding a delay to the 2nd stage., thus making the dynamic ~~logic~~ logic to go for extra gate.

8.b Explain the general structure of ratioless synchronous dynamic logic with relevant diagram 4M

Sol:-



2M

~~In~~ Under ratioed logic the valid o/p voltage of each stage is strictly determined by driver to load ratio.

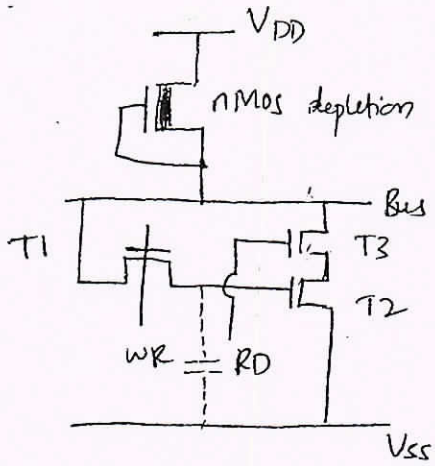
Under ratioless synchronous logic in order to correctly transfer a logic high level after charge sharing the ratio of the capacitors C_{out}/C_{in} must be made large enough during circuit design 2M

Since the valid logic low of $V_{out} = 0V$ can be achieved regardless of driver to load ratio, this ckt arrangement is known as ratioless dynamic logic. //

9.a) With necessary ~~circuit~~ ~~10.2~~ circuit diagram, explain 3T DRAM

Sol:- 3-T Dynamic RAM cell

(8M) 8



2M

WRITE Operation

When WR=1, RD=0 then T1 is ON. The content present on Bus will be stored as charges on gate capacitance of T2.

1M

READ operation

When WR=1, RD=0, If any value is written as charge on gate capacitance of T2, in the previous cycle, then it can be read via transistor T1 & Bus.

Again, we can read the value stored in its previous cycle on T2 by making WR=0 & RD=1.

2M

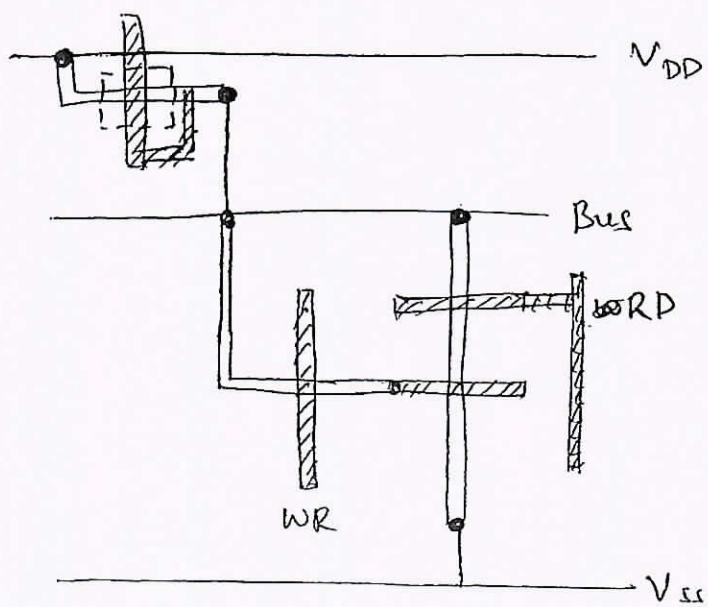
When RD=1 then T3 is ON & T2 will also be ON coz of charge present in gate capacitance. Thus T3 & T2 both are ON & they form a closed circuit to ground. And the bus gets connected to ground via T2 & T3.

Hence 0 will be read in place of 1.

Capacitor value	WR	RD	Operation	Remarks
initially 5V	0	0	Hold	Since the gate capacitance has 5V in it (T2) That value will be held as it is
↓ 0V	0	1	Read	Bus is pulled to ground & logic 0 is read for logic 1. (0V is read for 5V)
↓ 5V	1	0	write/ Read	Write into the gate capacitance of T1 or Read through T1 if any prior value is present.
↓ 0V	1	1	Read	Read from T1 in uncomplimented form or Read through T2 & T3 in complimented form

3M

layout

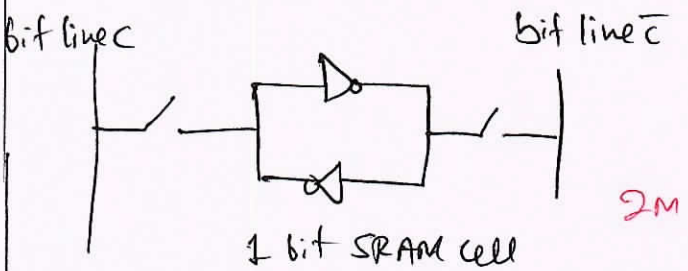


9.b Explain full CMOS SRAM cell with necessary ckt topology 8M

Soln SRAM memory ckts are designed to permit the modification of data bits to be stored in array as well as retrival on demand. 2M 8M

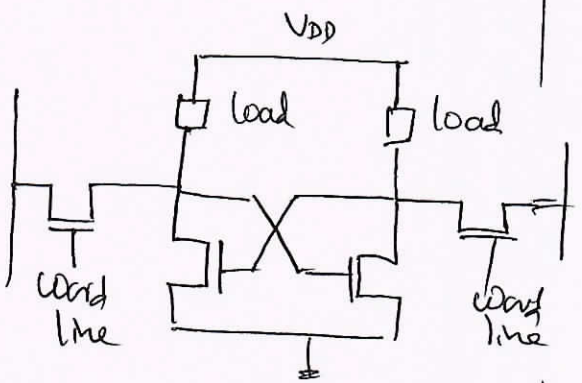
Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or '1'

Usually two ~~other~~ nmos pass transistors are implemented to connect the 1-bit SRAM cell to the complementary lines.

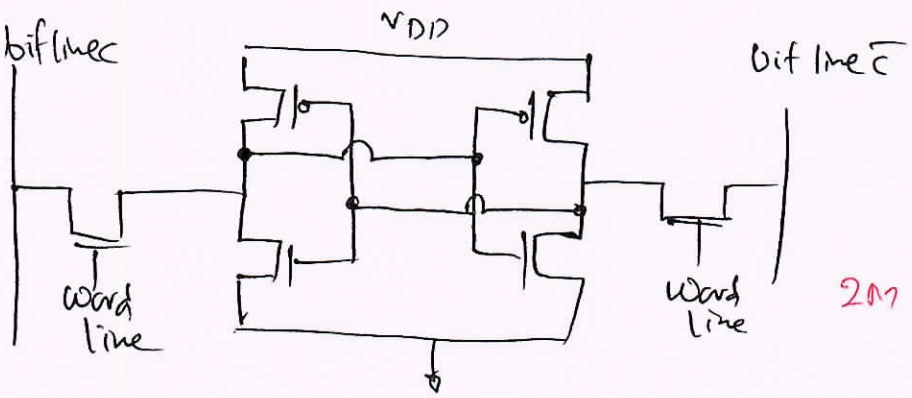


2M

(a) Symbolic representation



(b) generic circuit topology 2M



2M

Full CMOS SRAM cell

The load may be polysilicon resistors, depletion-nmos or pmos depending on type of memory.

9.b Continued..

The use of resistive load inverters with undoped polysilicon resistors in the latch structure typically results in a significantly more compact cell size compared with other alternatives.

- using a depletion load nmos will have better noise margin characteristics & lesser area

9.c Explain the terms i) observability (ii) Controllability (iii) Fault Coverage 4M

So/n The observability of a particular circuit node is the degree to which you can observe that node at the outputs of an integrated circuits.

Controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state. This metric is of importance when assessing the degree of difficulty in testing a particular signal within a circuit

Fault coverage is a measure of goodness of a set of test vectors. For the vectors applied what percentage of chip are covered for various faults are considered here //

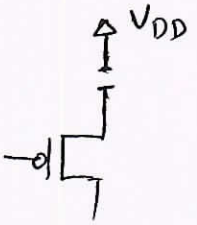
10.a What is a fault model? Explain stuck-at-model with examples 7M

Sol?

Fault model is used to identify various types & faults that arise post manufacturing & are one of most promising model indentifying various types & of faults. 1M

There are 2 types of stuck at faults
- Stuck at open/closed
- stuck at 1/0 2M

Stuck at open/closed



Consider a simple P-mosfet. The Source of Pmos was supposed to be connected to V_{DD} but due to some error, the line connecting V_{DD} is open this results into an open ckt bet Source & V_{DD} resulting in high impedence. 2M

Stuck at closed

These faults are very critical when we go for Combinational to Sequential circuit conversion

Stuck at faults = Stuck at 1/0 2M

Ex S-A-1

Consider a nand gate the i/p A is stuck at 1 which means, the value of A will be always held at '1' irrespective of any i/p to A.

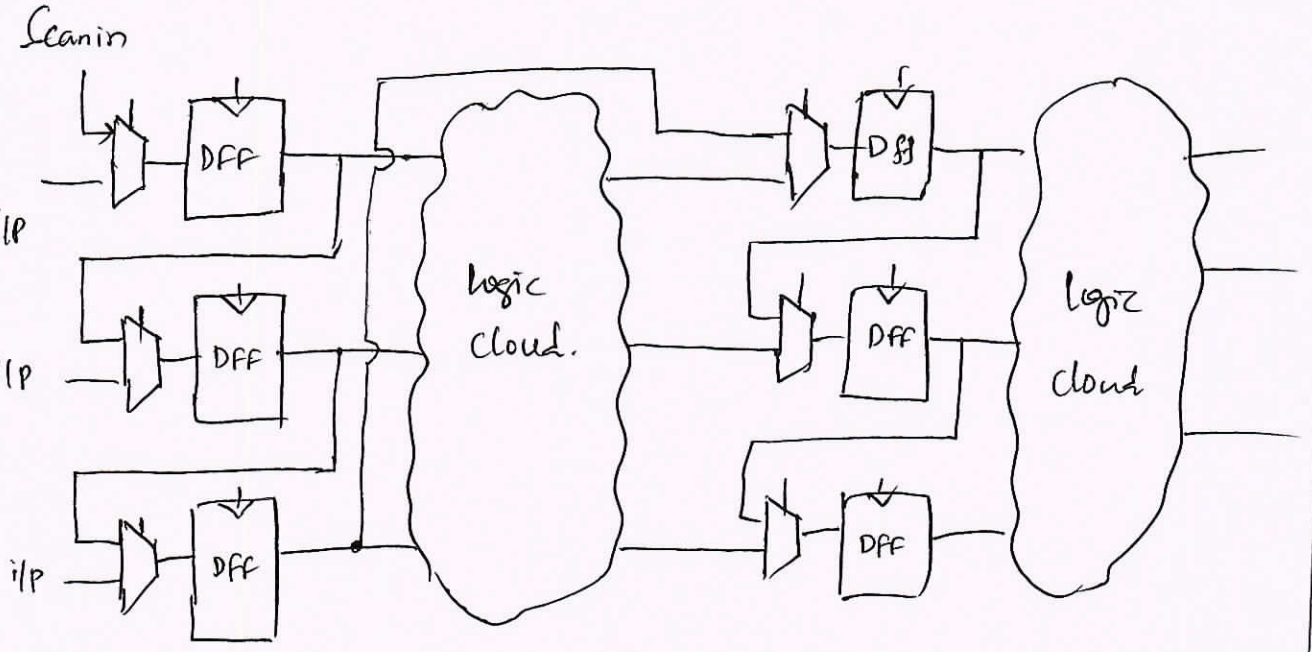
This may be due to a small metallic connection between pin A and VDD. This must be modelled To model this we will be using various fault models.

10.b Mention the approaches used in design for testability. Explain scan based testing using necessary diagram 7M

Sol/n There are 3 approaches in DFT
- Adhoc testing
- Scan based approaches
- Built in Self test

1M

Scan based testing



3M

The Scan based strategy has evolved to provide observability & controllability at each register.
- Here scan registers are used - The scan register is a D flip flop preceded by a multiplexer 3M
- When scan signal is deasserted, the register behaves as a conventional register, storing data on D i/p.

10.b Continued.

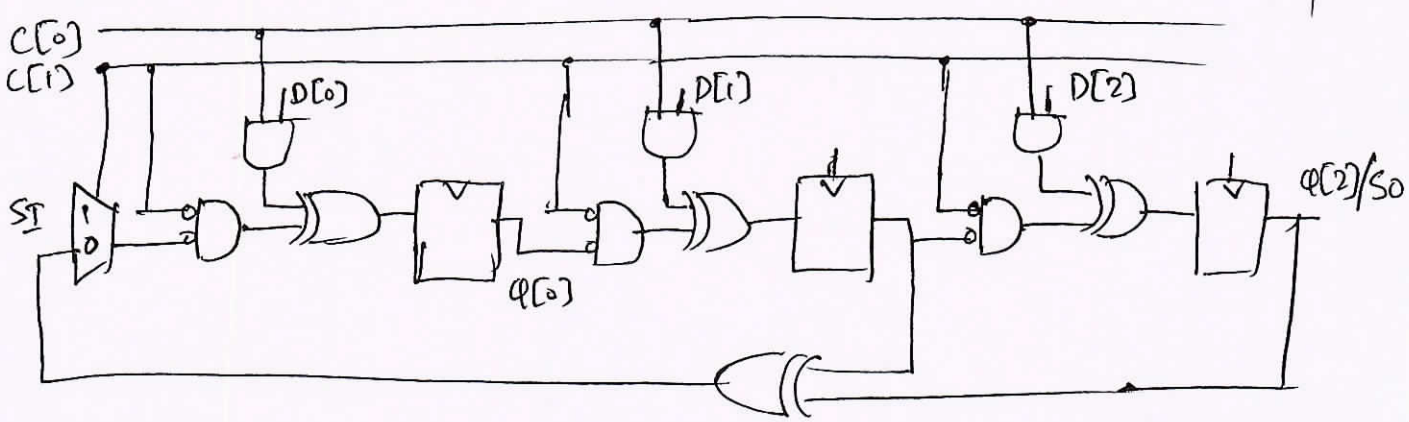
When SCAN is asserted, the data is loaded from the SI pins, which is connected in shift register fashion to the previous Q o/p in Scan chain.

- For the ckt to load the Scan chain, SCAN is asserted & CLK is pulsed 8 times to load the first two ranks of 4 bit registers with data.
- SCAN is deasserted & CLK is asserted for one cycle to operate the ckt normally with predefined i/p.

10.c Draw the circuit of 3 bit BIST register & explain GM

Soln:

3- bit BIST



- The combination of signature analysis & the scan technique creates a structure known as BIST i.e built in self test.
- The 3 bit BIST is shown in figure is a Scannable, resatable register that also can serve as a pattern generator & signature analyzer.
- In normal mode the flip flops behave normally with their D i/p & Q o/p.
- In scan mode the flip flop work as 3 bit shift register.

10.c

Continued...

- If all D i/p are held low, Q o/p loops through a pseudorandom bit sequence which ~~save~~ serve as i/p to combinational logic.
- BIST is performed first by resetting the syndrome in the o/p register. //