Model Question Paper-I/II with effect from 2022-23
(CBCS Scheme)

USN

First/Second Semester B.E. Degree Examination
BASIC ELECTRONICS
(MODEL QP)

Max. Marks: 100

TIME: 03 Hours

Note: Answer any FIVE full questions, choosing at least ONE question from each MODULE.

		Module -1	PO	CO	*Bloom's Taxonomy Level	Marks
Q.01	a	Explain the Forward and Reverse Characteristic of Semiconductor Diode.	1,2	1	2	8
	b	Explain Positive Half Wave Rectifier with input and output waveforms.	1,2	1	2	6
	c	Explain Zener Diode as Voltage Regulator with no load.	1,2	1	2	6
		OR				
Q.02	a	Explain RC π filter.	1,2	1	2	8
	b	Explain DC load line analysis for Semiconductor Diode.	1,2	1	2	8
	c	Write down the characteristic of Zener Diode.	1,2	1	2	4
		Module-2				
Q. 03	a	Explain BJT Current Amplification for increasing and decreasing IB Levels.	1,2	2	2	8
	b	Explain Common Base Input Characteristic of BJT.	1,2	2	2	6
	c	Explain the working of n channel JFET.	1,2	2	2	6
		OR				
Q.04	a	Explain the operation of enhancement MOSFET.	1,2	2	2	8
	b	Draw the DC load line for transistor and identify Q points.	1,2	2	2	8
	c	Explain Common Emitter Input Characteristics.	1,2	2	2	4
		Module-3				
Q. 05	a	Explain block diagram of Typical OpAmp.	1,2	3	2	6
	b	Explain working of a Differential Amplifier	1,2	3	2	8
	c	Explain OpAmp as an integrator circuit with an input and output waveform using square wave as input.	1,2	3	2	6
		OR				
Q. 06	a	Explain basic Differential Amplifier	1,2	3	2	8
	b	Define Op Amp Parameters. Gain, CMRR, Slew rate, input resistance	1,2	3	2	8
	c	Explain Inverting Amplifier.	1,2	3	2	4
		Module-4				
Q. 07	a	Convert Decimal to Binary : 1) 41, 2)153, 3) 0.6875,4) 0.513	1,2	4	2	8
	b	Write down Axiomatic Definition of Boolean algebra.	1,2	4	2	6
	c	Simplify the Boolean function to minimum number of literals (xy+ x'y+yz) (x'y+ x(y+z) + y'z')	1,2	4	2	6
		OR				
Q. 08	a	Convert Binary to Decimal I) 110111, 2) 10101010, 3) 0110, 4) 100.1010	1,2	4	2	8
	b	Explain SOP & POS with examples.	1,2	4	2	6
	c	Implement Half adder using basic gates.	1,2	4	2	6

		Module-5				
Q. 09	a	Explain the working principle of Capacitive Transducer.	1,2	5	2	8
	b	Explain the working principle and applications of Piezoelectric Transducer.	1,2	5	2	8
	c	Write down the applications of Thermal Transducer.	1,2	5	2	4
		OR				
Q. 10	a	Explain typical Radio Transmitter with neat block diagram.	1,2	5	2	6
	b	What is modulation? Explain the need for Modulation.	1,2	5	2	8
	c	What is noise? Explain the term Channel Noise and its effects.	1,2	5	2	6

-------------x-------------x-------------x-------------x-------------

Q1a) Explain Forward and Reverse Characteristics of Semi-conductor diode.

Sol⁰: Assuming the diode to be as a silicon diode, let us discuss the forward and reverse characteristics of diode.

A diode can be biased in two ways,

(i) Forward Bias:

When P type of diode is connected to +ve of the supply and N type of diode to -ve of the supply, then biasing is refered to as a forward biased diode configuration, and characteristics under such biasing condition are refered to as Forward Characteristics.

* Forward Bias condition
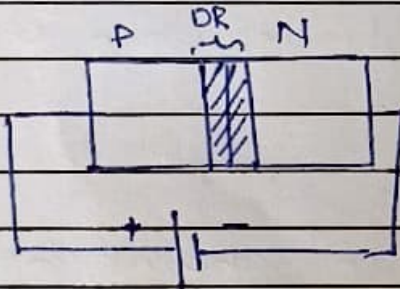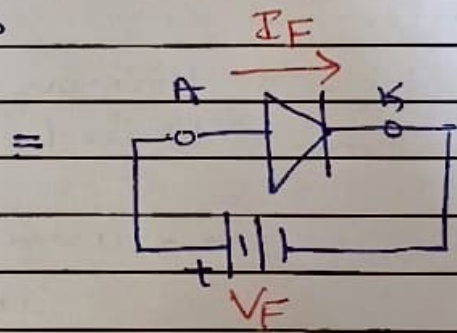
Fig 1   Fig 2

* Observations:

From layer diagram, we can observe that - the width of depletion region is going to decrease as V_F crosses the knee voltage (V_K), as a result of which the forward current also increases, Following Figure 3 shows the Forward characteristics of diode
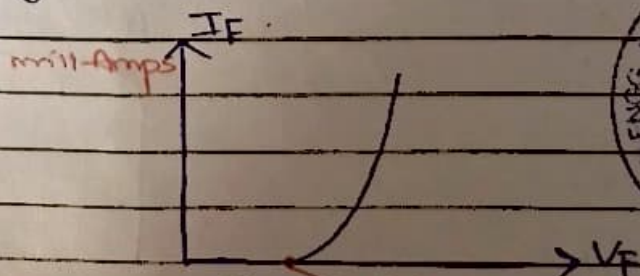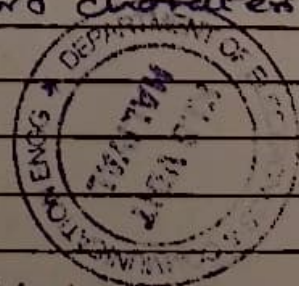

Fig 3

Teacher's Sign.

Q1a.... From Fig 3, Following characteristics are noted.

* **Knee Voltage (V₁s):** It is the amount of forward voltage needed to be applied across the diode due to which width of Depletion region decreases and hence forward current (IF) increases.

* **Forward voltage (VF):** It is the biasing voltage applied across the diode (P to +ve, N to -ve) such that it causes the diode to be in forward bias condition, typical value as 0.7v for Si and 0.3 for Ge, hence allowing the current flow from P to N.

* **Forward Current (IF):** It is the forward current flowing through the diode when the diode is forward biased.

Reverse Characteristics:

It is the characteristics of the diode observed, when diode is reverse biased i.e. P type connected to -ve of the supply and N-type connected to +ve of the supply. The layer diagram, device connection and characteristics are shown in Fig 4 through 6.

Fig 4   D.R

Fig 5

Fig 6
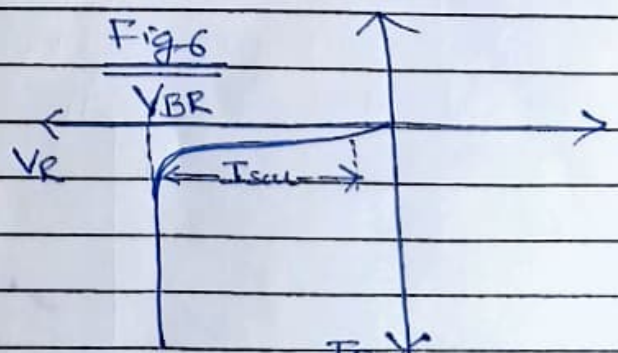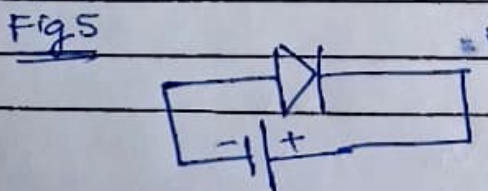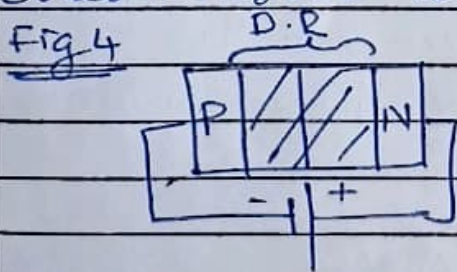
Q1a.. (Isat) : It is the constant reverse current, which flows through the diode during the reverse bias condition of the diode.

(VBR): Reverse breakdown voltage is the reverse bias voltage applied across the diode, for which the reverse current of the diode increases drastically, typical values are -50 to -70 V

Q1B> Explain Positive Half wave rectifier with input and output waveforms.

Sol⁰: A rectifier ckt is the one which can convert an AC signal into pulsating DC signal, A positive H.W.R is also a typical rectifier ckt which uses only one diode to convert AC to pulsating DC signal. Let us assume the diode under consideration is an Ideal diode and understand the operation.
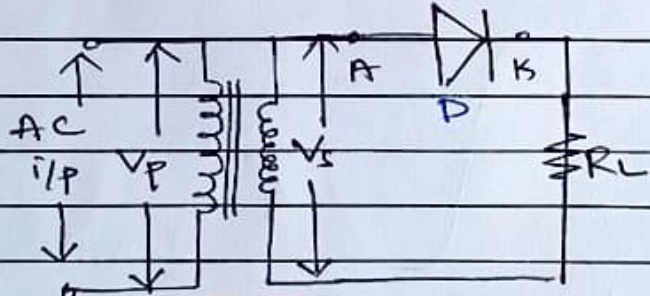
Circuit Diagram During +ve half of i/p signal

Fig 7

Fig 8

Fig 7, Shows that During +ve half of i/p signal, the polarity across secondary of transformer is + and - which makes, Diode D in forward state, hence it acts like a closed switch, and forward current flows through RL
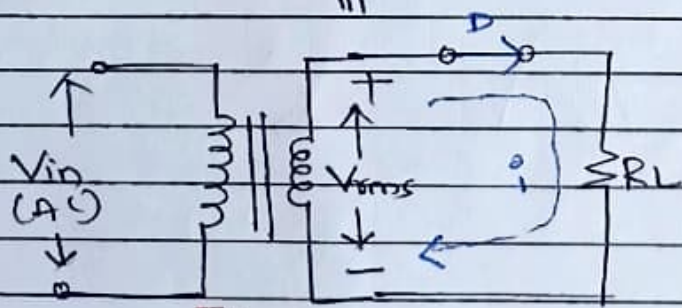
Q1B:— Now let us consider the condition during -ve half of the i/p signal

→ During -ve half of i/p signal, the polarity across secondary of transformer will be - and +, hence as a result of which diode "D" will be reverse biased and no current flows through the diode as it acts like an open switch, It is shown in Fig 9 and 10
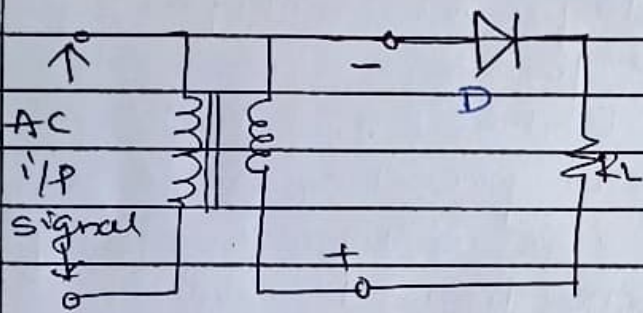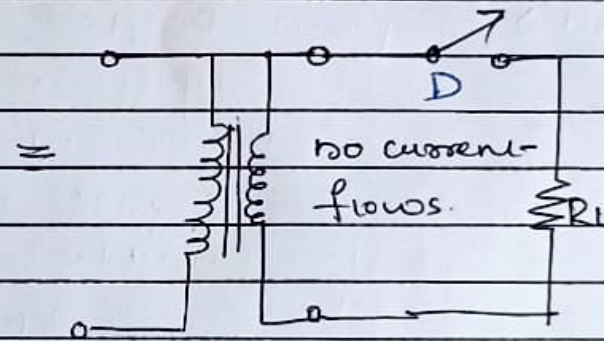

Fig 9   Fig 10
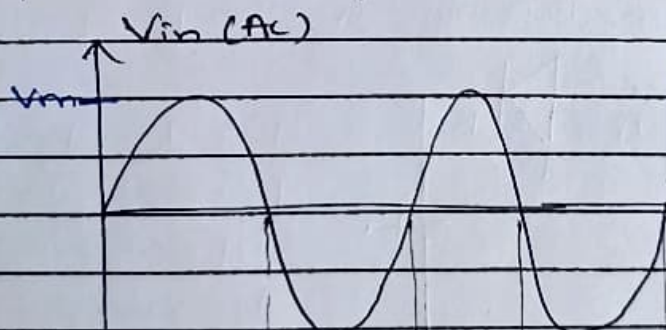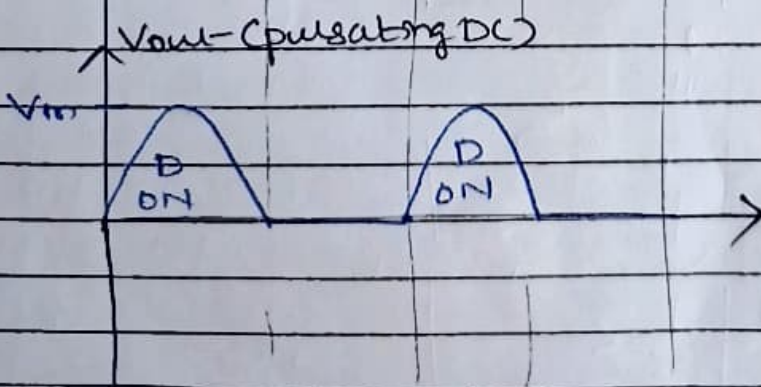
Input and output waveforms (Fig 11 and Fig 12)

Fig.11

Fig.12

Q1c | Explain Zener Diode as a voltage regulator with no load

Sol⁻: Regulator CKt With No Load.
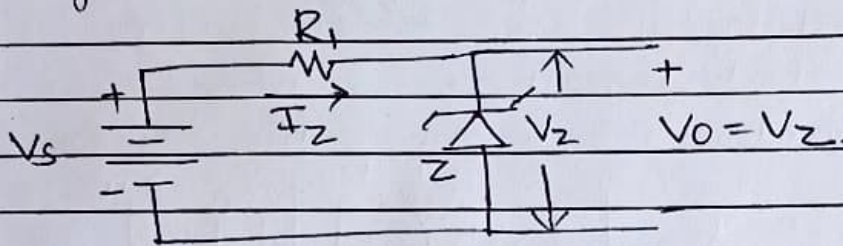

Fig 13.

Fig 13 Shows the CKt for A Zener diode as a voltage Regulator with no Load. From CKt, we can write

$$I_z = \frac{V_s - V_z}{R_1} \quad -①$$

The above CKt acts like a regulator whenever $V_s > V_z$, hence keeping V_z inturn V_{out} constant

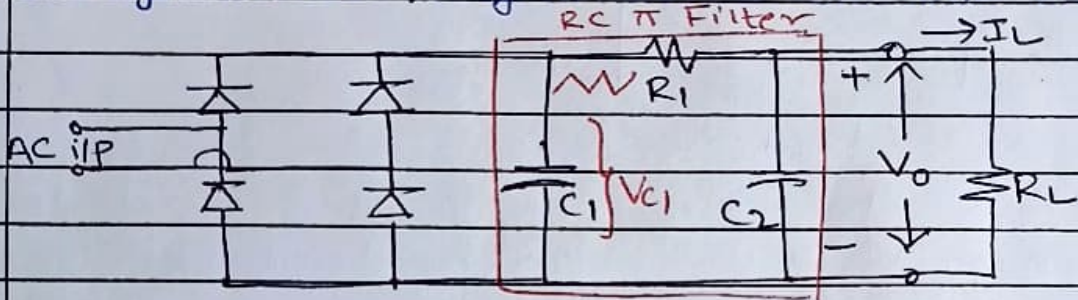Example: If $V_z = 9.1V$, and if $I_{zT} = 20mA$, with $V_s = 30V$; $R_1 = \dfrac{V_s - V_z}{I_z} = 1.05K\Omega$.

when $V_s = 27V$; $I_z = \dfrac{27 - 9.1}{1K\Omega} = 17.9mA$ //

Q. 2a) Explain RC π Filter

The ripple voltage that appears across the capacitor in a rectifier power supply can be attenuated by the use of an additional R and C ckt which togeather functions as an ac voltage divider. Fig 14 shows the ckt arrangements


Fig 14. RC π Filter ckt-

Assuming a constant o/p load current, C_1 continues to charge and discharge producing a saw tooth (ripple) waveform at C_1. This waveform is composed of a fundamental ac voltage (same frequency as the ripple) and a number of smaller-amplitudes, which are quickly attenuated then the fundamental frequencies components due to R_1 and C_2. The peak voltage V_p is given by $\boxed{V_p = V_r / \pi}$ —① where V_r is the ripple voltage peak to peak amplitude, given by

$$V_0 = \frac{V_i \, X_{C_2}}{\sqrt{R_1^2 + X_{C_2}^2}}$$

Q2B> Explain DC Load Line analysis for Semiconductor Diode

Sol^n: DC Loadline is the graphical analysis in which a straight line drawn over the forward characteristics of a diode, From this st line we will be able to determine the Q-Point (operating point of the diode) which intersects with the forward characteristics of the diode.

Example: Consider the following ckt, for understanding the procedure of DC load Line
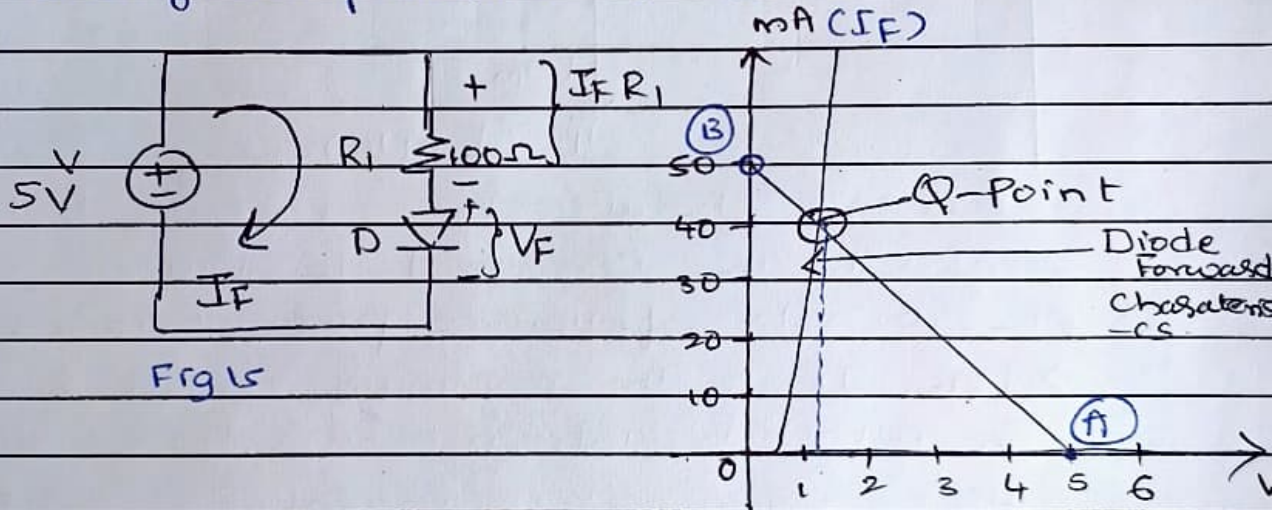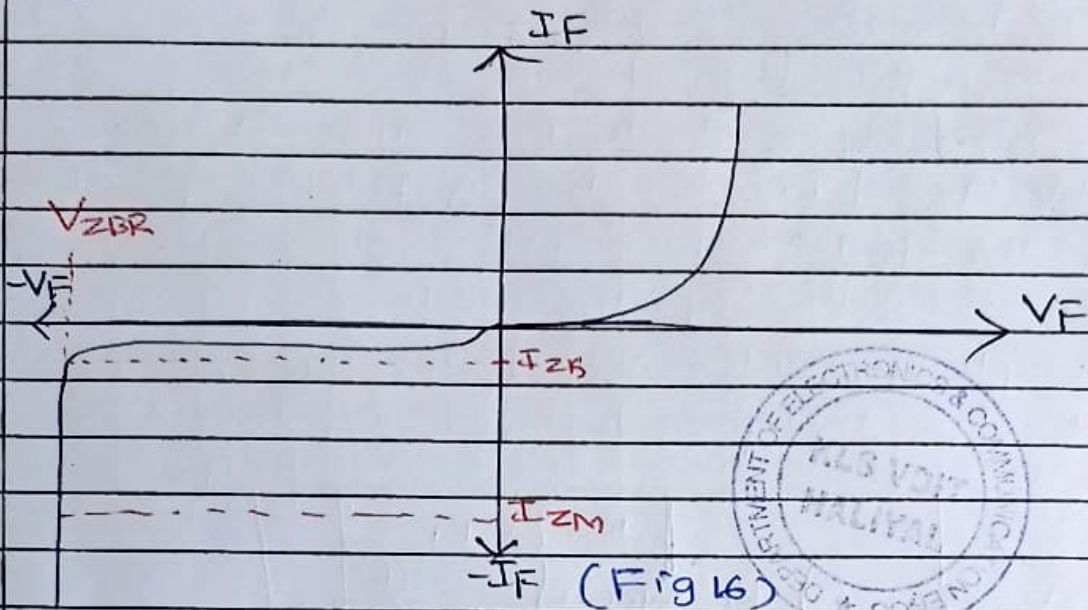

Fig 15

KVL to Fig 15 gives

$$V = I_F R_1 + V_F \quad -①$$

when $V_F \to 0$, then $V = I_F R_1$, $\therefore I_F = \dfrac{5}{100} = 50mA$,

let this be point ⑬

when $I_F \to 0$, $V = V_F = 5V$, let this be poin Ⓐ

then Q-point is (1.2V, 40mA).

Q2C> Write down the Characteristics of Zener Diode
Fig 16 Shows the Characteristics of Zenerdiode.

(Fig 16)

Forward characteristics of Zener diode are similar to the normal diode, But in reverse characteristics, following parameters are observed

1) I_{ZB} : It is the minimum reverse zener voltage for which breakdown occurs, this current is the minimum reverse current

2) I_{ZM} : It is the Maximum reverse zener current which flows through the Zener Diode after breakdown.

3) $V_{Z,BR}$: It is the reverse voltage at which, the reverse voltage remains constant but reverse current increases rapidly, typical values are -5.1V to -20V.

Q3a) Explain BJT amplification for increasing and decreasing the IB levels.

Soln: In BJT we have two current amplification factors i) α and ii) β, which are related as

$$\alpha = \frac{Ic}{Ie} \quad -\text{①} \qquad \beta = \frac{Ic}{Ib} \quad -\text{②}$$

here only eqn ② is typically used as the range of α lies between 0.95 to 0.995, which will not help in amplification process, but as β ranges from 50 to 400, then it helps in increasing β IB value w.r.t - β.
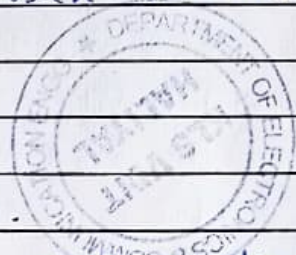
Example!

Let us assume that- $\beta = 50$, IB is varying between $I_{B,min} = 5mA$ and $I_{B,max} = 10mA$.

∴ Change in Ic is given by

$$Ic_1 = \beta \, I_{Bmin} = 0.25A \quad -\text{③}$$

$$Ic_2 = \beta \, I_{B,max} = 0.50A \quad -\text{④}$$

From eqn ③ and ④ we can notice that- how β helps to increase or decrease IB value (i/p) w.r.t Ic (o/p).

Q3b) Explain Common Base Input Characteristics of BJT

→ Common Base characteristics are obtained by making base terminal as common between emitter (E) and Collector (C)

→ Input characteristics are the plot of Input voltage (V_{BE}), Vs Input current (I_E) for constant output voltage (V_{CB}).
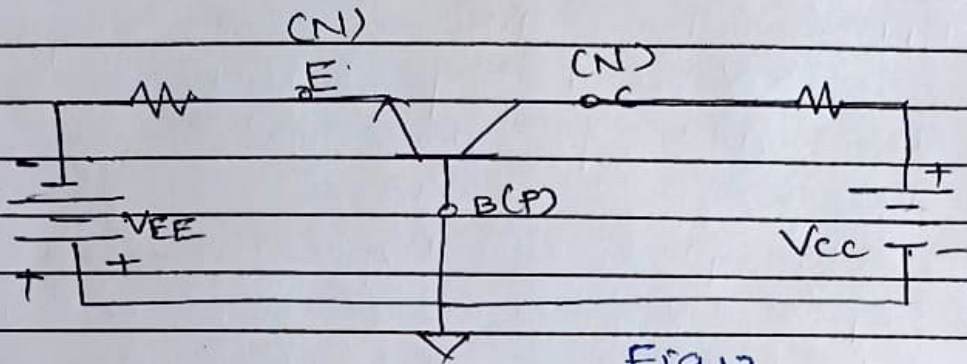
Q3b> Common Base Ckt Configuration
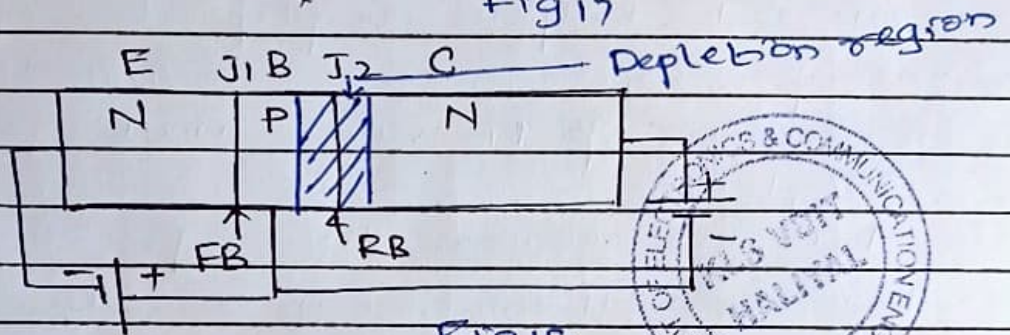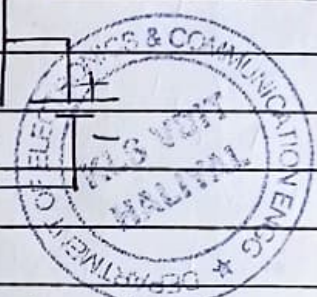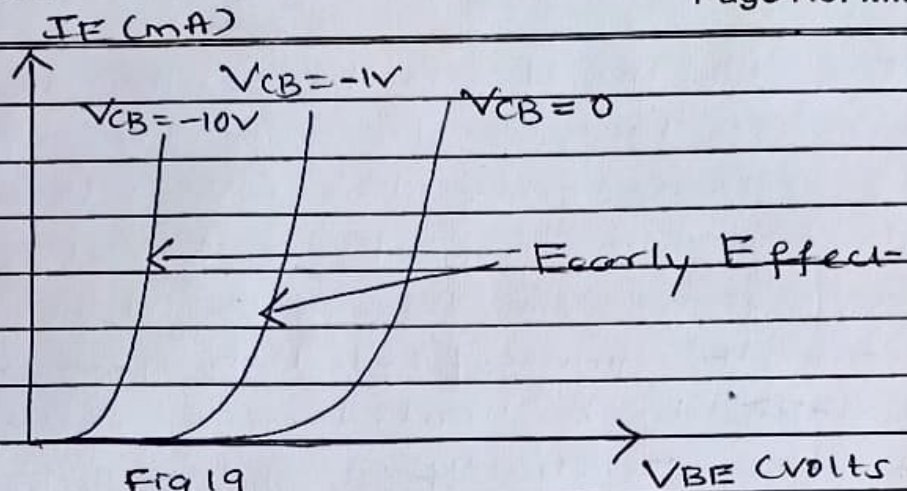

Fig 17

Fig 18

→ Fig 17 and 18 shows the typical ckt configuratio -n and layer diagram representation for common base configuration

→ For i/p charateristics, i/p terminal voltages V_{BE} is varied for constant o/p voltage V_{BC}.

→ J_1 is forward biased and J_2 is reversebiased

→ If $V_{CB}=0$, then for $V_{BE} = 0.3V$ or $0.7V$, then as J_1 is Forward Biased, I_E increases as shown in Fig 19

→ If V_{CB} is increased slightly, then depletion region increases more towards the base, then as we increase V_{CB} further, base terminal layer vanis hes and E and C layers get merged with ea - -ch other hence I_E increases well before knee voltage, this is known as "Early Effect"
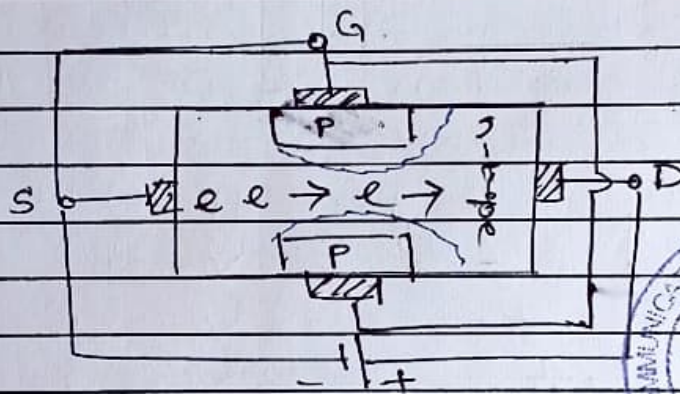
Teacher's Sign. ☐

Q3b>

I_E (mA)

$V_{CB} = -1V$

$V_{CB} = -10V$

$V_{CB} = 0$

Eearly Effect

Fig 19

V_{BE} (volts)

Q3c> Working of n-channel JFET

Construction Details (Fig 20 and 21)

G

P

S ⊶ e e → e → ▸D

P

− +

When
$V_{GS} = 0$ and
$V_{DS} = +ve$

± −⊶G

P

S ⊶ eee→ ▸D

P

+
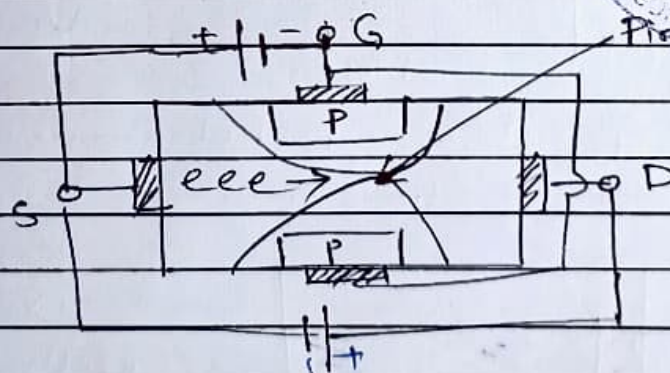
Pinch off

When $V_{GS} = -ve$
V_{DS} = more +ve
pinch off

The working of n-channel JFET can be understood
by considering the following cases
case(i): When $V_{GS} = 0$ and V_{DS} is +ve
In this condition, as source is connected to
−ve terminal, more no of electrons will be repelled

Teacher's Sign.

Q3(C) towards the drain, hence the drain current increases, but as drain in +ve, after reaching the certain voltage level (VDS) the reverse bias at drain increases, hence it extends the Depletion region more towards the drain (Fig 20, 21) hence the flow of electrons from source to drain is going to be limited as a result of which ID decreases slowly.

Case (iii): VGS = -ve, VDS is more +ve; Under these conditions as reverse bias increases more and more towards drain, hence blocking the path of flow of electrons, this condition is known as Pinch off condition (Fig 21), at this state ID remains constant.

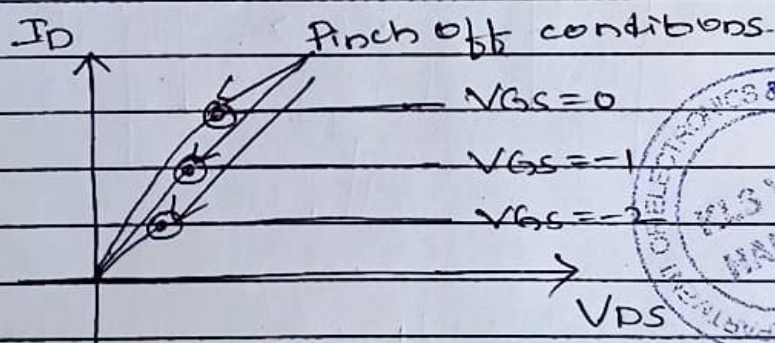

Fig 22

Q4a) Explain operation of Enhancement MOSFET
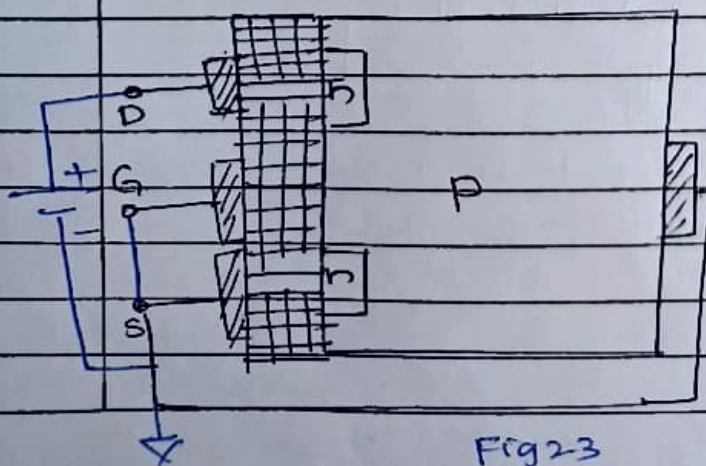
let us consider the n-channel Enhancement MOSFET

Consider VGS = 0 and VDS is +ve, as their is no path from source (n) to drain (n), no current flows, hence ID = 0

Fig 23

Q4a) Now as $V_{GS} = +ve$ and $V_{DS} = +ve$, hence the electrons present in the p-type substrait, start to accumulate in between source and drain, and as V_{DS} is made more $+ve$, the electrons from source will push the electrons present in between the source and drain and also as V_{DS} is $+ve$, electrons from drain are attracted towards $+ve$ of supply, hence I_D increases, the voltage at which this channel is formed and current starts to appear is called threshold voltage (V_{Th}).

Fig 24

Fig 25
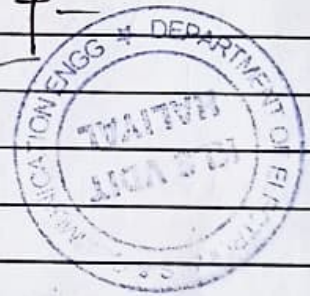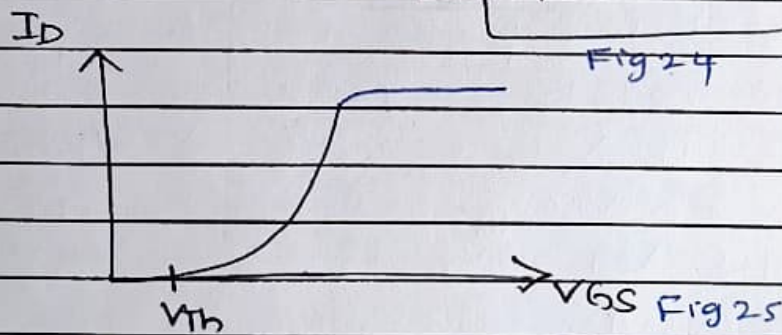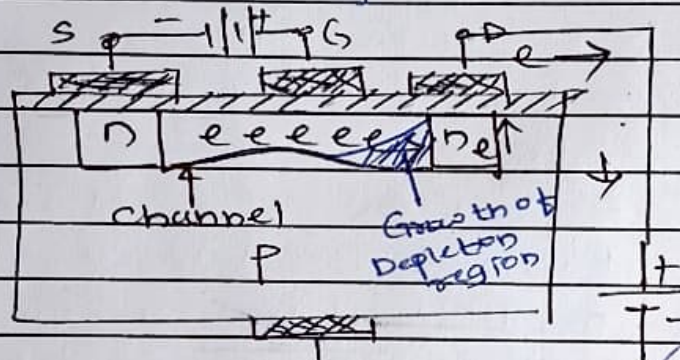
Now, if $V_{GS} > V_{Th}$ and V_{DS} is increased, then I_D also increase, hence depletion region towards drain also increases, hence flow of electrons is withheld and current will be consant.

Q4b) Draw the DC Load Line for Transistor and Identify the Q-points.

Consider the common emitter ckt

Let-
$V_{CC} = 12V$
$R_C = 2K\Omega$

Fig 26
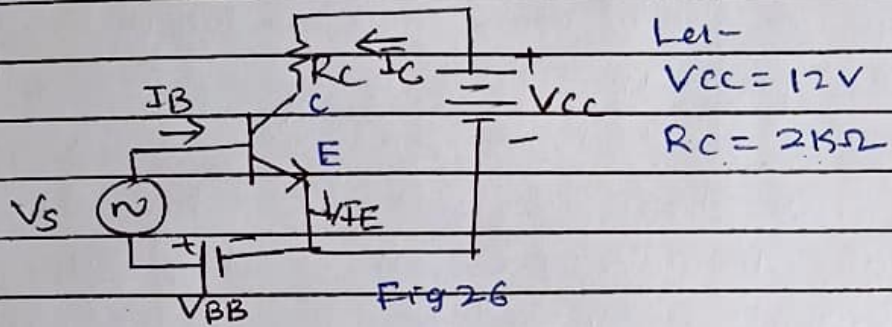
KVL to o/p loop gives.

$$V_{CE} = V_{CC} - I_C R_C \quad -①$$

$$\therefore I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad -②$$

As eq^n ② represents a straight line eq^n $y = mx + c$, we can have a slope $= -1/R_C$.
To draw the DC load line on o/p charsaterisbics of BJT, we need two points, Let- A represents point on X-axis and B on y-axis.
In eq^n ② if $V_{CE} = 0$, $I_C = V_{CC}/R_C$; and if $I_C = 0$, $V_{CE} = V_{CC}$ Ⓐ
If $\therefore$ we get- $V_{CE} = 12V$, $I_C = \frac{12}{2K\Omega} = 6mA$ Ⓑ
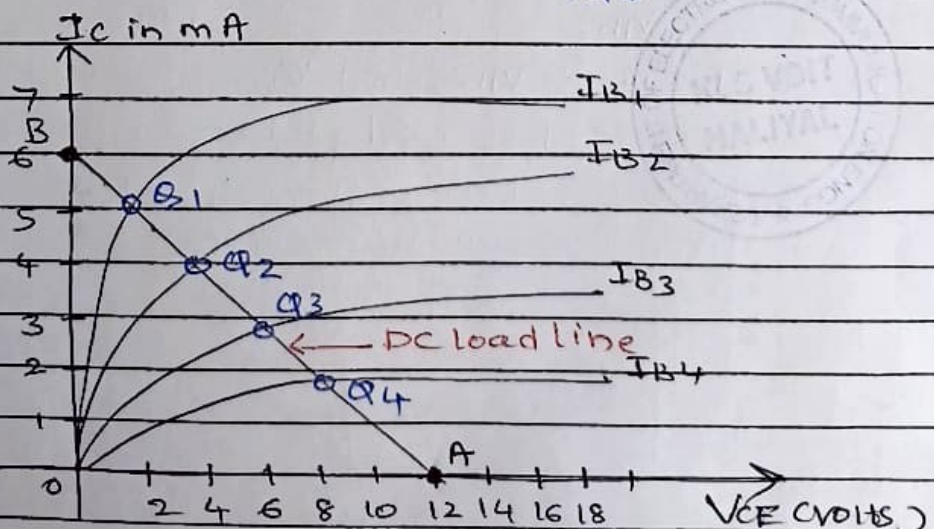
Fig 27

Q4b> In Fig 27, Q1, Q2, Q3 and Q4 indicate the operating points (Q-point) which is the intersections of o/p characters with DC Load line, the suitable Q point is Q3 for which $V_{CE} = 6V$, $I_c = 3mA$

Q4C> Explain Common Emitter Input characteristics.

Common emitter i/p characteristics are the plot of i/p voltage (V_{BE}) Vs I_B for constant V_{CE} values, for this consider the following CKT

Fig 28
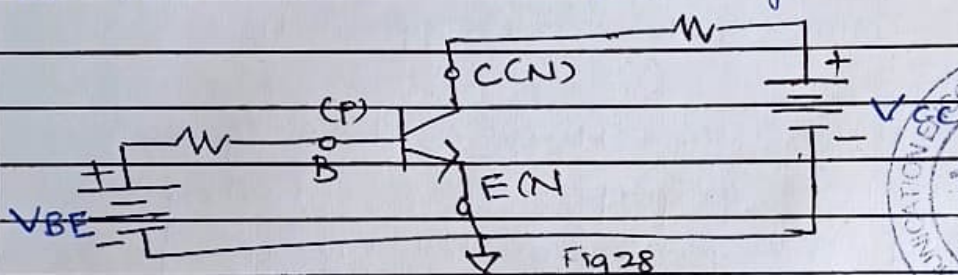
In order to plot the i/p characteristics in CE mode Vcc is varied and kept at a constant value which reflects the VCE values, Now for variable values of V_{BE}, I_B value are noticed and plotted.

. When $V_{CE} = 0$, the characteristics are similar to forward biased diode.

. If V_{CE} is increased, effective base width decreases resulting in reduction of recombination of carrier in base region, hence due to which I_B decreases and appears later as compared with $V_{CE} = 0$.

Fig 29

Topic : ....
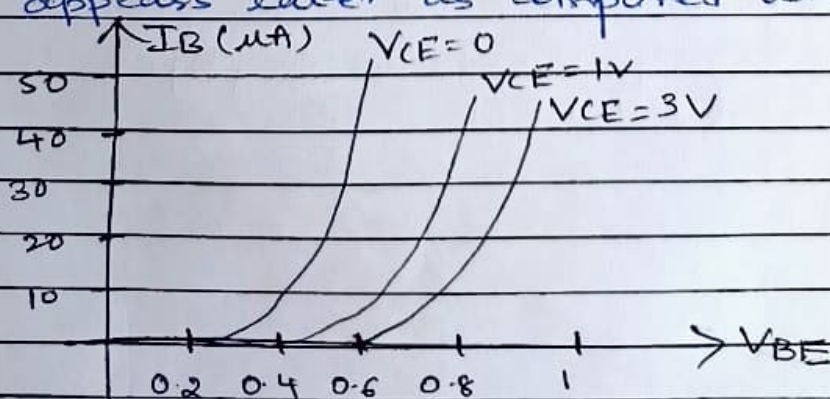
Q5a> Explain the Blocks Diagram of Typical Op-Amp

Fig 30 Shows the Blocks Diagram of Op-Amp

Input-1

Input Stage	Intermediate Stage	Level Shifting Network	Output Stage

Input-2 → Stage

→ Output
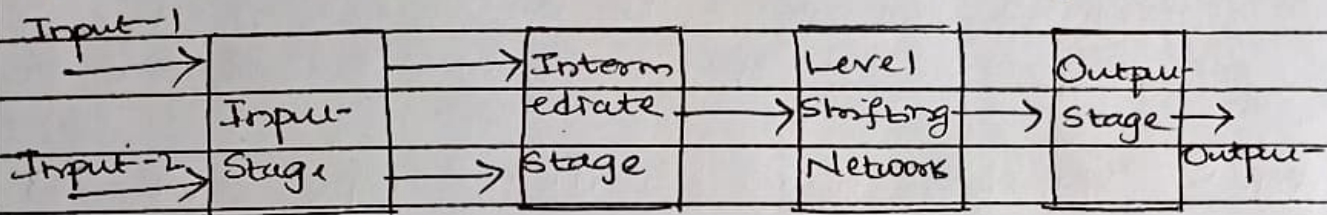
Fig 30

Input Stage: It is a dual input Balanced Differential amplifier used for providing a very high gain of the order of 60dB.

Intermediate Stage: It is a dual i/p unbalanced differential amplifier stage, which provides the half of the gain provided by the first stage and has two input terminals. It provides the voltage gain for the Op-Amp

Level Shifting Stage: It is an Emitter follower act which is used to Shift the DC level at the o/p of the intermediate stage of the Op-Amp. to zero volts w.r.t ground.

Output Stage: It is a low o/p impedance, large AC o/p voltage swing stage. It consist of push-pull complementary amplifier that meets the required levels.

Teacher's Sign.
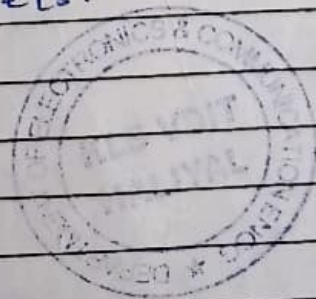
Q5b> Explain working of a Differential Amplifier
Using a basic differential op-Amp configuration,
a Subtractor and a summing amplifier may be
constructed as described below.

Fig31: A subtractor
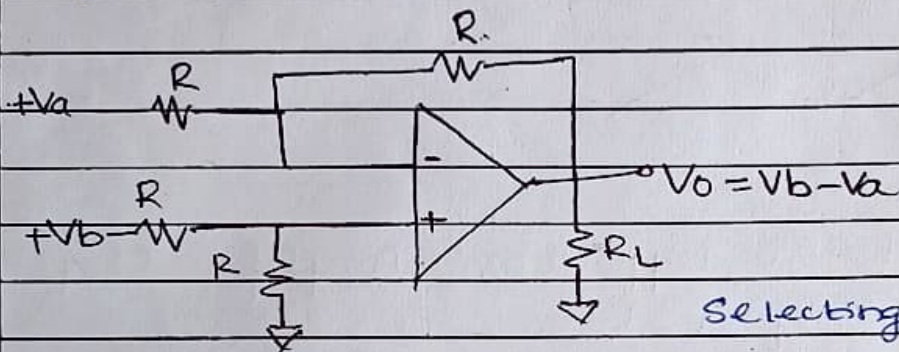
In this configu
ration, i/p
Signal can be
Scaled to desir
-d values by
Selecting appropriate
values for the external resistors, if all R values
are same then gain = 1, ∴ $\boxed{V_0 = V_b - V_a}$

Q5c> Explain op-Amp as a Integrator ckt with an i/p
and o/p waveform using square wave as i/p

ckt
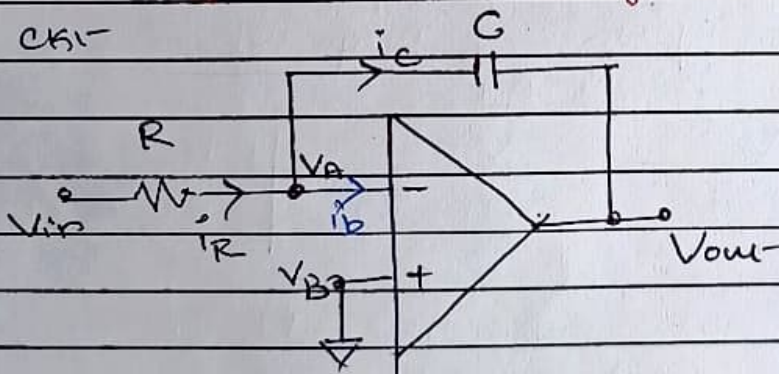
Apply KCL at V_A

$$i_R = i_c + i_b$$

$$\frac{V_{in} - V_A}{R} = c \frac{d(V_A - V_{out})}{dt}$$ and By virtual ground

concept $V_B = 0$, ∴ $V_A = V_B = 0$.

$$∴ V_{out} = -\frac{1}{RC} \int_0^t V_{in} \, dt.$$

Teacher's Sign.

Q5c) For a square wave i/p
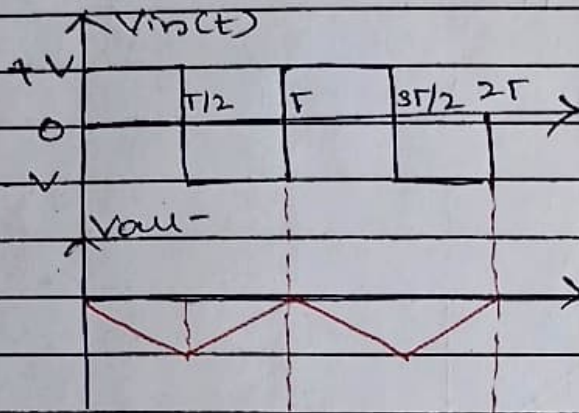
Q6a) Explain Basic Differenbal Amplifier (Repeated question ref Q5B.

Q6b) Define Op-Amp Parameters Gain, CMRR, Slew Rate, input resistance.

① Gain: There are two types of Gain in Op Amp

a) Differenbal Gain (Ad): It is the ratio of o/p voltage of the op-Amp Vour to i/p (Different-al) voltage of the op-Amp where ($V_{INV} \neq V_{NON}$ -INV). is called Ad

$$Ad = \frac{V_o}{Vd} = \frac{V_o}{V_{NI} - V_I} \quad \left| \begin{array}{l} \text{where} \\ V_{NI} \neq V_I. \end{array} \right.$$

b) Common mode Gain (Ac): It is considered when $V_{INV} = V_{NON-INV}$.

$$Ac = \frac{V_o}{Vd} = \frac{V_o}{V_{HI} - V_I} \quad \left| \text{where } V_{NI} = V_I \right.$$

Q6b) CMRR: Common mode Rejection Ratio is the ratio of magnitude of differential gain Ad to the magnitude of common mode gain Ac. is given by

$$CMRR = \left| \frac{Ad}{Ac} \right|, \text{ expressed in dB as.}$$

$$CMRR(dB) = 20 \log_{10} \left| \frac{Ad}{Ac} \right| dB$$

Slew Rate (SR): It is the maximum rate of change of o/p voltage w.r.t time and is expressed in volts per micro second.

$$\therefore SR = \left(\frac{dVo}{dt} \right)_{max} \quad V/\mu sec$$

Input Resistance (Ri): It is the resistance between the two input terminal of op-Amp, ideally.
$$Ri = \infty$$
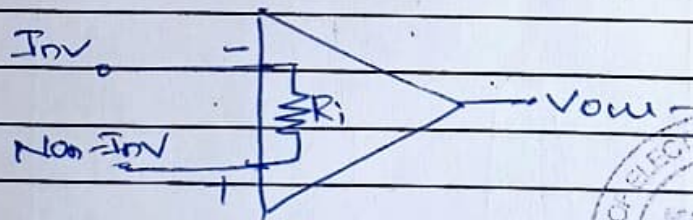
Q6c) Explain Inverting amplifier CKt-

Topic : ....
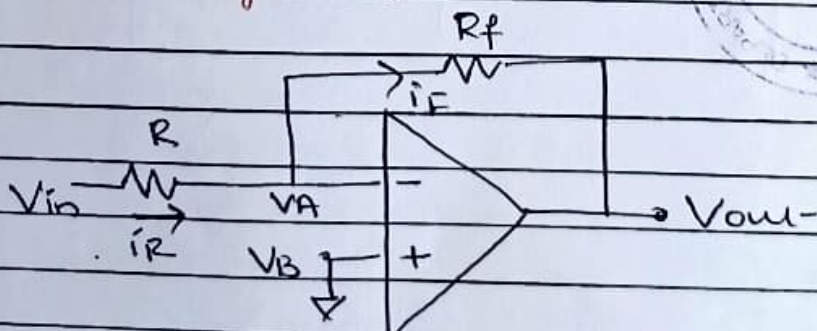
Q6C> KCL cu- V$_A$ gives

$$i_R = i_F$$

$$\frac{Vin - V_A}{R} = \frac{V_A - Vout}{Rf}$$

By virtual ground concept $V_A = V_B = 0$, ∴

$$\frac{Vin}{R} = \frac{-Vout}{Rf}$$

∴ $Vout = -\frac{Rf}{R} Vin$ —①

Comparing ① with $V_O = A_V Vin$ - we get-

$$Gain = -\frac{Rf}{R}$$

Example! If Vin = 2v, Rf = 10KΩ, R = 1KΩ, then

$$Vout = -\frac{10K}{1K} \times 2 = -20v$$
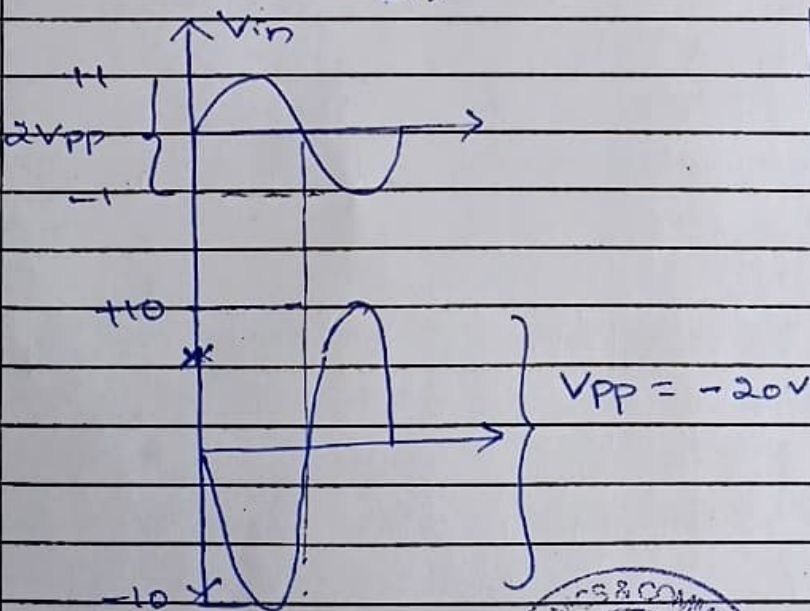
It is observed that there is 180 phase shift and amplification in Inverting Op-Amp configuration

Q7a) Convert Decimal to Binary

①
```
2 | 41
2 | 20 - 1 ↑
2 | 10 - 0
2 | 5 - 0
2 | 2 - 1
  | 1 - 0
```
$(41)_{10} = (101001)_2$

②
```
2 | 153
2 | 76 - 1
2 | 38 - 0
2 | 19 - 0
2 | 9 - 1
2 | 4 - 1
2 | 2 - 0
  | 1 - 0
```
$(153)_{10}$
''
$(10011001)_2$

③ $(0.6875)_{10}$

$0.6875 \times 2 = 1.375$ | 1
$0.375 \times 2 = 0.75$ | 0
$0.75 \times 2 = 1.5$ | 1
$0.5 \times 2 = 1.00$ | 1
$0 \times 2 = 0$

$(0.6875)_{10} = (0.10110)_2$

④ $(0.513)_{10}$

$0.513 \times 2 = 1.026$ | 1
$0.026 \times 2 = 0.052$ | 0
$0.052 \times 2 = 0.104$ | 0
$0.104 \times 2 = 0.208$ | 0
$0.208 \times 2 = 0.416$ | 0

$(0.513)_{10} \simeq (0.1000)_2$

Q7b) Write Down the Axiomatic Definition of Boolean Algebra.

Axiomatic Definition of Boolean Algebra is expressed w.r.t. dot (•) and plus (+) operators as follows

Q7b) Property	• Operator	+ operator
① Closure	YES	YES
② Identity	Designated by 1 $x \cdot 1 = 1 \cdot x = x$	Designated by 0 $x + 0 = 0 + x = x$
③ Commutative	$x \cdot y = y \cdot x$	$x + y = y + x$
④ Distributive	• is distributive w.r.t + as $x \cdot (y+z) = (x \cdot y) + (x \cdot z)$	+ is distributive over • as $x + y(\cdot z) = (x+y) \cdot (x+z)$
⑤ Complement	$x \cdot x' = 0$ os $x \cdot \bar{x} = 0$	$x + \bar{x} = 1$ $x + \bar{x} = 1$

Q7c) Simplify the Boolean Functions to Minimum number of literals

① $F = xy + x'y + yz$

$= (x \cdot y) + (x' \cdot y) + (y \cdot z)(x + \bar{x})$

$= (x \cdot y) + (x' \cdot y) + x \cdot y \cdot z + x' \cdot y \cdot z$

$= (x \cdot y)(1+z) + (x' \cdot y)(1+z)$

$= (x \cdot y) + (x'y)$

$= y(x + x')$

$= y$

② $F = (\bar{x}y + x(y+z) + \bar{y}z)$

$= (\bar{x}y + xy + xz + \bar{y}z)$

$= y(x + \bar{x}) + xz + \bar{y}z$

$= y + xz + \bar{y}z$

Q8a) Convert Binary to Decimal

① $(110111)_2$

$= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$= 32 + 16 + 0 + 4 + 2 + 1$

$= (55)_{10}$

② $(10101010)_2$

$= 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 128 + 0 + 32 + 0 + 8 + 0 + 1 + 0$

$= (169)_{10}$

③ $0110 = 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 0 + 4 + 2 + 0 = (6)_{10}$

④ $(100.1010)_2$

$(4.625)_{10}$

100
$= 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$
$= 4 + 0 + 0 = (4)_{10}$

Fractional part.
$= 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$
$= 1 \times 0.5 + 0 + 1 \times 0.125 = (0.625)_{10}$

Q8b) Explain SOP and POS with examples

SOP and POS stands for Sum of Product [AND-OR] and Product of Sum [OR-AND] expressions.

SOP: Sum of Products are the Boolean expression involving OR expressions between two or more Anded literals. There are two types of SOP i) Standard SOP   ii) Canonical SOP

Teacher's Sign.

Consider a function with literals (A, B, C).
$F_1 = (A \cdot B \cdot C) + (A \cdot \bar{B} \cdot C) + (\bar{A} \cdot \bar{B} \cdot \bar{C})$
$F_2 = (A \cdot B) + (A \cdot \bar{B} \cdot C) + (\bar{C})$

here F_1 is having all the literals hence it is refered to as canonical SOP, where as F_2 is in SOP form but not having all the literals, it is refered to as Standard SOP terms.

Canonical SOP are expressed as follows

Term	value	canonical form
a b c	1 1 1	m7
ā b c	0 1 1	m3
a b c̄	1 1 0	m6

Similarly the POS : Product of sum terms are also expressed as standard POS (may not cover all literals) and canonical POS (must cover all literals).

Standard POS $F_1 = (\bar{A} + \bar{B} + \bar{C}) \cdot (A + \bar{B}) \cdot (\bar{A} + \bar{C})$

canonical POS $F_2 = (\bar{A} + \bar{B} + \bar{C}) \cdot (A + \bar{B} + C) \cdot (\bar{A} + \bar{B} + \bar{C})$

canonical POS are expressed as

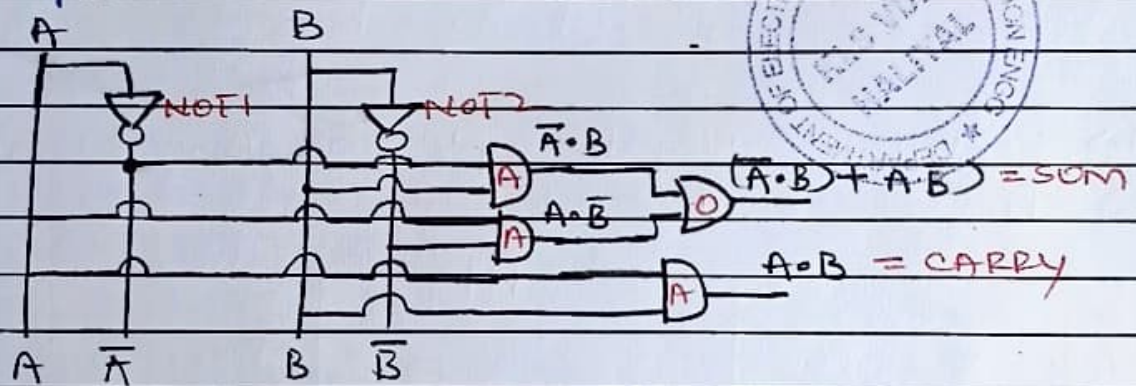| Term	value	canonical form
$(\bar{A} + \bar{B} + \bar{C})$	1 1 1	M7
$(A + \bar{B} + C)$	0 1 0	M2
$(\bar{A} + \bar{B} + c)$	1 1 0	M6

Q8C Implement Half adder using Basic gates
A Half adder ckt adds 2 one bit number and produces result sum and carry.

Truth Table

A	B	Sum	Carry
O	O	O	O
O	1	1	O
1	O	1	O
1	1	O	1

From sum
$$Sum = (\overline{A} \cdot B) + (A \cdot \overline{B})$$
From carry
$$Carry = A \cdot B.$$

Implementations.

Sum = $(\overline{A} \cdot B) + (A \cdot \overline{B})$
Carry = $A \cdot B$

Q9a) Explain working Principle of Capacitive Transducer

Capacitive Displacement Transducer

The equation for the capacitance between two plates seperated by air or another dielectric is
$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \quad -① , \text{ where}$$

C is Capacitance; ε_r is relative Permittivity ε_0 is permittivity of free space (8.84×10^{-12}), A is the cross sectional area. of plates in m^2, d is the distance between two plates.

In case of a capacitive displacement transducer which varies the distance between the plates (Δd), the sensitivity is Δc/Δd, possibly expressed in pF/μm. For a transducer which varies capacitor area, the sensitivity is (ΔC/ΔA) and can be further reduced to (Δc/Δl) as shown below.
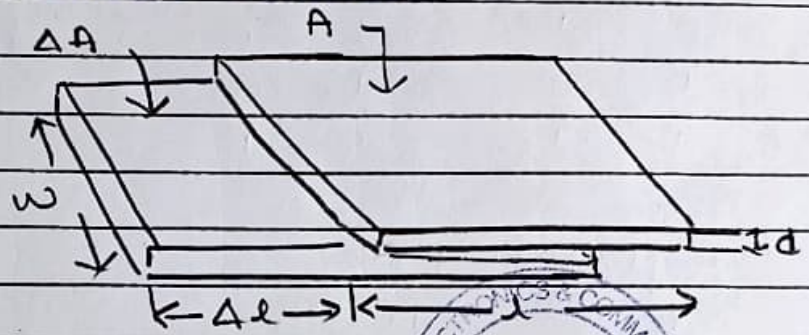
Q9b> Explain Working Principle and Applications of Piezoelectric Transducer.
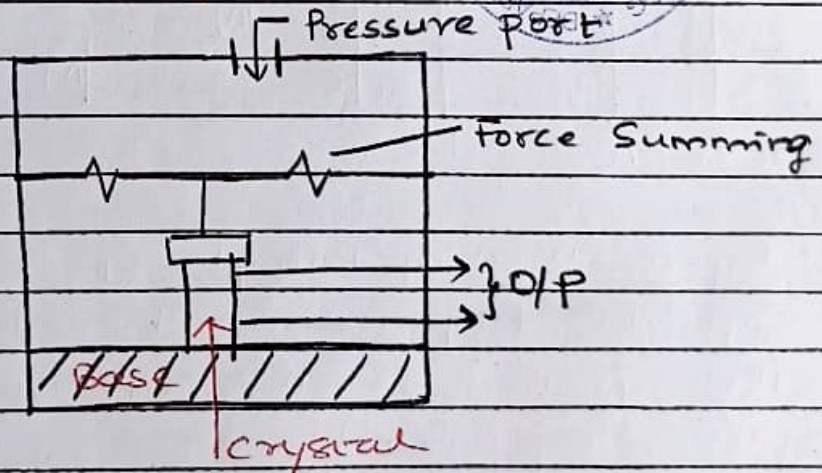
In this type of transducer Mechanical Energy is converted in to electrical energy and are based on the direct piezoelectric effect.

A Piezoelectric material is the one in which an electric potential appears across certain surface of a crystal if the dimension of crystal are changed by application of mechani

Teacher's Sign. AK

cal force., a crystal is placed between a
solid base and the force summing member. An
externally applied force that enters the
transducer through its pressure ports. An emf
across the crystal, proportional to the magnitude
of the applied pressure appears at the o/p. given
by

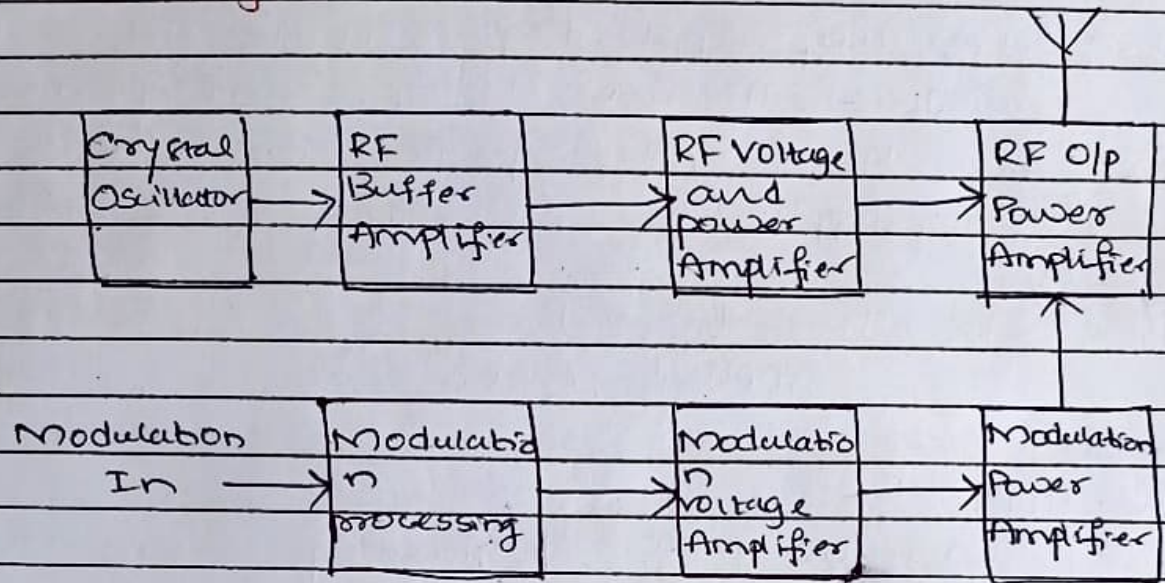$$K = \frac{\text{Transduced Force}}{\text{Applied force.}}$$

Applications:
① Measurement of force, pressure, acceleration.
② HF Accelerometers.
③ Dynamic pressure

99C> Write down the Applications of Thermal Transducers

① Used in Resistance Thermometers
② Used in Thermistors to relate resistance and
   temperature
③ Used in Thermocouple based Thermometers
④ Used in Semiconductor Temperature Sensor

10 a) Explain Typical Radio Transmitter with Neat-
Block Diagram

Crystal Oscillator → RF Buffer Amplifier → RF Voltage and Power Amplifier → RF O/p Power Amplifier → (antenna)

Modulation In → Modulation processing → Modulation voltage Amplifier → Modulation Power Amplifier

Block Diagram Of Radio Transmitter

In Radio Transmitters, The main modula-
-tion required to transmit the signals are
dependent on Frequency Modulation Concept.

Starting from Modulation In, there FM
signals are fed to the Modulating processi-
ng Block, where the frequency of the signals
to be transmitted are modulated w.r.t-
carrier signal, In order to transmit
these modulated signal over a long dista-
-nce. it is required to keep the amplitude
levels and Power levels of the message
signal frequency w.r.t carrier, hence voltage
and power amplifier stages will provide
these required conditions for transmitter

10 a) The role of crystal oscillator is to produce the constant-frequency level signal which is desired to transmit the signals over the longer distance

The RF Buffer Amplifier keeps buffering the required voltage levels, -i.e. to transfer a voltage from a first ckt, having a high o/p impedance level, to a second ckt with a low input-impedance.

A voltage Amplifier is used to amplify the voltage levels of an input RF signal without significantly changing its power and its primary function is to amplify the low level RF signal generated by the modulator to a level that is suitable for further amplification, by the power amplifier. The voltage amplifier must provide sufficient voltage gain to increase the signal level while maintaining a high SNR and low disturbon.

RF o/p power amplifier determines the strength and fidelity of the transmitted signal. The choice of Amplifier Type and design will depend on the specific application requirements and the desired performance characteristics of the transmitter.

10 b) **What is Modulation? Explain Need for Modulation**

Modulation is the process of altering one or more characteristics of a carrier signal in order to transmit information which is modified w.r.t message signals amplitude, frequency and phase.

Need For Modulation

① Efficient use of Bandwidth: modulation allows multiple signals to be transmitted over the same set of parameters like amplitude, frequency and phase

② Long Distance Transmission: Modulation allows a signal to be modulated and then amplified which will be suitable for transmitting the signals over long distances without changing the quality /without loss

③ Size of Antenna: When transmission occurs over a free space the antenna radiates signal and receiver receives it. For wavelength to be maintained hence length of antenna should be

$$L = \lambda = \frac{u}{f} = \frac{3 \times 10^8}{f} \, Hz$$

if $f = 20 KHz$, then $L = 15 km$

$\quad f = 1000 KHz$, then $L = 300 m$.

∴ higher frequencies are desired

10 c) What is noise? Explain the term channel noise and its effect

Noise in communication is the unwanted signal which reduce SNR ratio

Channel Noise and its effect

Channel Noise refers to any unwanted or random variations in a communication channel that can distort or interfer with the transmission of information. The effects of channel noise depends on the nature and severity of the noise and type of communication being affected.

Effects

In general noise can cause interference with the transmitted signal, leading to reduced data rates os dropped calls.

In Digital communication channel noise can result in corrupted data, leading to errors or loss of information

In Audio and video transmission, channel noise can cause distortion, resulting in degrade audio os video quality.