Model Question Paper-I/II with effect from 2022-23 (CBCS Scheme)

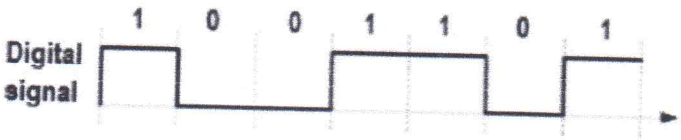
USN | | | | | | | | | | |

First/Second Semester B.E. Degree Examination
Introduction to Electronics Engineering

TIME: 03 Hours **Max. Marks: 100**

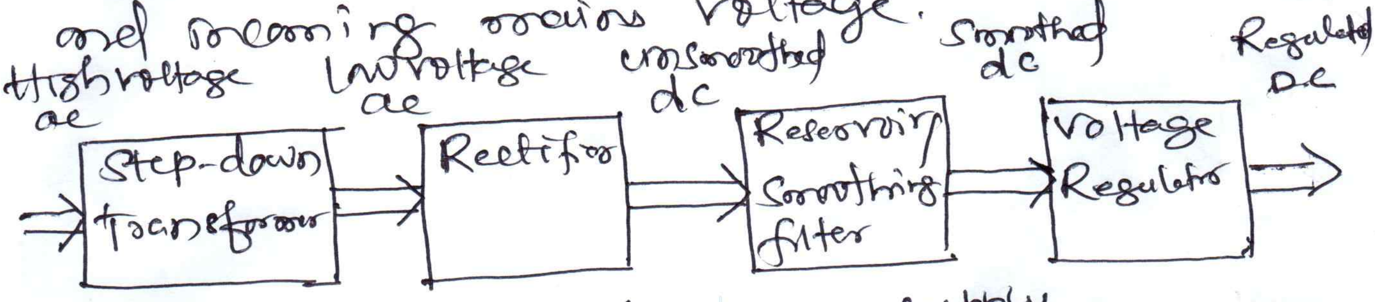
Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE.**

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	What is a regulated power supply? With neat block diagram Summarize the working of DC power supply. Also mention the principal components used in each block.	L2	6M
	b	Discuss the need of filter circuit. With circuit diagram and waveforms brief out the operation of smoothing filter for full wave rectifiers.	L2	7M
	c	With neat diagram Summarize working principle of the voltage divider bias CE amplifier with feedback.	L2	7M
		OR		
Q.02	a	A 5V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5V to a load having a resistance of 500 Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9V.	L3	7M
	b	What is voltage multiplier and mention its applications? With circuit diagram brief out the operation of voltage Tripler circuit.	L2	7M
	c	Illustrate how BJT is used as a switch.	L4	6M
		Module-2		
Q. 03	a	Sketch the circuits of each of the following based on use of Operational Amplifier a) Differentiator. b) Integrator .	L1	6M
	b	Write a note on Ideal characteristics of Op-Amp	L1	7M
	c	Explain the operation of Single stage Astable Oscillator with its circuit diagram.	L2	7M
		OR		
Q.04	a	Mention the condition of sustained oscillations. Determine the frequency of oscillations of a three stage ladder network in which C=10nF and R=10KΩ.	L2	6M
	b	With a neat circuit diagram and Waveforms, describe the operation of Crystal controlled Oscillator.	L2	7M
	c	With a neat circuit diagram explain single stage Multivibrators.	L2	7M
		Module-3		
Q. 05	a	With the help of truth table explain the operation of Full Adder with its circuit diagram and reduce the expression for Sum and carry.	L2	7M
	b	Mention the different theorems and Postulates of Boolean Algebra and Prove each of them with truth table.	L1	7M
	c	Subtract using (r-1)'s compliment method a)$4456_{(10)}-34234_{(10)}$ Subtract using r's compliment method a)$1010100_{(2)}-1000100_{(2)}$	L3	6M
		OR		
Q. 06	a	Convert the following a) $3A6.C58D_{(16)} = ?_{(8)}$ b) $0.6875_{(10)} = ?_{(2)}$	L3	8M

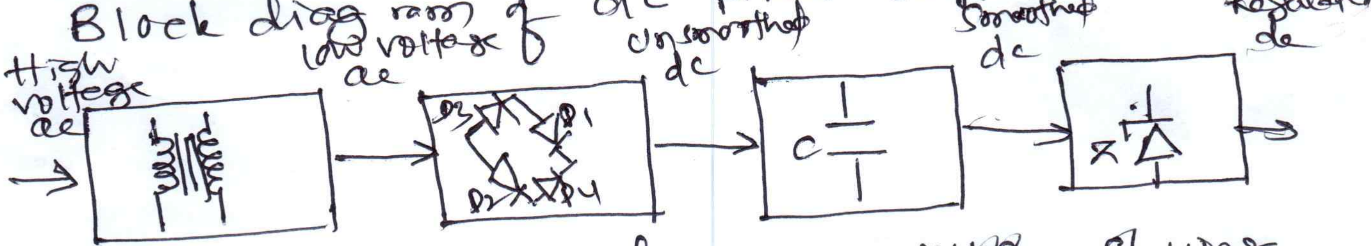
		c) Compute the 9's compliment of $25.639_{(10)}$ d) Compute the 1's compliment of $11101.0110_{(2)}$		
	b	State and prove De-morgan's Theorem with its truth table.	L1	5M
	c	Minimize the following function a)F(x,y,z) = xy+x'z+yz Find the compliment of the function F1 and F2 F1(x,y,z) = x'yz'+x'y'z F2(x,y,z)=x(y'z'+yz')	L3	7M
		Module-4		
Q. 07	a	Compare Embedded Systems and General Computing Systems, also provide the applications of Embedded systems.	L2	5M
	b	Write a note on core of an Embedded systems with its block diagram.	L2	8M
	c	Write a note on Transducers? Explain one type of Sensor and Actuator with its operation.	L2	7M
		OR		
Q. 08	a	Explain how 7 seg Display can be used to Display the data and write a brief note on operation of LED.	L2	7M
	b	What is an Embedded system and brief about the different elements of an Embedded systems.	L2	8M
	c	Write a note on classification of Embedded systems.	L2	6M
		Module-5		
Q. 09	a	Write a note on different types of modulations and briefly describe each in detail.	L2	8M
	b	Brief about Modern Communication System with its block diagram.	L2	7M
	c	List out the advantages of Digital Communication over Analog Communications.	L2	5M
		OR		
Q. 10	a	Explain with a neat diagram the concept of Radio wave Propagation and its different types.	L2	7M
	b	Consider the following binary data and sketch the ASK, FSK & PSK modulated waveforms.  Figure 10.b	L2	6M
	c	Describe about Radio signal transmission and Multiple access techniques.	L2	7M

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be ıttained by every bit of questions.

Q19. Regulated power supply is an electronic device that can provide stable D.C power to the load. which will stabilize the output voltage so that it remains relatively constant inspite of variations in both load current and incoming mains voltage.



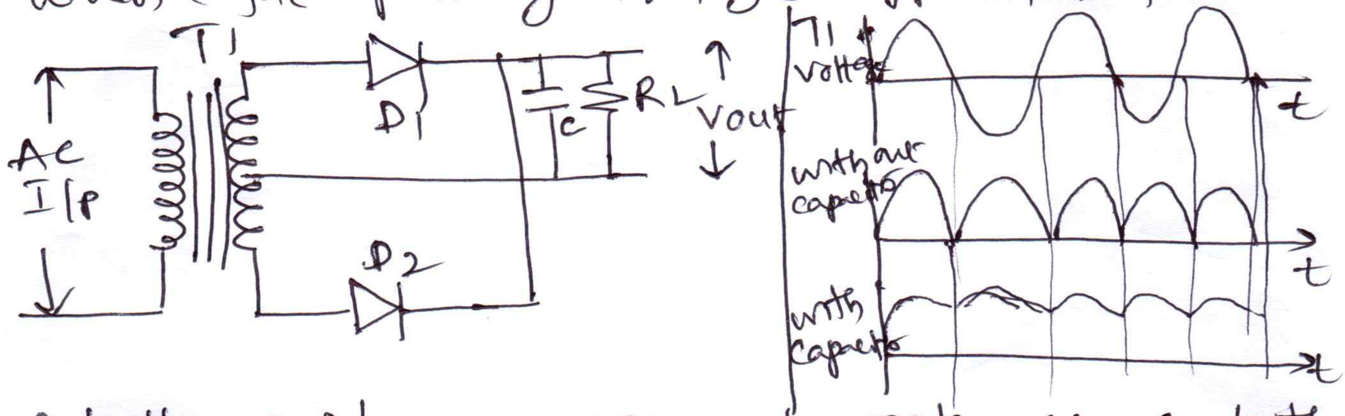
Block diagram of dc power supply



Block diagram of dc power supply showing principle components.

The mains input is set of relatively high voltage a step down transformer with appropriate turns ratio is used to convert this low voltage, ac output is then rectified using diode to produce an unsmoothened (pulsating) output. Then this is smoothed and filtered using connecting the capacitor across the load, which will be regulated by connecting zener diode the output remain constant inspite of variation of load and input voltage.

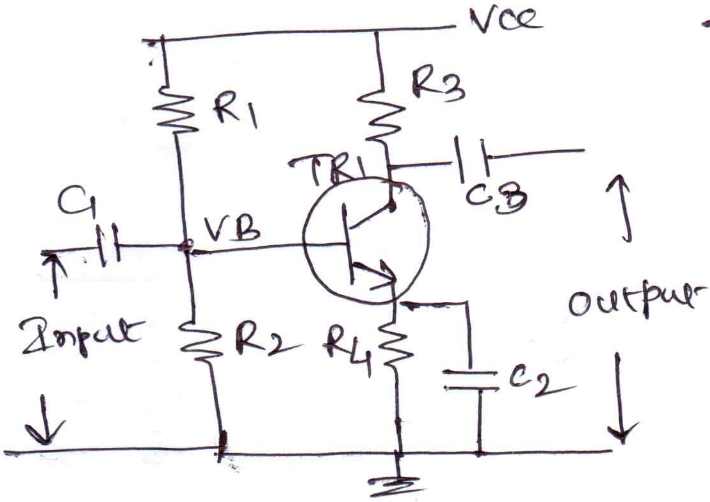
1 b The filter Circuit provides Considerable impro vement (Smoothing) in the Convertion of AC-DC The Capacitor has been added to ensure that the output voltage remains at or near the peak voltage even when the diode is not conducting when the primary voltage applied to the T_1



A better rectifier arrangement make use of both Positive and negative half cycles. positive half cycle diode D_1 allow Conduction while D_2 will not allow the Conduction. During negative halfcycle D_2 will allow the Conduction while D_1 will not allow the conduction.

The reservoire (filter) C can be added to ensure the output voltage remains at or near the peak voltage. It charges approximatly at the peak of positive half cycle and holds the voltage at this level when the diodes are in their non conducting states. Hence C_1 Charges very rapidly as soon as either D_1 or D_2 starts conducts. The time required for C_1 to discharge is in Contrast very much greater. The discharge Contrast is determined by Capacitor value

1C CE amplifier with feedback. The voltage divider CE amplifier with negative feed back provides effective bias stabilization.



The negative feedback path provides feedback ac signal component of dc bias. As a result of slight reduction of signal gain. The signal gain can be increased by removing the ac signal component from the feed back path so that only the dc component is present. In the circuit R1 & R2 forms a potential divider that determines dc base potential VB. The base emitter voltage is the difference between potential present at base VB and emitter VE. The potential at emitter is governed by the emitter current IE as the emitter voltage VE will increase consequently VBE will fall and produces reduction in the emitter current. The increase in bias results in an increase in emitter current compensating for the original charge.

$$VB = \frac{R2 \cdot Vce}{R_1 + R_2}$$

2a Power dissipation - 500mW = $P_{Z max}$ 33

diode regulated 5V

Load resistance 500Ω = R_L

R_s min = ? R_s max = ? R_s

$\therefore R_{s\,max} = R_L\left(\frac{V_{IN}}{V_Z} - 1\right) = 500\left(\frac{9}{5} - 1\right) = 500 \times (1.8 - 1)$

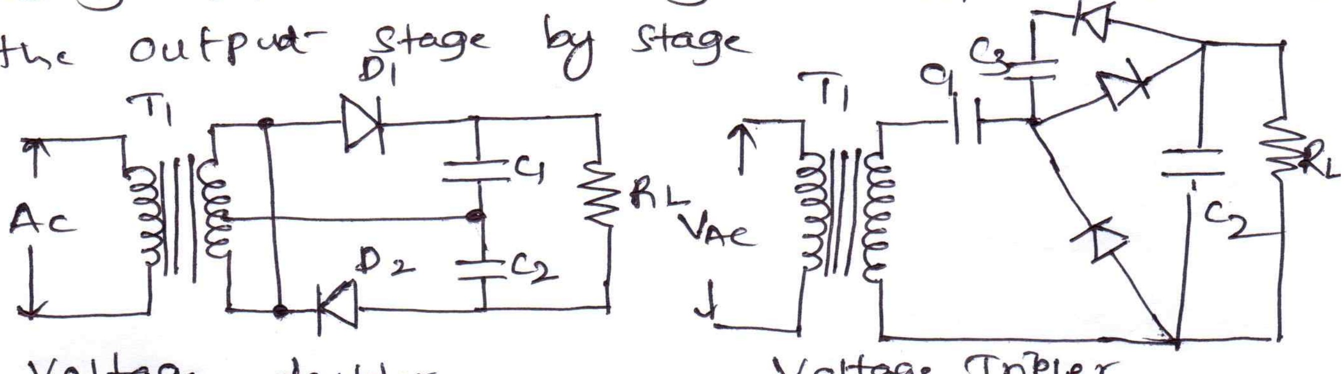
$R_{s,max} = 500 \times 0.8 = 400\,\Omega$

& $R_{s,min} = \frac{V_{IN} \cdot V_Z - V_Z^2}{P_{Z\,max}} = \frac{9 \times 5 - 5^2}{0.5} = \frac{45 - 25}{0.5} = 40\,\Omega$

R_s would be midway between two extremes

$R_s = 180\,\Omega$

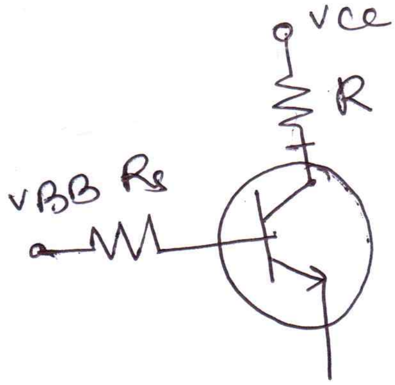
2b Voltage multiplier produce the higher voltage using the cascade arrangement. and it can increase the output stage by stage

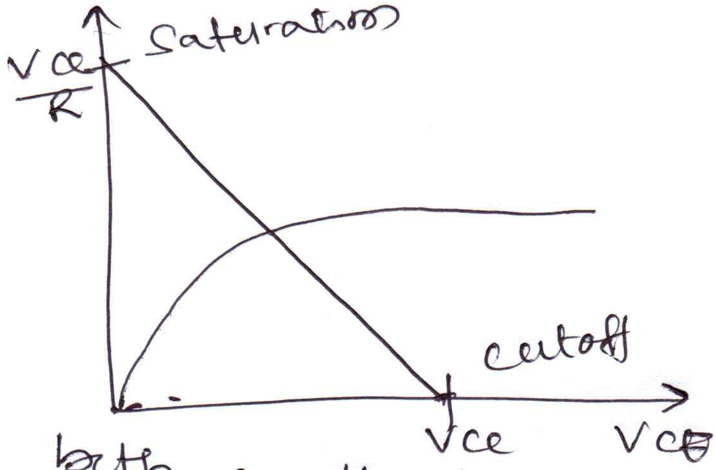


Voltage doubler Voltage Tripler

Voltage doubler C_1 charges to the positive peak. secondary voltage C_2 will charge to the negative peak secondary voltage since the output is taken from C_1 & C_2 connected in series the resulting output voltage will twice that produced by one diode alone. It can be extended to provide higher voltage but the efficiency of the circuit becomes increasingly impaired. and high order voltage multipliers provide relatively small current.

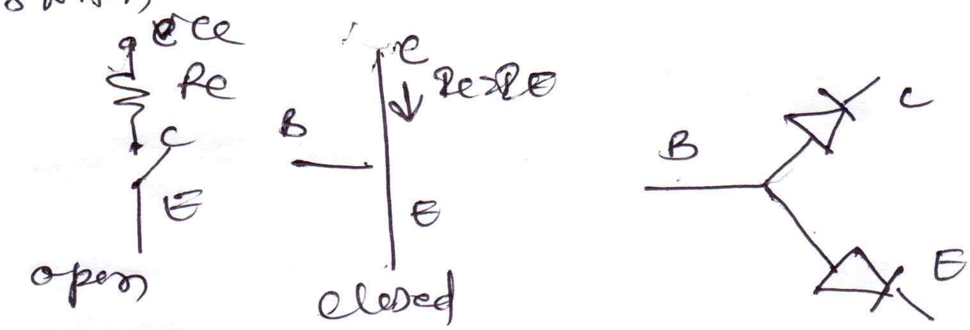
1.c BJT is used as switch. 31





In cutoff region both emitter to base and base to collector junction is reverse biased and no current flows through the transistor acts as open switch.

In saturation region both junctions are forward biased and transistor acts as closed switch



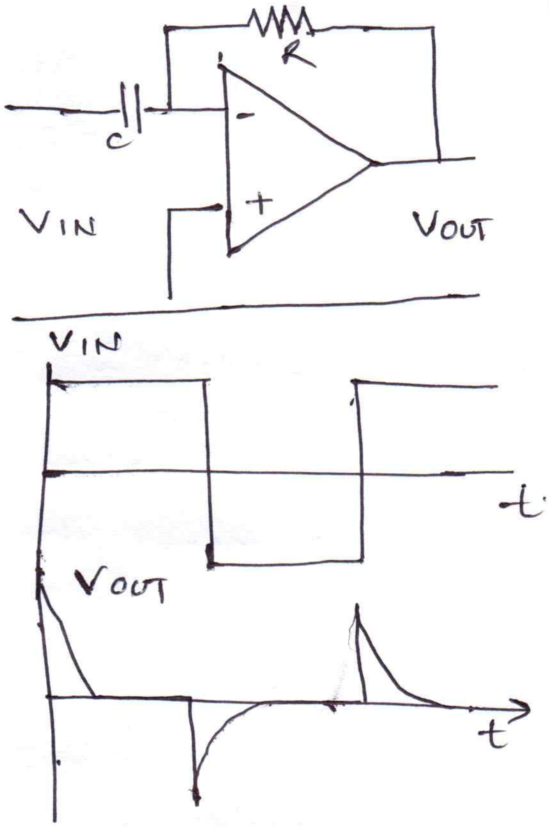
Active region – Emitter to base junction is forward biased and base collector junction is reverse biased. In active region transistor acts as an amplifier

In active region Collector current β times of the base current

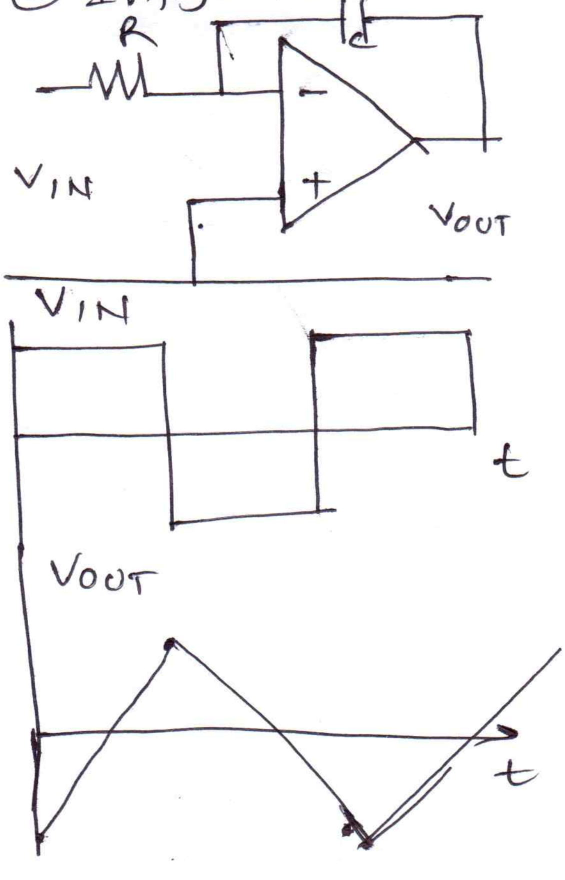
BJT → amplifier, filter, Rectifier, oscillator or even as a switch.

29

3a (i) Differentiator : Differentiator produces the output voltage equivalent to the rate of change of its input. If the input voltage remains constant the output voltage remains constant. Faster the input voltage changes the greater will the output be. The input output waveforms are shown in fig. output is inverted because signal applied to inverting input of the operational amplifier



(ii) Integrator



Integrator is operational amplifier circuit provides the opposite function of differentiator. The output voltage is equivalent to the area under the graph of input function rather than its rate of change. If the input voltage remains constant the output voltage will ramp up or down according to the polarity of the input. Notice that square wave input is converted to a wave that has triangular shape

3b Ideal Charecteristics of an op-amp

① The open loop voltage gain should be very high (Ideally Infinite)

② Input resistance of the opamp is very high (Ideally Infinite)

③ The output resistance should be very low (Ideally zero)

④ Full power bandwidth should be as wide as possible

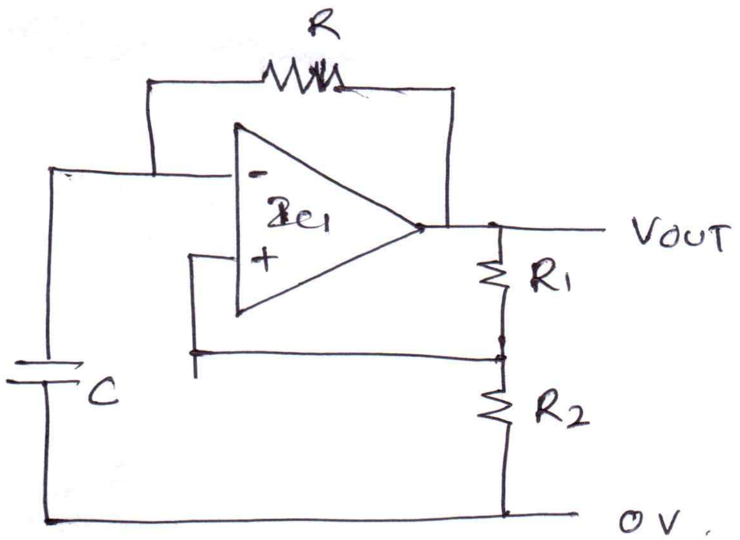
⑤ Slew rate should be as large as possible

⑥ Input offset should be as small as possible

parameter	Ideal	Real
1. Voltage gain	Infinite	1,00,000
2. Input resistance	Infinite	100MΩ
3. output resistance	zero	20Ω
4. Bandwidth	Infinite	2MHz
5. Slew rate	Infinite	10V/μs
6. Input offset	Zero	Less than 50mV

3c Single stage Astable oscillator

A simple form of Astable oscillator that produces square wave output using one operational amplifier. The circuit employs positive feed-back with the output fedback to the Non inverting input via the potential devider formed by R_1 and R_2. This circuit is shown in fig below.



Frequency can be made adjustable by varying R. Assume C is initially uncharged & voltage at the inverting input is slightly less than the voltage at Non-inverting input, the output will rise rapidly to +Vcc and voltage at inverting input begin to rise exponentially as capacitor C charges through the R.

The voltage at inverting input will reached and exceeds that present at the Non inverting input and output voltage fall to -Vcc and capacitor C charges in the other direction

The upper threshold the voltage max. at inverting

$$V_{UT} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

and The Lower threshold maximum negative value for the voltage at inverting input

$$V_{LT} = -\frac{V_{CC} \times R_2}{R_1 + R_2}$$

complete one cycle output waveform

$$T = CR\left(\ln\left(1 + 2\frac{R_2}{R_1}\right)\right)$$

4a. Conditions of sustained oscillation are 23

① The feedback must be positive i.e the signal feed back must arrive back in phase with signal at input

② The overall loop gain must be greater than 1

The frequency of oscillation of three stage ladder network C = 10nF and R = 10KΩ

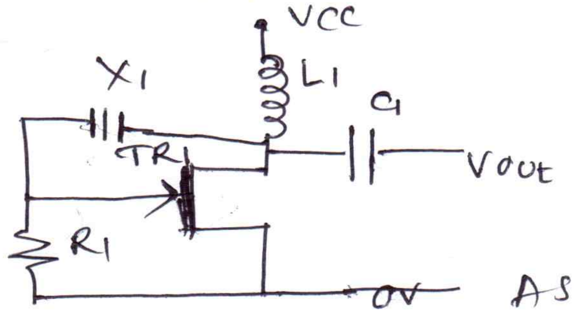
$$f = \frac{1}{2\pi\sqrt{6}\,CR} = \frac{1}{6.28 \times 2.45 \times 10 \times 10^{-9} \times 10 \times 10^{3}}$$

$$= \frac{1}{6.28 \times 2.45 \times 10^{-4}} = \frac{10^{4}}{15.386} = 647\ Hz$$

4b Crystal Controlled oscillator - Accurately maintain an exact frequency of oscillation the quartz crystal is used as the frequency determining element. quartz crystal stabilize the frequency of oscillation of a circuit to within few parts in a million

Crystal manufactured for operation in fundamental mode 100KHz to well over 100MHz

Simple crystal oscillator circuit provides feedback from drain to the source of JFET

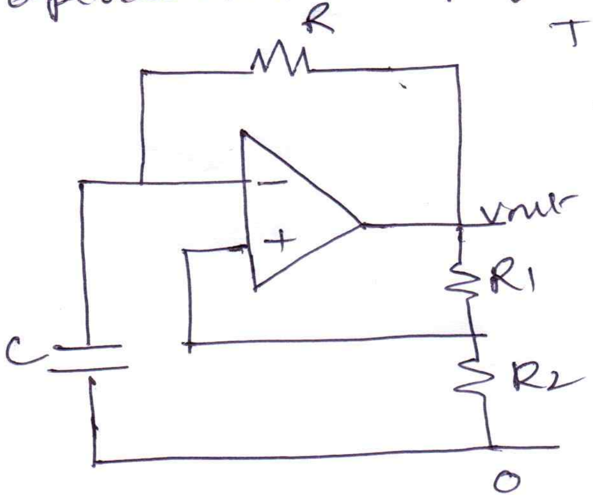


A simple JFET oscillator

4b. Quartz crystal vibrates whenever the a potential difference is applied across its faces. (The phenomenon is known as piezoelectric effect) The frequency of oscillation is determined by the crystal cuts and physical size

4c Single stage multi-vibrator: multi-vibrators are family of oscillator circuits produces output waveforms consisting of one or more rectangular pulses, multivibrators are regenerative, the active device present within the oscillator being operated as a switches alternatively cutoff and driven into saturation

mono stable multivibrator that produces the single o/p pulse referred as one shot single stage produces square wave output using one operational amplifier. The circuit is shown on for



The circuit employs positive feedback with o/p feed back to the non inverting i/p via the potential divider formed by R1 & R2

The frequency can be made adjustable by varying R

Assume C is initially uncharged at inverting input slightly less than the voltage at non inverting input. The o/p will rise to +Vcc The voltage at non inverting will reached and exceed non inverting and output voltage fall to -Vcc

19

5a Full Adder. Full adder is a combinational logic circuit that forms arithmetic sum of three input bits. It consists of three inputs and two outputs

Two input variables x & y and third input variable z represents the carry from previous lower significant position. The two output are designated by S (Sum) & C (carry)

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

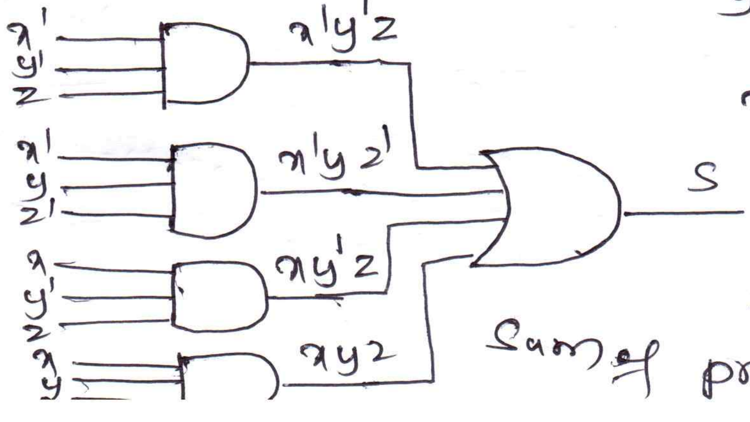
Sum = S

$S = x'y'z + x'yz' + xy'z' + xyz$

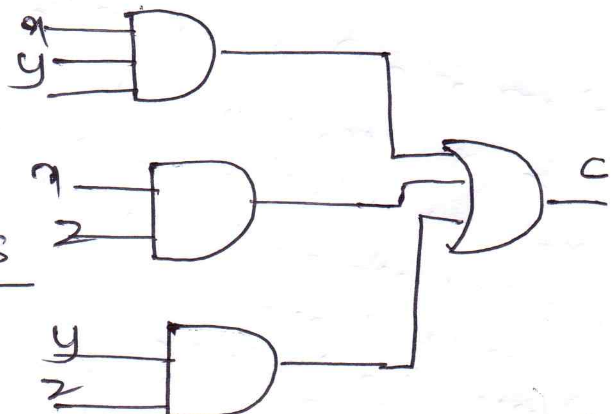
Carry = C

$\therefore C = x'yz + xy'z + xyz' + xyz$

$= xy + xz + yz$



Sum of products



1½

5b postulate 2 ⓐ $x+0=x$ ⓑ $x\cdot 1=x$ 17

Postulate 5 ⓐ $x+x'=1$ ⓑ $x\cdot x'=0$

Theorem 1 ⓐ $x+x=x$ ⓑ $x\cdot x=x$

Theorem 2 ⓐ $x+1=x$ ⓑ $x\cdot 0=0$

Theorem 3 Involution $(x')'=x$

Postulate 3 Commutative ⓐ $x+y=y+x$ ⓑ $xy=yx$

Theorem 4 Associative ⓐ $x+(y+z)=(x+y)+z$ ⓑ $x(yz)=(xy)z$

Postulate 4 Distributive ⓐ $x(y+z)=xy+yz$ ⓑ $(x+y)'=x'+y'$ $x+yz=(x+y)(x+z)$

Theorem 5, Demorgan's ⓐ $(x+y)'=x'y'$ ⓑ $(xy)'=x'+y'$

Theorem 6. Absorption ⓐ $(x+xy)=x$ ⓑ $x(x+y)=x$

① $x+x=x$

$x+x=(x+x)(1)=(x+x)(x+x')=x+xx'=x+0=x.$

② $x\cdot x=x \Rightarrow xx+0=xx+xx'=x(x+x')=x.$

③ $x+1=1 \Rightarrow 1\cdot(x+1)=(x+x')(x+1)=x+x'\cdot 1=x+x'=1$

④ $x\cdot 0=0$.

⑤ $(x')'=x$

Truth table .

x	y	xy	$x+xy$	$(x+y)$	$(x+y)'$	x'	y'	$x'y'$
0	0	0	0	0	1	1	1	1
0	1	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	0
1	1	1	1	1	0	0	0	0

5c ① (r−1)'s compliment $4456_{(10)} - 34234_{(10)}$

$$\begin{array}{r} 04456 \\ +\ 65765 \\ \hline 70221 \end{array}$$

65765 – 9's compliment

70221 – No carry   Ans = −29778 (9's compliment of 70221)

(ii) Substract using r's Compliment

$1010100_{(2)} - 1000100_{(2)}$

$$\begin{array}{r} 1010100_{(2)} \\ +\ 0111100 \\ \hline = 0010000 \end{array}$$

0111100 – 2's compliment of 1000100

$$\begin{array}{r} 1000100 - 0111011 \\ +\ 1 \\ \hline 0111100 \end{array}$$

∴ Ans = 0010000 = 10000

6.a. Convert

(i) $3A6.C58D_{(16)} = (\ \ \ )_8$

$0\ 011\ 101\ 011\ 0.110\ 001\ 011\ 000\ 110\ 1_{(2)}$

$1\ \ 6\ \ 4\ \ 6\ .\ 6\ 1\ 3\ 0\ 6\ 4_{(8)}$

∴ $3A6.C58D_{(16)} = 1646.613064_{(8)}$

(ii) $0.6875_{(10)} = (\ \ )_2$

$0.6875 \times 2 = 1.375$ — 1

$0.375 \times 2 = 0.750$ — 0

$0.750 \times 1 = 1.50$ — 1

$0.50 \times 1 = 1.000$ — 1

$0.6875_{(10)} = 0.1011$

6 c 9's Compliment of 25.639.

$10^2 - 10^{-3} - 25.639 = 99.999 - 25.639$
$= 74.360$

(d) 1's compliment 11101.0110(2) ⇒

$2^5 - 1 - 11101 = 11111 - 1 - 11101$
$= 11110 - 11101$
$= 00010$

1's compliment of 0.0110 ⇒ $1 - 2^{-4} - 0.0110$
$= 0.1001$

∴ 11101.0110 = 00010.1001

6b Demorgans theorem with truth table

(i) $(x+y)' = x'y'$ (ii) $(xy)' = x'+y'$

∴

x	y	x'	y'	(x+y)'	xy	x'y'	(xy)'	(x'+y')
0	0	1	1	1	0	1	1	1
0	1	1	0	0	0	0	1	1
1	0	0	1	0	0	0	1	1
1	1	0	0	0	1	0	0	0

6 c minimize the fallowing function

$F(x,y,z) = xy + x'z + yz$
$= xy + x'z + yz(x+x')$
$= xy + x'z + xyz + x'yz$
$= xy + x'z(1+y) + xyz$
$= xy + x'z.$

6 C ② $F_1(x,y,z) = \overline{x'yz' + x'y'z}$, Compliment

$= \overline{x'yz'} \cdot \overline{x'y'z}$

$= (\overline{x'yz'})(\overline{x'y'z})$

$= (\overline{x'} + \overline{y} + \overline{z'})(\overline{x'} + \overline{y'} + \overline{z'})$

$= (x + y' + z)(x + y + z')$

$F_2(x,y,z) = \overline{x(y'z' + yz')}$, Compliment

$= \overline{x(y'z' + yz')}$

$= \overline{x} + \overline{(y'z' + yz')}$

$= x' + (\overline{y'+z'}) \cdot (\overline{y+z'})$

$= x' + (\overline{y'} \cdot \overline{z'}) \cdot (y' + \overline{z})$

$= x' + (y \cdot z)(y' \cdot z)$

$= x' + (y+z)(y'+z') = F_2'$

$\Rightarrow x + (y'+z')(y+z)$

$= x' + (y+z)(y'+z') = F_2'$

7 a. Compare Embedded System and General Computing system.

General purpose Computing system	Embedded system
A system which is combining of general Hardware & general operating system for variety of application	A system which is a Combinational of special purpose hardware and embedded os for executing of Specific set of application

Contains general purpose operating system (GPOS)	may or may not contain operating system for functioning
Applications are alterable by user	If is pre-programmed & Non alterable
Performance is key deciding factor in the selection of system Faster is Better	Application specific requirements are the key deciding factors
less / not reduced operating power requirements	Highly tailored of power saving modes & operating system
Response requirements are not time critical	Response time requirement is highly critical
Need not deterministic in execution behaviour	Execution behaviour is deterministic Hard Real time systems

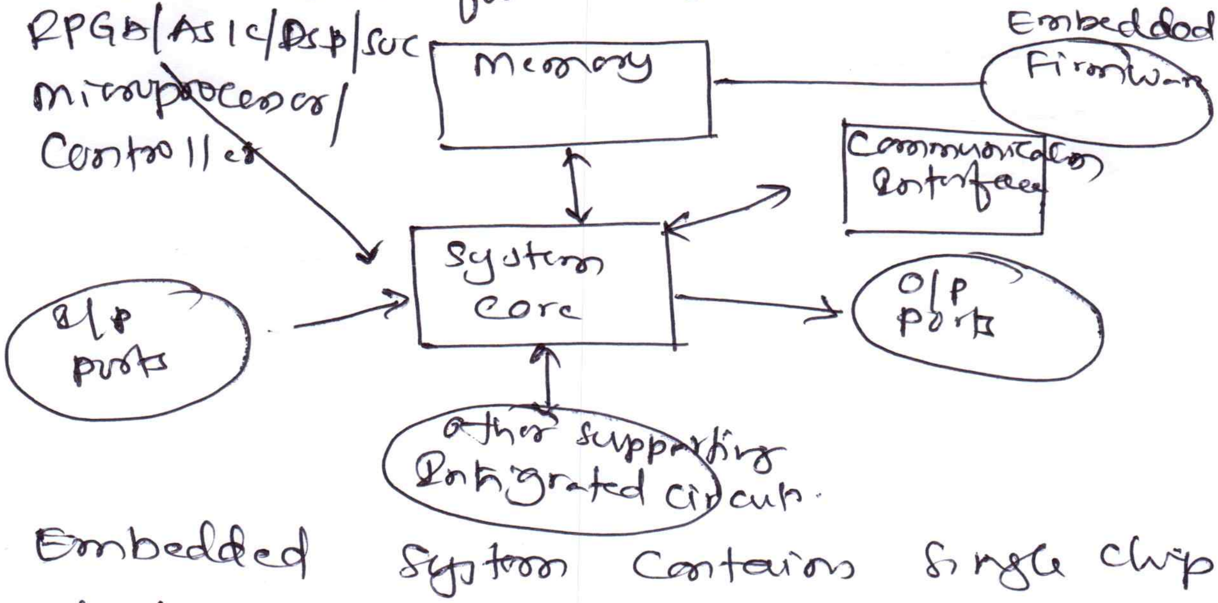
Applications of Embedded systems

1. Consumer electronics : camera, Camcords
2. Household applications : Washing machine, DVD
3. Home automation & security systems : AC, sprinkler, Alarm
4. Automotive industry : Antilock breaking system (ABS)
5. Telecom
6. Computer pheripherals
7. Health care
8. Measurement & Instrumentation
9. Banking and Retail
10. Card Readers.

7b Core of Embedded System with Block diagram

Embedded Systems are domain and application specific and are built around a Central core. The core of the embedded systems fall into any one Catagorie.

1. General purpose and domain specific processors
   1. microprocessor 2. microcontroller ③ Digital signal processor
2. Application specific integrated circuits (ASICs)
3. programmable logic devices.
4. commercial off the self components (COTS)



Embedded System contains single chip controller which acts as master of the system microprocessor (Intel 8085), Microcontroller (Atmel AT89C51) FPGA, (Field programmable gate array) Xilinx Application specific integrated circuit (ASIC).

Embedded System can be viewed as reactive system. The control is achieved by processing information coming from the sensor and user interfaces and controlling some actuators, that

regulate the physical variable
Keyboards, switch buttons - user interface i/p devices, LED, LCD, piezoelectric, buzzer, user interface output devices. Embedded systems are designed for handheld application.
Memory of the system is responsible for holding control algorithm and other important configuration details. For most of the embedded system for storing the algorithm or configuration data is of fixed type which is a kind of Read only memory (ROM) and not available for end user for modification. Random access memory (RAM) is used for most of the system as the working memory. The size of RAM varies from few bytes to kilo bytes or mega bytes, depending on the application.

7 c Transducers are devices that convert the energy in the form of sound, light, heat into its equivalent electrical signal or vice versa
Loudspeaker - low frequency electrical current into audible sounds, microphone transducers perform non electrical to electrical conversion

Transducer Converting Sand, pressure variation into voltage or current, microp hone is an input transducers, Loudspeak er is an output transducer.

Sensors: Sensors is the specific kind of the transducer that generates electrical signal measurement, instrumentation or control system signal is produced by sensor is elect rical analogy. Choice of sensor is governed by a number of factors accuracy, resolution cost and physical size.

Sensor is Active or passive.

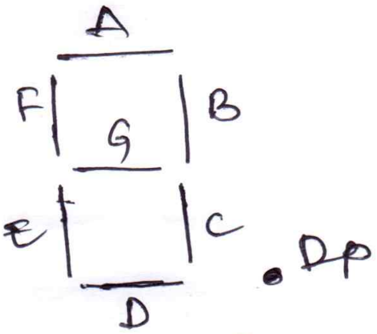
Active sensor generates current or voltage output, passive sensors requires source of current, or voltage and modifies this in some way.

Actuators: Actuator is a form of transducer device (mechanical or electrical) which converts signal to the corresponding physical action (motion). Actuator acts as an output device.

29

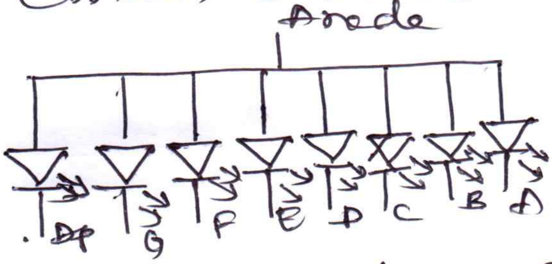
8a 7 Segment LED display is an output device for displaying alphanumeric characters. It contains 8 LED (light emitting diodes). 7 are used for displaying the alpha numeric and one is used to represent decimal point

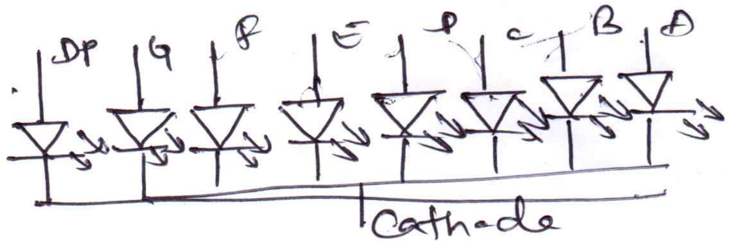
LED segments are named A to G and decimal point LED is named Dp



For example displaying number 4, the segments FGBC are lit All these 8 LEDs are connected to one port of the processor.

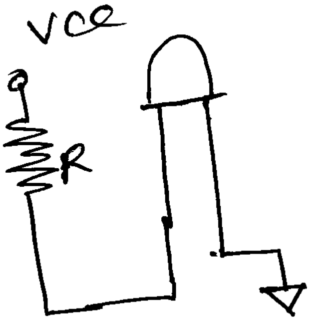
The seven segments LED are available in two different configuration Common Anode & Common cathode





Based on the configuration anode or cathode is connected to the port of the processor controller A segment to least significant port pin, Dp other most significant port pin is connected. The value of current range of 20mA. Current can be limitted by connecting the current limitter resistor to the anode or cathode of each segment

LED – Light Emitting diode is
important output device for visual indicati
on in any Embedded system. LED can be
used as an indicator for the status of various
signal. Indicating the presence of power condi
tion, like device ON, Battery low, Charging
LED is p-n junction diode and it contai
ns anode and cathode. For proper functi
oning of LED the anode should be connect
ed to positive terminal of the supply
voltage and cathode to the negative termi
nal of the supply voltage. The current flowing
through the LED must be limitted to a value
below a maximum current that it can
conduct and LED to limit the current
a resistor is used in series between the
power supply and the LED



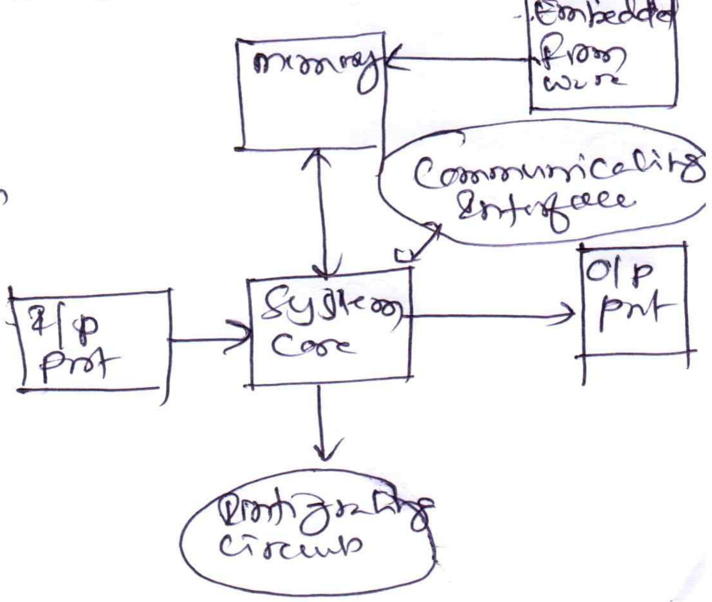
LED is interfaced to the processor
port port of the processor
Anode is directly connected
to the port pin and port
pin drives the LED.
cathode of LED is connected
to the port pin of the processor. and anode is
to the supply ~~logic~~ voltage through the
current limitting resistor.

8b Embedded system is an electronic/ electro mechanical system to perform a specific function and is a combination of both Hardware & Firmware (Software)

Elements of Embedded system, It contains a single chip controller which act as a master brain of the system, The controller can be a microprocessor (Intel 8085), microcontroller (Atmel AT89C51), Field programmable Gate Array, Digital signal processor (DSP) from Analog devices.

Embedded basically designed to regulate physical variable or manipulate the state of some device by sending some control signal to the actuators or device connected to the o/p port of the system. Embedded system can be reactive system the control is achieved by processing the information coming from the processor and user interface.

① Key board, Actuators
② Communication interface
③ Integrated circuits
④ I/O user interface.
⑤ memory
⑥ Embedded Firmware
⑦ System Core (FPGA) ASIC, DSP



8c Classification of embedded System

① Based on Generation ② complexity of performance
③ Based on deterministic behaviour ④ Based on trigger

① Classification based on generation

1. First Generation – Embedded system build around 8 bit microprocessor, 8085, Digital telephone keypads
2. Second Generation: Built around 16 bit microprocessor and microcontroller, Instruction set more complex and powerful than first generation, It contains embedded operating system
3. Third Generation – Powerfull 32 bit processor & 16 bit microcontroller. Application and domain specific processor. The instruction set and processor are powerfull and concept of pipelining evolved (ASIC), Robotics, media, and Industrial control
4. Fourth generation: Advanced system on chip, reconfigurable processor and multi core processor, high performance, tight integration and miniaturization into embedded device market

2. Classification based on complexity and performance

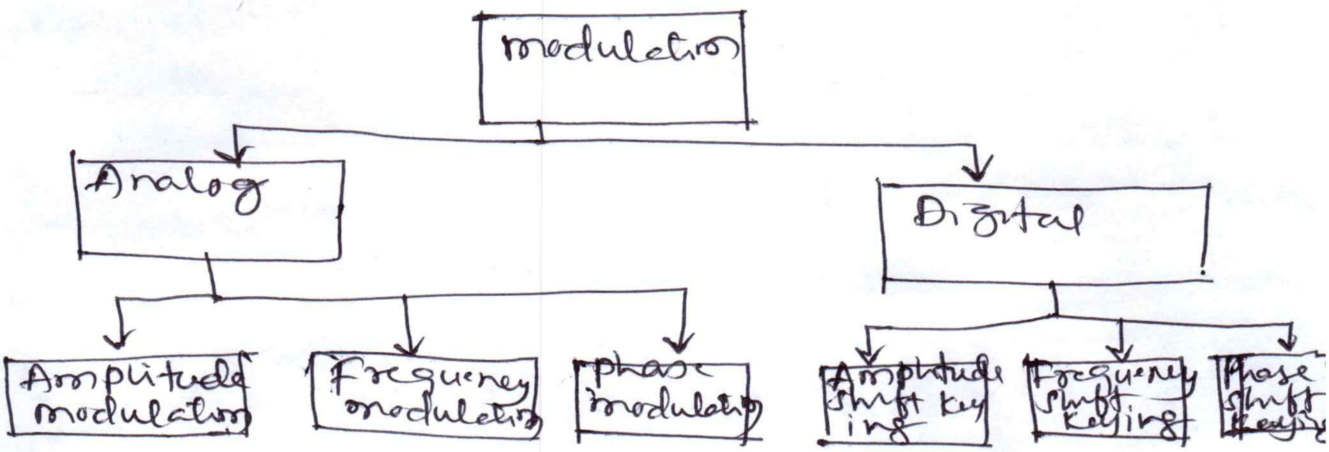
① Small scale embedded systems → embedded system which are simple application and not time critical. low performance and low cost, 8bit 16 bit microprocessor

② Medium scaled Embedded systems Slightly complex in hardware and Firmware, Built around medium performance low cost 16 or 32 bit. This contain an embedded operating system

③ 3. Large scale embedded systems: which involves complex hardware and Firmware. They built around high performance 32 or 64 bit RISC processors Reconfigurable system on chip (RSOC) & multi core processor and programmable logic devices. They contains multiple processor, Decoding / encoding of media cryptographic function implementation

9. a. Different types of modulation

Modulation is the process in which any of the parameter (amplitude, frequency or phase of the high frequency carrier signal is varied according to the instantaneous value of low frequency message signal. Keeping other parameter constant

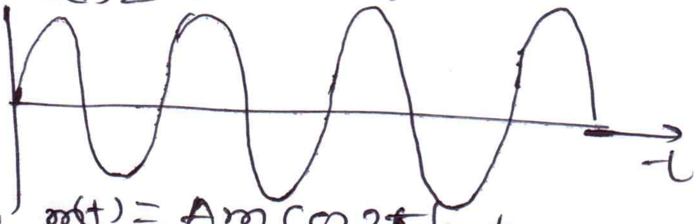


Analog modulation typically used for AM FM, Radio, Short wave Broad casting

Digital modulation involves transmission of binary (0 and 1)

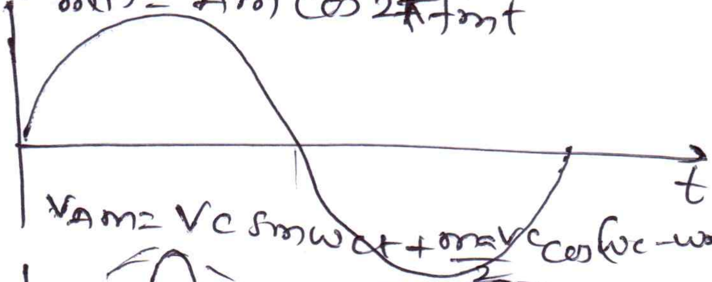
Amplitude modulation is the process in which the amplitude of carrier signal is according to the instantaneous value 33 of the message signal, where the frequency and phase are kept constant

$c(t) = A_c \cos 2\pi f_c t$



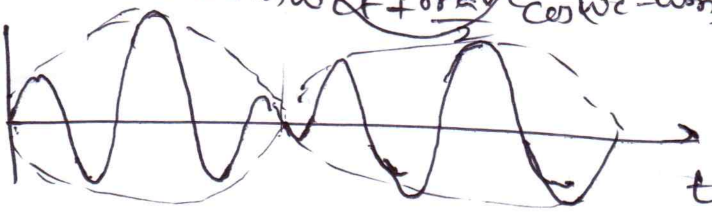
carrier signal

$m(t) = A_m \cos 2\pi f_m t$



message signal

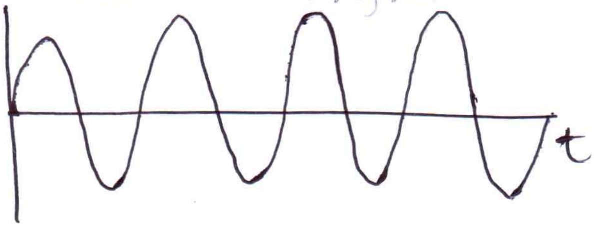
$V_{AM} = V_c \sin \omega_c t + \frac{m_a V_c}{2} \cos(\omega_c - \omega_m)t + \frac{m_a V_c}{2} \cos(\omega_c + \omega_m)t$



Amplitude modulated signal

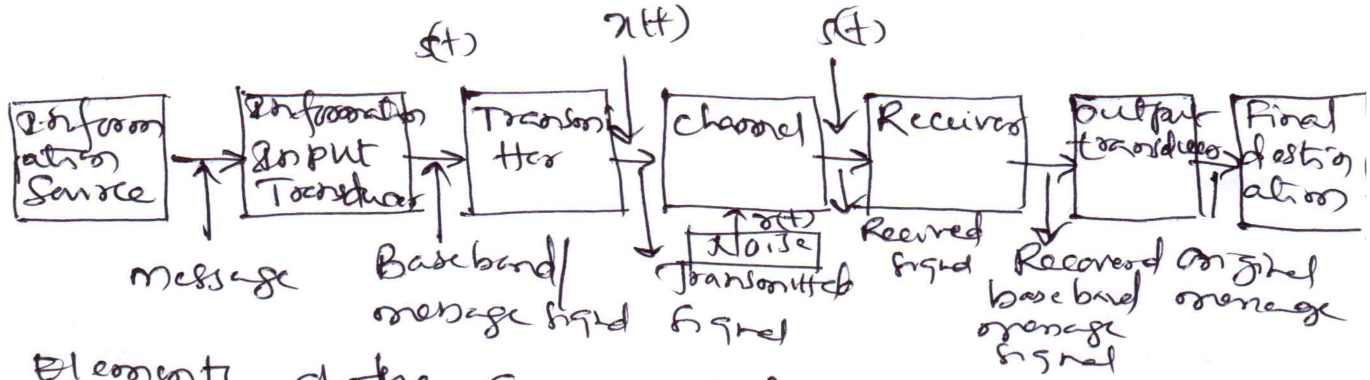
Frequency modulation is defined as a process in which the frequency of the carrier is varied in accordance with the instantaneous value of the message signal. whereas the amplitude and phase are kept constant

Carrier signal



9b Modern communication system

General from of basic communication system is shown in fig



Elements of the communication system

Information source and Transducer - Non electrical signal are converting it into electrical signal

Transmitter - Base band signal (Electrical form) applied to the input transducer. The transmitter performs the operation filtering, amplification and modulation. The nature of processing depends on the type of the communication system.

Base band signal which lies in the low frequency spectrum and is translated to a high frequency spectrum - carrier communication system.

s(t) → Base band signal, x(t) → modulated signal

s(t) is super imposed upon high frequency carrier

Finaly signal is passed to the transmissi on medium or channel. Transmitted signal should have the adequate power to withstand the channel noise. The channel characteristics also impose constraints on the Band width.

Hardwired channel

Transmission line, co-axial cable, twisted pair cables, wave guides, optical fiber

Softwired (No physical link) Air or open space

Noise - Noise is defined as unwanted electrical signal which is not having information 29

Receiver - The receiver is to reproduce original message signal. The reproduction of original signal is accomplished by a process of demodulation or detection

Demodulation is a reverse process of modulation. The received signal is r(t). The received signal is weak signal. voltage amplifier amplifies further processing, its voltage and power is amplified before send to the final destination block

Destination : Destination is the final stage which is used to convert an electrical message signal into its original form, the destination is loudspeaker which works as transducer that converts electrical signal to original sound signal.

9C Advantages of Digital Communication over Analog Communication

Most of the signals are in analog in nature. Digital signals are obtained from analog domain by technique, sampling, Quantization and encoding. digital signal have many advantages of digital communication over Analog communication

• Digital communication is lossless transmission 27
Internet and cyberspace could not exists without digital communication
Digital communication is fast, easier and cheaper
Digital communication is more immune to noise
Digital circuits are more reliable and consume less power

Digital circuit easy to design and cheaper than analog circuits
Hardware implementation is more flexible, easy to implement, less expensive, powerful microprocessors
• occurrance of cross-talk is very rare
• Encryption in digital domain allows security of data
• Compression allows data to reduce in lesser in size
• probability of error occurrance is reduced due to error detecting and error correcting codes.
• Spread spectrum techniques is used to avoid signal jamming
• multiplexing is quite easy
• Better voice quality over a long distance
• Deliver more information with greater portability
• Simple to use digital devices with flexible features.

10a. Radio waves propagation.

Radio waves exhibit the properties of light with the velocity 3×10^8 m/s. These EM wave consists of Electric and magnetic field components traversed perpendicular to one another in nature.

EM waves exhibit properties such as reflection, diffraction, absorption, Polarization and scattering

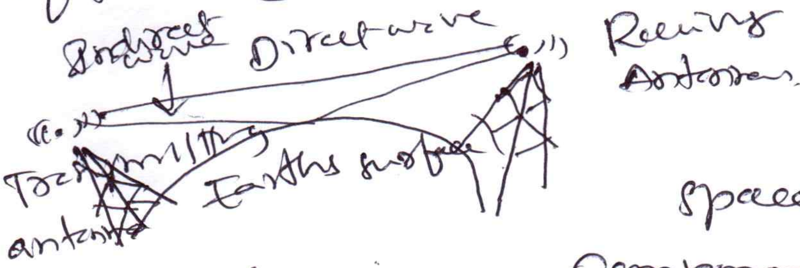
① Ground or surface wave: Ground wave can be used for radio wave propagation. Ground wave transmission is very reliable irrespective of atmospheric conditions. Frequency range 30 kHz to 3 MHz, Transmission distance 100–1000 km, Example AM radio broad cast

② Space or tropospheric wave propagation

Radio waves moves in the earth's troposphere or within about 12 km over the surface of the earth

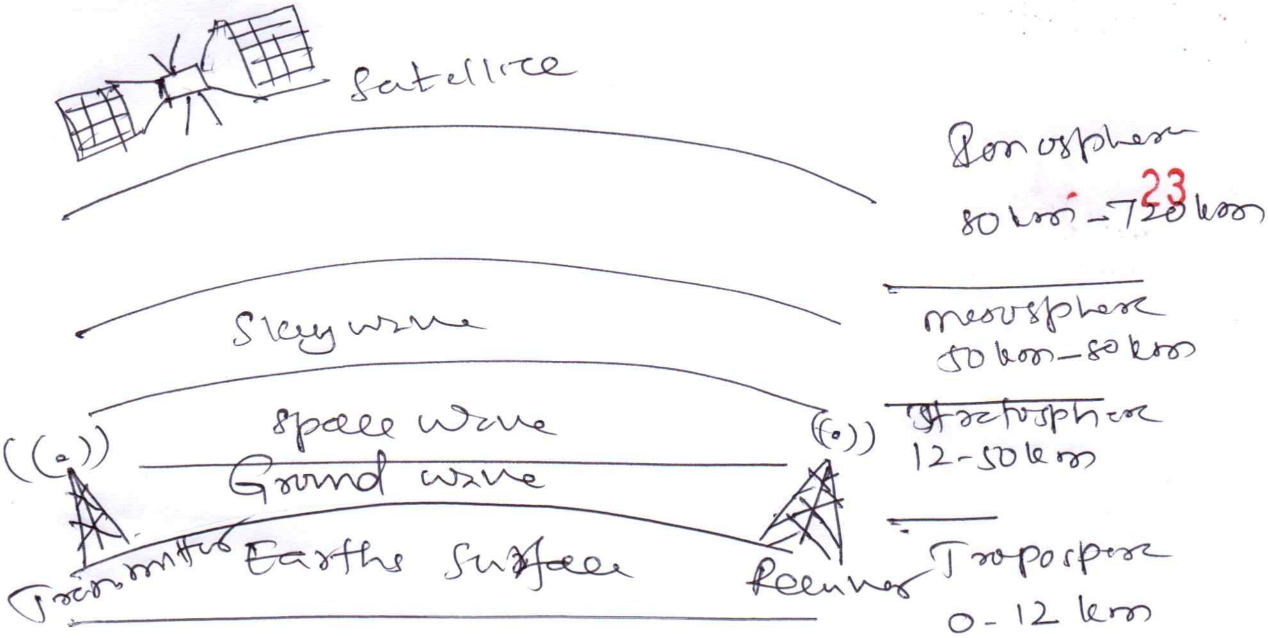
Frequency range 3-MHz to 30MHz

TV Transmission



Space wave made of two components ① Direct wave ② Indirect wave (Ground reflected wave

③ Sky wave: Radio waves transmitted from the transmitting antenna to the receiving antenna after reflection from Ionosphere

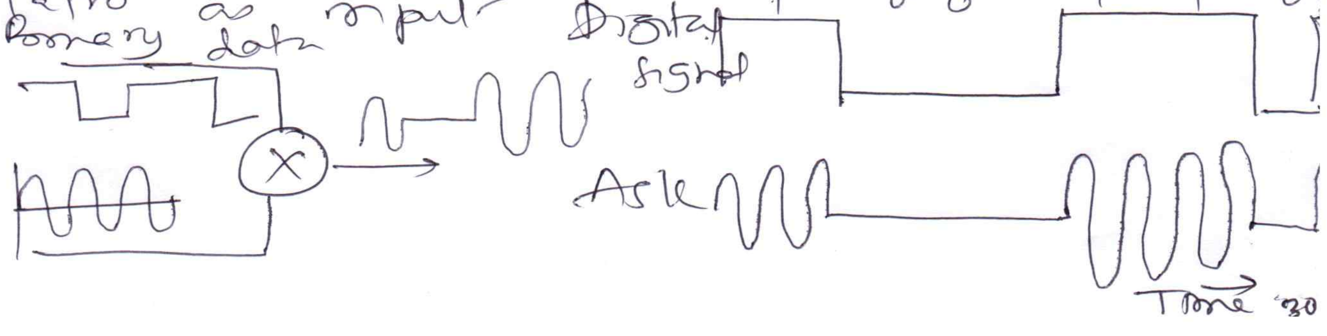


Sky wave is responsible for short wave transmission around the globe via successive reflections at the ionosphere and earths surface.

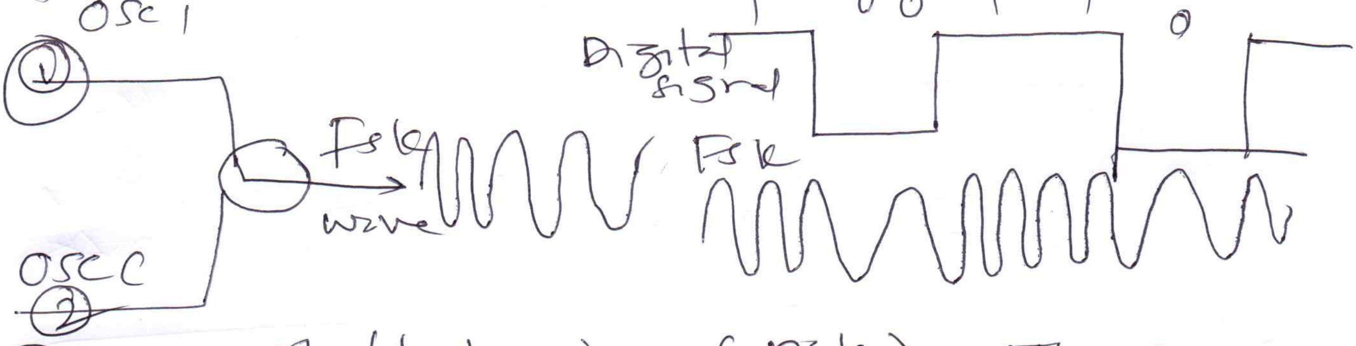
10b Modulation schemes: Digital modulation schemes are classified as

1. Amplitude shift keying (ASK)
2. Frequency shift keying (FSK)
3. Phase shift keying (PSK)

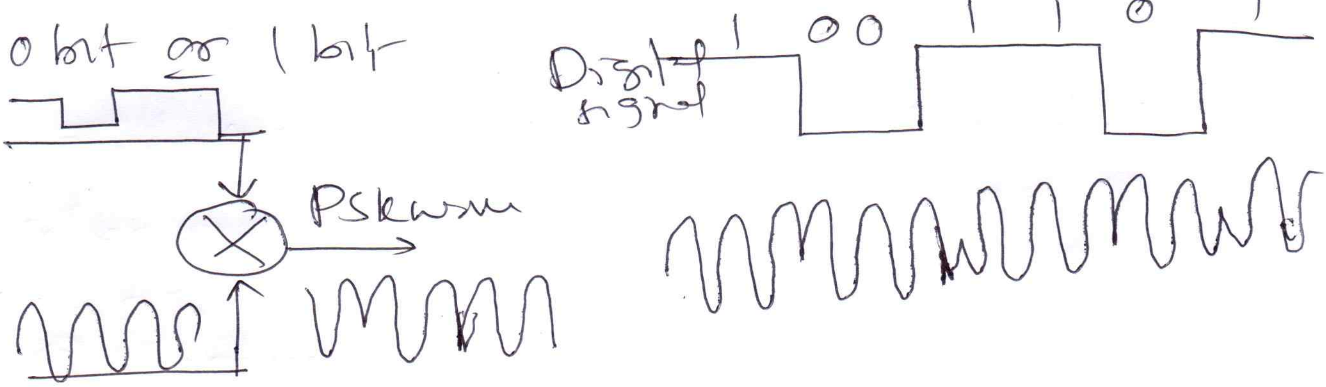
(1) ASK – represents digital data as a variation in the amplitude of a carrier wave. ASK signal can be generated when incoming binary data and sinusoidal carrier are applied to a product modulator as input



(ii) FSK — Digital signal is transmitted by switching between low frequency and high frequency in order to represent 0's and 1's

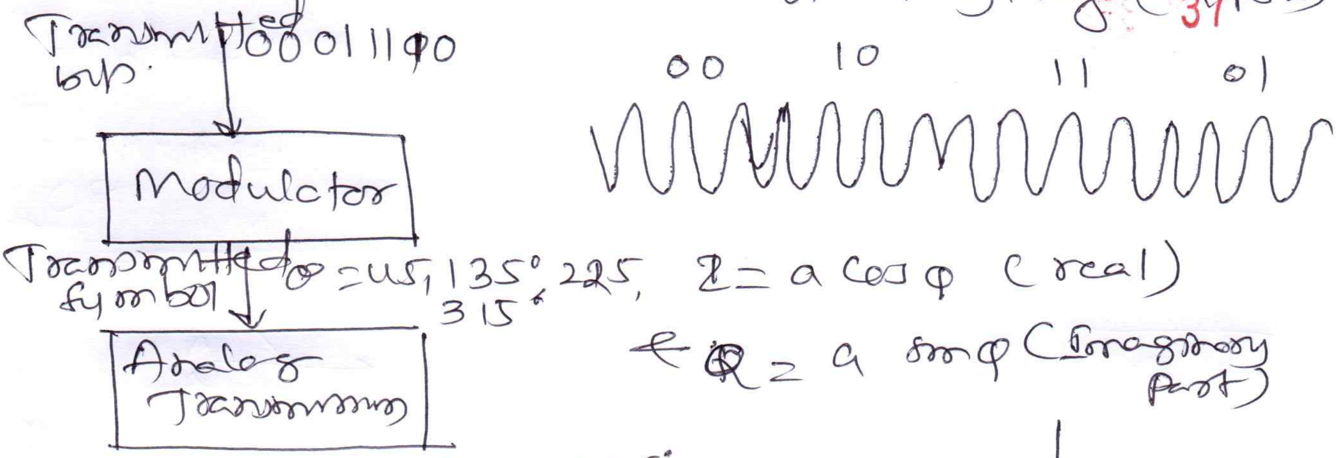


(iii) Phase Shift keying (PSK) — The carrier phase shifted between two different phases (0 and 180° depending on whether 0 bit or 1 bit



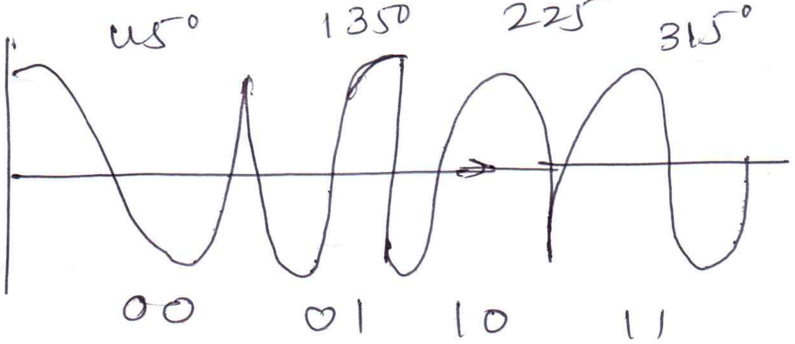
10c Radio signal transmission: wireless transmitter accepts 4 different binary streams of bits 00 01 10 10 from the application software and is encoded as radio wave known as a carrier is adjusting its amplitude or phase
Transmitter operates in two stages which generates radio waves.

Quadrature Phase Shift Keying (QPSK) 37

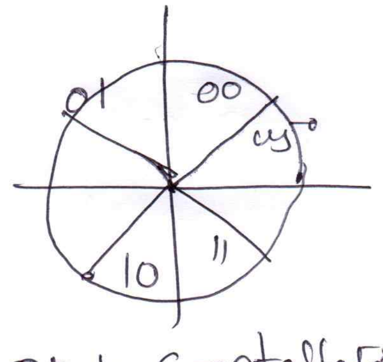


$\phi = 45, 135°, 225, 315°$, $I = a\cos\phi$ (real)

& $Q = a\sin\phi$ (Imaginary part)



QPSK representation



QPSK Constellation diagram

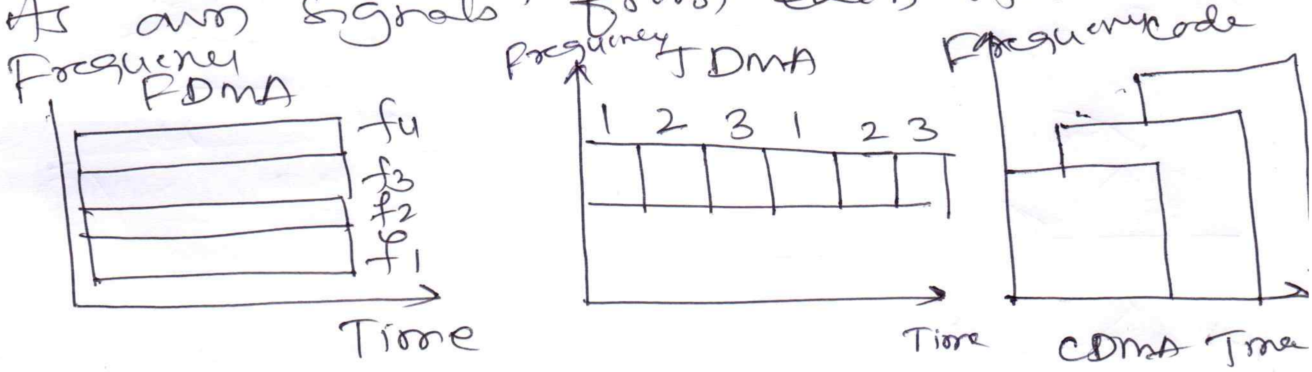
Multiple access Techniques: provide communication to the multiple users over a single channel. Multiple mobile users share the allotted spectrum in the most effective manner

① FDMA → Frequency division multiple access
Available band split into the small frequency channel and different channels are assigned to the different users

② TDMA → Time division multiple access
Various users can transmit at the same frequency band. Every user permitted to transmit specific time slot using common frequency band

③ Code division multiple access.

mobile receives signals on the same carrier frequency and at the same time but the signals are labelled by use of codes. which allows mobiles to separate its own signals from each other



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