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Scheme & Solution for Model Question Paper

Subject : Basic Electronics

Subject code : BBEE103

Prepared by : Dr. Arun Kakhandki

Faculty

HoD-ECE

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Dean (Academics)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG
KLS VDIT
HALIYAL

Model Question Paper-I/II with effect from 2022-23 (CBCS Scheme)

USN | | | | | | | | | | |

First/Second Semester B.E. Degree Examination

Basic Electronics

Max. Marks: 100

TIME: 03 Hours

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE.**
02. Missing data may be suitably assumed.

		Module -1	Bloom's Taxonomy Level	Marks
Q.01	a	Explain the forward and reverse characteristics of a silicon diode	L1	8
	b	Describe the working of a capacitor filter for a half wave rectifier with a neat circuit diagram and necessary waveforms.	L2	8
	c	Determine the peak output voltage and current for a bridge rectifier circuit when the secondary RMS voltage is 30V and the diode forward drop is 0.7V.	L3	4
		OR		
Q.02	a	Describe the working of full wave rectifier with a neat circuit diagram and necessary waveforms.	L1	8
	b	Explain how a Zener diode can be used as voltage regulator by considering the no load and loaded condition.	L2	8
	c	A diode with VF=0.7V is connected as a half wave rectifier. The load resistance is 500Ω and the secondary RMS voltage is 22V. Determine the peak output voltage and the peak load current.	L3	4
		Module-2		
Q. 03	a	Explain the output characteristics of a transistor in common emitter configuration.	L1	8
	b	Explain the working of an n-channel JFET.	L1	8
	c	With respect to BJT, describe the concept of obtaining the DC load line.	L2	4
		OR		
Q.04	a	Explain the Enhancement type MOSFET along with the drain characteristics.	L1	8
	b	Explain the common base output characteristics.	L1	8
	c	Describe how a transistor can be used a voltage amplifier.	L2	4
		Module-3		
Q. 05	a	With respect to an op-amp explain the following: I. Input offset voltage II. Slew rate	L1	8
	b	Describe a summing amplifier using an op-amp in an inverting configuration with three inputs.	L2	8
	c	An inverting amplifier using op-amp has a feedback resistor of 10KΩ and one input resistor of 1KΩ. Calculate the gain of the op-amp and the output voltage if it supplied with an input 0f 0.5V.	L3	4
		OR		

Q. 06	a	Describe the block diagram representation of an op-amp. Also describe its operational behavior with an equivalent circuit.	L1	8
	b	Describe an integrating amplifier using an op-amp in an inverting configuration.	L2	8
	c	Develop a summer circuit using op-amp to get the following output voltage $V_o = -(2V_1 + 2V_2)$	L3	4
		Module-4		
Q. 07	a	Convert the following: i. $(110.1101)_2=(?)_{10}$ ii. $(847.951)_{10}=(?)_8$ iii. $(CAD.BF)_{16}=(?)_{10}$	L3	6
	b	Express the Boolean function F=A+BC in a sum of minterms	L3	6
	c	Describe how NANd and NOR gates can be used as universal gates.	L2	8
		OR		
Q. 08	a	Simplify the following: i. $Y = AB + \bar{A}C + BC$ ii. $Y = (A + \bar{B} + \bar{B})(A + \bar{B} + C)$ iii. $Y = C(B + C)(A + B + C)$	L3	6
	b	Express the Boolean function $F = XY + \bar{X}Z$ in a product of maxterms	L3	6
	c	Describe the working of the full adder using basic gates.	L2	8
		Module-5		
Q. 09	a	Explain the working of the potentiometric resistive transducer.	L1	8
	b	Write a note on photodiodes.	L1	6
	c	Explain the various blocks involved in an electrical communication system.	L1	6
		OR		
Q. 10	a	Explain the working of Linear Variable Differential Transducer.	L1	8
	b	Write a note on piezoelectric transducer.	L1	6
	c	What is modulation? Describe the need of modulation in communication systems	L1	6

Basic Electronics - (BBEE103) Model QP

PAGE NO.: 1
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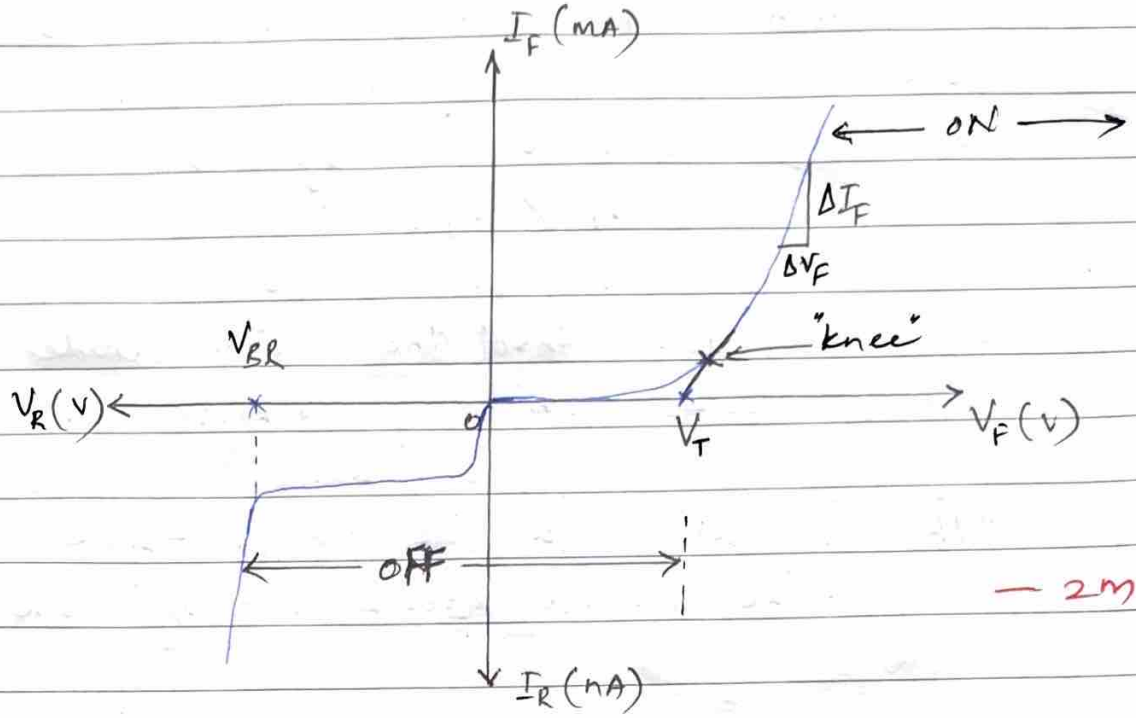
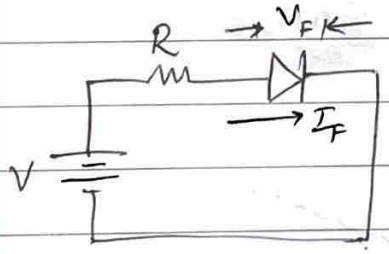
Module - 1

Q.1.) a) Explain the forward and reverse characteristics of a silicon diode — 8M

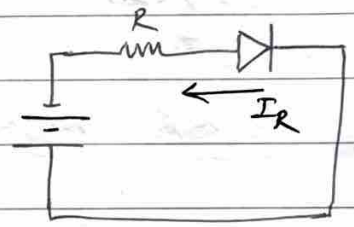


— 2M

Forward biased



Reverse biased



— 2M

V-I characteristics of a p-n junction diode is a plot of V/g. applied across the p-n jn and the current flowing thro' the p-n jn.

A diode conducts a large forward biased with its anode at a positive potential w.r.t. cathode. It conducts a comparatively much smaller current (reverse current) in reverse biased.

In forward biased, the forward current, I_F.

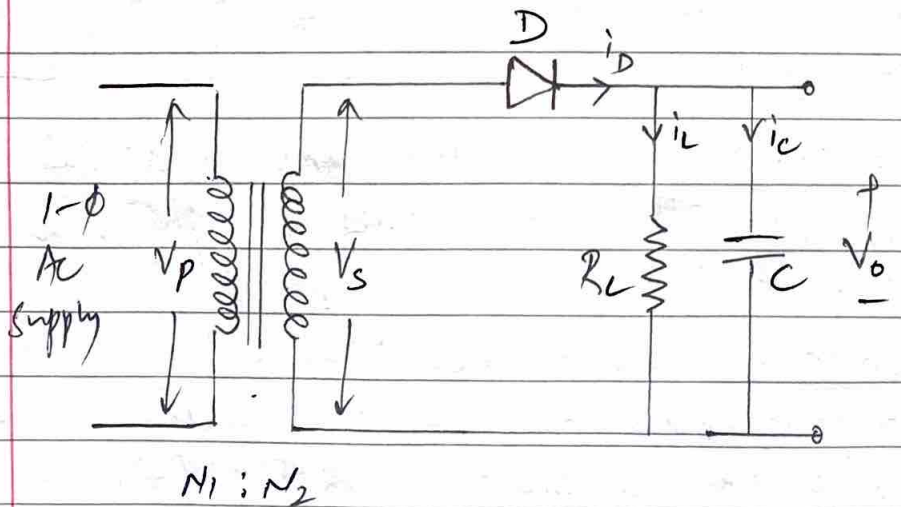
remains very low until the forward bias voltage across the diode exceeds 0.7 V, beyond which the current rapidly increases and the diode is said to be "ON". This V$_\gamma$ of 0.7 V is called the cut-in or threshold V$_\gamma$. $V_\gamma \approx V_T$. Thus diode turns-on for $V_F > V_T$.

When reverse biased, a very small current I_R which flows thro' the silicon diode until the p-n jn breaks down at a reverse V$_\gamma$. The diode is said to be "OFF" for forward V$_\gamma$s less than V_T. This V$_\gamma$ at which the p-n jn breaks down is called the "reverse breakdown V$_\gamma$". and $I_R << I_F$.

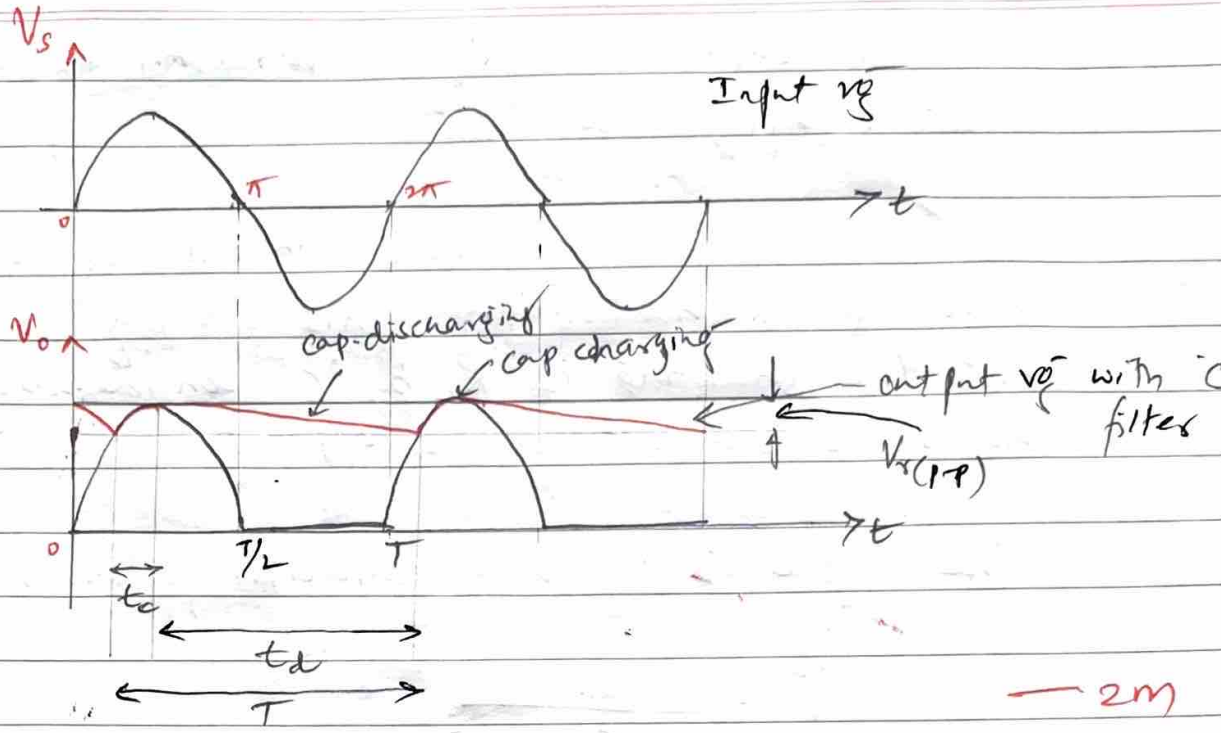
— 4m

Q. 1) b) Describe the working of a capacitor filter for a half-wave rectifier with a neat circuit diagram and waveforms — 8m

Soln HWR with capacitor filter :



— 2m



Notations :

$V_{o(p-p)}$ is peak-to-peak ripple vg on capacitor

t_c is charging time of capacitor

t_d is discharging time of capacitor

$T = t_c + t_d$ is time period of o/p waveform.

Working principle :

During +ve half-cycle of the ac supply, the diode conducts & charges the capacitor to the peak value of V_m.

During -ve half cycle, diode is reverse biased and capacitor starts discharging in to R_L and the vg. on the capacitor decreases. The discharging of the capacitor continues till the diode starts conducting again and charges the capacitor in the next +ve half-cycle of ac supply.

From the waveforms it is found that, without capacitor filter, V_o varies between zero and V_m

and with capacitor filter the variation is between $(V_m - V_{r(p-p)})$ and V_m.

With filter the variation in o/p V_o is smaller than that without filter. This clearly indicates that the shunting of R_L by C considerably reduces the ripple content of the o/p vg.

The ripple factor with capacitor filter is given by

$$\gamma = \frac{1}{2\sqrt{3}\, f \cdot R_L C}$$

γ can be kept small by using a large value of capacitor filter. — 4m

Q.1) c) Determine the peak output vg. and current for a bridge rectifier circuit when the secondary RMS vg. is 30 V and the diode forward drop is 0.7 V. R_L is 300 Ω — 4m

Solⁿ Given: $V_s = 30$ V rms $\quad V_T = 0.7$ V

$V_{po} = ?$ $\quad I_{po} = ?$

Load $R_L =$ 300 Ω.

$$\therefore \quad V_m = \sqrt{2} \cdot V_s = \sqrt{2} \times 30 = 42.43 \text{ V} \quad \text{— 1m}$$

Peak output vg, $V_{po} = V_m - 2V_F$

$= 42.43 - 2 \times 0.7$

$V_{PO} = 42.43 - 1.4$

$= 41.03\ V$ — 1 m

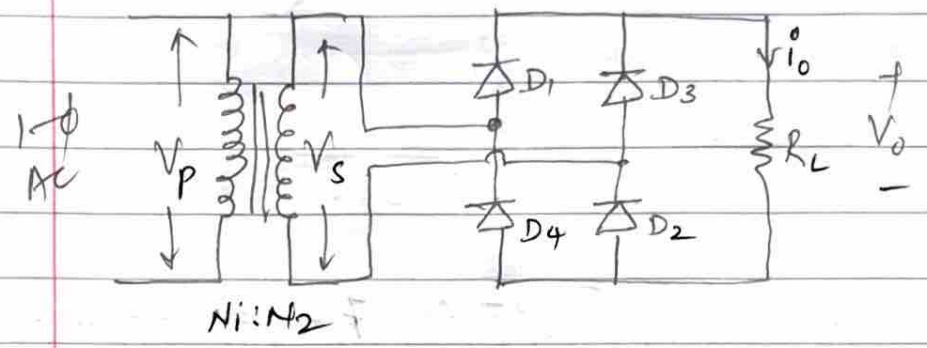
Peak output current, $I_{PO} = \frac{V_{PO}}{R_L}$

$= \frac{41.03}{300}$

$I_{PO} = 0.137\ A = 137\ mA$ — 2m

Q.2) a) Describe the working of full wave rectifier with a neat circuit diagram and necessary waveforms — 8m

Soln FWR : (Bridge rectifier)



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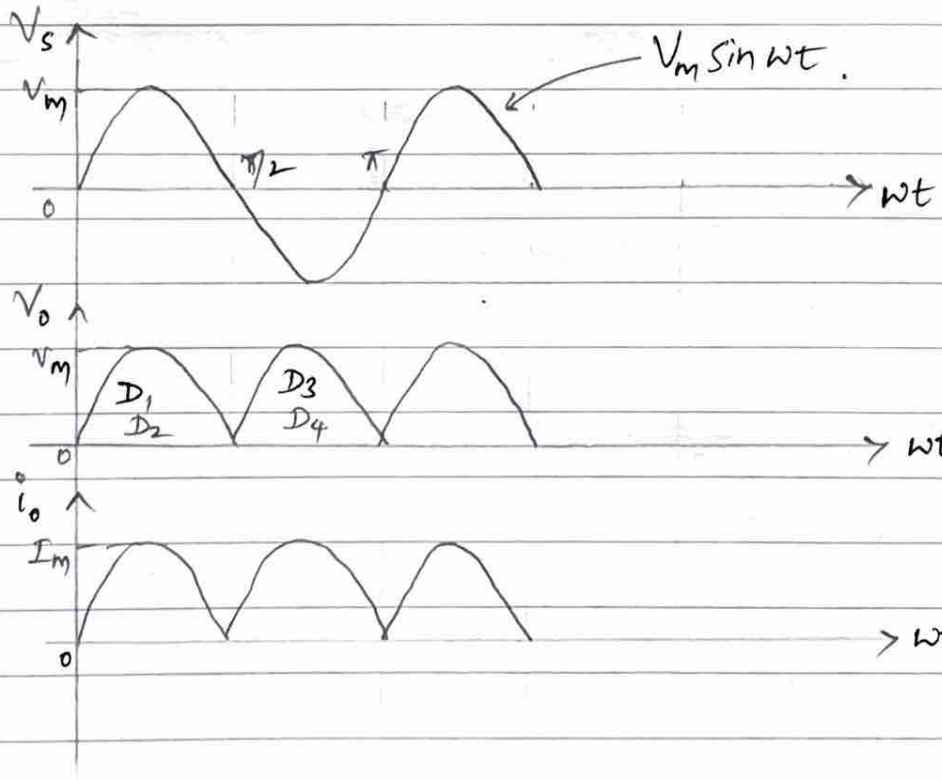


— 2m

The full wave bridge rectifier uses four diodes which are arranged in the form of a bridge.

Instantaneous primary vg. $V_p = V_m \sin \omega t$

Instantaneous secondary vg. $V_s = \frac{N_2}{N_1} \times V_p$

if $N_1 : N_2 = 1$ then $V_s = V_p = V_m \sin \omega t$.

During +ve half-cycle of ac supply, diodes D_1 & D_2 are forward biased and diodes D_3 & D_4 are reverse biased and $i_o = i_{d_1} = i_{d_2}$

During -ve half cycle of ac supply, diodes D_3 & D_4 are forward biased and diodes D_1 & D_2 are reverse biased and $i_o = i_{d_3} = i_{d_4}$

In FWR during both half-cycles of ac supply load current i_o flows thro' the load R_L in unidir-ectional.

If all the diodes are considered as ideal diodes then

$$I_m = \frac{V_m}{R_L}, \quad I_{dc} = \frac{2V_m}{\pi} \frac{1}{R_L}$$

$$I_{rms} = \frac{V_m}{\sqrt{2}} \frac{1}{R_L}, \quad V_{dc} = \frac{2V_m}{\pi}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

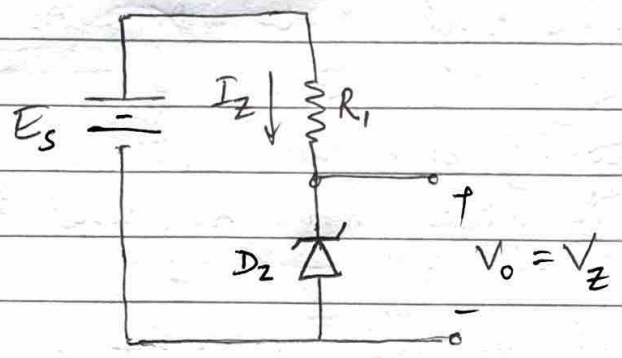
% regulation $= 0$, $\eta = 81.2\%$

$\gamma = 0.483$

— 4m

Q.2) b) Explain how a zener diode can be used as a voltage regulator by considering the no-load and loaded condition. — 8m

Soln: i) Zener diode vg. regulator with No-load condition -

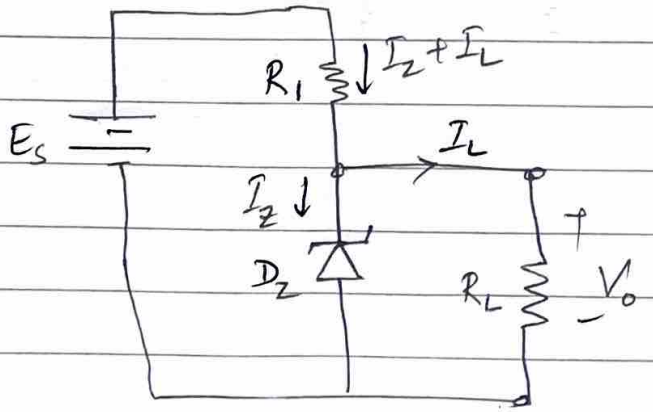


— 2m

The fig. shown above is usually employed as a voltage reference source that supplies only a ~~few~~ very low current (much lower than I_z) to the output. Resistor R_1 limits the zener diode current to the desired level.

I_z is calculated as, $I_z = \frac{E_s - V_z}{R_1}$ — 2m

ii) Zener diode vg. regulator with Loaded condition -



— 2m

When a zener diode regulator has to supply a load current (I_L), the total supply current flowing thro' resistor R_1 is the sum of I_L & I_Z.

It should be ensured that the minimum zener diode current is large enough to keep the diode in reverse breakdown.

The circuit current eqn is given by

$$I_Z + I_L = \frac{E_s - V_Z}{R_1}$$

— 2m

Q.2) c) A diode with $V_F = 0.7$ is connected as a HWR. The load resistance is 500Ω and the secondary rms vg is 22V. Determine the peak o/p vg. and the peak load current — 4m

Soln Given: $V_s = 22V$ rms, $V_F = 0.7V$, $R_L = 500\Omega$.

$\therefore V_m = \sqrt{2} \cdot V_s = \sqrt{2} \times 22 = \underline{31.1\ V}$ — 1m

Peak o/p vg, $V_{PO} = V_m - V_F$

$V_{PO} = 31.1 - 0.7 = \underline{30.4\ V}$ — 1m

Peak load current, $I_{PO} = \frac{V_{PO}}{R_L}$

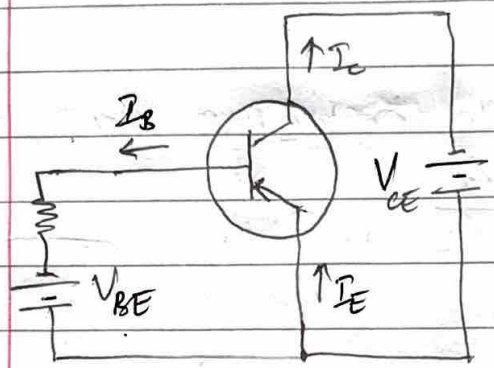
$= \frac{30.4}{500}$

$I_{PO} = \underline{60.8\ mA}$ — 2m

Module-2

Q.3) a) Explain the output characteristics of a transistor in CE configuration. — 8m

Soln: **CE configuration:**



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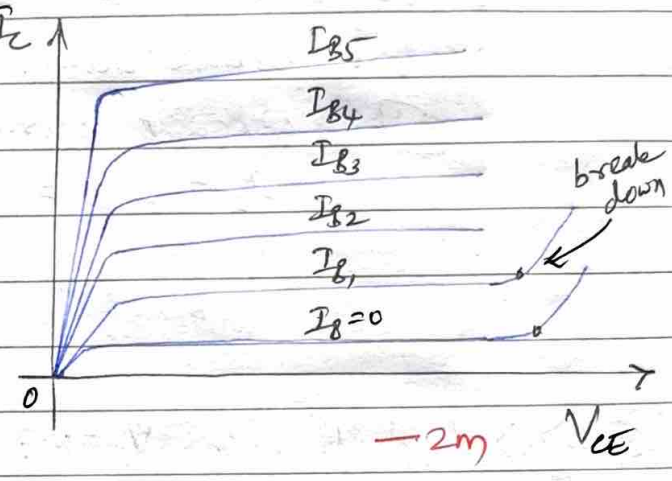


— 2m

The CE o/p characteristics shows the variation of I_c as a function of V_{CE} at constant I_B. I_B is set to a convenient value, V_{CE} is varied in suitable steps and at each step I_c value is recorded. The same procedure is repeated for different settings of I_B. When these results are plotted a family of o/p characteristics is obtained.

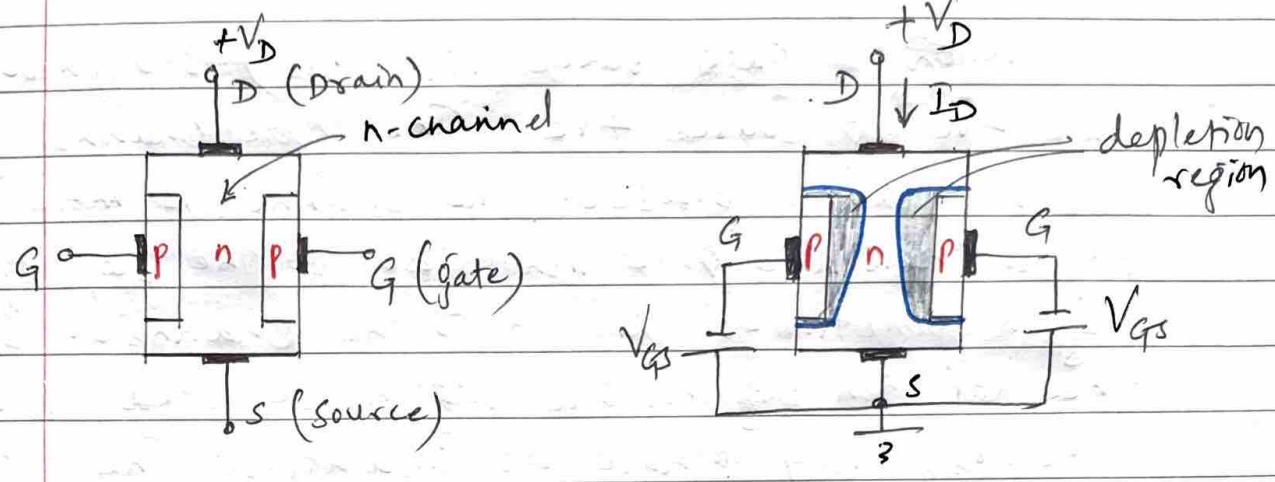
With increase in V_{CE}, the base width decreases due to increase in the depletion width of CB jn. Therefore more charge carriers are drawn from emitter to the collector. Thus 'I_c' increases to same extent with increase in V_{CE} although I_B is held constant.

As a result the slopes of the common-emitter output characteristics are much more pronounced than those of CB characteristics.

— 4m

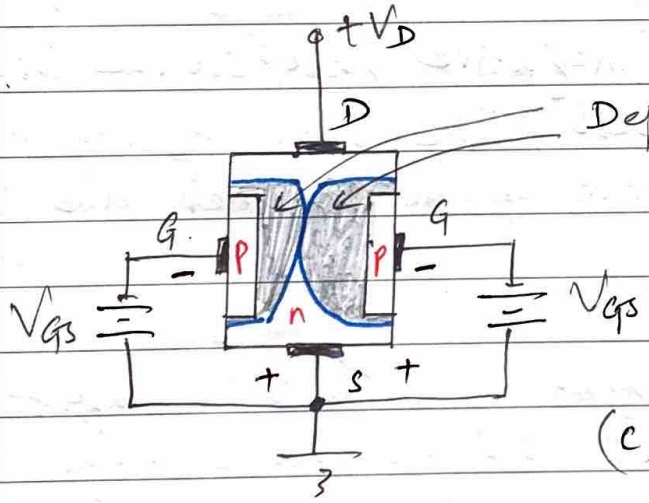
Q.3>b) Explain the working of an n-channel JFET. — 8m

Soln: n-channel JFET:



(a) No gate-source bias vg

(b) Small negative gate-source bias vg.



(c) Large negative gate-source bias vg.

— 4m

Operating principle:

In n-channel JFET, n-type semiconductor is sandwiched between two p-type semiconductors. The n-type semiconductor is referred to as "channel" and the two ends of the channel are drain (D) & source (S). P-type materials are connected together and their terminal is called as gate (G)

With no gate-source bias vg., a drain-source vg. (V_D) is applied, and drain current I_D flows from D to S.

When a gate-source vg. (V_{GS}) is applied with gate -ve & source +ve, the gate-channel pn jns are reverse biased. The channel is more lightly doped than the gate material, so the depletion region penetrates deep in to the channel. Because the depletion regions are regions depleted of charge carriers, they behave as insulators. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced.

When the negative gate-source bias vg. is further increased, the depletion regions meet at the centre of the channel, and I_D is cut-off.

When an ac signal is applied to the gate, the negative half-cycle causes the gate-channel depletion region to widen and the channel resistance is increased. This decreases the drain current.

When ac signal goes +ve the width of the depletion regions decreases, the channel resistance is reduced and the drain current increases.

Thus the gate-source vg., V_{GS}, of the JFET controls the drain current, I_D and the FET behaves as a voltage controlled current source.

— 4m

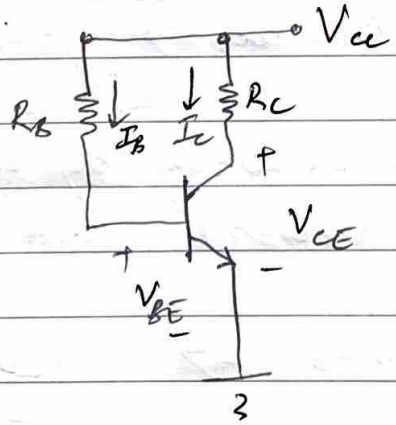
Q.3) c) With respect to BJT describe the concept of obtaining DC load line. — 4m

Soln: The dc load line for a transistor (BJT) circuit is a straight line drawn on the transistor output characteristics.

Ex-

For CE circuit, the load line is a graph of collector current (I_c) versus collector-emitter v$_{\text{ge}}$ (V_{CE}), for a given value of collector resistance (R_c) and a given supply v$_{\text{ge}}$. (V_{cc}). The load line shows all corresponding levels of I_c and V_{CE} that can exist in a particular circuit.

Consider an npn transistor in CE configuration biased in the active region.



— 1m

The dc supply v$_{\text{ge}}$. V_{cc} forward biases the B-E j$_{\text{n}}$ and reverse biases the CB j$_{\text{n}}$.

Applying KVL to BE j$_{\text{n}}$ ⇒

supply v$_{\text{ge}}$ = v$_{\text{ge}}$ a/c R_B + BE v$_{\text{ge}}$ V_{BE}

$$V_{cc} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{cc} - V_{BE}}{R_B} \quad \text{—— (1)}$$

but $I_c = \beta I_B$ or $h_{FE} I_B$ ——— (2)

Now, applying KVL to C-E ckt ⇒
Supply voltage = voltage across R_c + CE voltage V_{CE}

$$V_{cc} = I_c R_c + V_{CE} \quad \text{——— (3)}$$

From eqn (2) ⇒ when I_B is set to zero then $I_c = 0$

∴ Eqn (3) becomes

$$V_{CE} = V_{cc}$$

When $V_{CE} = V_{cc}$, the tr. is said to be in cut-off region. The co-ordinates of the pt. (say pt. A) on the o/p characteristics corresponding to the cut-off of tr. is given by

$$A(V_{CE}, I_c) = A(V_{cc}, 0) \longrightarrow \text{on X-axis}$$

When tr. is fully turned-on by adjusting I_B such that, $I_c R_c = V_{cc}$

∴ Eqn (3) becomes ⇒ $V_{CE} = 0$

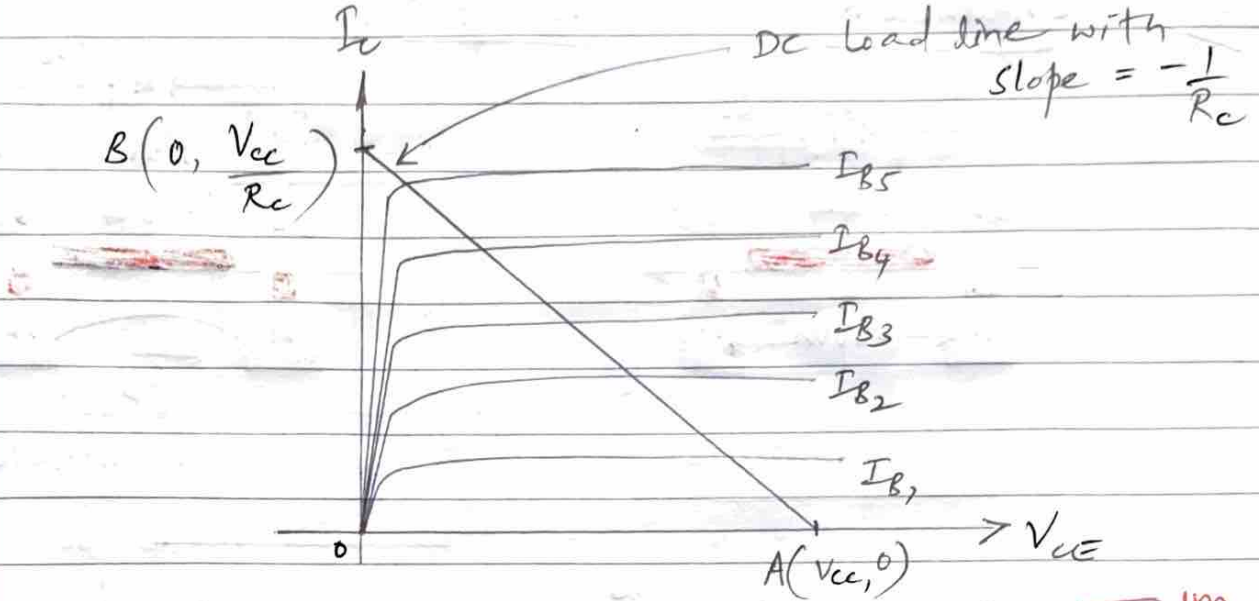
When $V_{CE} = 0$, the tr. is said to be in saturation region.

∴, The co-ordinates of pt. (say pt. B) on Y-axis is

$$B(V_{cc}, I_c) = B\left(0, \frac{V_{cc}}{R_c}\right) \longrightarrow \text{on Y-axis}$$

— 2m

The straight line obtained by joining pts. A & B on the CE output characteristics is called the DC load line.



The dc load line eqn can be obtained by eqn (3).

ie,

$$V_{cc} = I_c R_c + V_{CE}$$

$$I_c R_c = -V_{CE} + V_{cc}$$

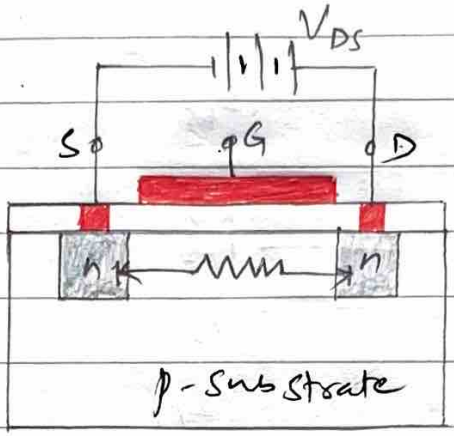
$$I_c = -\frac{1}{R_c} \cdot V_{CE} + V_{cc}$$

$$Y = mx + c$$

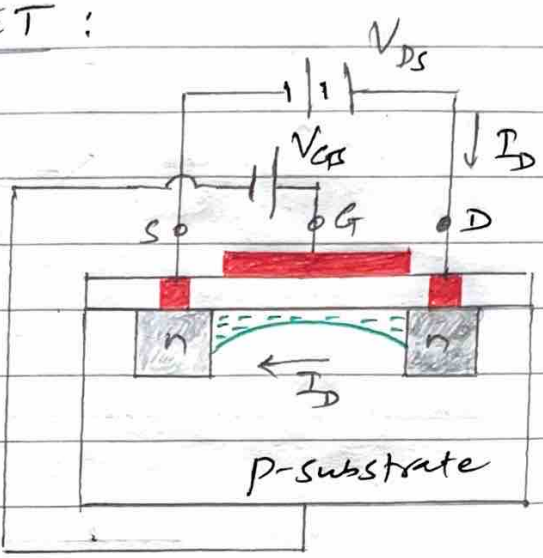
where $m = -\frac{1}{R_c}$ is the slope of the dc load line.

Q.4) a) Explain the enhancement type MOSFET along with the drain characteristics — 8 m

Soln: Enhancement type MOSFET :



(a) V_{DS} applied with gate open-circuited



(b) V_{DS} applied with V_{GS} & effect of $+V_{GS}$

— 2m

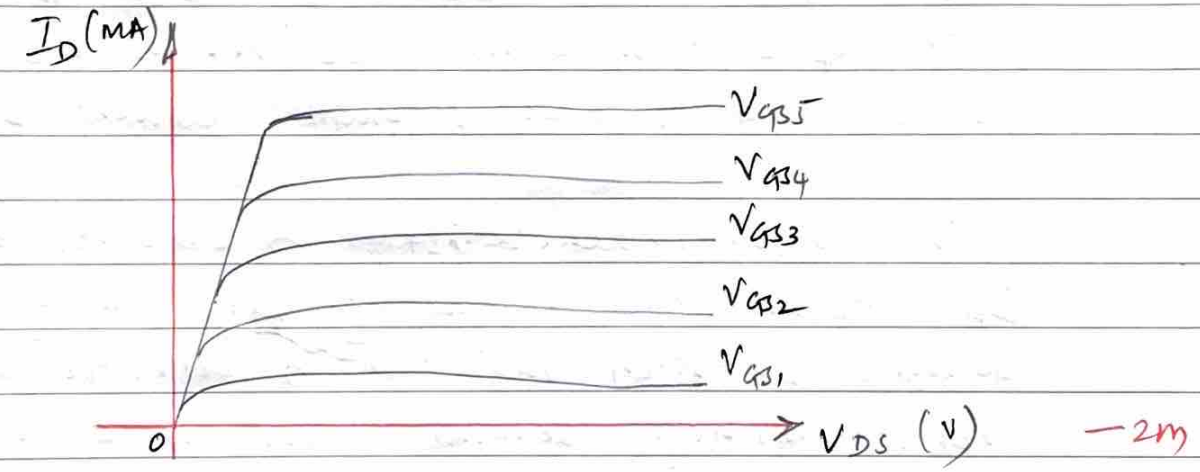
As shown in fig (a), the drain terminal of the MOSFET is +ve w.r.t. source, and the gate is open-circuited. The pn jn close to the drain terminal is reverse biased, so that only a very small (reverse-leakage) current flows from D to S.

As shown in fig (b), source terminal is connected to the substrate and that a +ve gate vg. is applied. Negative (minority) charge carriers within the substrate are attracted to the +ve plate that constitutes the gate. These charge carriers accumulate close to the surface of the substrate below the gate terminal. The minority charge carriers constitute an n-type channel between drain & source, and as the gate-source vg. is

made ~~+ve~~ more +ve, more electrons are attracted in to the channel, causing the channel resistance to decrease. A drain current flows along the channel between D & S terminals, and because the channel resistance is controlled by gate-source (V_{GS}) vg., the drain current is also controlled by V_{GS}.

The channel conductivity is said to be "enhanced" by the +ve gate-source vg., and so the device is known as an "enhancement mode" MOSFET (EMOSFET or EMOS Transistor).

Drain Characteristics of EMOSFET:



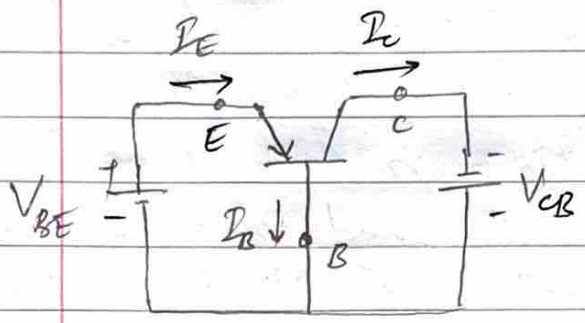
—2m

On drain characteristics, the drain current increases as the +ve gate-source bias vg. is increased. Because the gate of the MOSFET is insulated from the channel, there is no gate-source leakage current & the device has an extremely high (gate) input resistance.

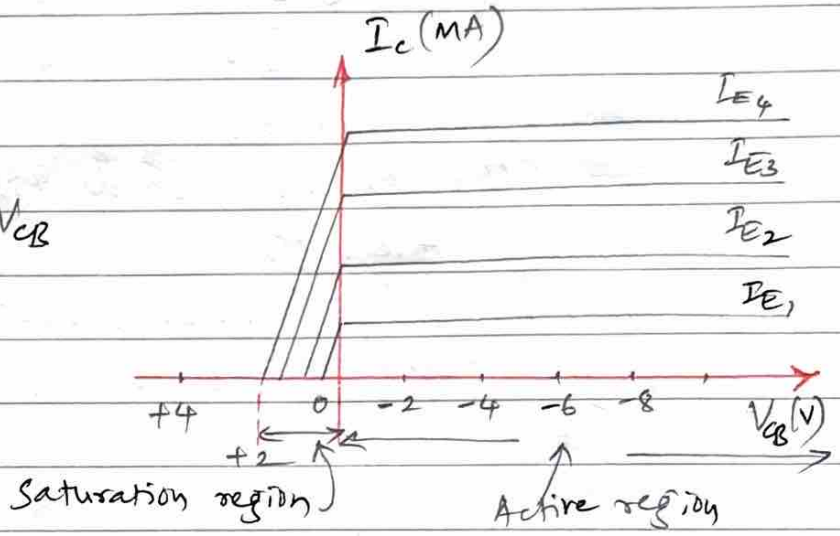
—4m

Q4.) b) Explain the common base output characteristics. — 8m

Soln: Characteristics of common-base configuration:



— 4m



The output characteristics of CB configuration is a plot of collector current I_C versus CB vg. V_{CB} for different values of emitter current I_E.

The output characteristics is obtained by keeping I_E constant and by noting variation in collector current I_C with variation in collector to base vg V_{CB}. Similarly several curves are obtained.

The region for which the CB jn is forward biased is called the saturation region while the region for which the collector-base jn is reverse biased is called the active region.

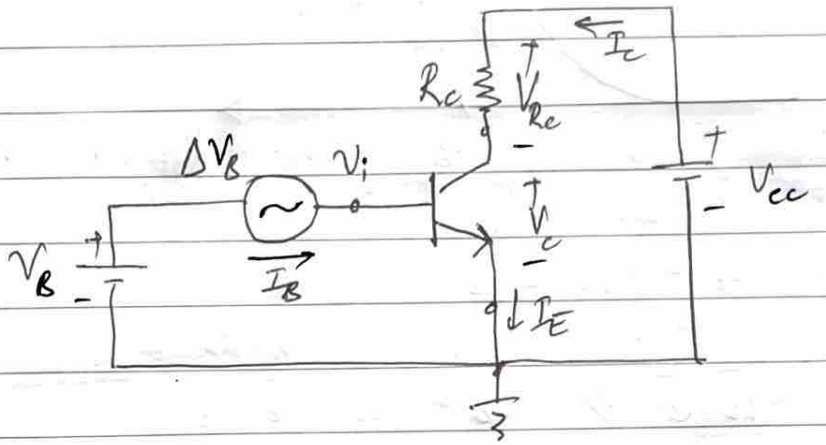
If the reverse biased vg. V_{CB} equals the limit specified for the device, breakdown occurs, the device fails and the collector current shoots up.

— 4m

Q.4) c) Describe how a transistor can be used as a voltage amplifier — 4m

Soln: Voltage amplification in a transistor :

Let us consider the ckt as shown below:



— 1m

For a given I_B, I_C can be obtained as

$$I_C = \beta_{dc} \cdot I_B$$

Applying KVL to collector - Emitter ckt -

$$V_C + V_{RC} - V_{CC} = 0$$

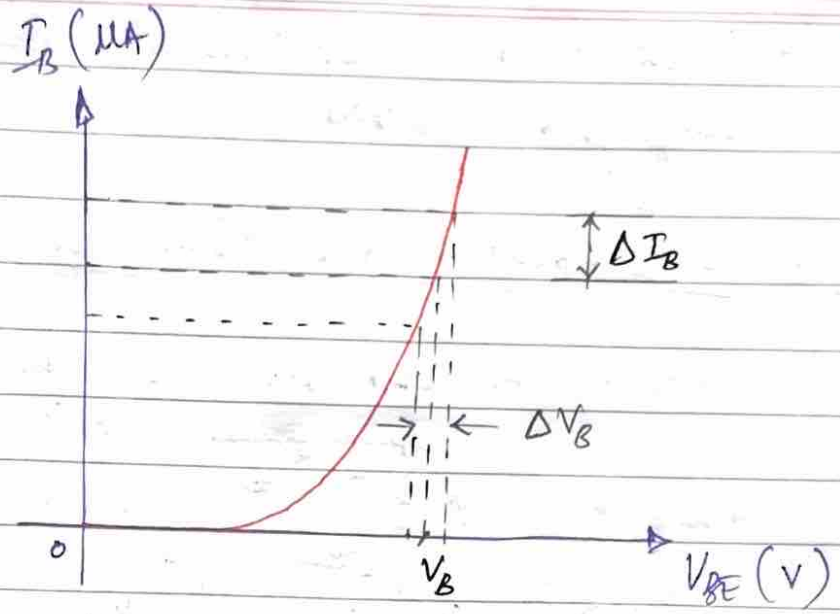
$$\therefore V_C = V_{CC} - V_{RC}$$

Where V_{RC} = Vg. across R_C

$$= I_C R_C$$

$$\therefore V_C = V_{CC} - I_C R_C \quad \text{——— (1)}$$

For a given change in input vg. ΔV_B, the change can be found in base current ΔI_B from the transistor input characteristic as shown below.



— 1m

$$\therefore \Delta I_c = \beta_{dc} \cdot \Delta I_B$$

and from eqn ① $\Rightarrow$ $V_c = V_{cc} - I_c R_c$

$$v_o = |\Delta V_c| = |\Delta I_c R_c|$$

(Since V_{cc} is a constant)

The vg. gain of the transistor is defined as

$$A_v = \frac{\Delta V_c}{\Delta V_B}$$

Where ΔV_c is the change in collector vg. and ΔV_B is the change in base vg.

The circuit has a vg. gain since the change in output vg. is more than the change in input vg.

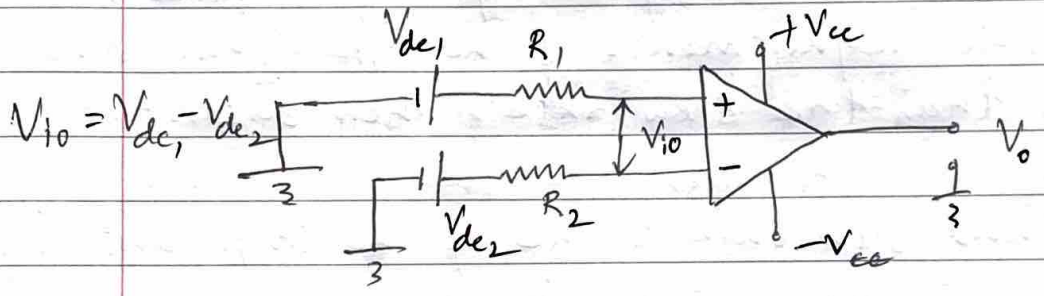
— 2m

Module-3

Q.5) a) With respect to an op-amp explain the following
i) Input offset voltage
ii) Slew rate — 8m

Soln.: i) **Input offset voltage:**

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the o/p. as shown in the figure.



— 2m

V_{dc_1} & V_{dc_2} are dc vgs and R_s represents the source resistance.

Input offset vg. is denoted by V_{io}. This vg. V_{io} could be positive or negative; therefore, its absolute value is listed on the data sheet.

The smaller the value of V_{io}, the better the input terminals are matched. — 2m

ii) **Slew rate : (SR)**

Slew rate is defined as the maximum rate of change of o/p vg. per unit of time and is expressed in volts per microseconds.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/\mu s$$

Slew rate indicates how rapidly the output of an op-amp can change in response to changes in the input frequency. The slew rate changes with change in voltage gain and is normally specified at unity (+1) gain.

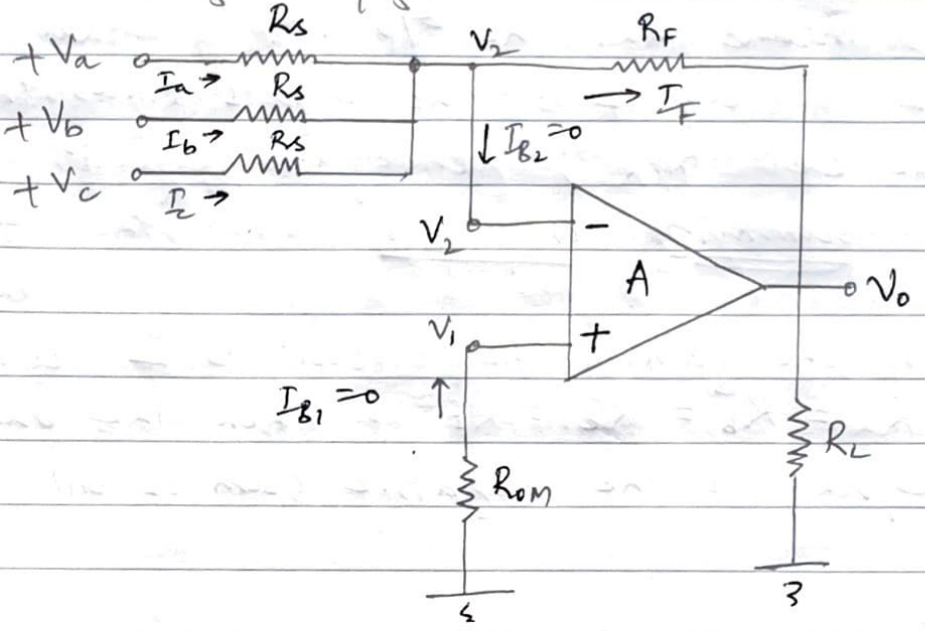
The slew rate of an op-amp is fixed; therefore if the slope requirements of the o/p signal are greater than the slew rate, then distortion occurs.

Thus slew rate is one of the important factors in selecting the op-amp for ac applications, particularly at relatively high frequencies.

— 4m

Q.5) b) Describe a summing amplifier using an op-amp in an inverting configuration with three inputs. — 8m

Soln: Summing amplifier with three inputs in non-inverting configuration :



— 2m

The op-amp in inverting configuration with three inputs V_a, V_b & V_c is as shown in above figure.

Applying KCL at node V_2 ⇒

$$I_a + I_b + I_c = I_B + I_F \quad \text{— (1)}$$

For ideal op-amp, input resistance R_i and gain 'A' are infinite and due to virtual ground

$V_1 = V_2 = 0$

$$\therefore \frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

$$\therefore V_o = -\left(\frac{R_F}{R_a} V_a + \frac{R_F}{R_b} V_b + \frac{R_F}{R_c} V_c\right) \quad \text{— (2)}$$

— 2m

If $R_a = R_b = R_c = R$ then eqn (2) becomes

$$V_o = -\frac{R_F}{R}(V_a + V_b + V_c) \quad \text{— (3)}$$

This means that the o/p vg. is equal to the negative sum of all the inputs times the gain of the ckt R_F/R; hence the circuit is called a "Summing amplifier" — 2m

When the gain of the circuit is 1, i.e., $R_a = R_b = R_c = R_F$, then the output vg. is equal to the negative sum of all input vgs i.e.

$$V_o = -(V_a + V_b + V_c) \quad \text{— 2m}$$

(Q.5)c) An inverting amplifier using op-amp has a feedback resistor of 10kΩ and one input resistor of 1kΩ. Calculate the gain of op-amp. and the o/p vg. if it supplied with an i/p of 0.5V — 4m

Sol:- Given: $R_F = 10\,k\Omega$, $R_1 = 1\,k\Omega$, $A = ?$, $V_o = ?$, $V_i = 0.5V$

Gain $A = \frac{R_F}{R_1} = \frac{10\,k\Omega}{1\,k\Omega} = 10$ — 2m

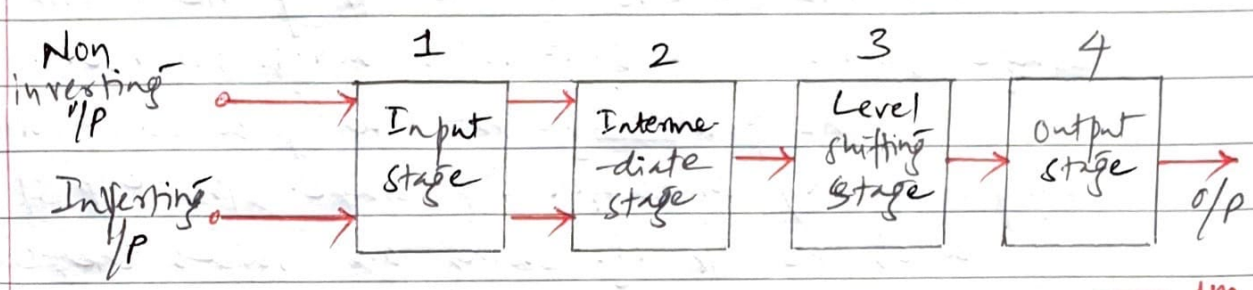
o/p vg. $V_o = A \cdot V_i$

$= 10 \times 0.5\ V$

$V_o = 5\ V$ — 2m

Q.6)a) Describe the block diagram representation of an op-amp. Also describe its operational behavior with an equivalent ckt. — 8m

Soln: Block diagram representation of an op-amp.:



— 1m

Block 1 — Input stage ⇒ Dual I/P, balanced O/P, differential amplifier

Block 2 → Intermediate stage ⇒ Dual I/P, unbalanced O/P, differential amplifier

Block 3 → Level shifting stage ⇒ Seen as emitter follower using constant current source

Block 4 → Complementary symmetry push pull amplifier → O/P stage.

The input stage is the dual I/P, balanced O/P differential amplifier. This stage generally provides most of the V$_d$. gain of the amp. and also establishes the input resistance of the op-amp.

The intermediate stage is usually another differential amp. which is driven by the O/P of the first stage. In most amplifiers the intermediate

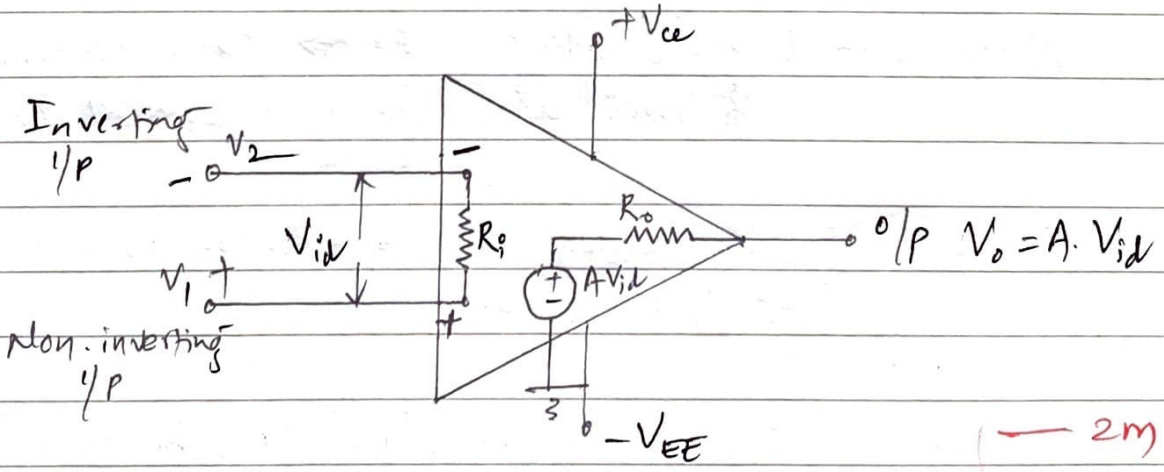
stage is dual i/p, unbalanced (single-ended) o/p.

Because direct coupling is used, the dc o/p vg. of the intermediate stage is well above ground potential. Therefore, generally, the level translator (shifting) circuit is used after intermediate stage to shift the dc level at the o/p of the intermediate stage downward to zero volts w.r.t. ground.

The final stage is usually a push-pull complementary amplifier o/p stage. The o/p stage increases the o/p vg. swing and raises the current supplying capability of the op-amp. A well designed o/p stage also provides low o/p resistance.

— 3m

Equivalent circuit of an op-amp.



— 2m

Operational behavior:

The equivalent ckt of an op-amp includes important values from the data sheets: A, R_i & R_o.

AV_{id} is an equivalent Thevenin vg. source and

R_o is the Thevenin equivalent resistance looking back in to the o/p terminal of an op-amp.

The o/p vg. is given by

$$V_o = A V_{id}$$

$$V_o = A (V_1 - V_2) \quad \text{——— (1)}$$

where A = Large signal vg. gain

V_{id} = difference i/p vg

V_1 = vg. at non-inverting i/p terminal

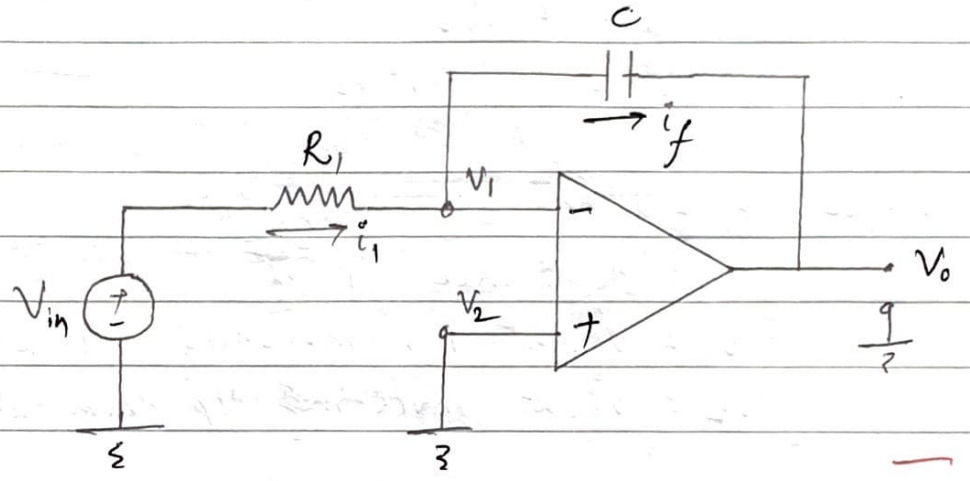
V_2 = vg. at inverting i/p terminal

The o/p vg. V_o is directly proportional to the algebraic difference between the two input voltages. ie, the op-amp amplifies the difference between the two input vgs; it does not amplify the input vgs themselves. Therefore the polarity of the o/p vg. depends on the polarity of the difference voltage.

— 2m

Q.6) b) Describe an integrating amplifier using an op-amp in an inverting configuration. — 8m

Soln.: Op-amp as an integrator.



— 2m

Circuit has a capacitor in feedback loop.
Due to virtual ground $V_1 = V_2 = 0$
Due to high input impedance, current flowing in to its inverting input terminal is zero.
Therefore same current flows thro' R_1 & C.

ie, $i_1 = i_f$ ——— (1)

but $i_1 = \frac{V_{in} - V_1}{R_1} = \frac{V_{in} - 0}{R_1} = \frac{V_{in}}{R_1}$ ——— (2)

and $i_f = C\frac{dV}{dt}$

$= C\frac{d}{dt}(V_1 - V_o) = C \cdot \frac{d}{dt}(0 - V_o)$

$i_f = -C \cdot \frac{dV_o}{dt}$ ——— (3)

Substitute eqn (2) & (3) in eqn (1)

$$-i_1 = i_f$$

$$\Rightarrow \quad \frac{V_{in}}{R_1} = -C\frac{dv_0}{dt}$$

$$\frac{dv_0}{dt} = -\frac{1}{R_1 C} V_{in}$$

integrating both sides w.r.t. t then

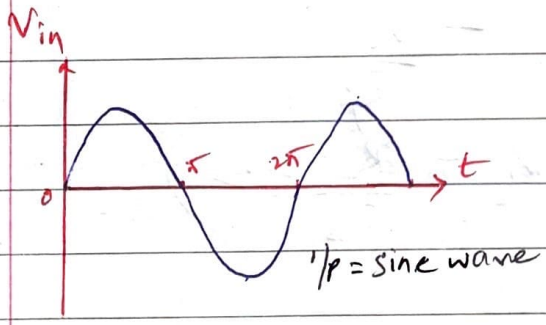
$$\int_0^t \frac{dv_0}{dt} = -\int_0^t \frac{1}{R_1 C} V_{in}$$

$$V_0 = -\frac{1}{R_1 C}\int_0^t V_{in}\,dt + V_{c(t=0)}$$

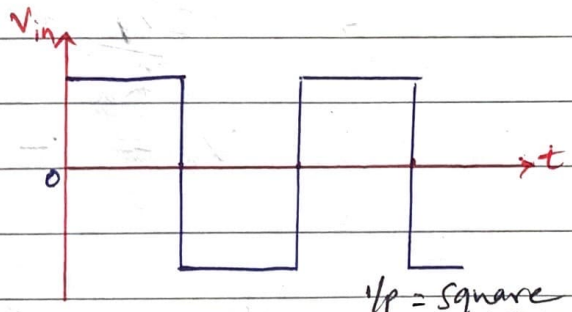
— 4m

Where $V_{c(t=0)}$ is the initial vξ. on the capacitor at $t=0$. If initial vξ. on the capacitor is zero at $t=0$ then

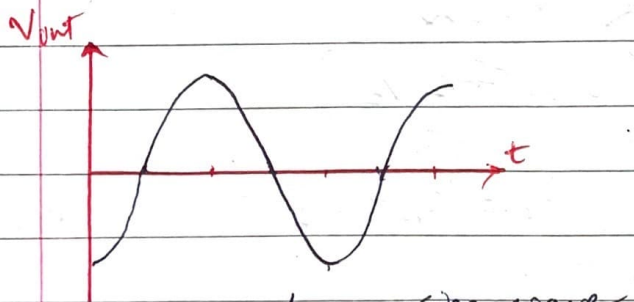
$$V_0 = -\frac{1}{R_1 C}\int_0^t V_{in}\,dt \quad \text{ie,} \quad V_0 \propto \int_0^t V_{in}\,dt$$



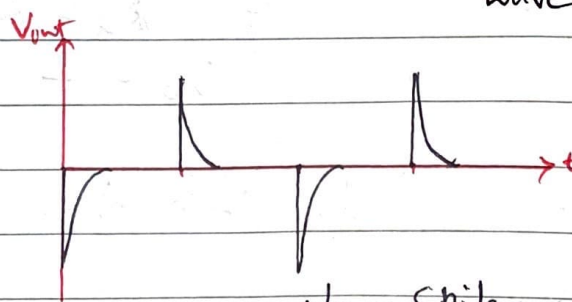
I/p = sine wave



I/p = square wave



O/p = cosine wave

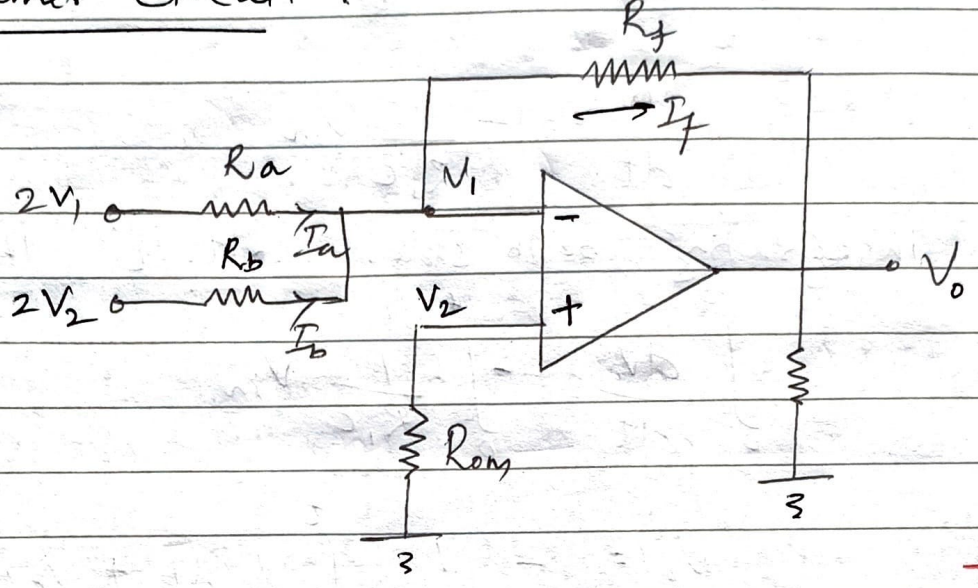


O/p = Spike

— 2m

Q.6) c) Develop a summer circuit using op-amp to get the following output voltage $V_o = -(2V_1 + 2V_2)$ — 4m

Soln **Summer circuit:**



— 2m

Due to virtual ground $V_1 = V_2 = 0$.
Due to high input impedance, current flowing thro' its inverting input terminal is zero.

Applying KCL at node V_1 ⇒

$$I_a + I_b = I_f$$

$$\Rightarrow \frac{2V_1}{R_a} + \frac{2V_2}{R_b} = -\frac{V_o}{R_f}$$

$$\therefore V_o = -\left(\frac{R_f}{R_a} 2V_1 + \frac{R_f}{R_b} 2V_2\right)$$

If $R_a = R_b = R$ then

$$V_o = -\frac{R_f}{R}(2V_1 + 2V_2)$$

If gain $A = 1$ i.e., $R_a = R_b = R_f = R$ then

$$\boxed{V_o = -(2V_1 + 2V_2)}$$

— 2m

Module-4

Q.7) a) Convert the following — 6m

(i) $(110.1101)_2 = (?)_{10}$

(ii) $(847.951)_{10} = (?)_8$

(iii) $(CAD.BF)_{16} = (?)_{10}$

Soln.: (i) $(110.1101)_2 = (?)_{10}$

$= 1\times2^2 + 1\times2^1 + 0\times2^0 + 1\times2^{-1} + 1\times2^{-2} + 0\times2^{-3} + 1\times2^{-4}$

$= 4 + 2 + 0 + \frac{1}{2} + \frac{1}{4} + 0 + \frac{1}{16}$

$= 6 + 0.5 + 0.25 + 0.0625$

$= (6.8125)_{10}$ — 2m

(ii) $(847.951)_{10} = (?)_8$

		reminder
8	847	
8	105	7 ↑
8	13	1
	1	5

$= (1517)_8$

	integer
$0.951 \times 8 = 7.608$	7
$0.608 \times 8 = 4.864$	4
$0.864 \times 8 = 6.912$	6
$0.912 \times 8 = 7.296$	7 ↓

$= (0.7467)_8$

$\therefore (847.951)_{10} = (1517.7467)_8$ — 2m

(iii) $(CAD \cdot BF)_{16} = (?)_{10}$

$= C \times 16^2 + A \times 16^1 + D \times 16^0 + B \times 16^{-1} + F \times 16^{-2}$

$= 12 \times 16^2 + 10 \times 16^1 + 13 \times 16^0 + 11 \times 16^{-1} + 15 \times 16^{-2}$

$= 3072 + 160 + 13 * \frac{11}{16} + \frac{15}{256}$

$= (3245.746094)_{10}$ — 2m

Q.7) b) Express the Boolean function $F = A + \bar{B}C$ in a sum of minterms. — 6m

Soln $F = A + \bar{B}C \Rightarrow F(A, B, C)$

The function has three variables A, B & C.
The first term A is missing two variables B and C

$\therefore A = A(B + \bar{B})(C + \bar{C})$

$= (AB + A\bar{B})(C + \bar{C})$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$ — (1) -2m

The second term $\bar{B}C$ is missing one Variable A

$\therefore \bar{B}C = \bar{B}C(A + \bar{A})$

$= A\bar{B}C + \bar{A}\bar{B}C$ — (2) -2m

Combining functions (1) & (2)

$F = A + \bar{B}C$

$F = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$

Deleting duplicate terms

$F = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$ - 2m

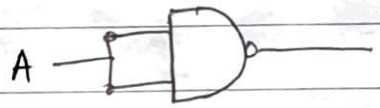
$F = m_1 + m_4 + m_5 + m_6 + m_7 = \Sigma(1,4,5,6,7)$

Q.7) c) Describe how NAND and NOR gates can be used as universal gates. — 8M

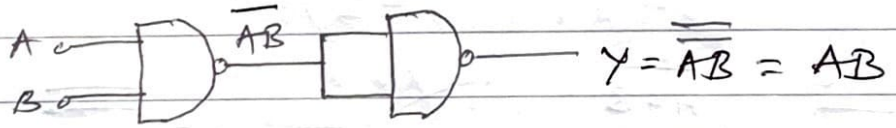
Soln: Both NAND gate and NOR gate are called a "universal gate" because all the logic gates NOT, AND and OR can be constructed using only NAND gate or NOR gate.

(i) construction of NOT, AND & OR gates using NAND only : — 4M

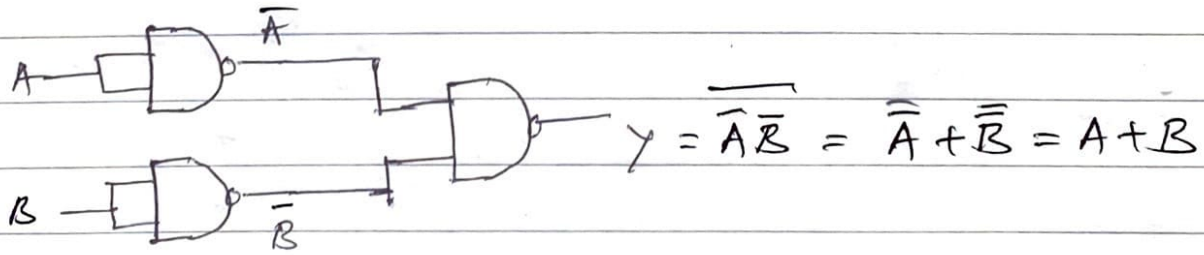
NOT gate using NAND gate -



AND gate using NAND gate -

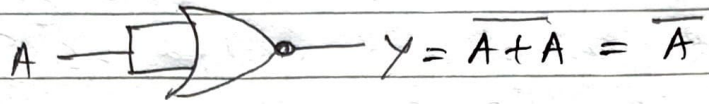


OR gate using NAND gate -

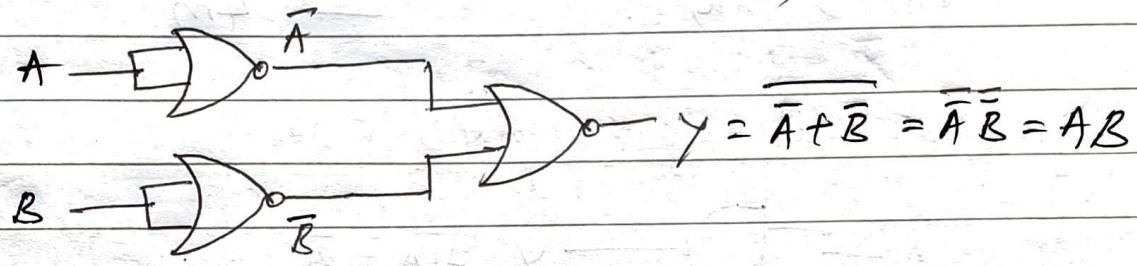


(ii) Construction of NOT, AND & OR gates using NOR gate only : — 4m

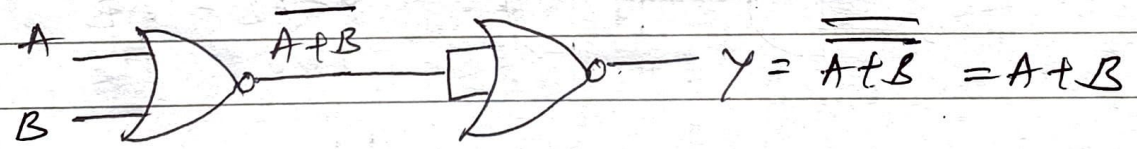
NOT gate using NOR gate only -

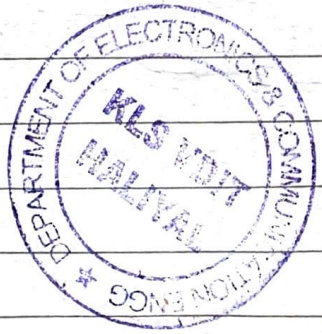


AND gate using NOR gate only



~~X~~OR gate using NOR only





Q.8) a) Simplify the following — 6m

(i) $Y = AB + \bar{A}C + BC$

(ii) $Y = (A + \bar{B} + \bar{B})(A + \bar{B} + C)$

(iii) $Y = C(B + C)(A + B + C)$

Soln (i) $Y = AB + \bar{A}C + BC$

$= AB + \bar{A}C + BC(A + \bar{A})$

$(A + \bar{A} = 1$, complementary law$)$

$= AB + \bar{A}C + ABC + \bar{A}BC$

$= AB + ABC + \bar{A}C + \bar{A}BC$

$= AB(1 + C) + \bar{A}C(1 + B)$

$Y = AB + \bar{A}C$ — 2m

(ii) $Y = (A + \bar{B} + \bar{B})(A + \bar{B} + C)$

$= (A + \bar{B})(A + \bar{B} + C)$

$= A + A\bar{B} + AC + A\bar{B} + \bar{B} + \bar{B}C$

$= A + A\bar{B} + AC + \bar{B} + \bar{B}C$

$= A(1 + \bar{B}) + AC + \bar{B}(1 + C)$

$Y = A + AC + \bar{B} = A(1 + C) + \bar{B} = A + \bar{B}$

— 2m

(iii) $Y = C(B + C)(A + B + C)$

$= ABC + BC + BC + AC + BC + C$

$= ABC + BC + AC + C$

$= BC(A + 1) + C(A + 1)$

$= BC + C$

$= C(1 + B)$

$Y = C$ — 2m

Q.8) b) Express the Boolean fn $F = xy + \bar{x}z$ in a product of maxterms. — 6m

Soln:

$$F = xy + \bar{x}z$$
$$= xy(z + \bar{z}) + \bar{x}z(y + \bar{y})$$
$$= xyz + xy\bar{z} + \bar{x}yz + \bar{x}\bar{y}z$$

By distributive law $x + yz = (x + y)(x + z)$

∴ Express the Boolean fn $F = xy + \bar{x}z$ in a product of maxterm form.

First convert the fn in to OR terms using the distributive law.

ie,

$$F = xy + \bar{x}z$$
$$= (xy + \bar{x})(xy + z)$$
$$= (x + \bar{x})(y + \bar{x})(x + z)(y + z)$$
$$F = (\bar{x} + y)(x + z)(y + z)$$ — 1m

Now fn F has three variables : x, y & z

Each OR term is missing one variable in,

$$\therefore (\bar{x} + y) = \bar{x} + y + z\bar{z} = (\bar{x} + y + z)(\bar{x} + y + \bar{z})$$
$$x + z = x + z + y\bar{y} = (x + y + z)(x + \bar{y} + z)$$
$$y + z = y + z + x\bar{x} = (x + y + z)(\bar{x} + y + z)$$

Combining all the terms — 3m

$F = (\bar{x}+y+z)(\bar{x}+y+\bar{z})(x+y+z)(x+\bar{y}+z)$
$(x+y+z)(\bar{x}+y+z)$

Removing duplicate terms & re-arranging ⇒

$F = (x+y+z)(x+\bar{y}+z)(\bar{x}+y+z)(\bar{x}+y+\bar{z})$

$F = M_0 M_2 M_4 M_5$

$F = \pi(0, 2, 4, 5)$ — 2m

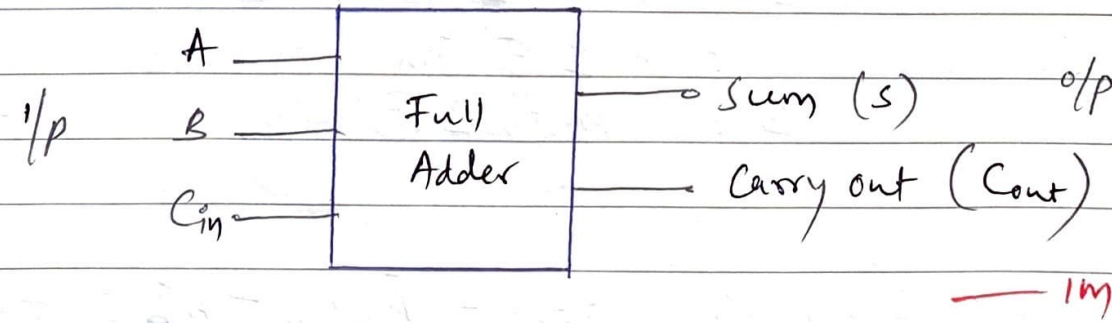
Q.8.) c) Describe the working of full adder using basic gates — 8m

Soln: Full adder (FA) using basic gates:

Half adder is used to add only two numbers. To add three bits full adder is developed.

Full adder is used to add three 1-bit binary numbers. It has three input states and two output states.

BD of FA:



— 1m

A, B: I/p bits ; Cin: carry from previous stage
S, Cout: O/p bits

Truth Table of a Full adder

	I/P			O/P	
	A	B	C_{in}	S	Cout
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

— 2m

Boolean expression for o/p sum & carry are:

$$Sum = S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$
$$= \bar{A}\bar{B}C_{in} + ABC_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in}$$
$$S = C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

if $Z = \bar{A}B + A\bar{B} = A \oplus B$ then
$\bar{Z} = AB + \bar{A}\bar{B} = A \odot B$

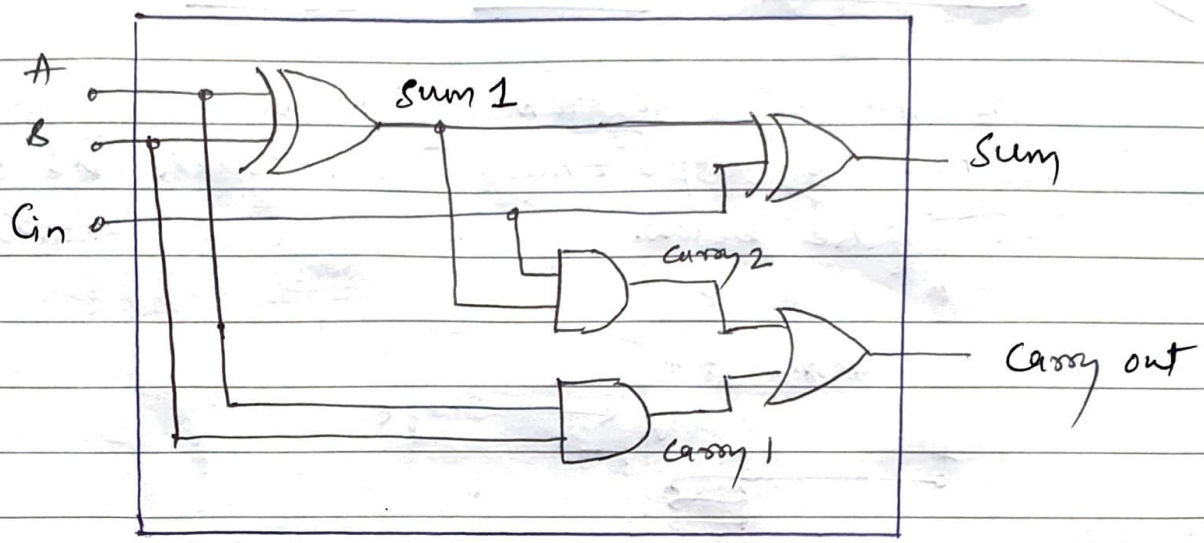
$$\therefore \quad S = C_{in}\cdot\bar{Z} + \bar{C}_{in}Z$$
$$= Z \oplus C_{in}$$
$$S = A \oplus B \oplus C_{in}$$

— 2m

$$\text{Carry out} = C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$$
$$= C_{in}(\bar{A}B + A\bar{B}) + AB(C_{in} + \bar{C}_{in})$$
$$= C_{in}(A \oplus B) + AB$$

$\therefore$ $C_{out} = AB + BC_{in} + AC_{in}$ — 1m

Implementation of FA using basic gates :



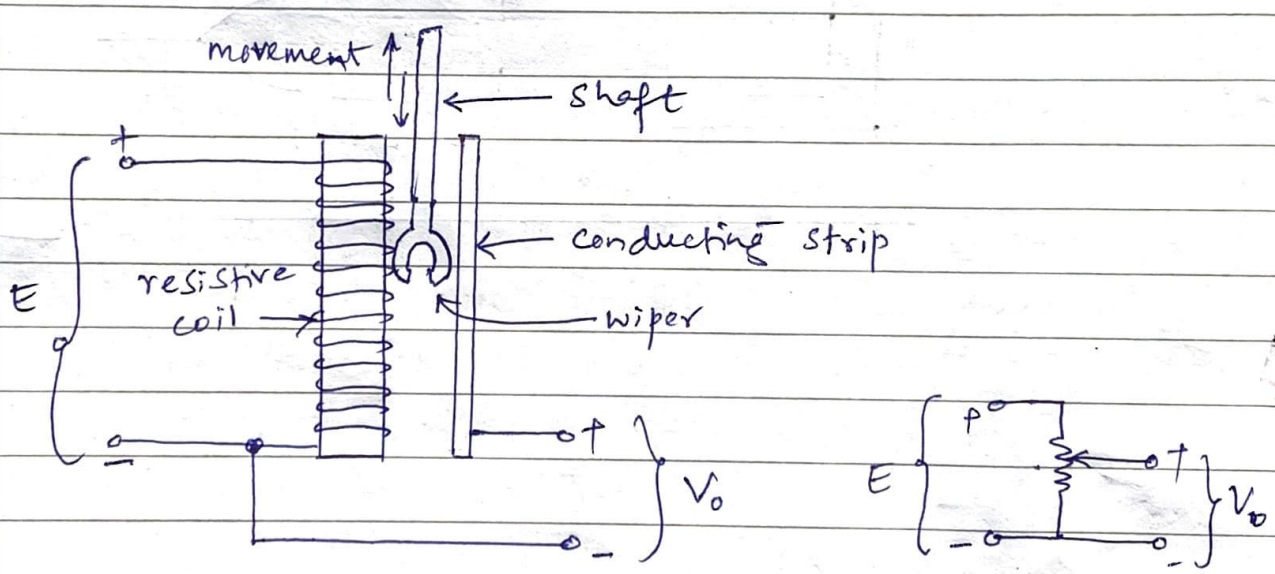
— 2m

Module-5

Q.9) a) Explain the working of potentiometric resistive transducer — 8m

Soln.: **Potentiometric resistive transducer:**

A straight potentiometer may be used as a position, or displacement, transducer as shown in the figure below.



(a) Transducer conduction (b) Circuit diagram

— 4m

A shaft is connected to the potentiometer moving contact, or wiper. The potentiometer has a supply vg. (E), and so the position of wiper determines the o/p vg (V_o). The shaft displacement can be measured electrically, and the measurement can be displayed or perhaps transmitted for further processing.

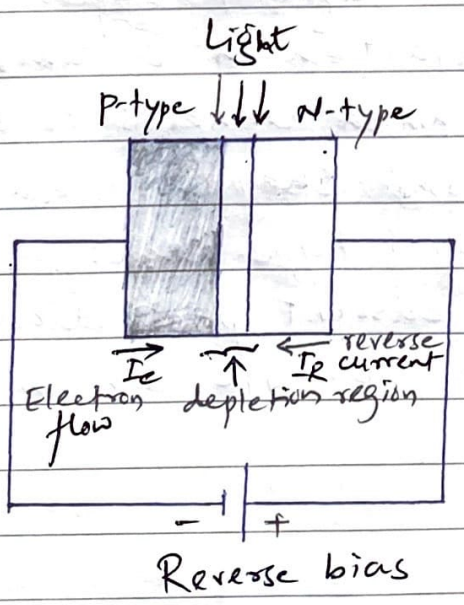
The advantage of this type of transducer potentiometer is that it can be as large or as small as required also the potentiometer can be perfectly linear, thus giving a linear sensitivity.

— 4m

Q.9) b) Write a note on photodiode. — 6m

Solu: Photodiode:

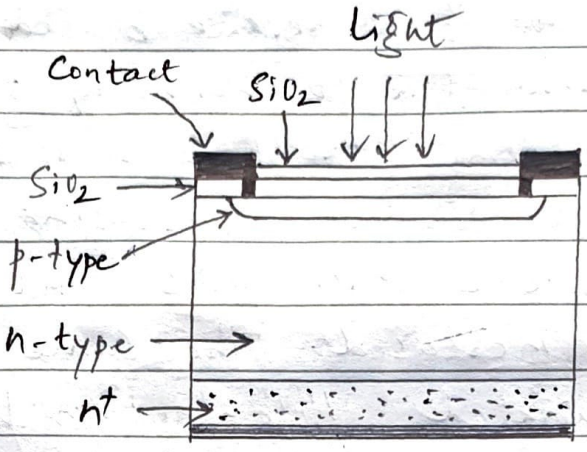
When a pn jn is reverse biased, there is a small reverse current due to thermally generated holes & electrons being attracted across the jn as minority charge carriers. Increasing the jn temp generates more hole-electron pairs, and so the reverse current is increased. The same effect occurs if the jn is illuminated. Hole-electron pairs are generated by the incident light energy, and minority charge carriers are swept across the jn, thus creating a reverse current flow. Increasing the jn illumination increases the reverse current level. Diodes designed to illumination are known as photodiodes.



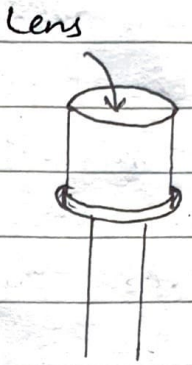
— 2m

Fig: A photodiode has a reverse-biased pn-jn designed to be light sensitive.

The cross section of the diffused diode is as shown below.



Cross section



TO Can-type package

2m

From the cross section of photo diode it is seen that a thin, hearily doped p-type layer is situated at the top, where it is exposed to incident light. The junction depletion region penetrates deeply in to the lightly doped n-type layer. This is in contact with a lower, heavily doped n-type layer, which connects to a metal film contact. A ring shaped contact is provided at the top of the p-type layer.

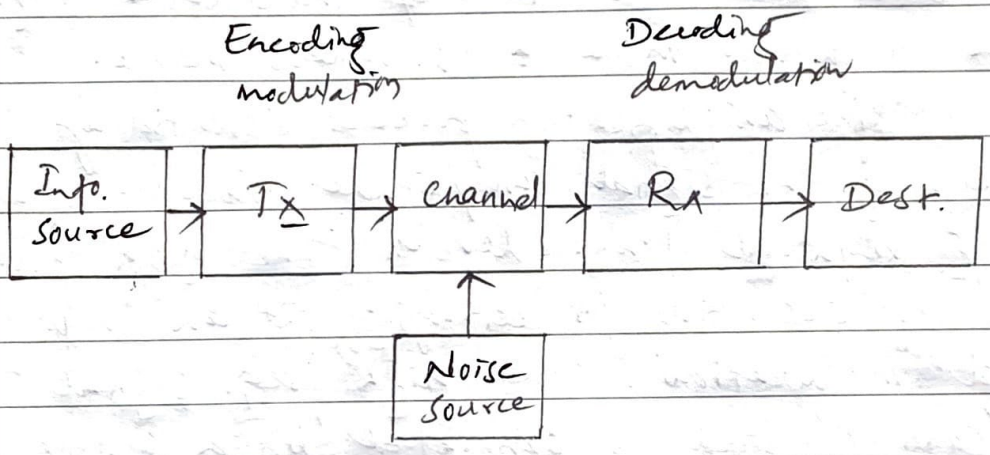
Low current photo diodes are usually contained in a TO-type can with a lens at the top.

4m

Q.9) c) Explain the various blocks involved in communication system. — 6m

Soln: **Communication System:**

A communication system will have five blocks, including the information source and destination blocks.



— 1m

Information source:

The objective of any communication s/m is to convey information from one point to the other. The information comes from the information source, which originates it. Information may include some thoughts, news, feeling, visual scene, etc. The information source converts this information in to a physical quantity. Such as speech signal, written script or picture. This physical manifestation of the information is termed as "message" signal.

— 1m

Transmitter:

The objective of transmitter blocks is to collect the incoming message signal & modify

it in a suitable fashion, such that it can be transmitted via the chosen channel to the receiving point. The functionality of the transmitter blocle is mainly decided by the type or nature of the channel chosen for communication. The transmitter blocle involves several operations like amplification, generation of high-frequency carrier signal modulation and then radiation of modulated signal either in wired mode or wireless mode.

The amplification process essentially involves amplifying the signal amplitude values & also adding required power levels. The high frequency signal is essential for carrying out an imp. operation called "modulation". The high freq. signal is termed as "carrier" and is generated by a stable oscillator. Modulation can be of amplitude modulation, frequency modulation, and phase modulation. The modulated signal can be transmitted or radiated in to the atmosphere using an antenna as the transducer, which converts the signal energy in guided waveform to free space EM waves and vice versa. ← Im

Channel :

Channel is the physical medium which connects the transmitter with that of receiver. The choice of a particular channel depends on the feasibility & also the purpose of communication s/m. The nature of modification of message signal in the transmitter blocle is based on the choice of the

communication channel. This is because the message signal should smoothly travel thro' the channel with least opposition so that maximum information can be delivered to the receiver. — 1m

Receiver :

The receiver block receives the incoming modified version of the message signal from the channel and processes it to recreate the original form of the message signal. There are variety of receivers in communication s/m's, depending on the processing required to recreate the original message signal and also final presentation of the message to the destination. Most of the receivers are of "super heterodyne" type, which performs reception, amplification, mixing, demodulation & recreation of message signal. — 1m

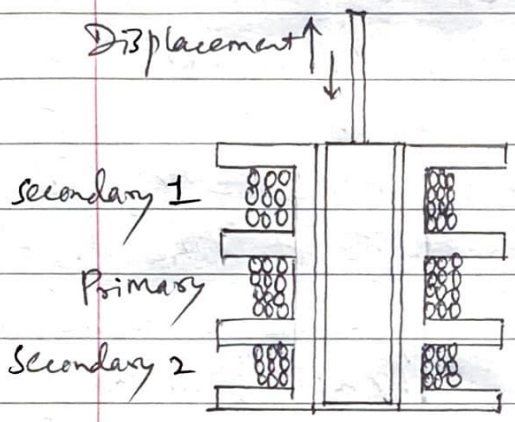
Destination :

The destination is the final block in the communication s/m which receives the message signal and processes it to comprehend the information present in it. Usually, humans will be the destination block. The incoming different types of message signals are processed by the respective perception s/m to comprehend the information. — 1m

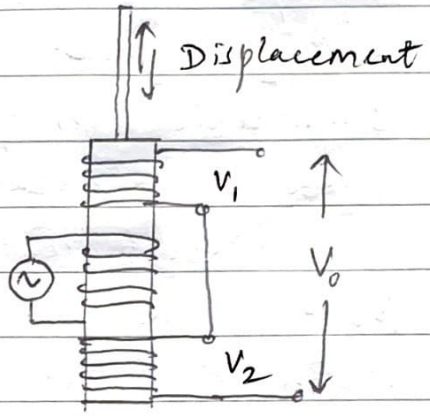
Q. 10) a) Explain the working of Linear Variable Differential Transducer (LVDT) — 8m

Soln: **Linear Differential Transducer (LVDT):**

LVDT is essentially a transformer with one primary winding, two secondary windings, and an adjustable core.

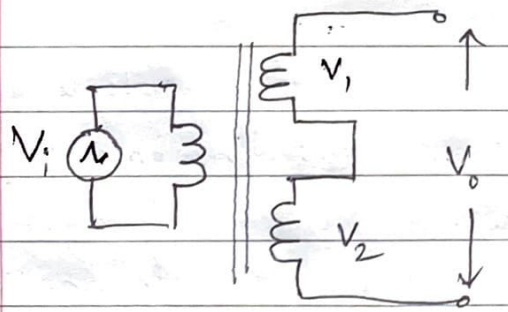


(a) Cross section

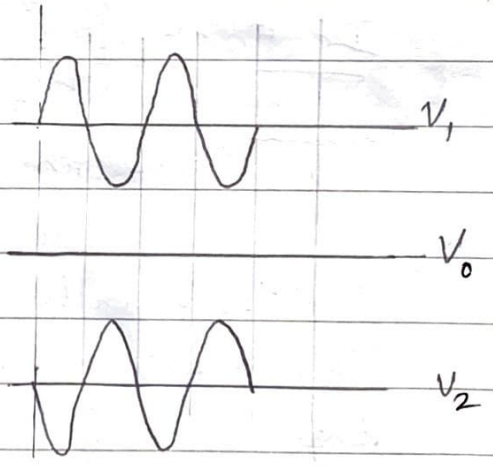


(b) Coil connections

— 2m



(c) Circuit diagram



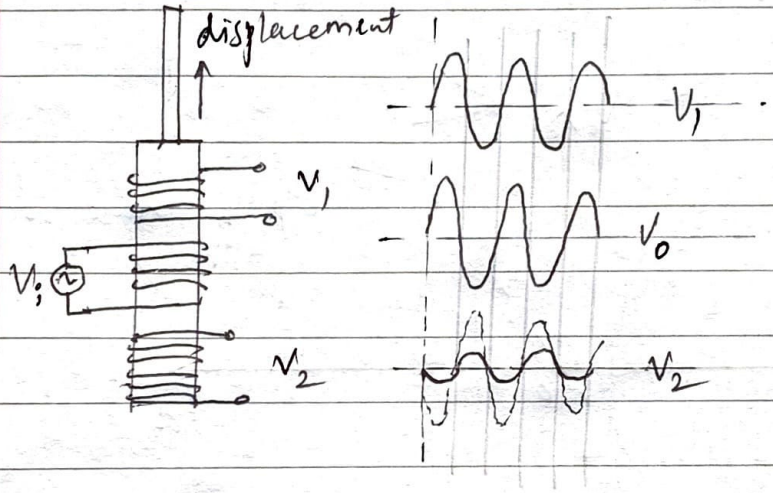
(d) Waveforms.

— 1m

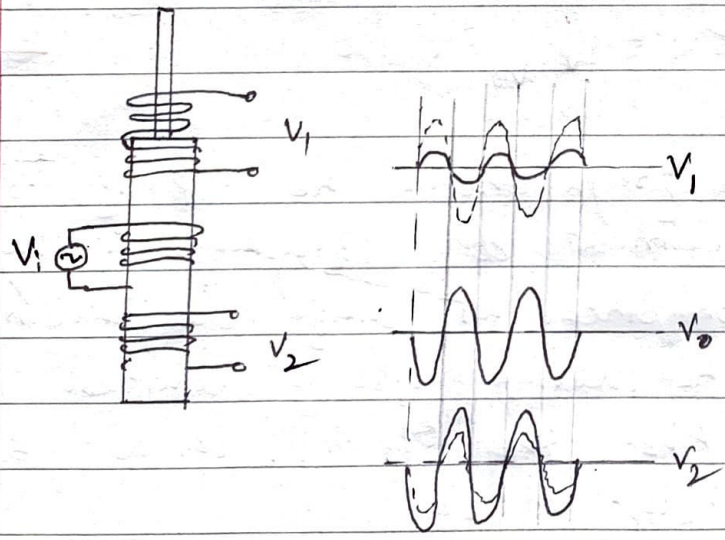
Secondary o/p vgs V_1 & V_2 are equal in magnitude when the moveable core is situated with equal section of core opposite to each secondary winding.

o/p vg. V_1 is in phase with the primary

input V_i, and that o/p V_2 is in antiphase to V_i. The secondary windings are connected in series so that the voltages cancel to produce zero output from transducer when they are equal and in antiphase.



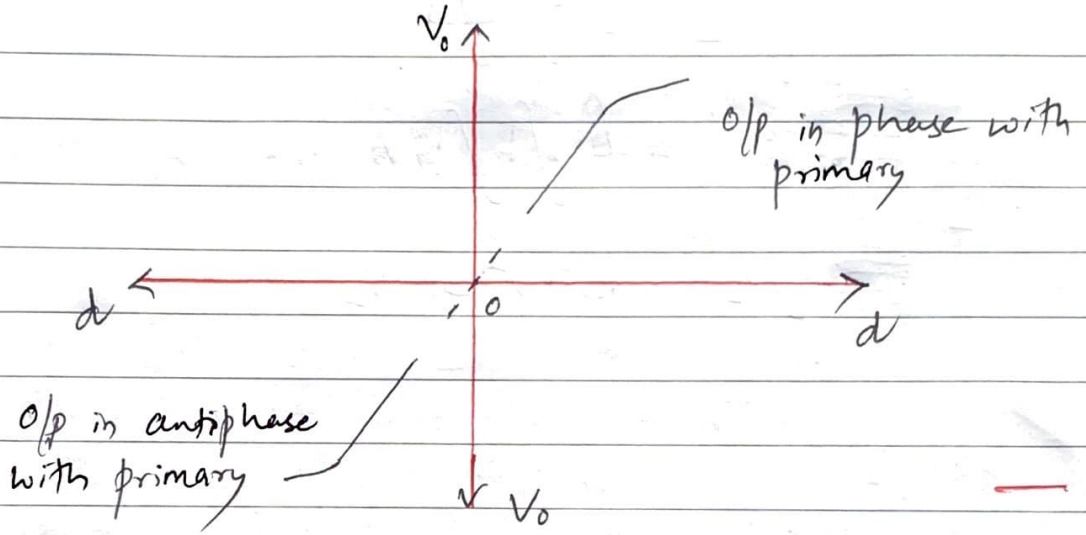
(a) core displaced up



(b) Core displaced down

When the LVDT core is displaced upward, there is an increase in the flux from the primary linking to secondary N_1 and a decrease in that linking to N_2. This causes an increase in the amplitude of V_1 and a decrease in V_2, thus producing a different o/p V_o.

Similarly, when the core is displaced in a downward direction, V_2 increases & V_1 decreases. In this case, V_0, increases but with a 180° phase shift from the input. So, the o/p vg. amplitude and phase give a measure of the core displacement and direction of motion.



— 1m

The above graph shows the o/p vg. V_0 versus the core displacement 'd'. Graph is mostly linear but becomes non-linear at large displacements. Consequently, the device use is limited to the linear range. Also, the o/p vg. can not be reduced completely to zero.

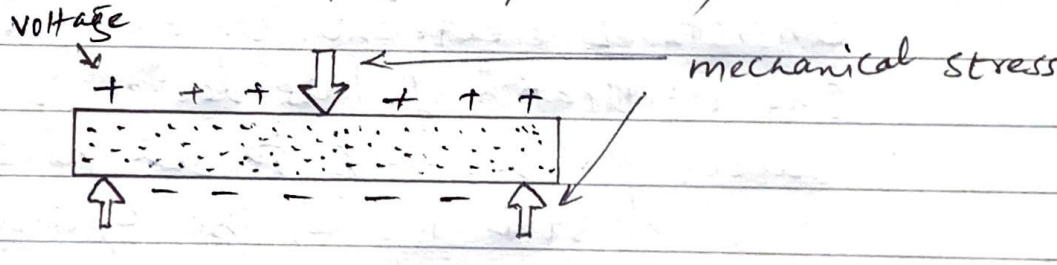
— 2m

Q.10) b) Write a note on piezoelectric transducer. - 6M

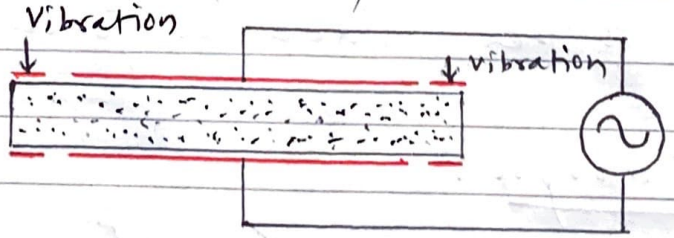
Soln: **Piezoelectric transducer:**

Piezolectric transducers are a type of electro-acoustic transducer that convert the electrical charges produced by some forms of solid materials into energy.

If a mechanical stress is applied to a wafer of quartz crystal, a voltage proportional to the stress appears at the surfaces of the crystal as shown



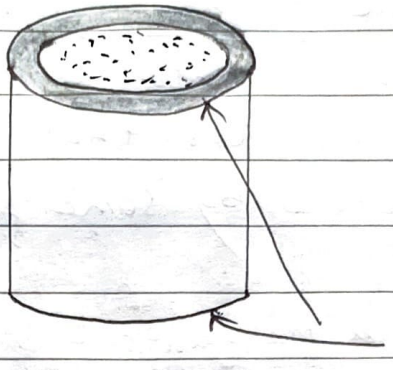
When the stress is removed, the vg disappears. The crystal also vibrates or resonates, when an alternating vg. with the natural resonance freq. of the crystal is applied to its surfaces as shown below.



—2m

These properties are the result of the crystal structure of the quartz, and all materials that behave in this way are termed piezoelectric. Because the crystal resonance frequency is extremely stable piezoelectric crystals are widely used to stabilize the freq. of oscillators. They are also used in pressure transducers.

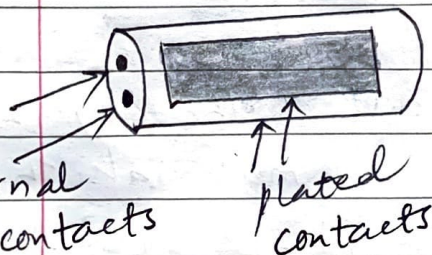
Cylindrical transducer:



— 1m

Cylindrical-shaped synthetic piezoelectric device consists of electrical contact plates at on each end. One application of this device is a pressure transducer for listening to sea noises. With a preamplifier inserted inside, the cylinder ends are sealed and the device is suspended at the end of a long cable from a boat or a buoy. The pressure variations, due to ship engine noise, for example, generate electrical signals at the transducer terminals. These are amplified and fed to the surface for processing. — 2m

Bimorph:



— 1m

A ceramic device known as bimorph when supported at one end, electrical signals are generated at the internal and external electrodes by vibrations applied to the other end. This type of device is basic to a record player cartridge. The minute vibrations generated as the stylus moves in a record track are converted into electrical signals which are then amplified & applied to speakers. — 2m

Q.10) What is modulation? Describe the need of modulation in communication systems - 6M

Soln.: In communication system, the transmitter modifies the message signal in to a suitable form for transmission over the channel, by using process known as "modulation" — 1M

Modulation is defined as the process by which some characteristic or property of a high frequency "sine wave" called the "carrier wave" is varied in accordance with the strength of a message signal is called as "modulation" — 2M

Need for modulation: — 3M

The distance that can be traveled by a signal in an open atmosphere is directly (inversly) proportional to its frequency (wavelength) Most of the message signals like speech and music are in the audio frequency range (20 Hz - 20 KHz) and hence they can hardly travel for few meters on their own. Further, for efficient radiation & reception, the transmitting and receiving antennas would have to have lengths comparable to a quarter-wavelength of the frequency used. For a message at 1 MHz, its wavelength is 300 m & hence antenna length should be about 75 mts. Alternatively, for a signal at 15 KHz, the antenna length will be about 5000 mts, which is practically impossible. Hence, it is required to modulate the message signal over the high freq. carrier signal so that we can have a practical value for the height of the antenna.