KLS VDIT, HALIYAL

Transforming through Technology

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG.

Hands-on Workshop on

IC Design using Cadence

5th & 6th April 2023

9 AM onwards

Resource Person

Mr. Priyanshu Datta &

Mr. P. Rajendra

INSTITUTION'S INNOVATION COUNCIL
(Ministry of Education Initiative)

PRESIDENT,
INSTITUTION'S INNOVATION COUNCIL,
KLS VDIT, HALIYAL -581329
IIC CODE: IC20221479

ENTUPLE TECHNOLOGIES

Ministry of Education's INNOVATION CELL
(GOVERNMENT OF INDIA)

Workshop Coordinator
Prof. Deepak Sharma

Principal
KLS Vishwanathrao Deshpande
Institute of Technology, Haliyal

Dr. Mahendra M. Dixit
Prof. & Head (E&CE)

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Dr. V. A. Kulkarni,
Principal

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Date: 06.04.2023

Report on workshop – IC DESIGN USING CADENCE

Date of Workshop	:	**5th & 6th April 2023**
Workshop Title	:	**Hands on workshop on "IC Design using Cadence"**
Resource Persons	:	**Mr. Priyanshu Datta** and **Mr. P. Rajendra, Entuple Technologies, Bengaluru**
Occasion of Event	:	**Workshop on Prototype / Process Design and Development**
Venue	:	**VLSI Lab, Dept. of E&CE, KLS VDIT, Haliyal**
Coordinator	:	**Prof. Deepak Sharma**

The following is the brief report on "**Hands on workshop on – IC Design using Cadence**" related to the Activity of **Workshop on Prototype / Process Design and Development** as per IIC guidelines.

Day – 1: 5th April 2023

- The Department of Electronics & Communication Engg., KLS VDIT, Haliyal successfully conducted "**Hands on workshop on – IC Design using Cadence**". **Mr. Priyanshu Datta** and **Mr. P. Rajendra, Entuple Technologies**, **Bengaluru** were the Resource Persons for the workshop.
- **Prof. Deepak Sharma**, Coordinator formally welcomed gathering and briefed about the relevance of the workshop and introduced the Resource Persons.
- Resource persons began the workshop with **VLSI design flow**. They demonstrated the schematic design of Inverter on **Generic Process Design Kit** (gpdk) **180nm Technology** using **Virtuoso Tool** in **Cadence Software**. Symbol of the Inverter was created and functionality of the same was verified using **Spectre Tool**.
- **Physical verification** was done in afternoon session. Layout of Inverter was designed and the design was physically verified by Design Rule Check, Electrical Rule Check & Layout Versus Schematic.
- **Parasitic (RC) extraction** was carried out which was followed by back annotation of the design. Finally, GDS II file was created at the end of session 2 for Day -1 of the workshop.

Day – 2: 6th April 2023

- Second day workshop started with the **Design & Digital verification** of 4 – bit Up – Down Counter was demonstrated by the Resource persons.
- The **Verilog Code** for the design was **simulated** and **synthesis** has been carried out.
- The steps in back end design during **layout design** included floor planning, pre-placement, pin & block placement, routing.
- The complete steps in **IC design** using **Cadence** has been demonstrated by the resource persons.
- More than 60 Students and 10 Faculty Members have attended the workshop from E&CE and E&EE Departments.

Dr. Mahendra M. Dixit,
President IIC,
Prof. & Head (E&CE),
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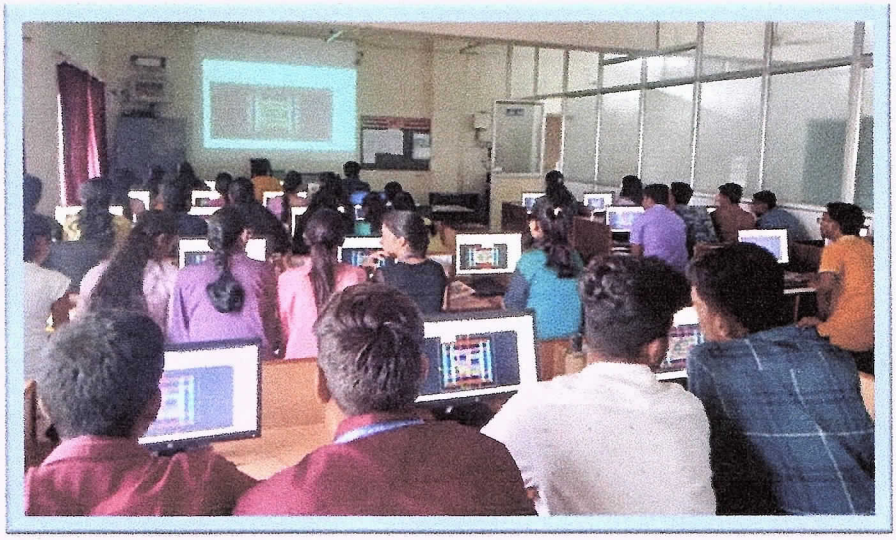
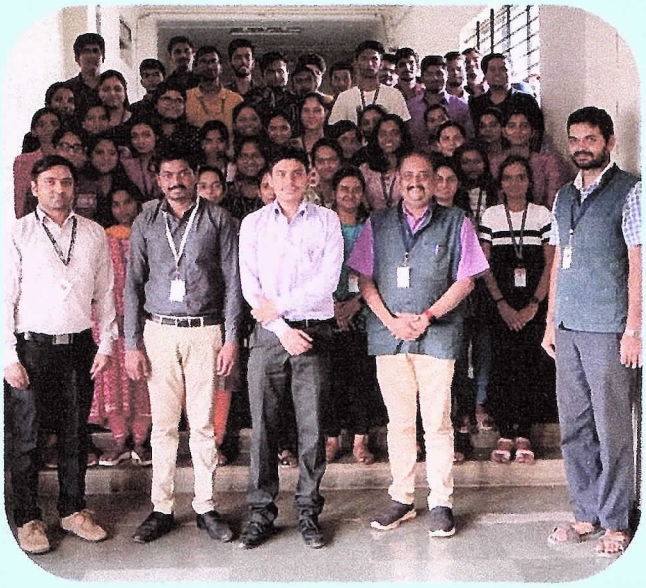
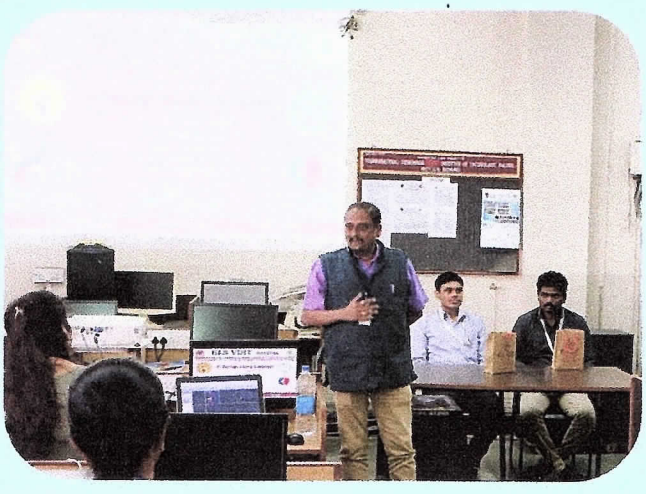
GLIMPSES OF EVENT







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