

KLS Vishwanathrao Deshpande Institute of Technology

(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada

Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in



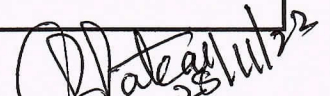
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper Scheme & Solution

Faculty Name	:	Prof. Nikhili A. Kulkarni
Course Name	:	Basic Electronics
Course Code	:	BBEE103
Year of Question Paper	:	JUNE/JULY 2023
Date of Submission	:	28.11.2023


Faculty Member


HoD


Dean (Acad.)

Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T., HALIYAL (U.K.)

Dean, Academics
KLS VDIT, HALIYAL

CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

BBEE103/203

First/Second Semester B.E./B.Tech. Degree Examination, June/July 2023
Basic Electronics for EEE Stream

Time: 3 hrs.

Max. Marks: 100

- Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
 2. M : Marks, L: Bloom's level, C: Course outcomes.
 3. Assume missed data.*

Module - 1			M	L	C
Q.1	a.	Explain forward and reverse characteristics of semiconductor diode.	8	L2	CO1
	b.	Calculate forward and reverse resistances offered by a silicon diode with $I_f = 100\text{mA}$ at $V_R = 50\text{V}$. Assume V_F for silicon diode to be 0.75V and reverse current $I_R \approx 100\text{nA}$.	4	L3	CO1
	c.	What is piecewise linear characteristic? With neat diagram explain diode approximation of Ideal diode and practical diode.	8	L2	CO1
OR					
Q.2	a.	Describe the working of full wave bridge rectifier.	8	L2	CO1
	b.	Explain zener diode as voltage regulator with no load and with load.	6	L2	CO1
	c.	Illustrate RC- π filter.	6	L2	CO1
Module - 2					
Q.3	a.	Explain output characteristics of a transistor in common base configuration.	6	L2	CO2
	b.	Describe the procedure for drawing dc - load line on transistor CE output characteristics.	8	L2	CO2
	c.	Calculate I_c and I_B for a transistor that has $\alpha_{DC} = 0.98$, $I_B = 100\mu\text{A}$. Also determine the value of β_{DC} for the transistor.	6	L3	CO2
OR					
Q.4	a.	Explain common Emitter input characteristics.	6	L2	CO2
	b.	Explain how transistor can be used as current amplifier.	6	L2	CO2
	c.	Explain the working of N-channel JFET.	8	L2	CO2

Module – 3					
Q.5	a.	Explain Inverting and Non-inverting amplifier.	8	L2	CO2
	b.	Define Op-Amp. Mention any 5 ideal characteristics of an op-amp.	6	L2	CO2
	c.	Draw a summer circuit with $V_1 = +1V$, $V_2 = +3V$, $V_3 = +2V$, $R_1 = R_2 = R_3 = 2K\Omega$. Determine the output voltage when $R_F = 3K\Omega$.	6	L3	CO2
OR					
Q.6	a.	Explain the working of op-amp as Differentiator.	8	L2	CO2
	b.	Define : i) Input offset current ii) Input bias current iii) slew rate iv) CMRR	6	L2	CO2
	c.	With block diagram, explain basic structure of an Op amp. Also write its equivalent circuit diagram.	6	L2	CO2
Module – 4					
Q.7	a.	Convert the following : i) $(2AB.8)_{16} = ()_{10}$ ii) $(416.12)_{10} = ()_8$ iii) $(25.375)_{10} = ()_2$ iv) $(16.2)_8 = ()_{16}$	6	L2	CO3
	b.	Find complement of the function i) $F_1 = x'yz' + x'y'z$ ii) $F_2 = x(y'z' + yz)$ Using De-Morgan's theorem.	8	L2	CO3
	c.	Explain the working of Half adder.	6	L2	CO3
OR					
Q.8	a.	Express the Boolean function $F = A + B'C$ in sum of minterms.	6	L3	CO3
	b.	Mention the postulates and theorems of Boolean algebra.	8	L2	CO3
	c.	Explain the working of full adder.	6	L2	CO3
Module – 5					
Q.9	a.	Describe the working of LVDT.	6	L2	CO4
	b.	Explain the working principle of capacitive pressure transducer.	6	L2	CO4
	c.	With neat block diagram, explain the working of communication system.	8	L2	CO4
OR					
Q.10	a.	Describe a Thermistor and sketch approximate resistance/temperature characteristics for a thermistor.	6	L2	CO1
	b.	Write a short notes of photo diodes	6	L2	CO5
	c.	What is modulation? Describe the need of modulation in communication system.	8	L2	CO5

Q1A) Explain V-I characteristics of a PN Junction Diode for both forward and reverse characteristics - 8M //

Sol → Let us consider silicon diode, following figure shows the Forward and Reverse characteristics

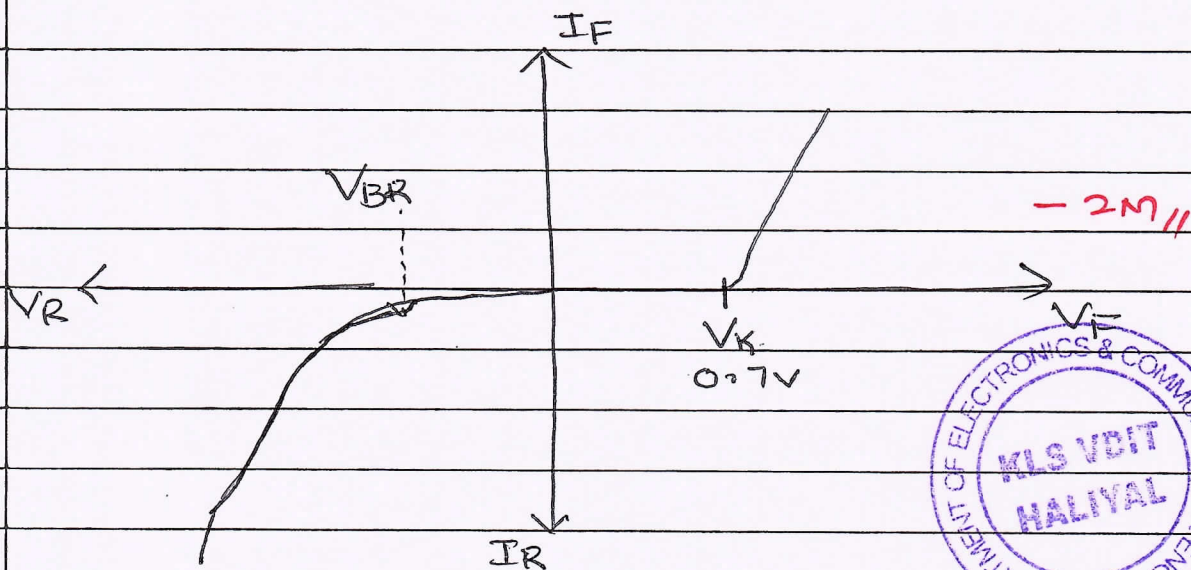


Fig 1a: Forward and Reverse characteristics of Si Diode

In Fig 1a

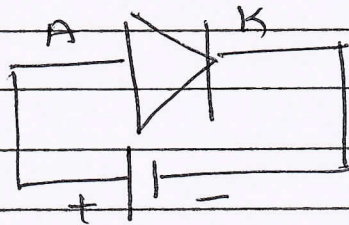
V_F and I_F are the Forward voltage and Forward current - which are applied across the diode and flowing through the diode respectively

V_R and I_R are the Reverse voltage applied across the diode during reverse bias and I_R is the reverse current - flowing through the diode

V_K : It is the knee voltage, which will be 0.7V for Si diode and 0.3V for Ge diode. It is the forward voltage at which current flows through the diode during forward bias condition.

V_{BR}: It is the reverse breakdown voltage, i.e., It is the reverse voltage at which PN junction breaks and a large reverse current flows through the diode, typical values are -75V for Si and -50V for Ge. 2M //

Forward Bias: A Diode is said to be forward biased if the Anode (P-Type) is more +ve than the Cathode (N-type)



Reverse Bias: A Diode is said to be reverse biased if the Anode (P-Type) is less positive or -ve w.r.t. Cathode (N-Type). 2M //

Q1b) Given: $I_f = 400\text{mA}$ @ $V_R = 50\text{V}$, $V_F = 0.75\text{V}$
 $I_R = 100\text{nA}$. 4M //

$R_F = \frac{V_F}{I_f} = \frac{0.75\text{V}}{400\text{mA}} = 1.875\Omega$	$R_R = \frac{V_R}{I_R} = \frac{50\text{V}}{100\text{nA}} = 500\text{M}\Omega$
---	---

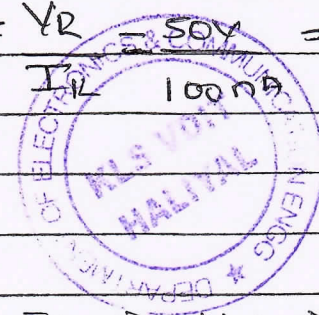
2M //

2M //

Q1c) Diode Approximations

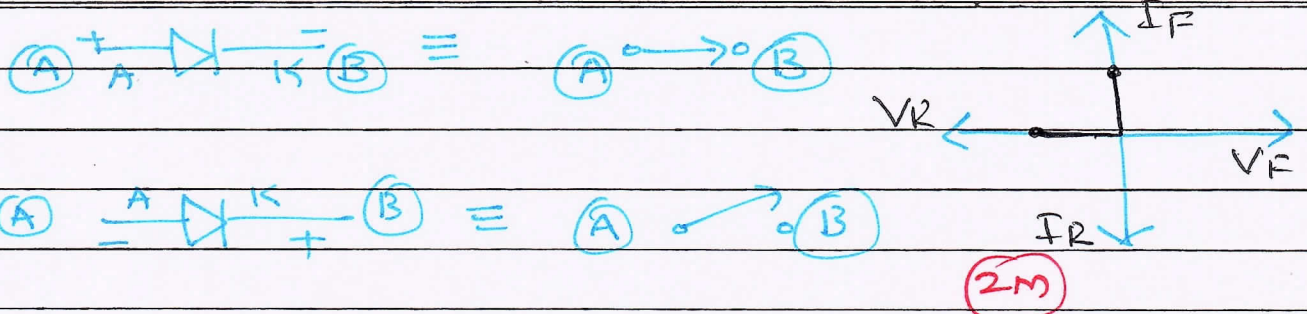
There are 3 Approximations

1) **Ideal Diode Approximation**: It is the ideal approximation in which Diode is represented by closed switch in Forward Bias condition and open switch in Reverse condition



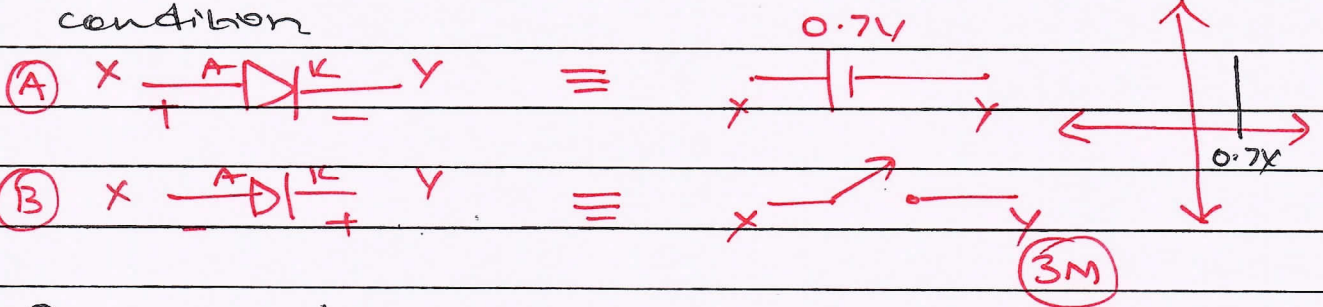
8M

Q1c)



(2M)

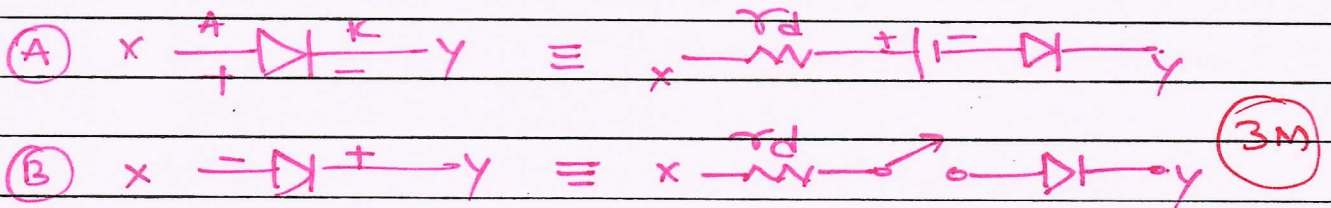
2) DC Equivalent- Ckt: In this diode is replaced by its equivalent- knee voltage during forward bias and by open ckt- by reverse bias condition



(3M)

3) Piecewise Linear Characteristics

In this along with the knee voltage, the forward resistance or dynamic resistance is also included in the representation

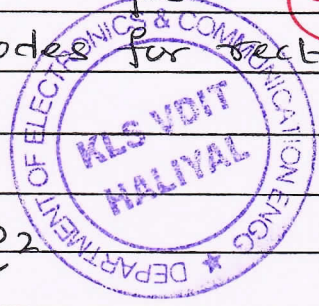
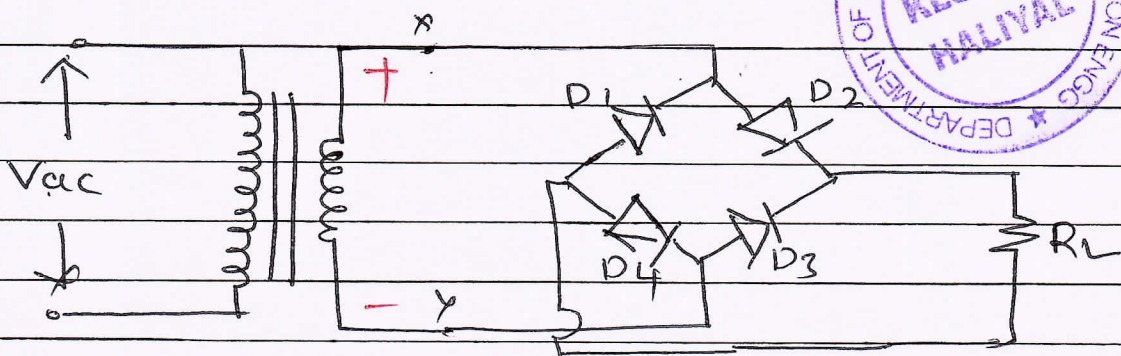


(3M)

Q2a)

Working of Full Wave Bridge Rectifier! Circuit-Diagram: It uses 4 diodes for rectification process.

(8M)

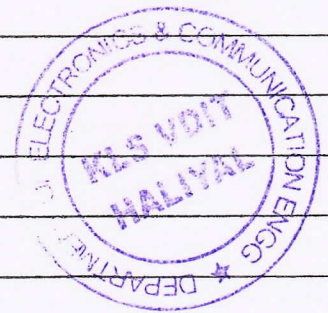
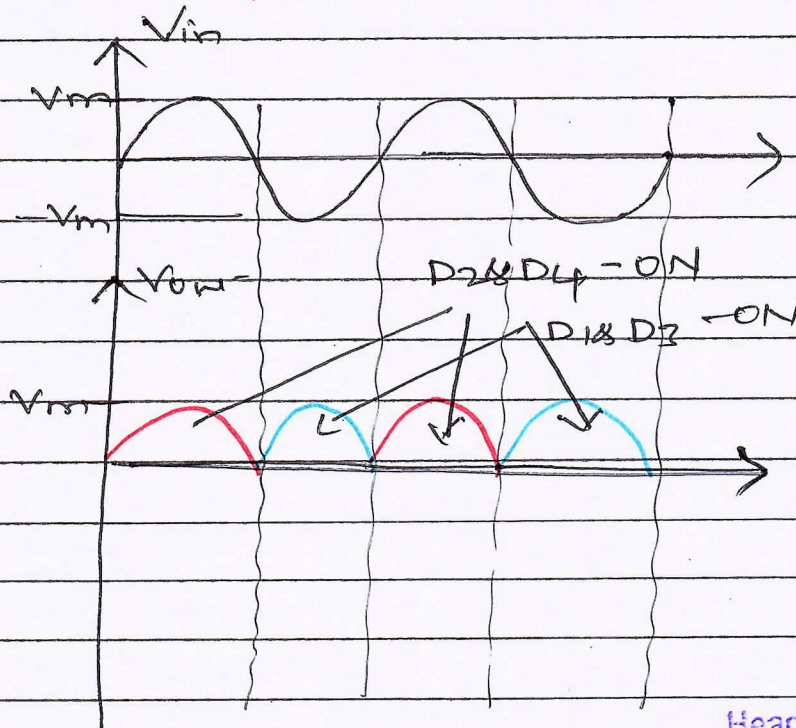
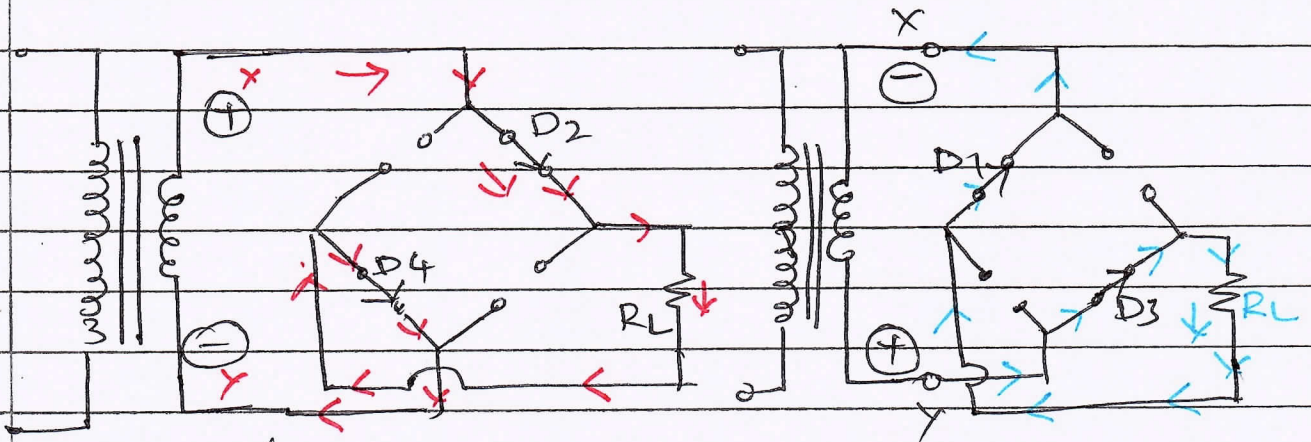


Teacher's Sign. *OK*

During +ve half of the input signal, point X will be +ve w.r.t Y, hence Diode D_2 and D_4 will be forward biased whereas Diode D_1 and D_3 will be reverse biased, hence current flows through $X - D_2 - RL - D_4 - Y$ as shown below, Similarly During -ve half of V_{in} X will be -ve w.r.t Y, hence conduction takes place from $Y - D_3 - RL - D_1 - X$.

4M//
During +ve half cycle

4M//
During -ve half cycle



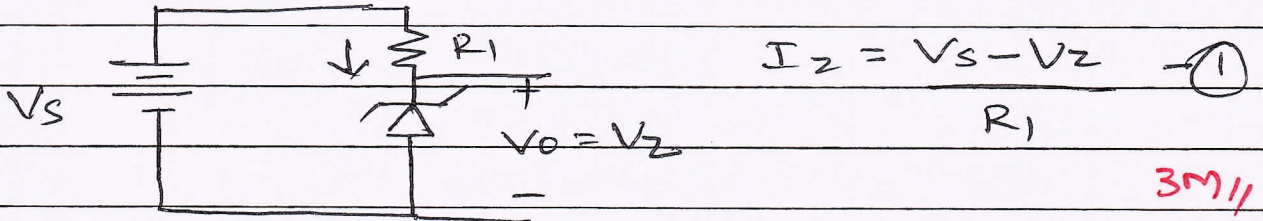
Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T. HALIYAL (U.K.)

Teacher's Sign

Q2b) → Zener Diode as a voltage Regulator! (6M)

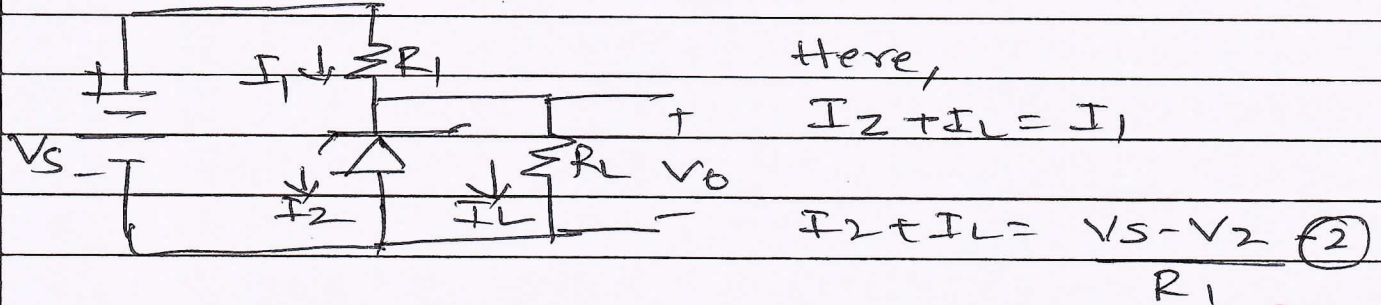
Zener Diode is used to maintain a constant DC o/p voltage in crks like rectifiers

→ Consider the crk- with no load

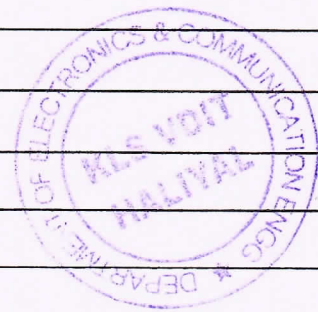


From Eqn (1) we can understand that- V_z depends on $(I_2 \times R_1) / V_s$, if V_s is greater than V_z then V_z remains constant but I_2 increases. ($V_o = V_z$)

→ Consider the crk- with load



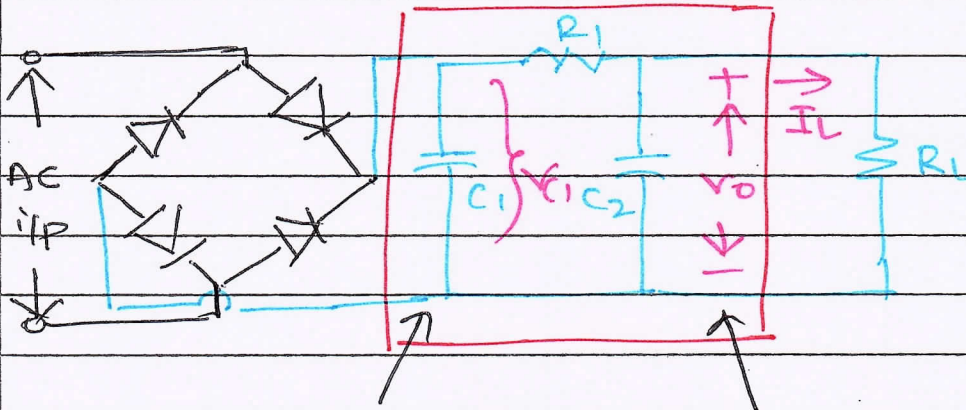
From Eqn (2), we can conclude that- I_2 is $= I_1 - I_L$, again if current through Zener is more than current through R_L will be less such that- $V_o = V_z$



Q2C)

RC-π Filter RC-π Filter

6M



Ripple Voltage across C_1

AC voltage across C_2



Here additional capacitor C_1 and R_1 will attenuate the ripple contents from transformer O/p.

The shape of C_1, R_1, C_2 is like π symbol hence the name RC- π Filter

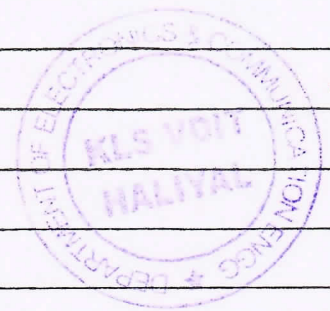
The harmonic components are more severely attenuated by voltage division across R_1 and C_2

\therefore Peak voltage is $V_p = \frac{V_r}{\pi}$ 2M //

$\therefore V_{oc2}(ac) = \frac{V_i X_{C2}}{\sqrt{R_1^2 + X_{C2}^2}}$ 2M //

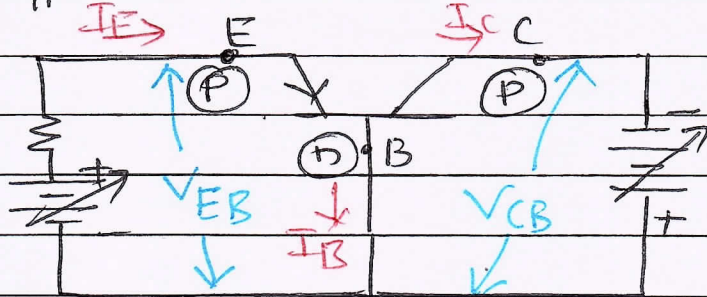
$X_{C2} = \frac{R_1}{\sqrt{(V_i/V_o)^2 - 1}}$

$X_{C2} \approx R_1 / (V_i/V_o)$ 2M //



Q3a) Common Base O/P Characteristics - (6M)

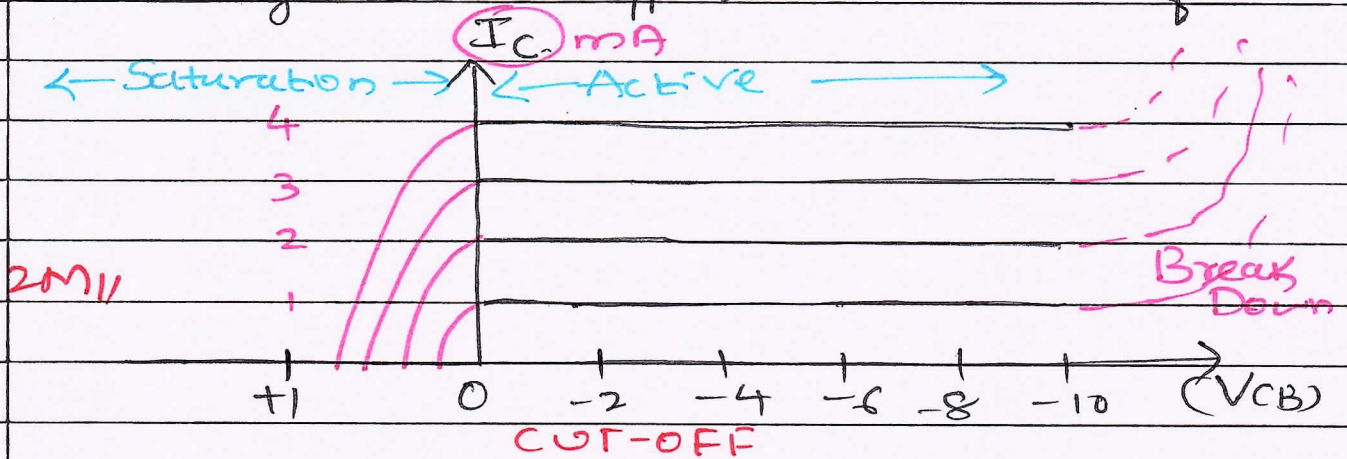
Consider the following ckt for common base o/p characteristics.



O/P characteristics are the plots of O/P voltage (V_{CB}) vs O/P Current (I_C) for various i/p across

entire value (I_E), For common base, Base will be common b/w i/p and o/p.

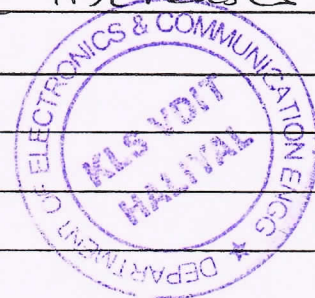
Following are the o/p characteristics of CB.



Saturation region: When V_{CB} is forward biased (left side), where I_C remains constant.

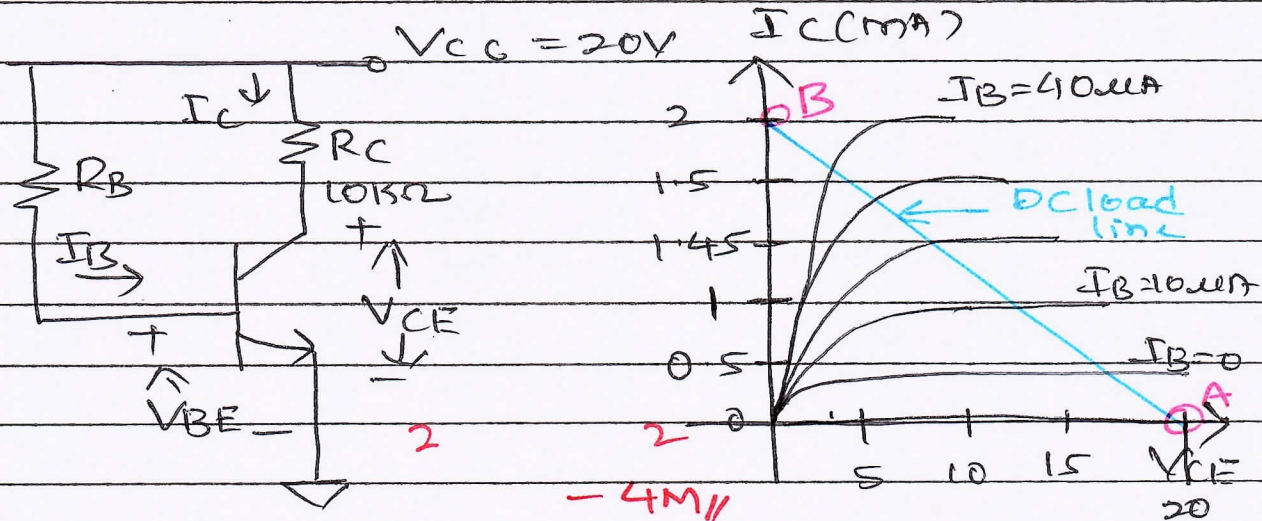
Active region: When V_{CB} is reverse biased (right side), where I_C increases. 2M

Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T. HALIYAL (U.K)



Teacher's Sign.

Q3b) DC load line on BJT in CE o/p char^s.
 It is the straight-line drawn on the o/p char^s of BJT, which is the plot of VCE vs IC.



Step 1: KVL to o/p path: $V_{CE} = V_{CC} - I_C R_C$ — (1)

Step 2: Assume $I_C = 0$, $\therefore V_{CE} = 20V$ — (2) (A)

Assume $V_{CE} = 0$, $\therefore I_C = 2mA$ — (3) (B)

Step 3: join point (A) and (B), this is the DC load line for $R_C = 10k$, and $V_{CC} = 20V$. $4M\Omega$

Q3c) Given $I_C = I_E = ?$, $\alpha = 0.98$, $I_B = 100\mu A$
 $\beta_{DC} = ?$

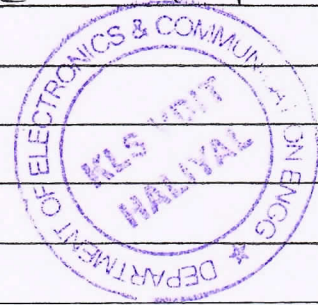
we have $I_E = I_B + I_C$; $\alpha = \frac{I_C}{I_E}$ $\beta = \frac{I_C}{I_B}$

$\therefore \beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}} = 49$

$I_C = \beta I_B$
 $I_C = 4.9 mA$

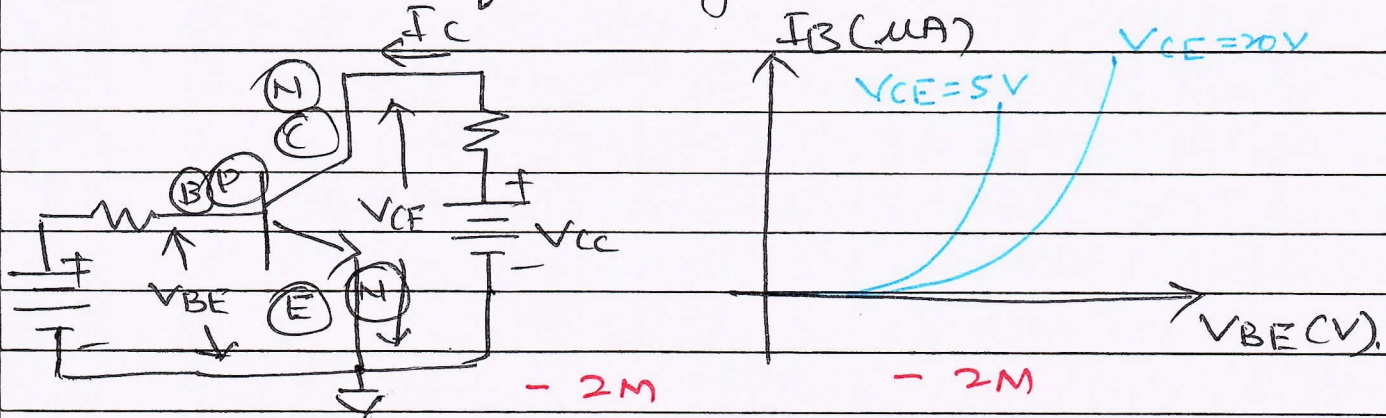
$I_E = 5 mA$

$1 + 1 + 1 = 3M$



Q4a) common Emitter input characteristics.
 It is the curve b/w input current I_B and input voltage V_{BE} for constant o/p voltage (V_{CE}).

consider the following ckt-

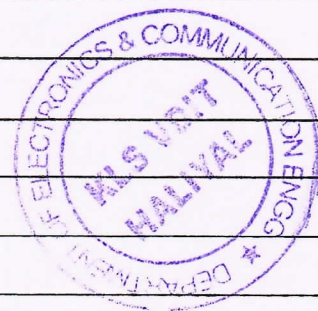


From the characteristics we observe that-

* C/E mode i/p characteristics resembles to that of a PN-junction diode, as V_{BE} crosses cut-in voltage, I_B increases for fixed level of V_{CE}

* But as observed above, for various V_{CE} , I_B may increase rapidly or slowly

* If V_{CE} is increased, due to early effect- I_B decreases and as V_{CE} is reduced, as early effect is not observed I_B increases the same is shown and can be observed



-2M

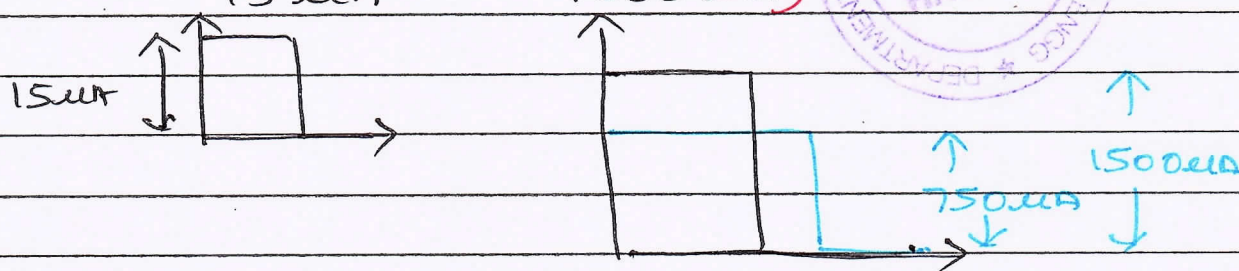
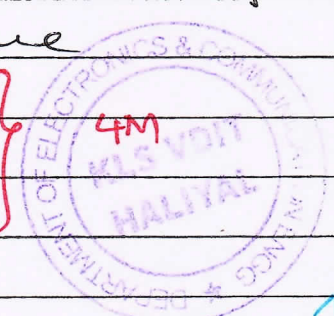
Q4b) Transistor as current-amplifier
 In BJT we have two current amplification factors α which can range from 0.95 to 0.995 and β which can range from 40 to 300. which are related as

$$\alpha = \frac{I_C}{I_E} \quad \text{and} \quad \beta = \frac{I_C}{I_B} \quad \left. \vphantom{\alpha} \right\} 2M$$

as α can vary approximately till 1, $I_C \approx I_E$ hence it will not contribute any amplification.

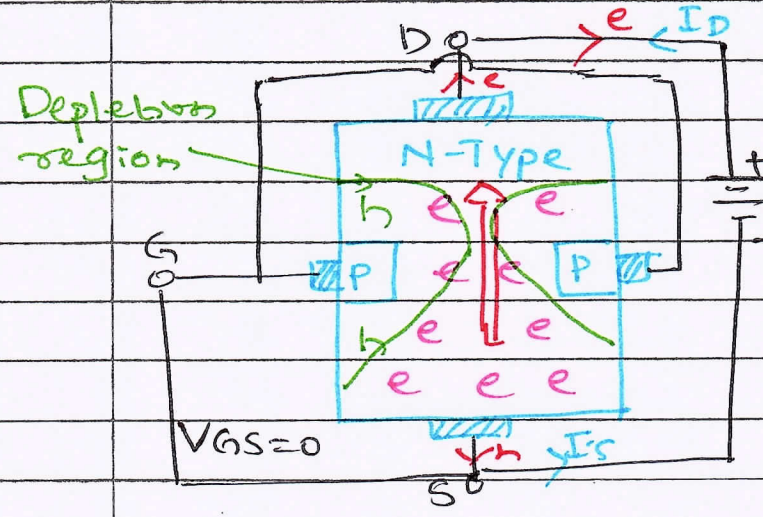
Now consider $\beta = I_C/I_B$, consider following cases for various β value

β	I_B	I_C
50	15 μA	750 μA
100	15 μA	1500 μA



Q4c) N-Channel JFET: working can be understood by following cases

(i) when $V_{GS} = 0$, $V_{DS} = +ve$ - 4M //

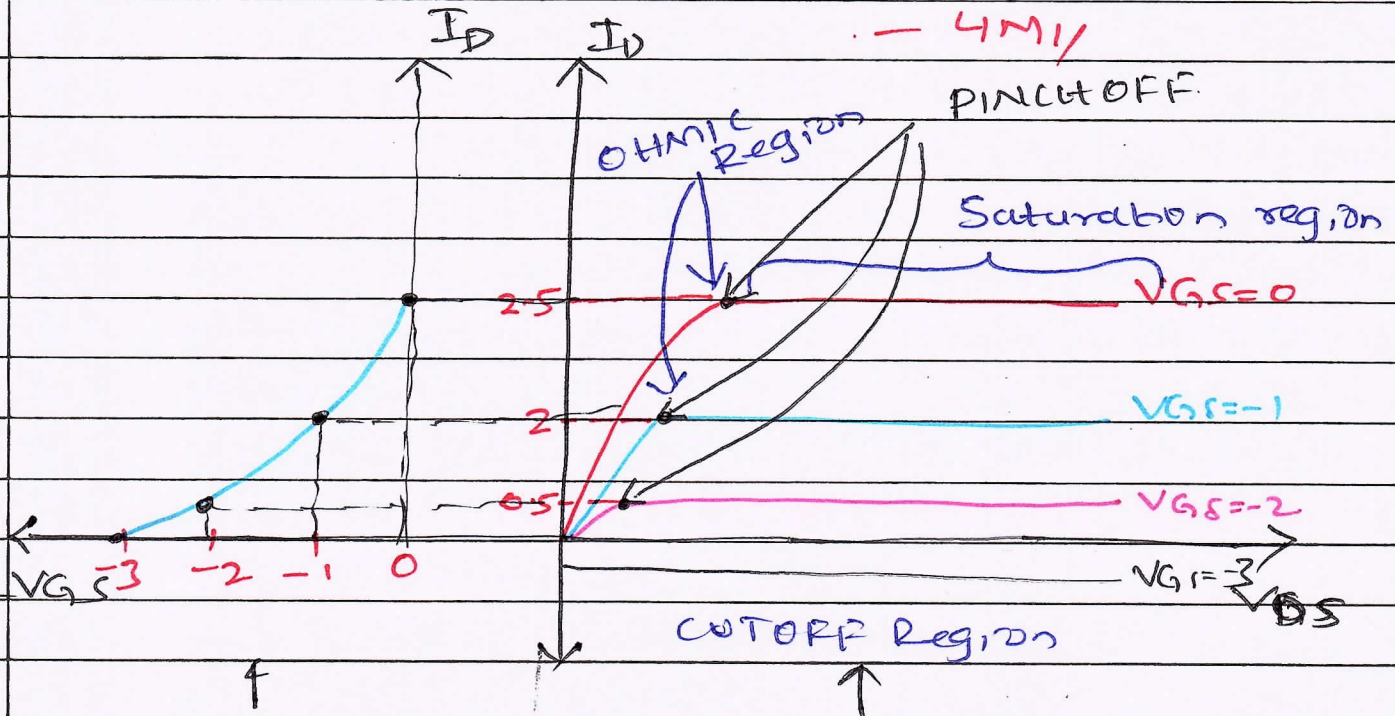


In this biasing maximum electrons reach drain hence contributing $V_{DS} I_D$, But - if V_{DS} is increased further, Drain to Gate region will be reverse biased, hence flow of electrons will be restricted

If the V_{DS} is increased further, then flow of electrons will be completely blocked, the voltage of V_{DS} at which this condition takes place is called "Pinch off" V_{DS}

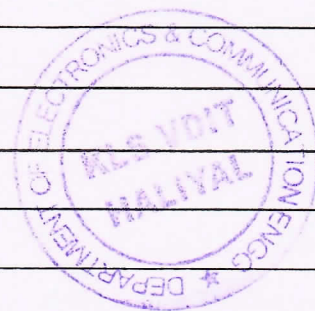
Case (ii) : If V_{GS} is -ve and V_{DS} is +ve, as Gate is of P-Type, if it is made -ve with V_{DS} then PINCHOFF condition reaches much earlier than when $V_{GS} = 0$ and $V_{DS} = +ve$

This is shown in the below characteristics.



Transfer charact
(I_D vs V_{GS})

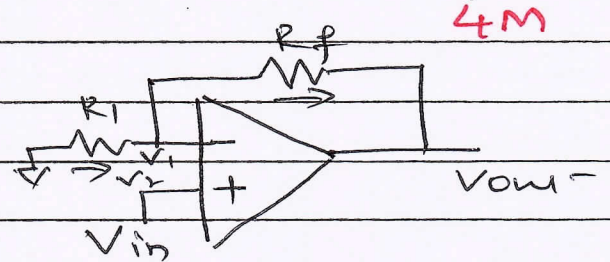
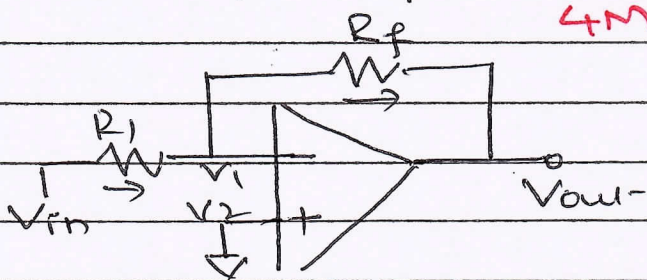
Drain Characteristic
(V_{DS} vs $I_D @ V_{GS}$)



Q5a) Inverting and Non Inverting Amplifier
 If the i/p is connected only to the inverting input, it is referred to as inverting configuration, and as non-inverting configuration if i/p is connected only to non-inverting i/p only

Inverting Ampⁿ Ckt-

Non-Inverting Ampⁿ



KCL at V_1

$$\frac{V_{in} - V_1}{R_1} = \frac{V_1 - V_{out}}{R_f}$$

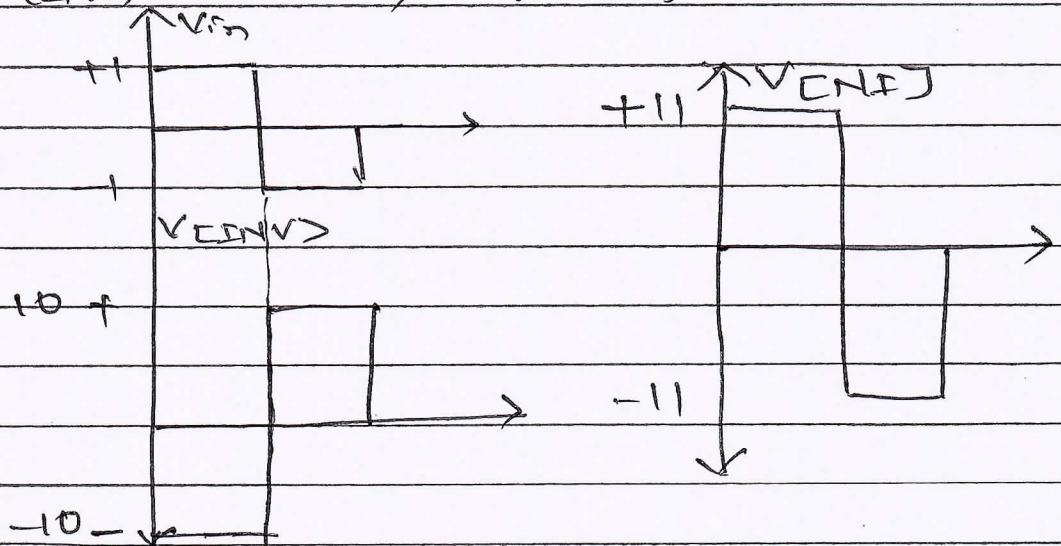
By Virtual ground $V_1 = V_2 = 0$

$$\therefore V_{out} = -\frac{R_f}{R_1} V_{in} \quad \text{(INV)}$$

$$\text{Gain} = -\frac{R_f}{R_1}$$

Assume $V_{in} = 2V$, $R_f = 10K$, $R_1 = 1K$

$$\therefore V_{out} \text{ (INV)} = -20V, \quad V_{out} \text{ (NI)} = 22V$$



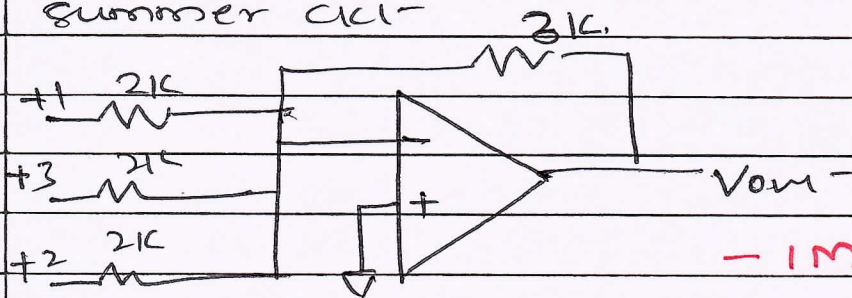
Q5b) Op-Amp is an Electronic device having two differential i/p's namely Inverting and Non-Inverting and one o/p pin which produces Differential amplified signals and also it can perform Arithmetic operation and as well as AC/DC amplification

5- Ideal parameters op-amp values

Parameter	Ideal value
Open loop voltage gain (A_v)	$= \infty$
O/P resistance (R_{out})	$= 0$
I/P resistance (R_{in})	$= \infty$
Bandwidth (BLW)	$= \infty$
Slew rate (CSR)	$= \infty$

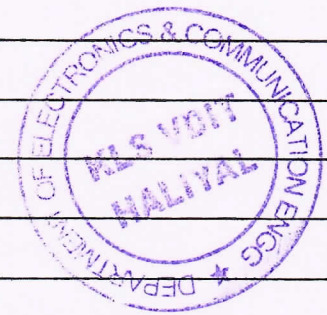
Q5c) Given $V_1 = +1V$; $V_2 = +3V$; $V_3 = +2V$
 $R_1 = R_2 = R_3 = 2K\Omega$, $R_f = 3K\Omega$

From Given data, it is a summer ckt-



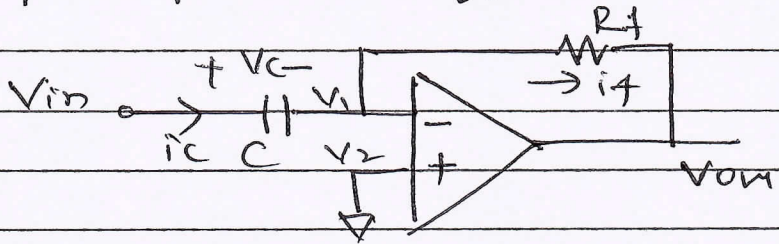
$$V_{out-} = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$= -1.5 [1 + 3 + 2] = -1.5 [6] = -9V$$



5M //

Q 6a) op-amp as Differentiator



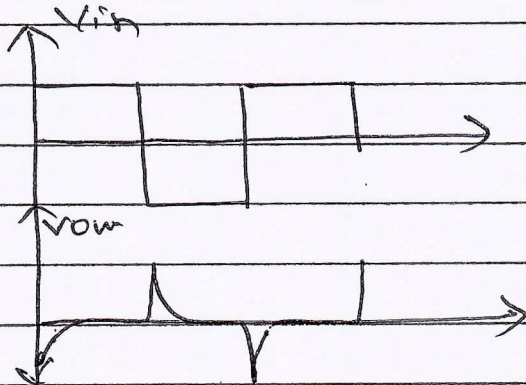
3M//

KCL @ V1

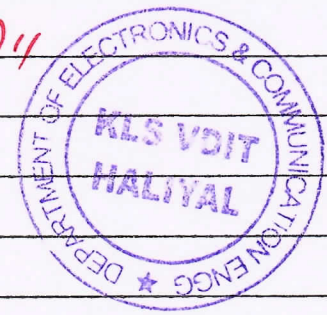
$$C \cdot \frac{d(V_{in} - V_1)}{dt} = \frac{V_1 - V_{out}}{R_f} \quad \left| \text{Let } R_f = R \right.$$

3M//

$$\therefore V_{out} = -RC \frac{dV_{in}}{dt} \quad \left| \begin{array}{l} \text{By virtual ground} \\ V_1 = 0 \end{array} \right.$$



2M//



Q 6b) Input offset current: The difference in magnitude of I_{b1} and I_{b2} is called I_{io}

$$I_{io} = |I_{b1} - I_{b2}| \quad 1M$$

Input Bias current: I_I is the current flowing through the two terminals when device is biased

$$I_I = \frac{|I_{b1}| + |I_{b2}|}{2} \quad 2M$$

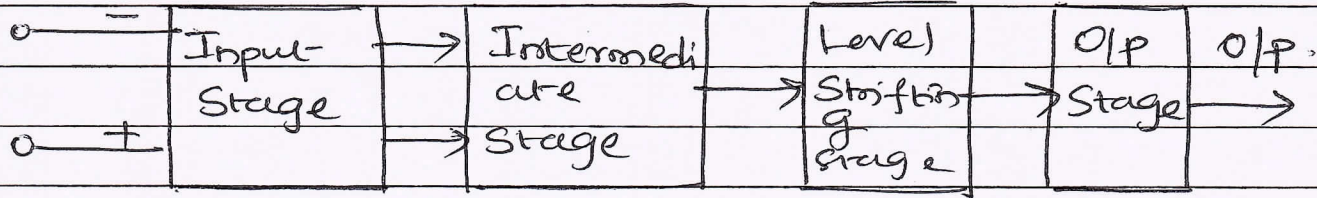
Slew Rate: S_R is the maximum rate of change of op voltage w.r.t time $S_R = \frac{dV_{out}}{dt} \Big|_{Max}$

1M

CMRR: It is ratio of differential gain to common mode gain $CMRR = \left| \frac{A_d}{A_c} \right|$

2M

Q6c Op-Amp Block diagram and ckt-



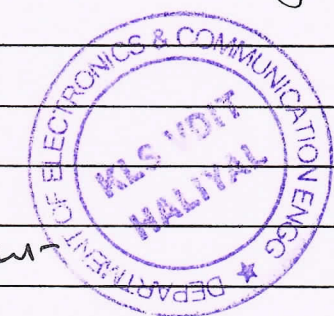
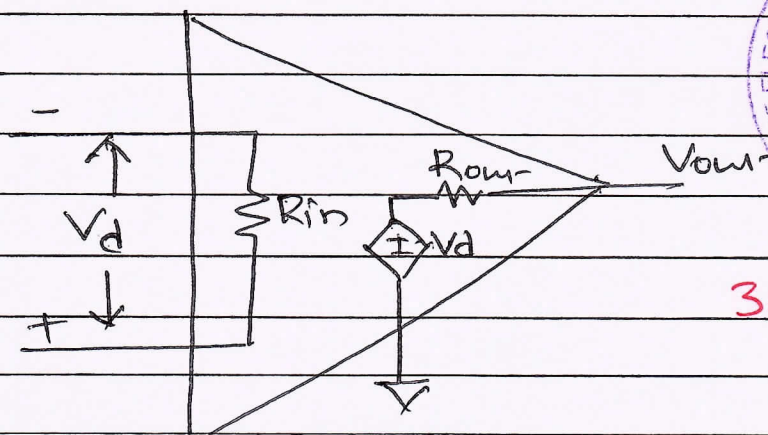
Input- Stage: The basic requirement of the i/p stage of op-amp are A_V , R_i , R_{out} , $CMRR$ etc

3M/1

Intermediate stage: It is the stage two i/p are differentiated and amplified as per the application need.

Level Shifting stage: During the amplification if o/p levels are going beyond by $+V_{CC}$ or $-V_{EE}$ by + OFFSET pin

Output stage: It is the o/p pin through which o/p is taken



3M/1

Q7a) (i) $(2AB.8)_{16} = ()_{10}$
 $= 2 \times 16^2 + A \times 16^1 + B \times 16^0 + 8 \times 16^{-1}$
 $= 512 + 160 + 12 + 0.5 = (684.5)_{10}$

(ii) $(416.12)_{10} = ()_8 = (640.07405)_8$

8	416	$0.12 \times 8 = 0.96 = 0$
8	52 - 0	$0.96 \times 8 = 7.68 = 7$
	6 - 4	$0.68 \times 8 = 5.44 = 5$
		$0.44 \times 8 = 3.52 = 3$
		$0.52 \times 8 = 4.16 = 4$

(iii) $(25.375)_{10} = ()_2 = (11001.011)_2$

2	25	$0.375 \times 2 = 0.75 = 0$
2	12 - 0	$0.75 \times 2 = 1.50 = 1$
2	6 - 0	$0.50 \times 2 = 1.00 = 1$
2	3 - 0	$0.00 \times 2 = 0.00 = 0$
	1 - 1	

(iv) $(16.2)_8 = ()_{16}$

1 6 0 2
 001 110 010 → Group of 4
 $0000 1110 0100 = (0E.4)_{16}$

Q7b) $F_1 = \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z$, By DMT we get -
 $\bar{F}_1 = \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z = (\bar{X}Y\bar{Z}) + (\bar{X}\bar{Y}Z)$
 $= (\bar{X} + \bar{Y} + \bar{Z}) \cdot (\bar{X} + \bar{Y} + Z)$
 $= \bar{X}\bar{X} + \bar{X}Y + \bar{X}\bar{Z} + \bar{X}\bar{Y} + \bar{Y}Y + \bar{Y}Z + XZ + XY + Z\bar{Z}$
 $= 1 + \bar{X}Y + \bar{X}(\bar{Z} + Z) + \bar{Y}(X + Z)$
 $= 1 + \bar{X}Y + \bar{X} + \bar{Y}Z$
 $= (1 + \bar{X}) + \bar{X}Y + \bar{Y}Z$
 $= 1 + \bar{X}(1 + \bar{Y}) + \bar{Y}Z$
 $= 1 + \bar{X} + \bar{Y}Z$
 $= 1 + \bar{Y}Z$



Q7b)

$$F_2 = X [\bar{Y}\bar{Z} + YZ] = X\bar{Y}\bar{Z} + XYZ$$

$$\bar{F}_2 \stackrel{DM}{=} (\bar{X}\bar{Y}\bar{Z}) + (\bar{X}YZ) = (\bar{X}\bar{Y}\bar{Z}) \cdot (\bar{X}YZ)$$

$$= (\bar{X} + Y + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z})$$

$$= \bar{X} \cdot \bar{X} + \bar{X}\bar{Y} + \bar{X}\bar{Z} + \bar{X}Y + \bar{Y}\bar{Y} + Y\bar{Z} + \bar{X}Z + \bar{Y}Z + Z\bar{Z}$$

$$= \bar{X} + \bar{X}\bar{Y} + \bar{X}\bar{Z} + \bar{X}Y + Y\bar{Z} + \bar{X}Z + \bar{Y}Z$$

$$= \bar{X}(1 + \bar{Y}) + \bar{X}(\bar{Z} + Z) + \bar{X}Y + Y\bar{Z} + \bar{Y}Z$$

$$= \bar{X} + \bar{X} + \bar{X}\bar{Y} + Y\bar{Z} + \bar{Y}Z$$

$$= \bar{X} + \bar{X}\bar{Y} + Y\bar{Z} + \bar{Y}Z = \bar{X}(1 + \bar{Y}) + Y\bar{Z} + \bar{Y}Z$$

$$= \bar{X} + Y\bar{Z} + \bar{Y}Z$$

4M //

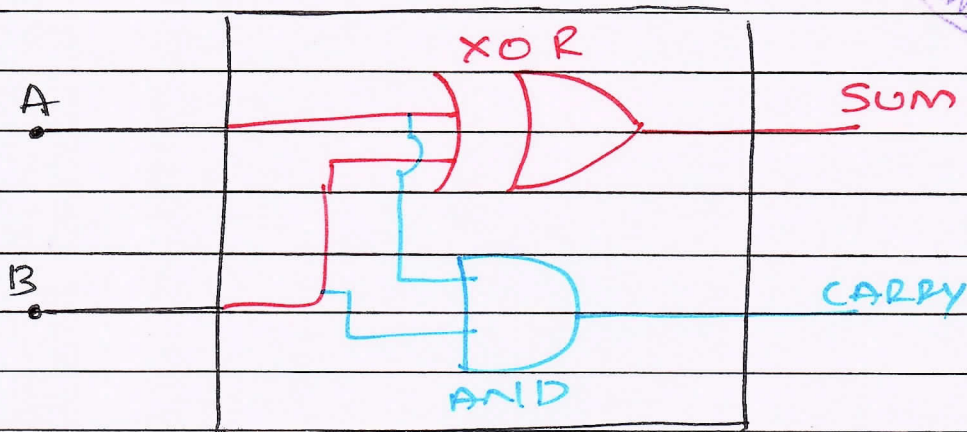
Q7c) working of half adder

It is a 1 bit adder which adds two one bit numbers say (A & B) and produces results (1 bit of sum (S) and carry (C)), consider the following Truth table

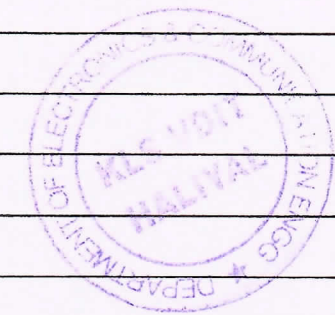
A	B	S	C	$S = \bar{A}B + A\bar{B} = A \oplus B$
0	0	0	0	$C = A \cdot B$
0	1	1	0	
1	0	1	0	
1	1	0	1	

3M //

Logic Diagram



HALF ADDER



Q 8a) $F = A + \bar{B}C$ In sum of minterms

$$F = A(B + \bar{B}) + \bar{B}C(A + \bar{A})$$

$$= AB + A\bar{B} + A\bar{B}C + \bar{A}\bar{B}C$$

$$= AB(C + \bar{C}) + A\bar{B}(C + \bar{C}) + A\bar{B}C + \bar{A}\bar{B}C$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$= \bar{A}\bar{B}C + A\bar{B}C + A\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$= m_1 + m_4 + m_5 + m_6 + m_7$$

$F(A, B, C) = \sum(1, 4, 5, 6, 7)$

Q 8b) Mention Postulates and theorems of Boolean Algebra

Theorems and Postulates	
① Demorgans Thm $(\overline{x+y}) = \bar{x} \cdot \bar{y}$	$(\overline{xy}) = \bar{x} + \bar{y}$
② commutative " $x+y = y+x$	$x \cdot y = y \cdot x$
③ Idempotent - $x+x = x$	$x \cdot x = x$
④ complementary $x + \bar{x} = 1$	$x \cdot \bar{x} = 0$
⑤ Absorption $x + xy = x$	$x(x+y) = x$
⑥ Identity $x+0 = x$	$x \cdot 1 = x$
⑦ Distributive $x(y+z) = xy + xz$	$x(yz) = (xy)z$

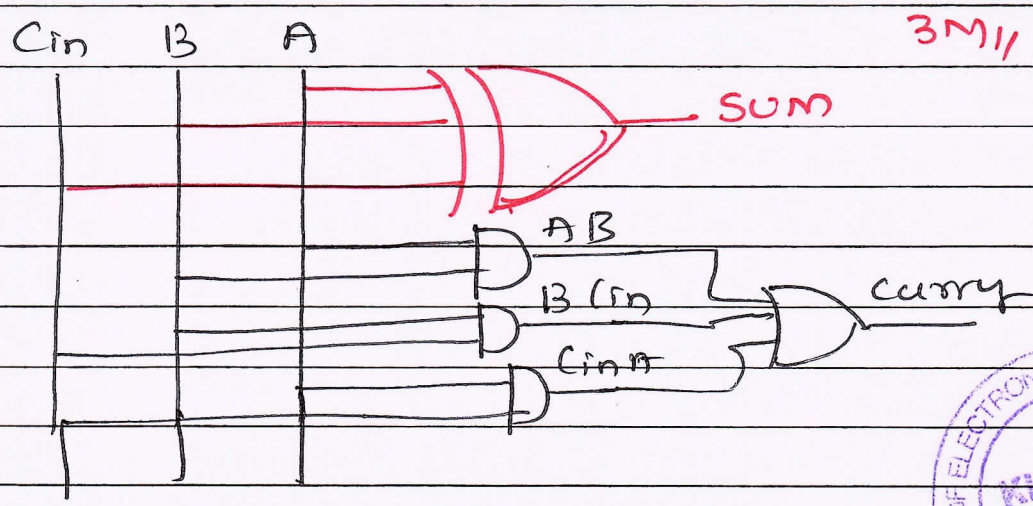
Q 8c) A Full adder is a 1-bit adder which can add 3-1 bit numbers i/p say A, B & C and produces 2-1 bit results Sum (S), and Carry (carry)

A	B	Cin	Sum	Carry	A	B	Cin	Sum	Carry
0	0	0	0	0	1	0	1	0	1
0	0	1	1	0	1	1	0	0	1
0	1	0	1	0	1	1	1	1	1
0	1	1	0	1					
1	0	0	1	0					

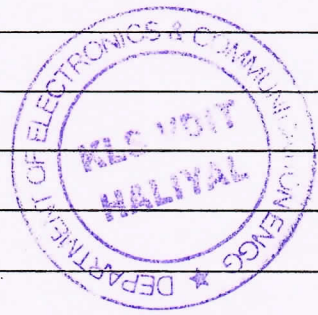
Q8C

Sum = $A \oplus B \oplus C_{in}$

Carry = $AB + BC_{in} + C_{in}A$



3M //

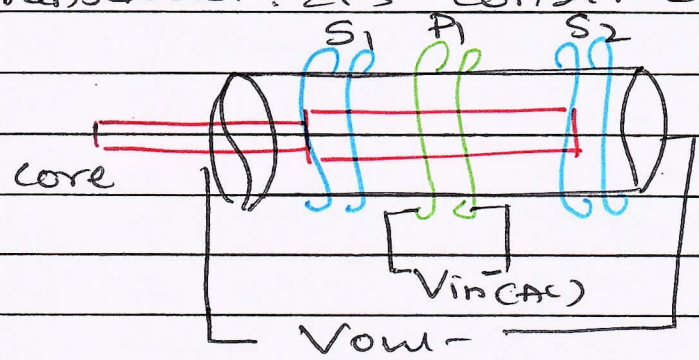


Module-5

Q9a)

Working of LVDT

LVDT stands for Linear Variable Differential Transducer. Its construction is shown below.



It consists of 2 Secondary windings S_1 & S_2 and Primary winding P_1 , movable core

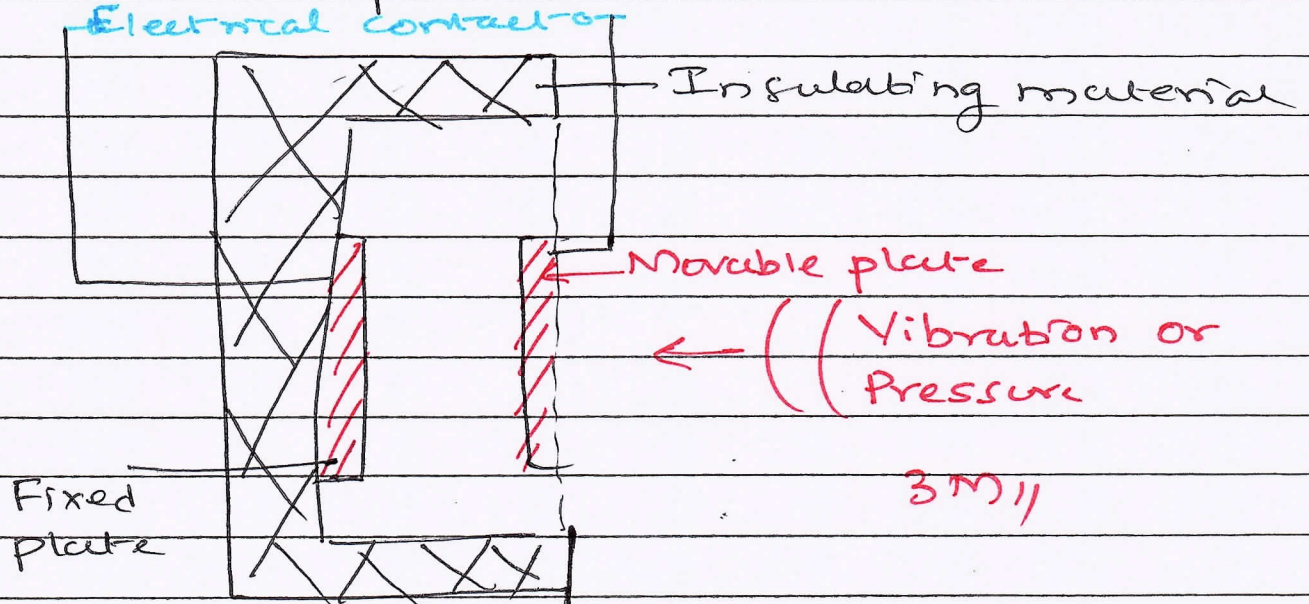
If core is moved towards S_1 , then

$V_{out} = V_{S1} - V_{S2}$, if core is towards S_2 , $V_{out} = V_{S2} - V_{S1}$, which indicates the change in voltage with change in distance **there displacement - is converted to voltage**

3M //

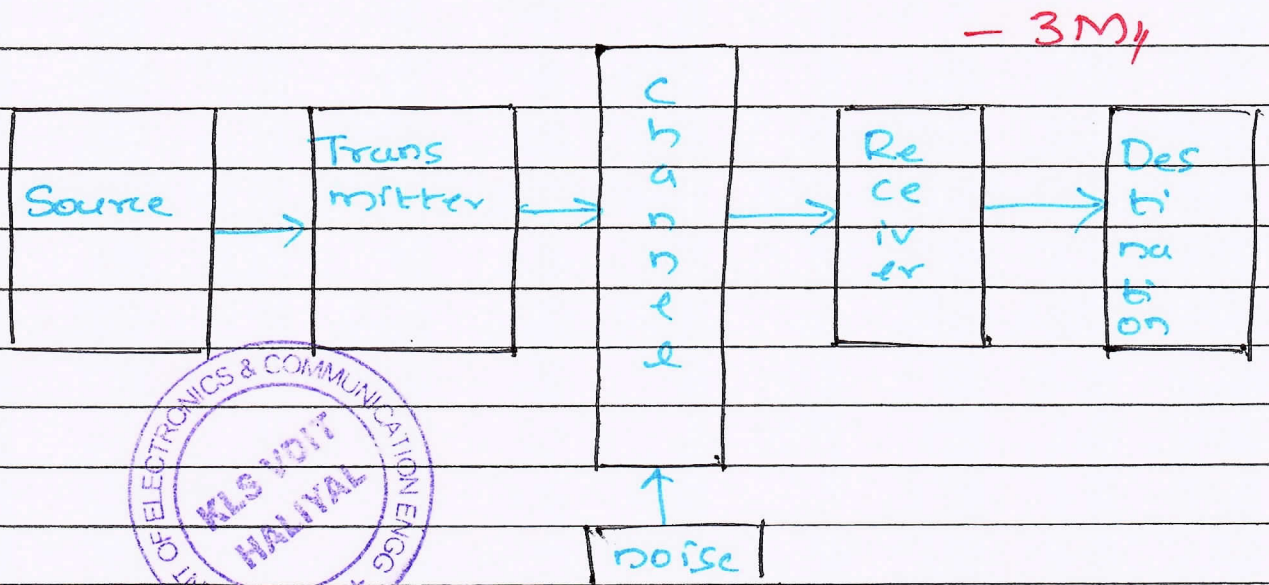
Q9b) Capacitive Pressure Transducer

Working Principle: Pressure is converted to suitable capacitance value



It is like an Audio setup of microphone where vibrations of sound are converted to capacitance value, such that charge $Q = CV$ changes w.r.t. vibration and hence voltage also. 3M

Q9c) Working of communication system



Q9C) Information Source: It is the place from which communication data will be established, it can be in either audio, video or any other physical form. Let us assume an audio setup. In this place we can have an audio signal

2M)

Transmitter: The basic function of transmitter is to convert information into suitable electrical signal, in this audio (voice) will be converted into electrical signal using a microphone

1M)

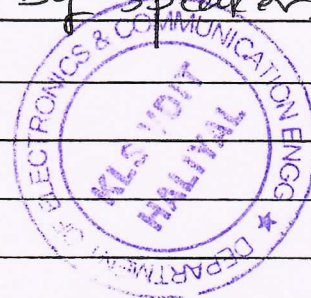
Channel: It is the medium through which the information will be traveling/reaching the destination. It can be a wired/wireless channel

1M)

Noise: It is an unwanted signal which exists in nature which may get added up with the channel

Receiver: The function of the receiver is to convert the electrical signal received from channel into suitable form, here electrical signal is converted back to audio by speakers

1M)



Q 10 a)

Thermistors

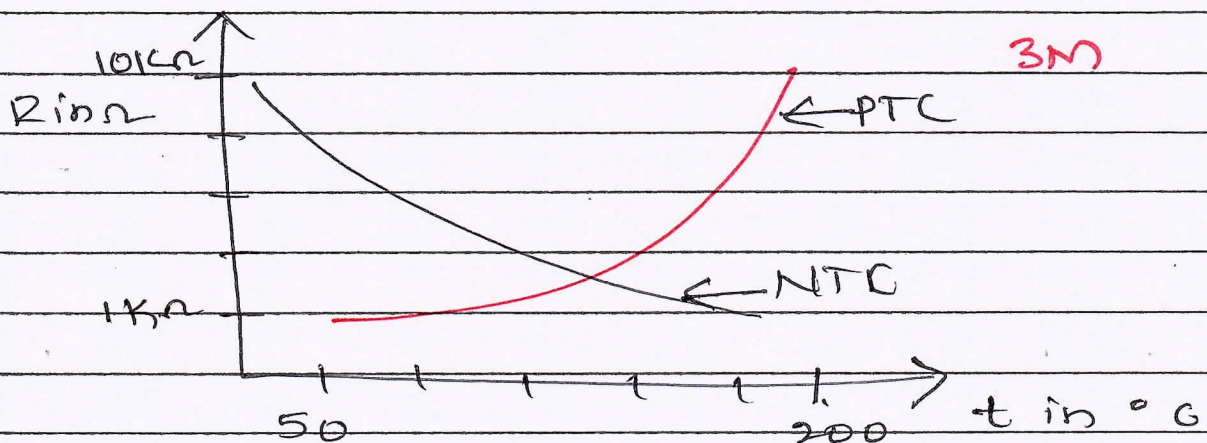
→ Thermally sensitive resistor

→ These perform the transduction of temperature to resistance conversion

→ These possess two types of change in resistance

NTC (Negative temperature Resistance, where resistance is inversely proportional to temperature) 3M

PTC (Positive temperature Resistance, where resistance and temperature are directly proportional to each other.)



Q 10 b) Short-Note on Photo Diode

→ It is a transducer device which converts light-energy into suitable electrical energy

→ Symbol and construction, use



Q.10b) 2. Photo Diode:

Photo diode is a semiconductor device which requires light energy along with the biasing voltage. Generally it is operated in reverse bias condition, in which if it is exposed to the sufficient intensity of light, it allows the flow of electrons along with the minority charge carriers.

Following Fig shows the construction details, package and symbol.

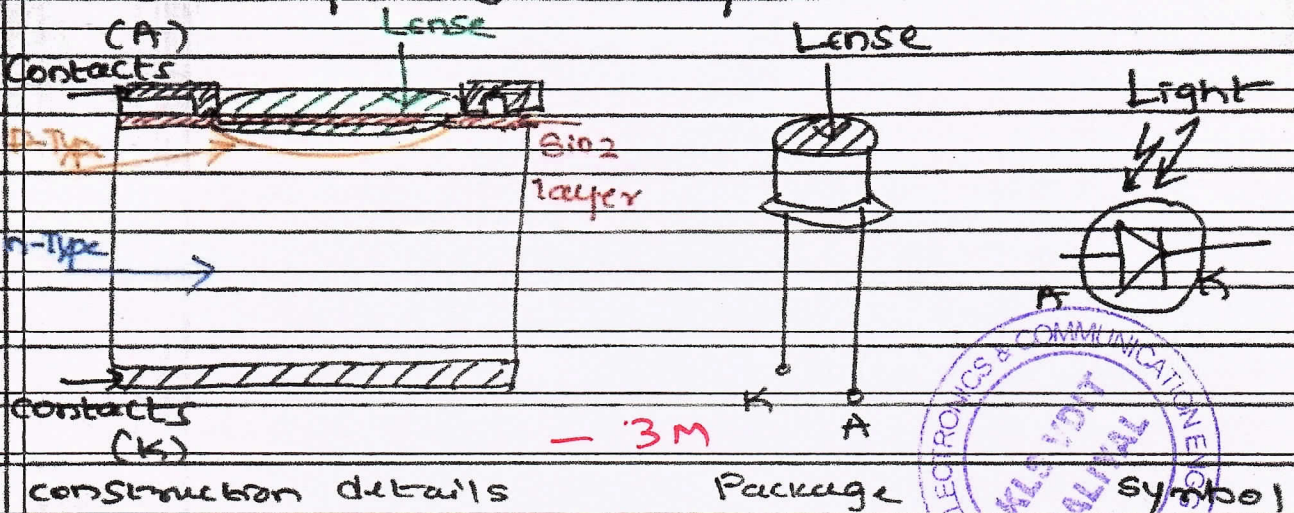


Fig 5.25

From Fig 5.25 construction details, we can note that a typical photo diode consists of P-N junction layer, at the junction a photo sensitive lens is provided, through which light enters in to the junction. The contacts near P-layer forms the anode (A) and contact near N-layer form the cathode (K). Also we can see the package view. From symbol we can note that incoming arrows indicate the direction of light.

- 3M

Q 10C) Defⁿ of Modulation and Need for Modulation:

Modulation: Process of changing any one parameter like Amplitude, frequency or phase of carrier wave w.r.t the message signal.

Need For Modulation:

1) To Reduce Height of Antennas

wave length $\lambda = \frac{c}{f}$, if $f = 3\text{kHz}$ and

if $f = 1\text{MHz}$, we can see that height of antenna required will be 25km ($\lambda/4$) and 35m ($\lambda/4$) respectively, hence by frequency modulation we can control the height of antenna

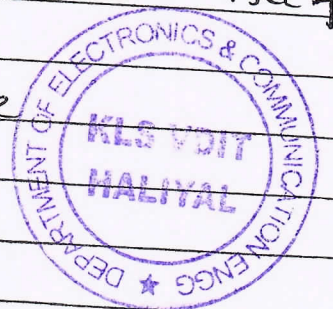
2) To increase the distance of communication: By frequency and phase modulation can be employed

3) To avoid overlapping of signals: In modulation by using Guard bands we can avoid interference

4) To reduce the effect of noise

6M //

110 //



Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T. HALIYAL (U.K.)

Teacher's Sign.