KLS Vishwanathrao Deshpande Institute of Technology

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper
Scheme & Solution

Faculty Name	:	DEEPAK SHARMA
Course Name	:	VLSI DESIGN
Course Code	:	18EC72
Year of Question Paper	:	2023 - 24
Date of Submission	:	15/04/2024

Faculty Member

HoD
Head of the Department

Dean (Acad.)

KLS V.D.I.T., HALIYAL (U.K.)

CBCS SCHEME

USN | | | | | | | | | | |

18EC72

Seventh Semester B.E. Degree Examination, Dec.2023/Jan.2024
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Missing data may be suitably assumed.

Module-1

1 a. Derive an expression for drain current in linear and saturation region. **(08 Marks)**

b. Draw the CMOS inverter circuit and explain its D.C. characteristic. **(08 Marks)**

c. Implement a 2:1 MUX using transmission gate. **(04 Marks)**

OR

2 a. Explain the non ideal IV effect of MOSFET with respect to CMOS channel length modulation and mobility degradation. **(08 Marks)**

b. Explain the operation of nMOS transistor with IV characteristics. **(08 Marks)**

c. Sketch a static CMOS gate computing $y = \overline{(A + B + C)D}$ **(04 Marks)**

Module-2

3 a. Explain CMOS nWell process with necessary diagrams. **(12 Marks)**

b. Mention different types of MOSFET capacitances with necessary diagrams and equations also MOSFET Capacitances in cut off, linear and saturation region. **(08 Marks)**

OR

4 a. Define scaling. Explain constant field scaling and constant voltage scaling and why constant voltage scaling is usually preferred over full scaling. **(07 Marks)**

b. With neat diagram, explain the Lambda based design rules for two metal layers. **(06 Marks)**

c. Draw the layout for $f = \overline{ABC}$ and estimate the cell area. **(07 Marks)**

Module-3

5 a. Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit in vertex. **(06 Marks)**

b. Estimate t_{pdr} and t_{pdf} for the 3 input NAND gate shown in Fig.Q.5(b) if the output is loaded with h identical NAND gates. **(08 Marks)**

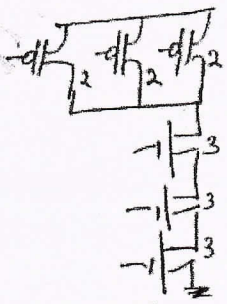


Fig.Q.5(b)

c. Explain eVSL with an example. **(06 Marks)**

6 a. Explain: i) Pseudo-nMOS ii) Ganged CMOS with necessary circuit examples. **(06 Marks)**

OR

b. If a unit transistor has R = 10KΩ and c = 0.1fF in a 65nm process, compute the delay, in picoseconds, of the inverter Fig.Q.6(b) with a fan out of h = 4. **(06 Marks)**

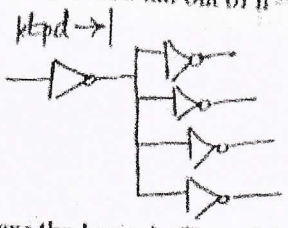


Fig.Q.6(b)

c. Explain linear delay model compare the logical effort of the following gates with the help of schematic diagrams: i) 3-input NAND gate ii) 3 input NOR gate. **(08 Marks)**

Module-4

7 a. Explain Resettable latches and flipflops using CMOS transmission gate. **(06 Marks)**

b. Explain Dynamic logic. **(06 Marks)**

c. Consider the two nFET chain in Fig.Q.7(c). The power supply is set to a value of V_{DD} = 3.3V and the nFET threshold voltage is V_{Tn} = 0.55V. Find the output voltage V_{out} at the right side of the chain for the following values: i) V_{in} = 2.9V ii) V_{in} = 3.0V iii) V_{in} = 1.4V iv) V_{in} = 3.1V **(08 Marks)**

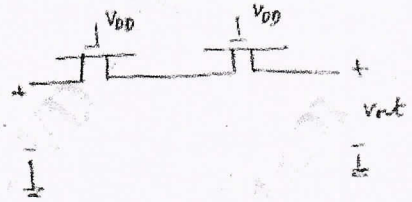


Fig.Q.7(c)

OR

8 a. Explain pulsed latches with schematic and waveforms. **(06 Marks)**

b. The output of an nFET is used to drive the gate of another nFET as shown in Fig.Q.8(b). Assume that V_{DD} = 3.3V and V_{tn} = 0.6V. Find the output voltage V_{out} when the input voltages are at following values:

i) V_a = 3.3V and V_b = 3.3V

ii) V_a = 2.0V and V_b = 2.5V.

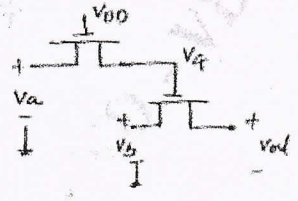


Fig.Q.8(b)

(08 Marks)

c. Explain Domino logic. **(06 Marks)**

Module-5

9 a. With neat schematic diagram explain the operation of Full CMOS static RAM cell. **(10 Marks)**

b. Explain the different fault models. **(10 Marks)**

OR

10 a. With neat schematic diagram explain the operation of three transistor DRAM cell. **(10 Marks)**

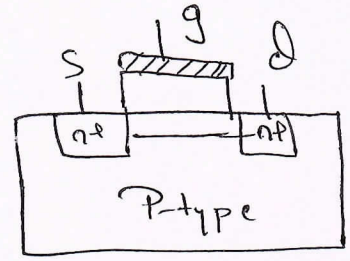
b. Write short notes on: i) Built in Self Test ii) Scan Design. **(10 Marks)**

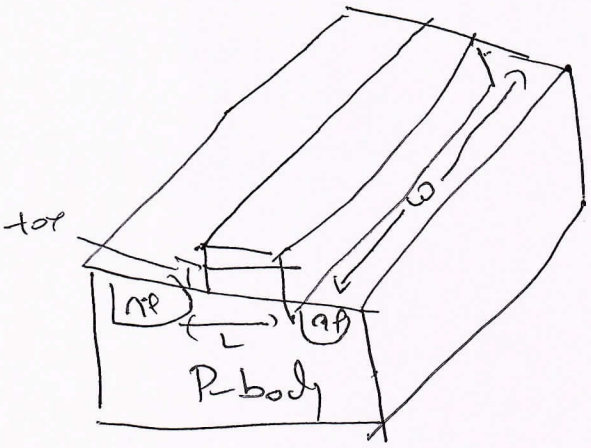
* * * * *

module-1

1 a] Derive an expression for drain current in linear and Saturation region — 8m

Ans -





Linear region / non-Saturated region

$$Q = CV = C_g V_{gs}$$

$$Q_{channel} = C_g\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)$$

$$C_g = \frac{\varepsilon_{ox} WL}{t_{ox}} = C_{ox} WL$$

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$$\mathcal{E} = \frac{V_{ds}}{L} \text{ and } T = \frac{L}{\mu \frac{V_{ds}}{L}}$$

$$I_{ds} = \frac{Q_{channel}}{T} = \frac{C_g\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)}{\frac{L}{\mu \frac{V_{ds}}{L}}} \quad — (2m)$$

$$\boxed{I_{ds} = \frac{\mu C_{ox} W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}} \rightarrow \text{current in linear region}$$

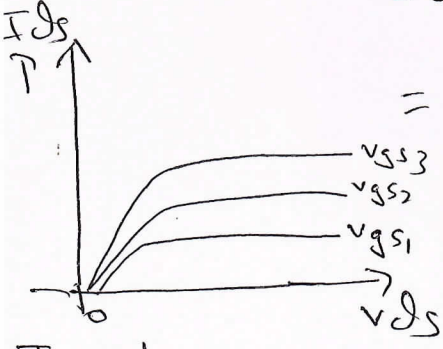
— (2m)

In Saturation region Substitute $(V_{ds} = V_{gs} - V_t)$

$$I_{ds} = \frac{\mu C_{ox} W}{L}\left[V_{gs} - V_t - \frac{(V_{gs} - V_t)}{2}\right](V_{gs} - V_t)$$

$$= \frac{\mu C_{ox} W}{L}\left(\frac{V_{gs} - V_t}{2}\right)^2 = \boxed{\frac{B}{2}(V_{gs} - V_t)^2}$$

Saturation current — (2m)

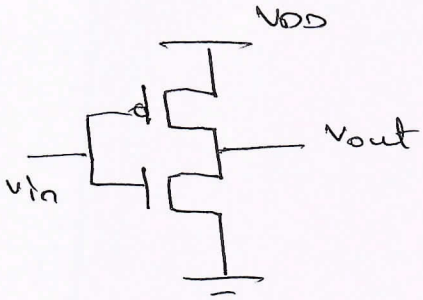


I-V characteristics — (2m)

1b) Draw the Cmos inverter ckt and explain its DC characteristic – 8m

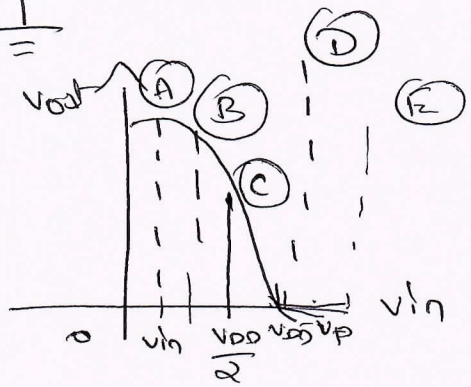
~~1b~~ Cmos Inverter

Ans



$V_{gsn} = V_{in}$, $V_{gsp} = -(V_{DD} - V_{in})$ – (1m)

$V_{dsn} = V_{out}$, $V_{dsp} = (V_{DD} - V_{out})$ – (1m)

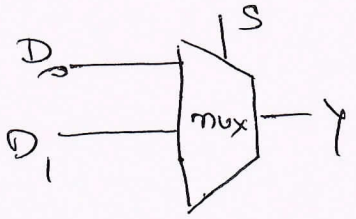


explanation – (3m)

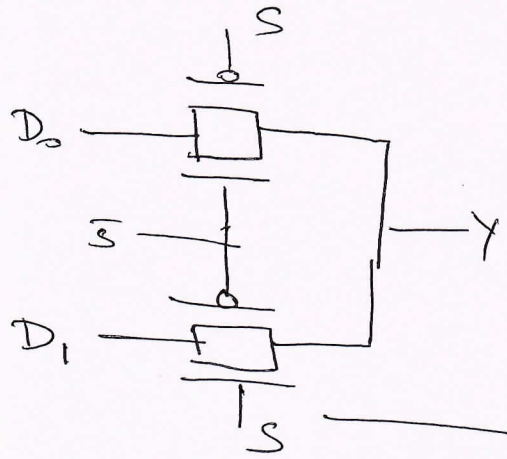
V_{TC} – (3m)

1c] Implement a 2:1 mux using transmission gate – 4m

Ans



S	Y
0	D_0
1	D_1



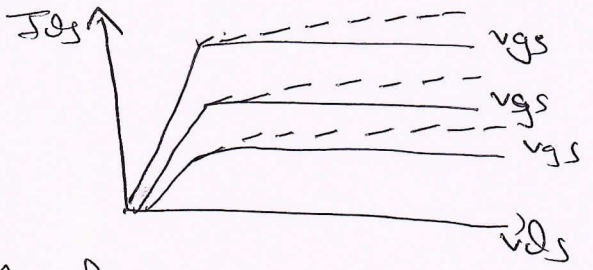
Explanation → (2m)

→ (2m)

2a] Explain the non-ideal IV effect of MOSFET with respect to CMOS channel length modulation and mobility degradation. — 8m

= Channel length modulation

From the I-V characteristics, when V_{ds} is greater than or equal to $V_{gs}-V_{th}$, the MOSFET becomes saturated, as shown below



$L_{eff} = L - L_D$

$$I_{ds} = \frac{B}{2} V_{GT}^2 \left(1 + \frac{V_{ds}}{V_A}\right) \quad -(2m)$$

See for the given value of V_{gs}, even if V_{ds} is increased beyond $V_{gs}-V_t$, the drain current (I_D) remains constant

But in reality, if V_{ds} is increased beyond $V_{gs}-V_t$, the drain current (I_D) increase slightly, this phenomenon is called as "channel length modulation" — (2m)

(represented by dotted line in graph)

Mobility degradation

With

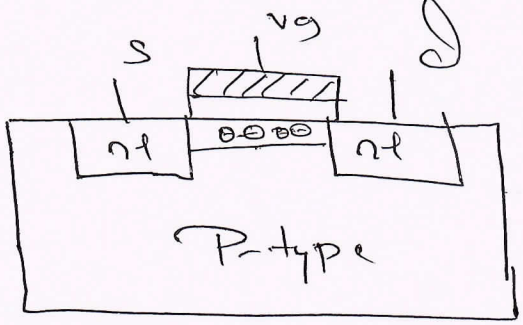
$V = \mu E$

v - velocity

μ - mobility

E - Electric field.

As we increase V_{gs}, there will be more number of electrons attracted towards the channel. As the channel length is less & more electrons are getting accumulated. In the channel, the mobility electrons gets degraded because of collission This effect is called mobility degradation (2m)

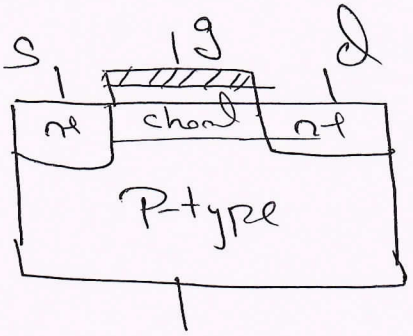


$\mu_{eff-p} = \frac{1.85\ cm^2/V\text{-}S}{1 + |V_{gs}| + 1.5|V_{th}|}$ $0.388\ V/nm\ t_{ox}$ (1m)

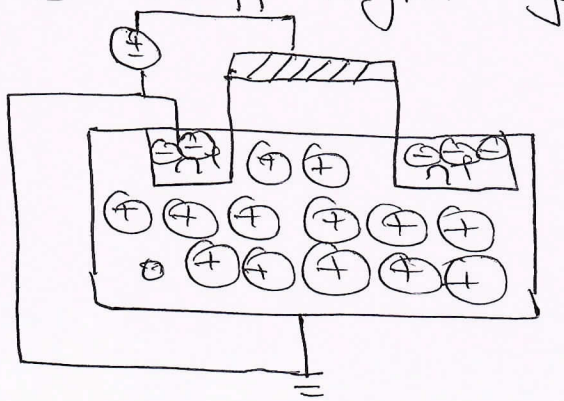
$\mu_{eff-n} = \frac{S_{no}\ cm^2/V\text{-}S}{1 + \left[\frac{V_{gs} + V_t}{0.054\ V/nm\ t_{ox}}\right]^{1.55}}$ (1m)

2b] Explain the operation of nMos transistor with I-V characteristics- (8M)

= consider the nmos with p-substrate



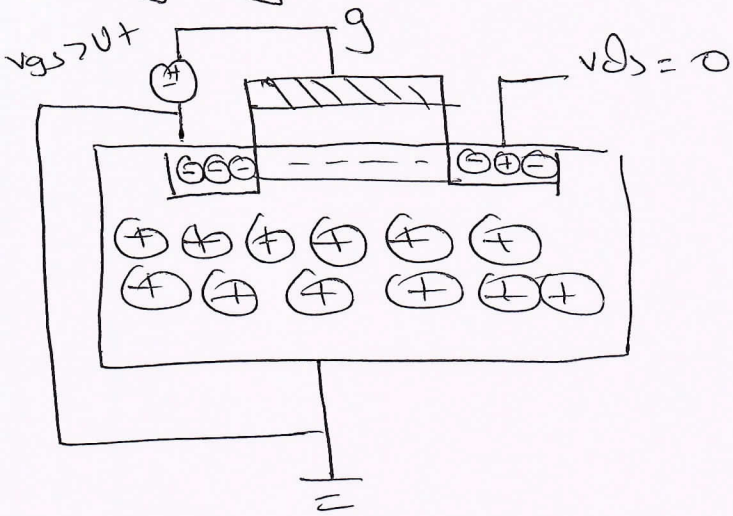
Case 1] cutoff region $V_{gs} < V_t$ (3m)



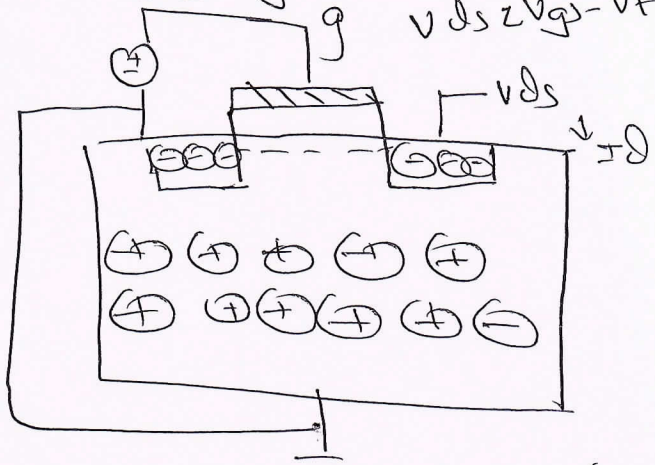
Ids = 0

explination

case ii] $V_{gs} > V_t$ and $V_{ds} \geq 0$

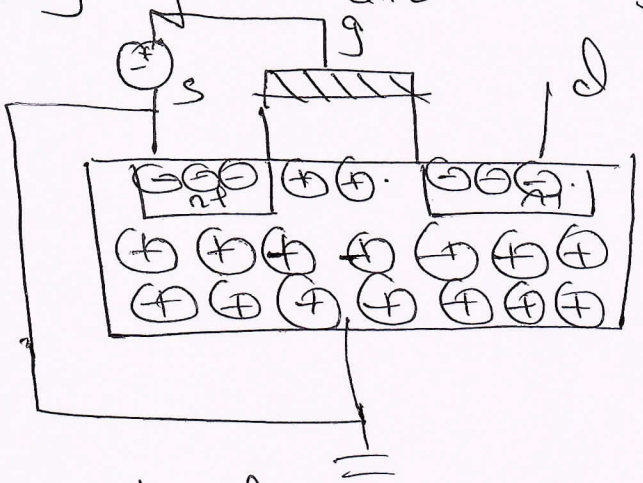


case iii] $V_{gs} > V_t$ and $V_{ds} \geq V_{gs} - V_t$



I_{ds} Increase with V_{ds} — (2 m)

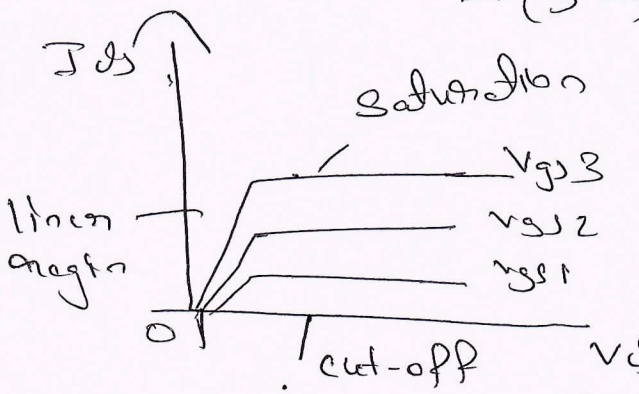
case iv] $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$



Channel pinches off

I_{ds} independent of V_{ds}

— (3 m)



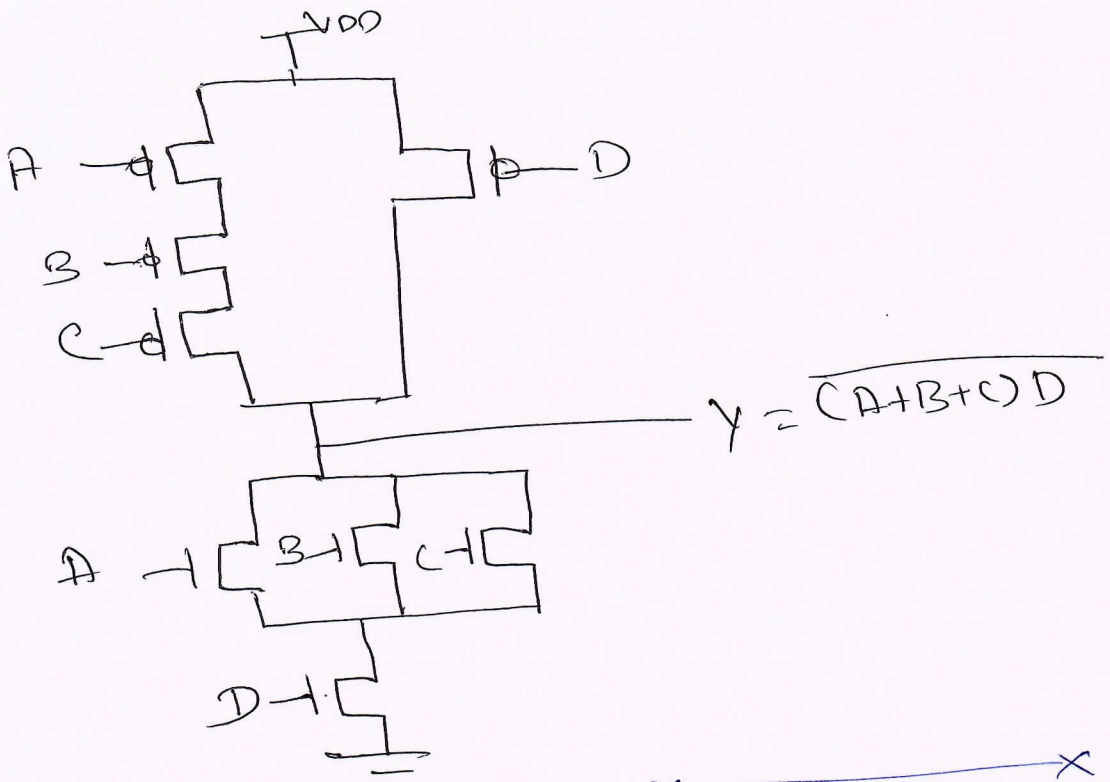
I-V characteristics of n-mos transistor

2] Sketch a Static cmos gate computing $y = \overline{(A+B+C)D}$ (4 m)

P.T.O

2 c]

=



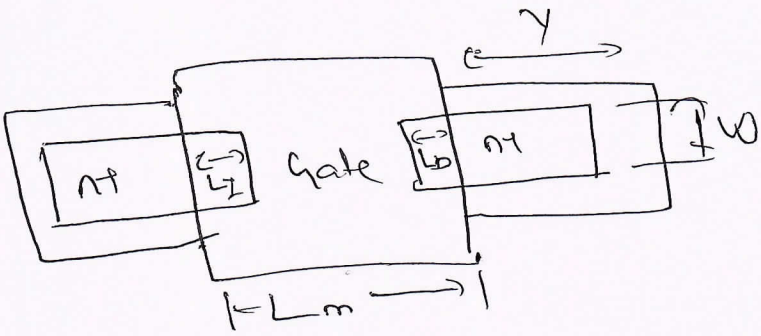
module-2

3 a] explain cmos n-well process with necessary diagram (12m)

= following steps -

- n-well formation (n-well mask)
- gate formation (polysilicon mask)
- n^+ diffusion regions (n^+ diffusion mask)
- Definition of p^+ regions (p^+ diffusion mask)
- Contact cut defination (Contact mask)
- metallization (metal mask) — 06 × 02 m each

3b] mention different types of MOSFET Capacitance with necessary diagram and equations also MOSFET Capacitance in cutoff, linear and Saturation region – (8m)



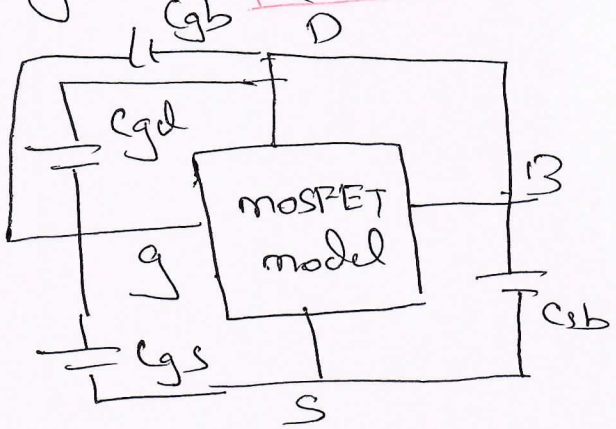


Diagram – (4m)

explanation of oxide related Capacitance with Cgb Cgs & Cgd, Cgr equation
└ (2m)

explanation of junction capacitance with five junction capacitance indication
└ (2m)

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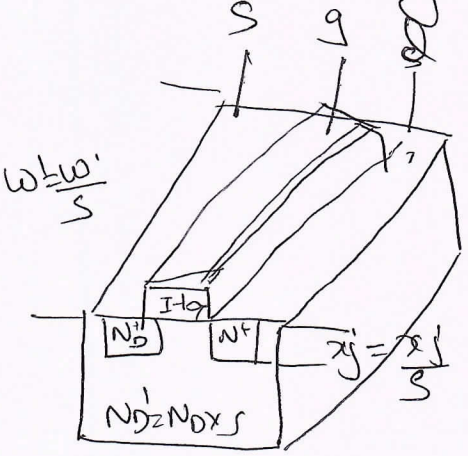
4 a] Define Scaling, explain constant field Scaling and constant voltage Scaling and why constant voltage Scaly is usually preferred than over full Scaly – (7m)



Definition of Scaling and diagram – (2m)

Constant field scaling

Current

$$I_D' = \frac{k_n'}{2}\left[2(V_{GS}' - V_{TS}')V_{DS}' - V_{DS}'^2\right]$$

$$= \frac{Sk_n}{2}\frac{1}{S^2}\left[2(V_{GS} - V_T)(V_{DS} - V_{DS}^2)\right]$$

$$I_{D(lin)}' = \frac{k_n}{S \cdot 2}\left[2\cdot(V_{GS} - V_{T_0})(V_{DS} - V_{DS}^2)\right] = \boxed{\frac{I_{D(lin)}}{S}}$$

Power :- $P = I_D \cdot V_{DS}$

$$P' = I_D' V_{DS}' = \frac{I_D}{S}\cdot\frac{V_{DS}}{S}$$

$$\boxed{P' = \frac{P}{S^2}}$$

$$\text{Current density} = \frac{I_D}{A_{rea}} = \frac{I_D'}{A_{rea}'} = \frac{\frac{I_D}{S}}{\frac{L}{S}\cdot\frac{L}{S}} = \frac{I_D \times S}{A_{rea}}$$

$$\boxed{J' = JS}$$

$$\text{Power density} = \frac{P'}{A_{rea}} = \frac{\frac{P}{S^2}}{\frac{A_{rea}}{S^2}} = \boxed{\frac{P}{A_{rea}}} \quad \text{(3m)}$$

Constant voltage Scaling

$$\text{Current} = I_D'(lin) = \frac{k_n'}{2}\left[2(V_{GS}' - V_{TS}')\cdot V_{DS}' - V_{DS}'^2\right]$$

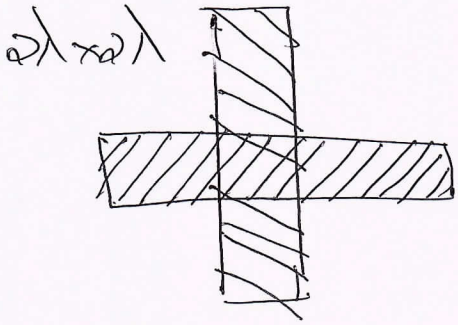
$$I_D' = \frac{S\cdot k_n}{2}\left[2(V_{GS} - V_{T_0})\cdot V_{DS} - V_{DS}^2\right] = \boxed{S\, I_{D(lin)}}$$

$$\text{Current density} = \frac{I_D'}{A_{rea}} = \frac{S\cdot I_D}{\frac{A_{rea}}{S^2}} = \boxed{\frac{S^3 I_D}{A_{rea}}}$$

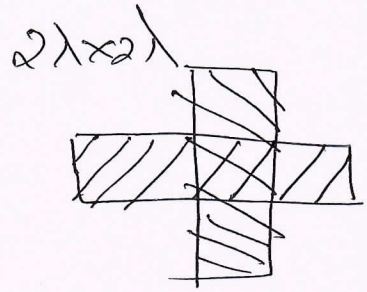
$$\text{Power density} = \frac{P'}{A_{rea}} = \frac{I_D' V_{DS}'}{A_{rea}'} = \frac{S\, I_D V_{DS}}{A_{rea}\, S^2} = \boxed{\frac{S^3 P}{A_{rea}}} \quad \text{(3m)}$$

(4b)

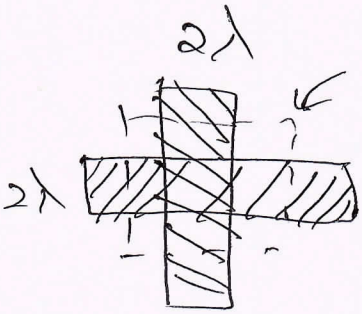
6 m



nmos enhancement

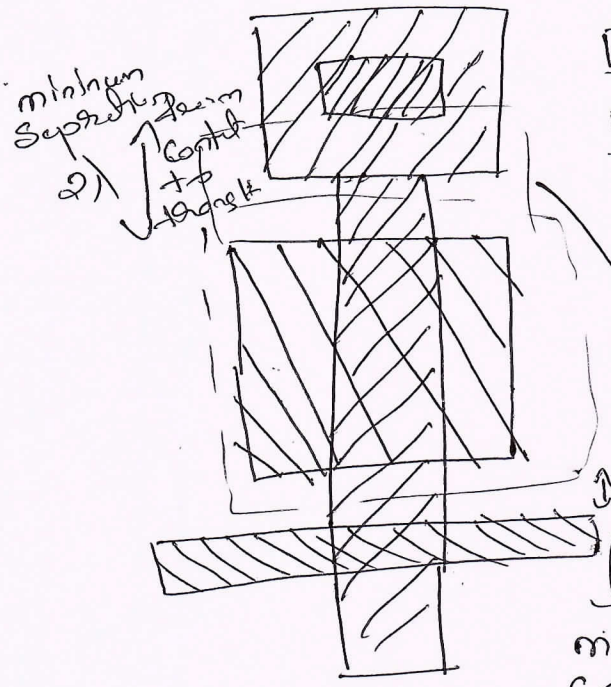


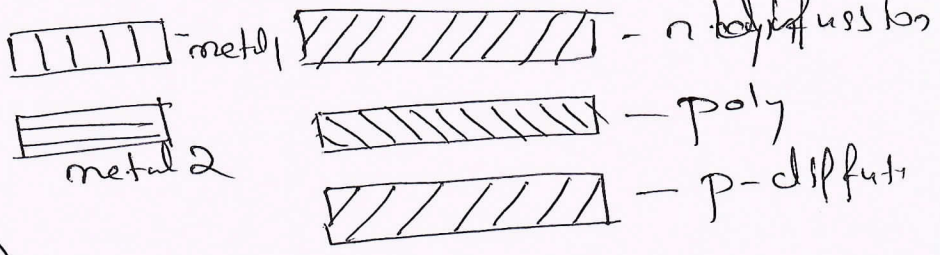
Pmos enhancement



nmos depletion

-(2 m)





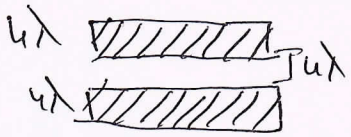
implant for an nmos depletion mode transistor to extend 2λ minimum 2λ beyond channel in all direction

minimum Seperation from implant to another transistor

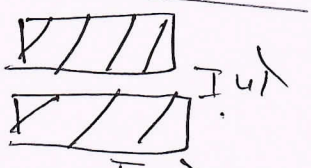
-(2 m)

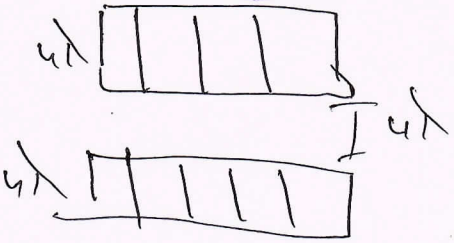
minimum width and minimum Seperation

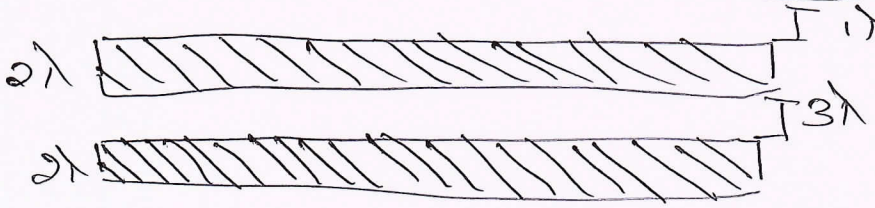
minimum width



minimum Seperation

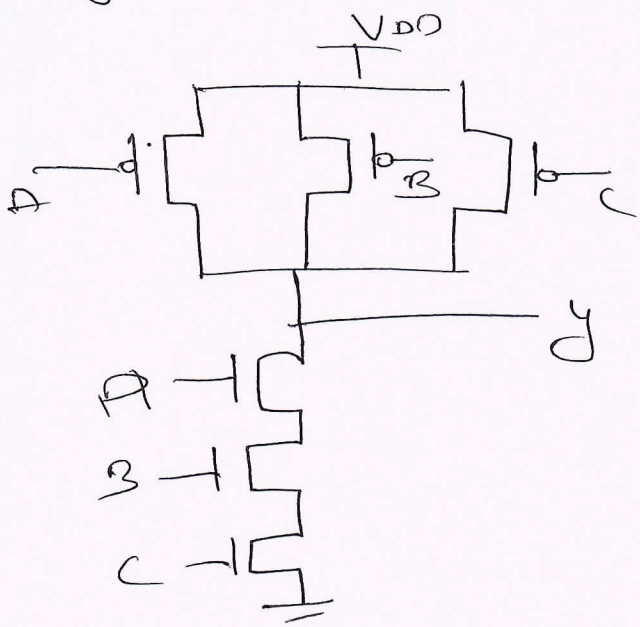




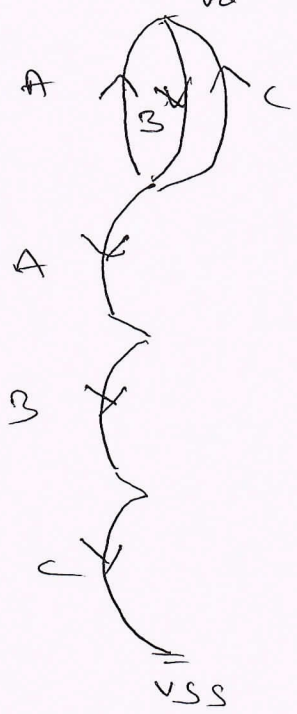


-(2 m)

4c] $y = \overline{ABC}$

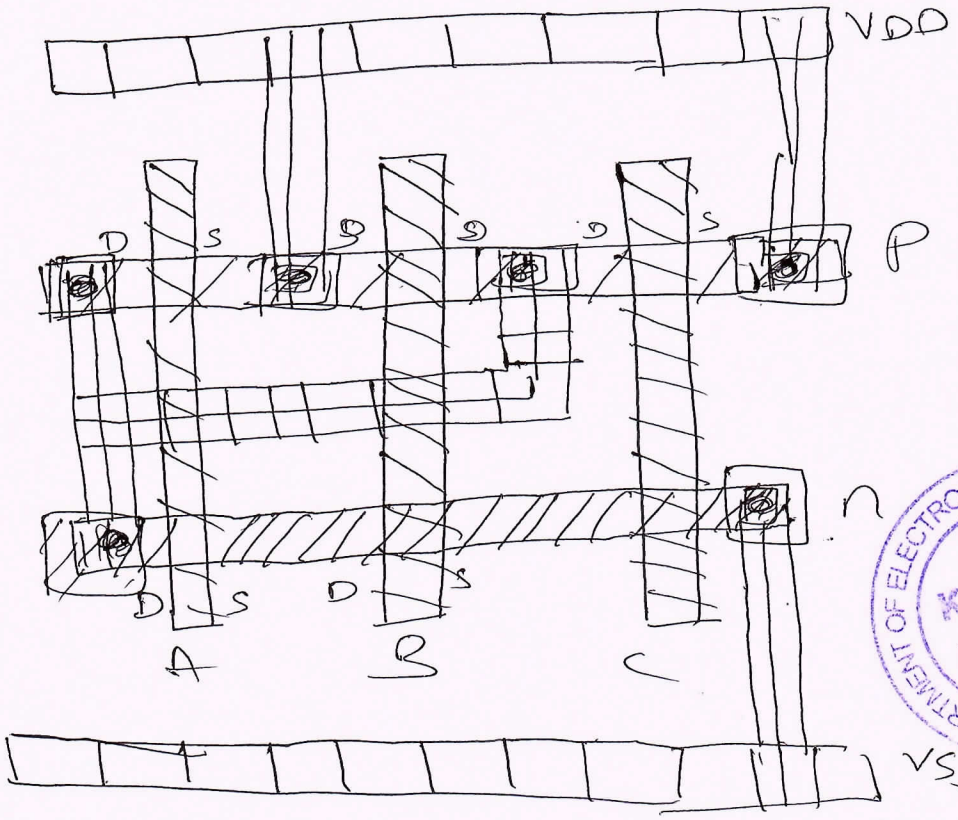


Euler graph



(7 m

(3 m)



(3 m)

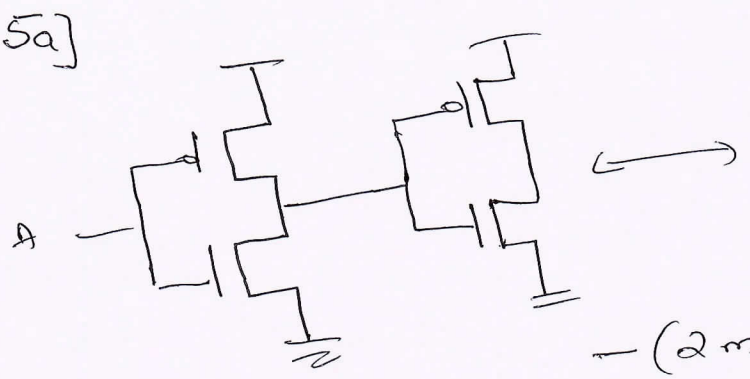
Area = Height = $(4+1) * 8\lambda = 5 \times 8\lambda = 40\lambda$

width = $4 * 8\lambda = 32\lambda$

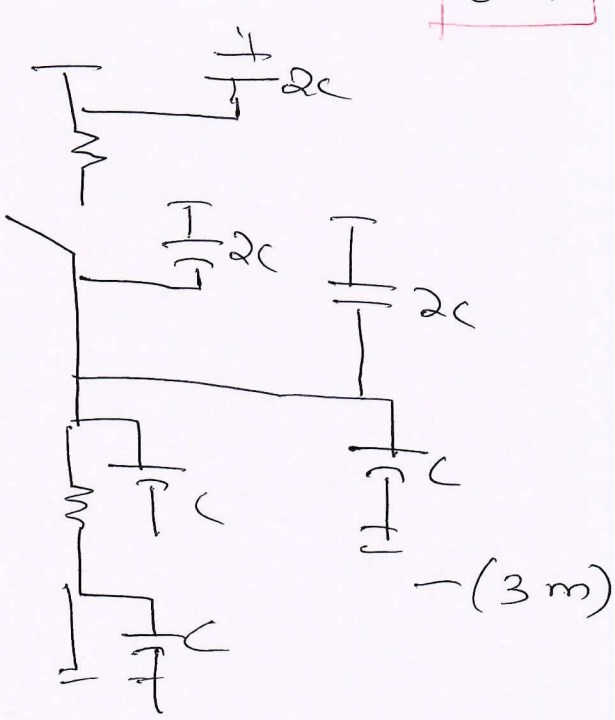
module - 3

6 m

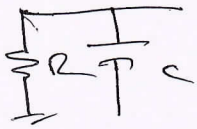
5a]



– (2 m)



– (3 m)



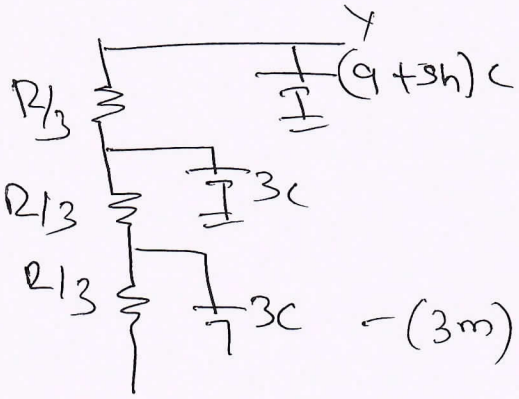
– (1 m)

5 b] $t_{pdf} = (3c)\left(\frac{R}{3}\right) + (3c)\left(\frac{R}{3}+\frac{R}{3}\right) + (9+5h)c\left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)$

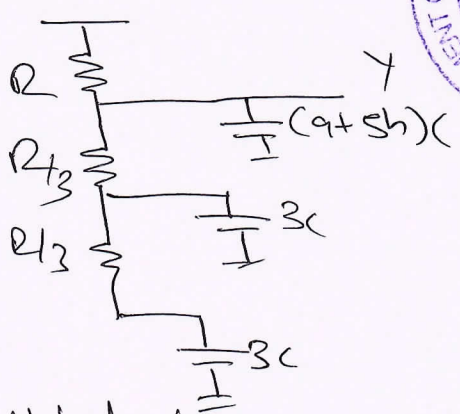
8 m

$= 12 + 5hRc$

$t_{pdp} = (15+5h)Rc$ – (2 m)



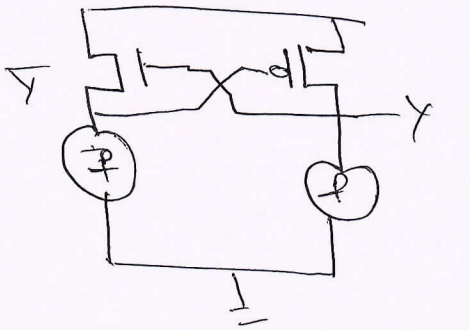
– (3m)

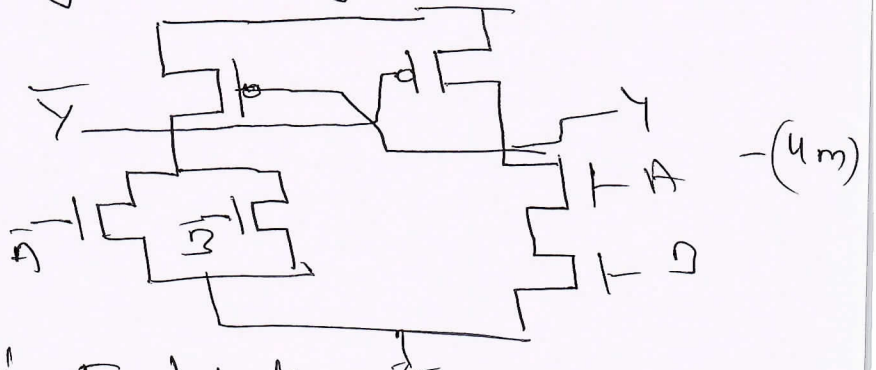


– (3m)

5 c] CVSL cascade voltage switch logic

6 m





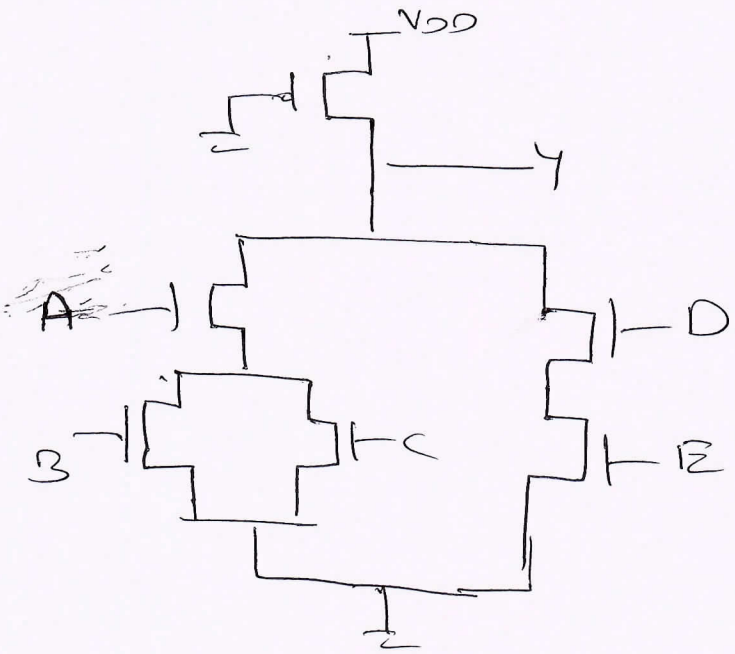
– (4m)

+ ~~Explan~~ Explanation – (2 m)

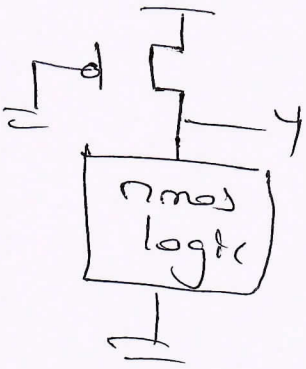
6] a) pseudo nmos — (6m)

A modified version of cmos technology is known as pseudo nmos, in which pmos is used as load instead of depletion mosfet

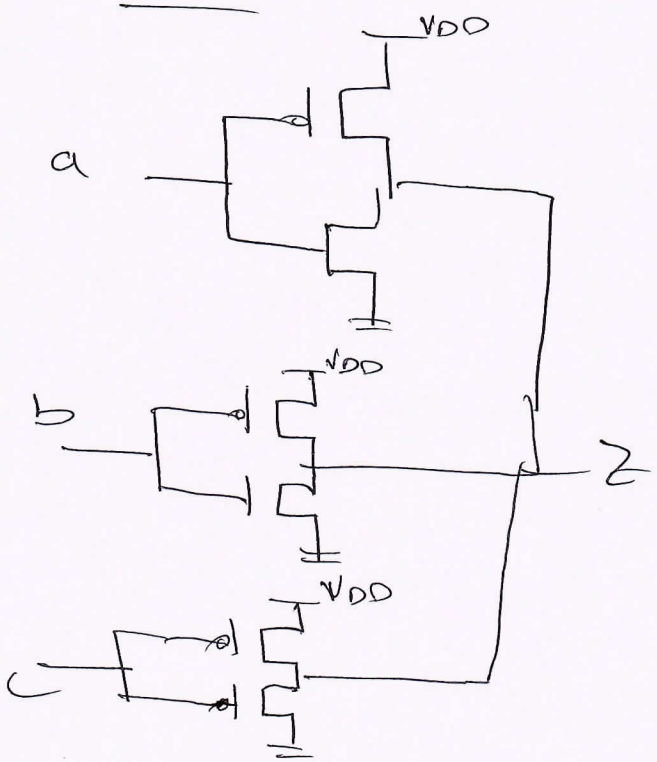
$Y = \overline{A(B+C)+DE}$ — (3m)



general form



general cmos



— (3m)

Bdriven >1 $Z = \overline{a+b+c}$

Blow

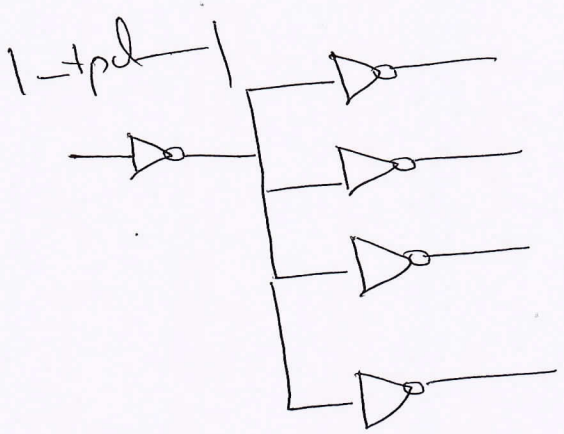
Bdriven <1 $Z = \overline{abc}$

Blow

explanation

6b)

6 m



-(1 m)

RC product in 65nm process is

RxC -(1 m)

$= 10k \times 0.1fF$

$= 1ps$

Fan out is equal to 4

∴ delay is $(3+3h)RC$ -(2m)

$= (3+3\times4) \times 1ps$

$= 15ps$ -(2m)

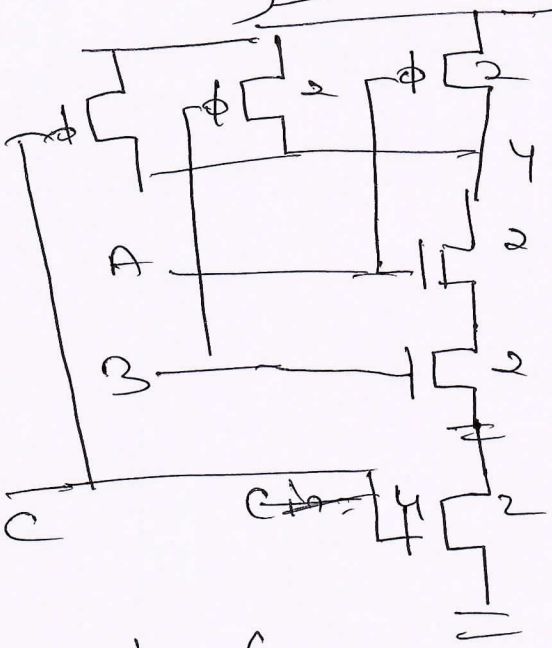
– (8m)

6c]

Explanation of linear delay model with the equation. $d = f + p$ – (2m)

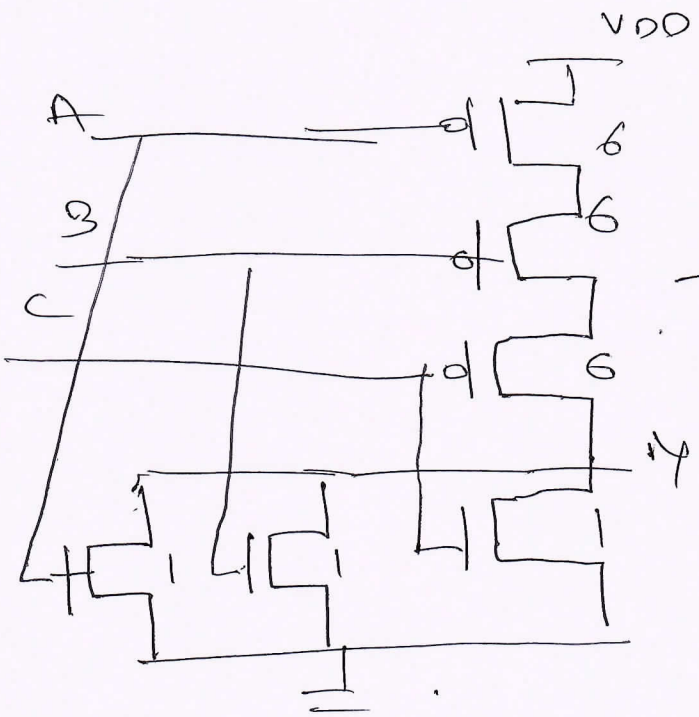
logical effort computation

2 i/p NAND



Cin = 6

3 i/p NOR



– 2m

logic effort $g = \frac{6}{3}$

3 i/p NAND – (2m)

Cin = 7

logic effort

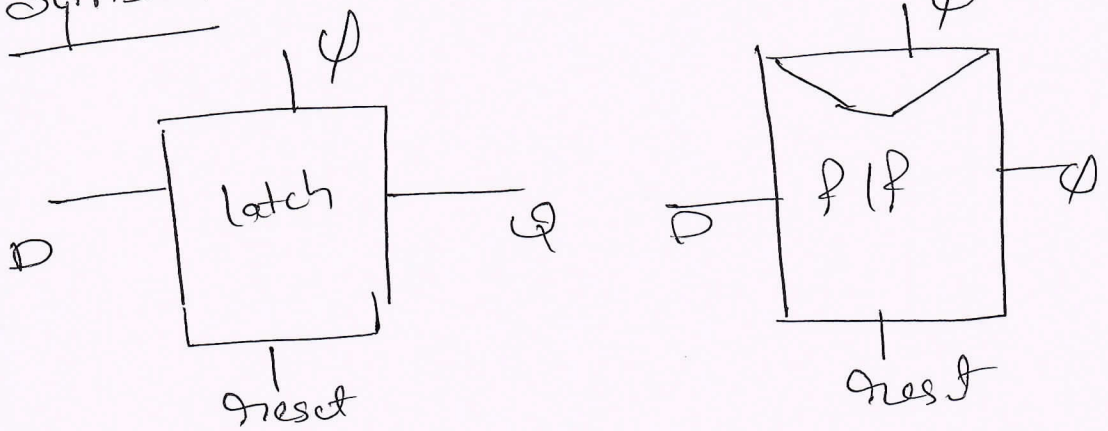
3 i/p NOR = $g = \frac{7}{3}$.

– (2m)

module - 4 -(6m)

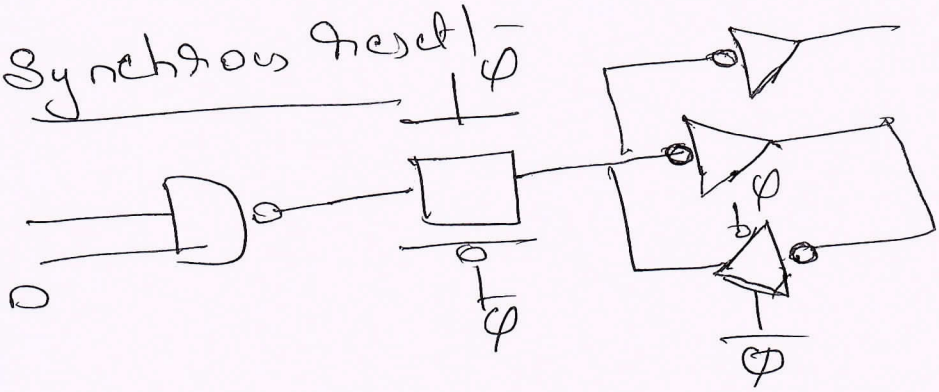
7 a) -(1m)

Symbol



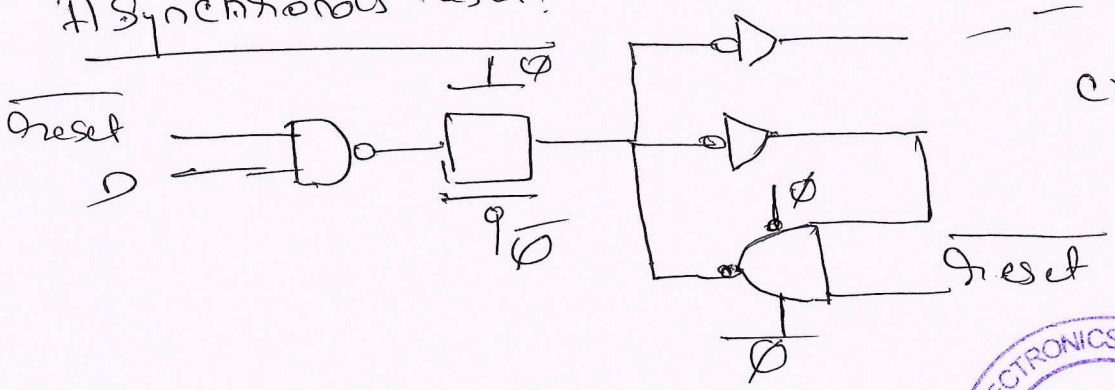
Synchronous reset — definition } - 1m
Asynchronous reset — definition

Synchronous reset!-



-(1m)
explanation
-(1m)

Asynchronous reset!-



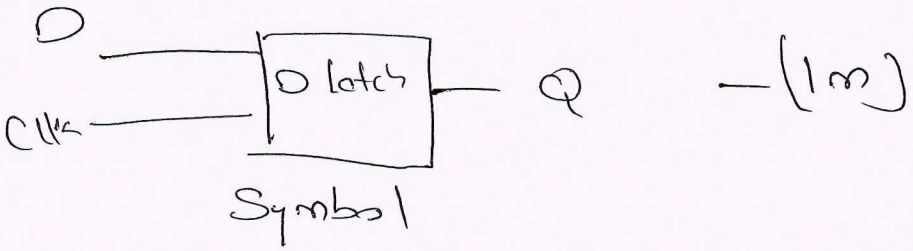
-(1m)
explanation
-(1m)

7 b] (6m)

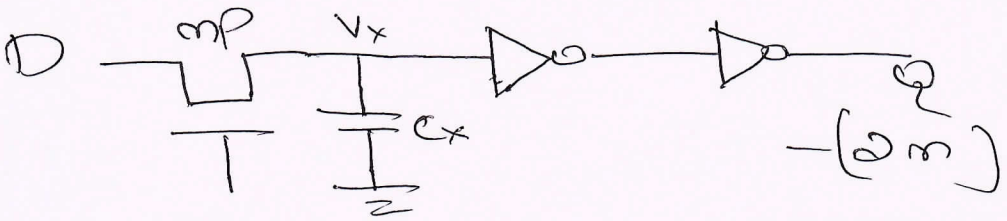
Dynamic logic implementation offers lower power consumption than Static logic implementation —(1m)

example for Dynamic logic ckt

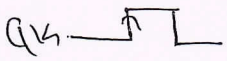
Dynamic D latch ckt.



Symbol —(1m)



—(2m)



explanation —(2m)

7 c) $V_{out(max)} = V_{DD} - V_{tn}$ (8m)

Case 1] $V_{in} = 2.9$, $V_o = 3.3 - 0.55 = 2.75V$

Case 2] $V_{in} = 3$, $V_o = 3.3 - 0.55 = 2.75V$

Case 3] $V_{in} = 1.4$ $V_o = V_{in} = 1.4V$

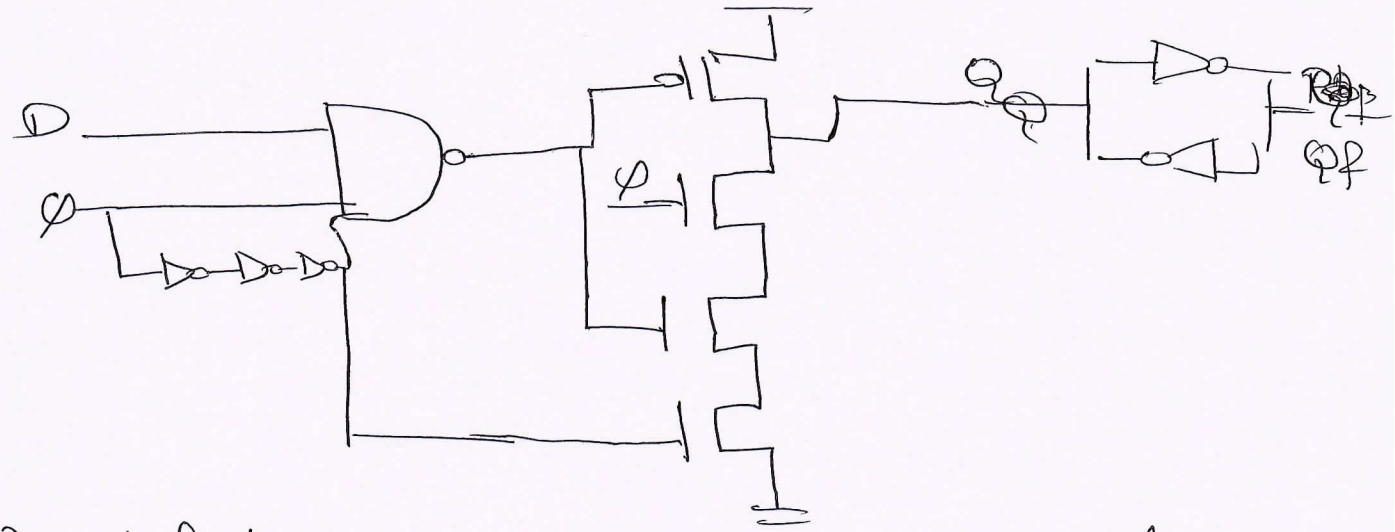
Case 4] $V_{in} = 3.1$ $V_o = V_{DD} - V_{Tn} = 2.75V$

} 2m each

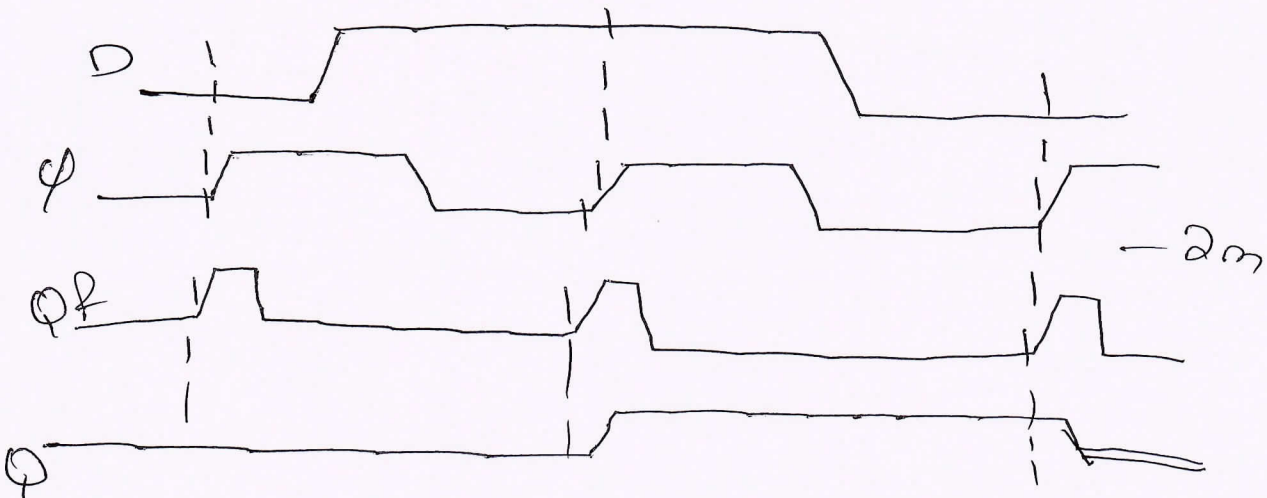
PTO

8a] Pulsed latches — (6m)

— 2m



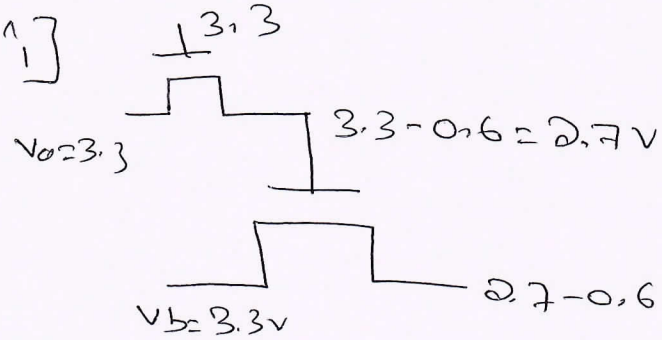
A pulsed latch can be built from a conventional cmos transparent latch driven by a brief clk pulse — 1m



— 2m

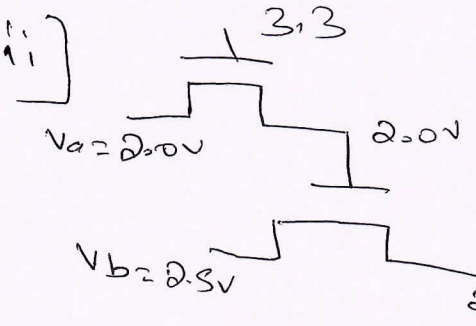
explanation — (1m)

8.b] 8m

i] 

-(4m)

Vout = 2.1V

ii] 

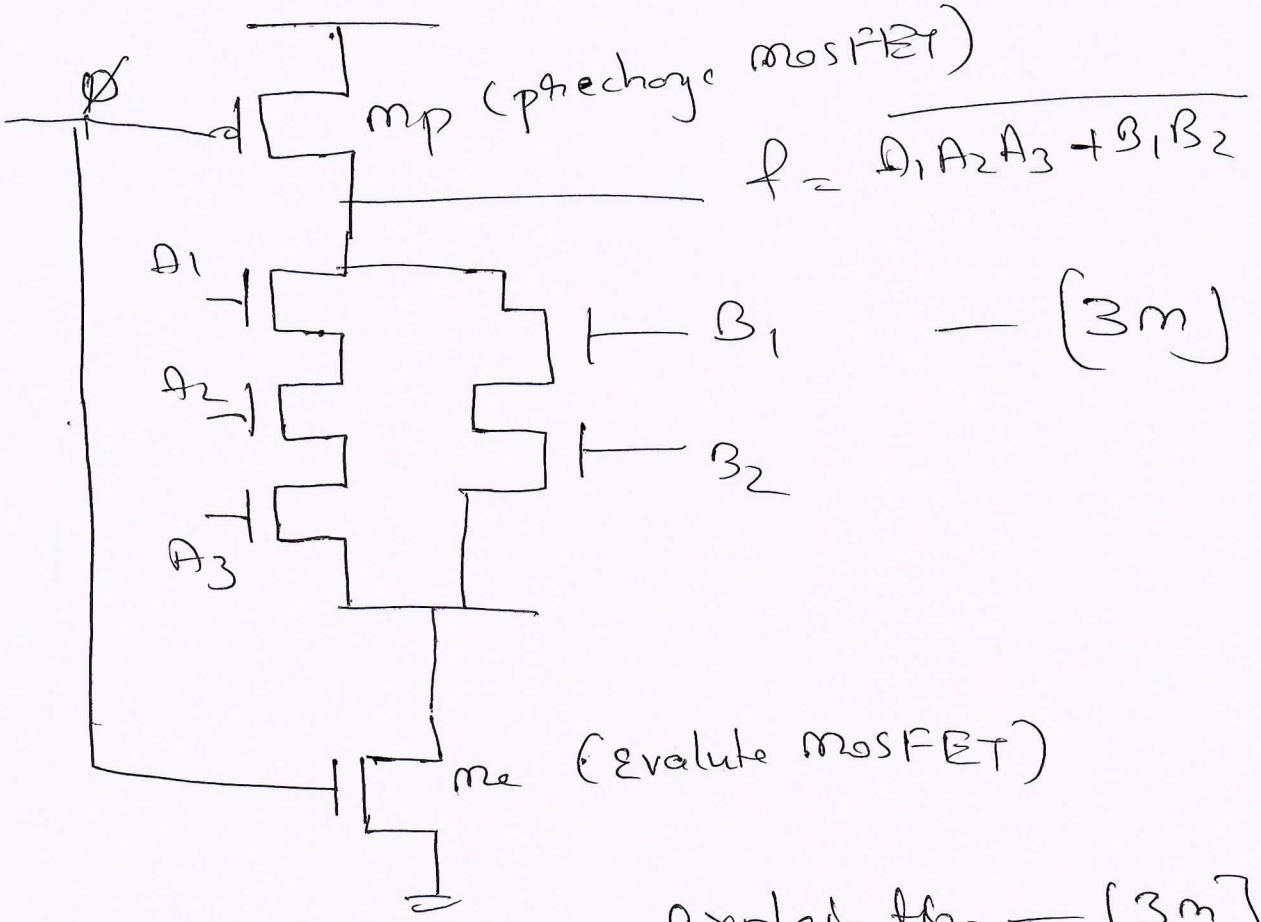
-(4m)

Vout = 1.4V

[6m]

8c] let us consider a dynamic cmos logic gate which implement the function

$$f = \overline{A_1A_2A_3 + B_1B_2}$$



— [3m]

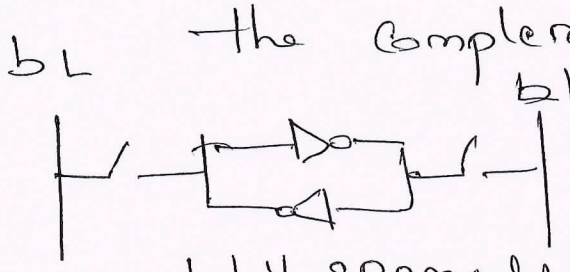
explaination — [3m]

module-5

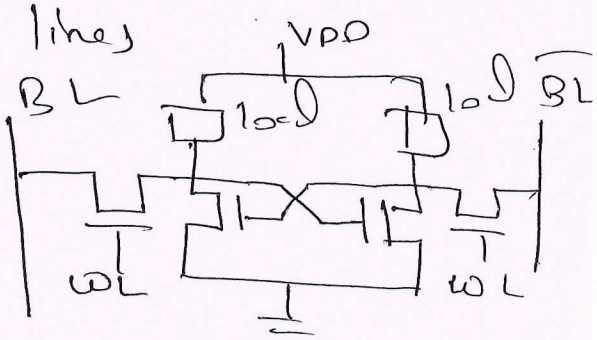
10m

9a] SRAM memory ckts are designed to permit the modification of data bits to be stored in array as well as retrieved on demand. Depending on the preserved state of the two inverter latch ckt, the data being held in the memory cell will be integrated either as logic one) —2m

Usually two nmos pass transistor are implemented to connect the 1-bit SRAM cell to the complementary lines



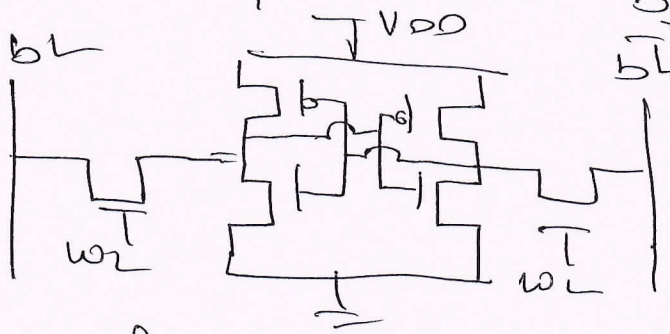
1-bit SRAM cell



a) Symbolic representation

b) gate ckt

—5m



full cmos SRAM cell

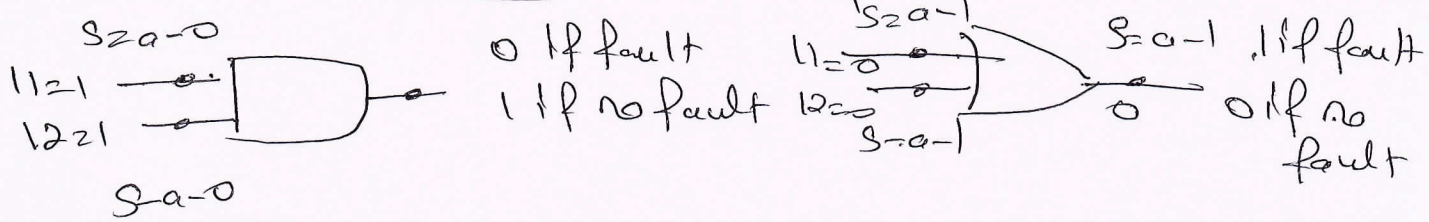
Explanation of all three fig —3m

9b) — 10m

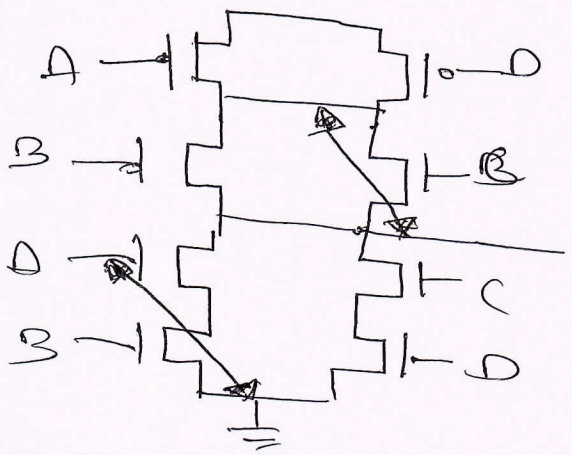
Fault models

- In order to determine good and bad parts in a chip. It is necessary to propose a fault model. This model will help to know where and how fault occur, what is their impact on ckt. The most popular model is called the Stuck-At model. The short ckt / open ckt. is another model can be a close fit to reality but this is difficult to implement

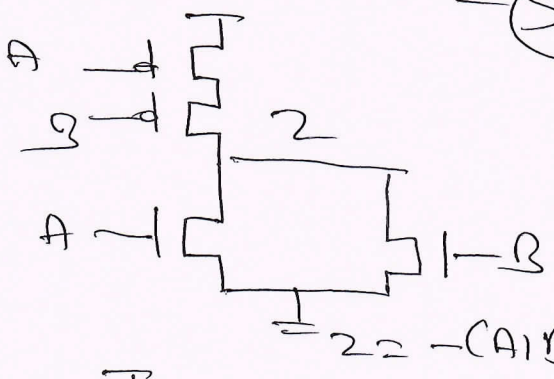
Stuck-At Faults — explanation (5m)

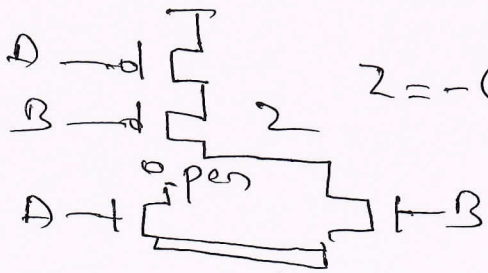


Short-ckt & open ckt fault:- explanation — (5m)



CMOS – Bridging faults

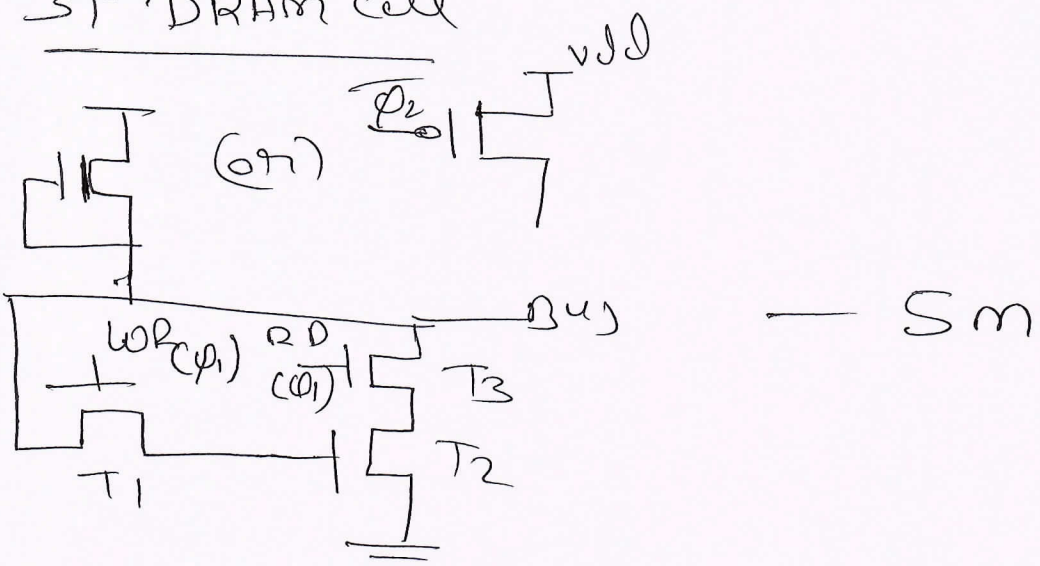




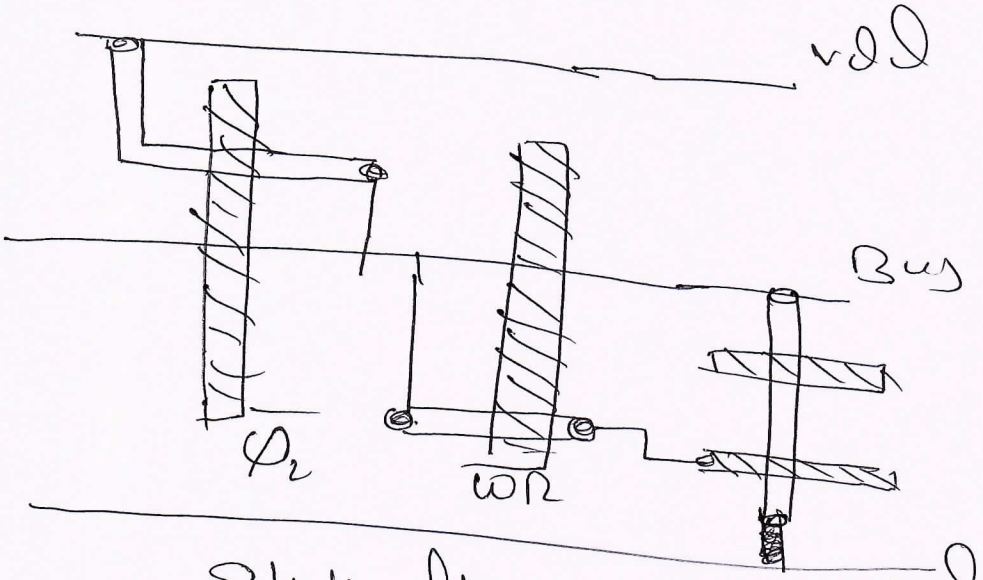
CMOS open fault that causes

10] a) — (10m)

3T DRAM cell



— 5m

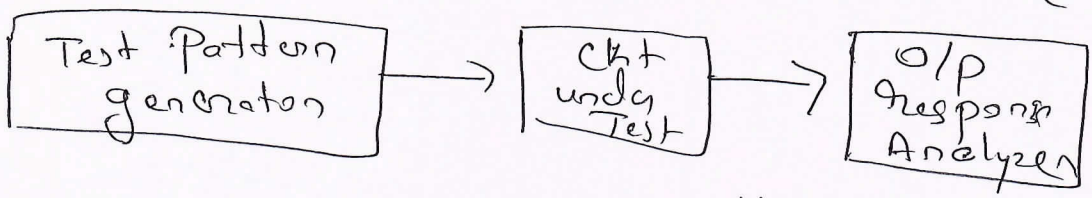


Stick digram of 3T-DRAM

explanation — (5m)

10] b] 1] Built in Self Test — [10m]

The Structure of BIST — [5m]



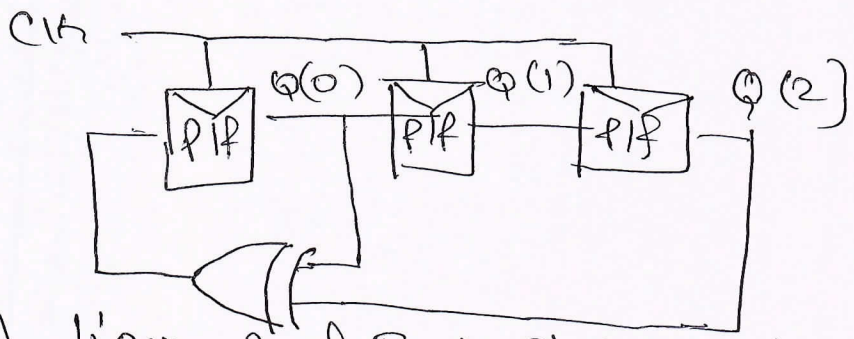
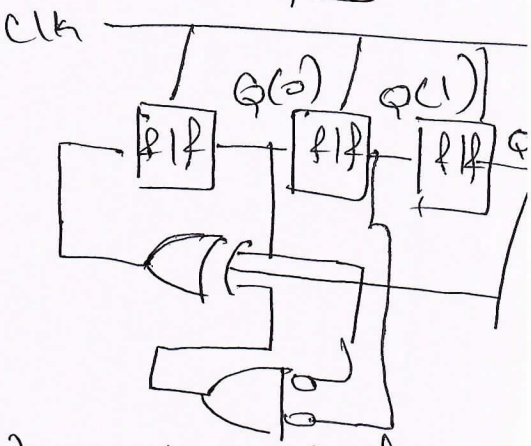


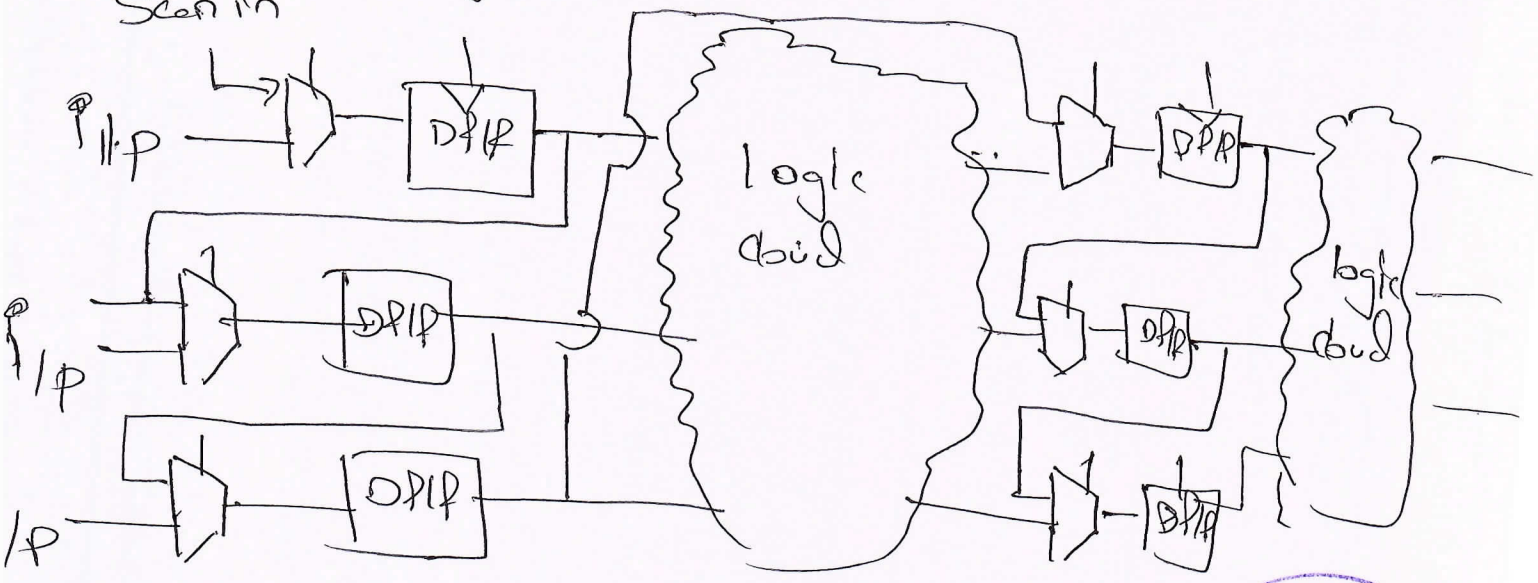
fig 1] liner feed Back Shift register [LFSR]



2] complete feedback shift register [CFSR]

explanation + Digram — [5m]

2] Scan Design



explanation + Digram — (5m)