CBCS SCHEME

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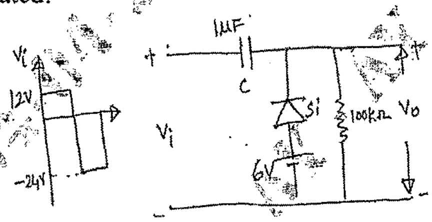
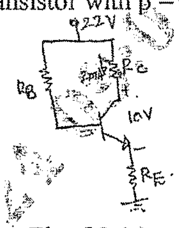
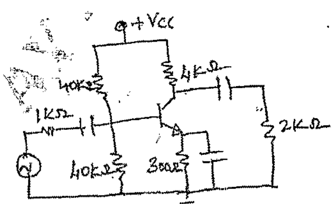
BEE303

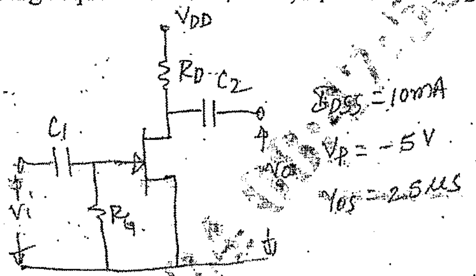
Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With circuit diagram and waveform, explain Full Wave Bridge rectifier.	6	L2	CO1
	b.	Explain the analysis of Double end clipper circuit which clips both the peaks of an sinusoidal AC signal.	7	L4	CO1
	c.	For the circuit shown in Fig. Q1 (c) analyze and plot the waveform for V_0 for the input indicated.  Fig. Q1 (c)	7	L4	CO1
		OR			
Q.2	a.	What are the factors affect the stability of operating point in a transistor?	5	L1	CO1
	b.	Discuss the exact analysis of voltage divider bias to find I_B, I_{CQ}, V_{CEQ} and I_{CSat}.	7	L4	CO1
	c.	Design the values of R_B, R_E and R_C for the emitter bias circuit shown in Fig.Q2 (c). Assume silicon transistor with $\beta = 100$.  Fig. Q2 (c)	8	L3	CO1
		Module – 2			
Q.3	a.	Mention the advantages of h-parameters for transistor analysis.	5	L1	CO2
	b.	Discuss the analysis of single stage amplifier, frequency response.	7	L4	CO2
	c.	A transistor with $h_{ie} = 1.1\ K\Omega$, $h_{fe} = 50$, $h_{re} = 205 \times 10^{-4}$, $h_{Oe} = 25\ \mu A/V$ is connected in CE configuration given in Fig. Q3 (c). Calculate A_i, A_{is}, A_V, A_{VS}, R_i and R_O.  Fig. Q3 (c)	8	L3	CO2

		OR			
Q.4	**a.**	Obtain the expression for Miller effect capacitance.	6	L2	CO2
	b.	Explain the high frequency analysis of BJT amplifier.	7	L2	CO2
	c.	Determine the lower cut-off frequency for the emitter follower using BJT amplifier with $C_S = 0.1\ \mu F$, $R_S = 1\ K\Omega$, $R_1 = 12\ K\Omega$, $R_2 = 4\ K\Omega$, $R_E = 1.5\ K\Omega$, $C = 0.1\ \mu F$, $\beta = 100$, $V_{CC} = 15\ V$, $V_{BE} = 0.7\ V$, $r_0 = \infty$ and $h_{ie} = 1.04\ K\Omega$.	7	L3	CO2
		Module – 3			
Q.5	**a.**	With two stage cascaded amplifier, explain the need of cascading.	6	L2	CO3
	b.	Write a note on cascade connection.	6	L1	CO3
	c.	Explain the DC analysis of Darlington emitter follower.	8	L2	CO3
		OR			
Q.6	**a.**	What are the characteristics of negative feedback amplifiers?	6	L1	CO3
	b.	An amplifier has mid-band voltage gain of 1000 with $f_L = 50\,Hz$ and $f_H = 50\,kHz$, if 5% negative feedback is applied then calculate gain, f_L and f_H with feedback.	6	L3	CO3
	c.	Obtain expression for input and output resistance of voltage series amplifier.	8	L2	CO3
		Module – 4			
Q.7	**a.**	With waveforms, explain classification of power amplifiers.	6	L2	CO3
	b.	Derive an expression for second harmonic distortion using 2 point method for power amplifier.	6	L3	CO3
	c.	With circuit diagram and waveform, explain working of class B push pull amplifier. Also show that conversion efficiency is 78.5%.	8	L2	CO3
		OR			
Q.8	**a.**	With block diagram, explain the principle of working of an oscillator.	6	L2	CO3
	b.	Explain the principle of tuned oscillators. Also obtain expression for frequency of oscillations of Hartley oscillator.	6	L3	CO3
	c.	A quartz crystal has the following constants, $L = 50\ mH$, $C_1 = 0.02\ PF$, $R = 500\ \Omega$ and $C_2 = 12\ PF$. Determine the values of f_S and f_P. If the external capacitance across the crystal changes from 5 PF to 6 PF, find the change in frequency of oscillations.	8	L3	CO3
		Module – 5			
Q.9	**a.**	Give the comparison between BJT and MOSFET.	6	L2	CO3
	b.	Explain the construction and working of n-channel JFET.	7	L2	CO3
	c.	Obtain the expression for A_V, Z_i and Z_O for fixed bias common source amplifier using JFET.	7	L3	CO3
		OR			
Q.10	**a.**	Explain the characteristics of n-channel E-MOSFET. Also describe its working.	10	L2	CO3

	b.	Design the fixed bias FET common source amplifier shown in Fig. Q10 (b) to meet the following requirements. $A_V = 12$, $Z_i = 10\ M\Omega$, $V_{DD} = 40$ V.  Fig. Q10 (b)	10	L3	CO3

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Dec 2023 – Jan 2024

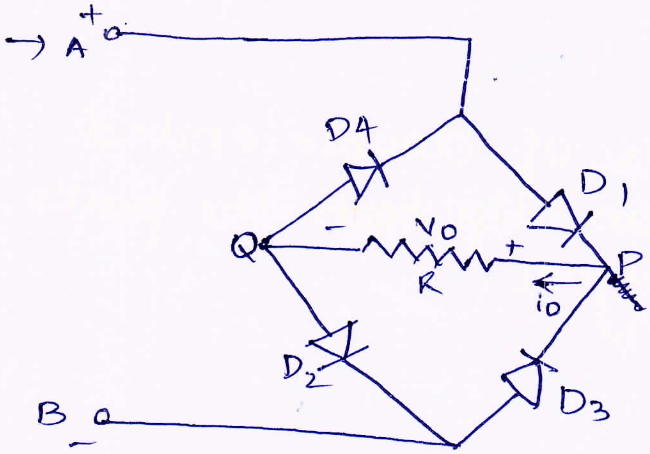
Analog Electronic Circuits

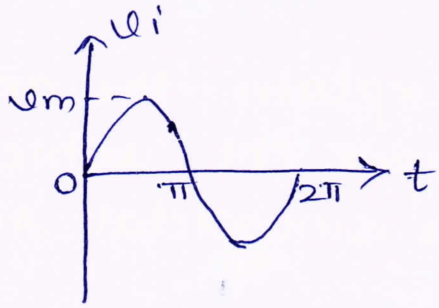
Sub Code : BEE303.

Semester : 3rd

Prepared By : Prof. Ravindra Motekar.

1a) With circuit diagram & waveform. Explain Full wave Bridge rectifier.





Applying KVL we get

$$v_i - V_K - v_o - v_K = 0$$

$$v_o = v_i - 2V_K$$

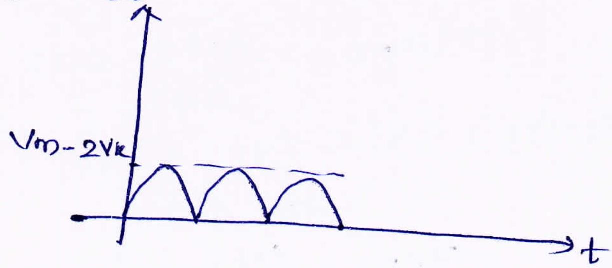
When v_i is at its peak value V_m, the peak level of V_o is.

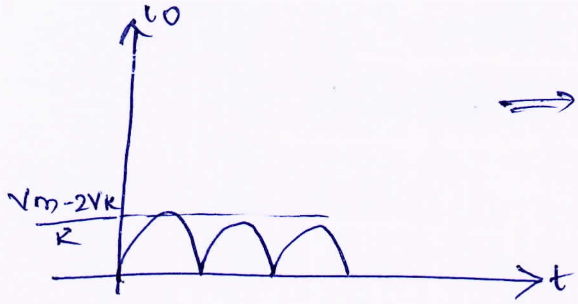
$$V_{om} = V_m - 2V_K$$

∴ o/p current is $i_o = \frac{V_m - 2V_K}{R} \sin\omega t$

or $i_o = I_o \sin\omega t$.

∴ o/p voltage





⟹ O/p current

WKT $V_{dc} = 0.636\,V_m$.

$\therefore I_{dc} = \frac{V_{dc}}{R}$

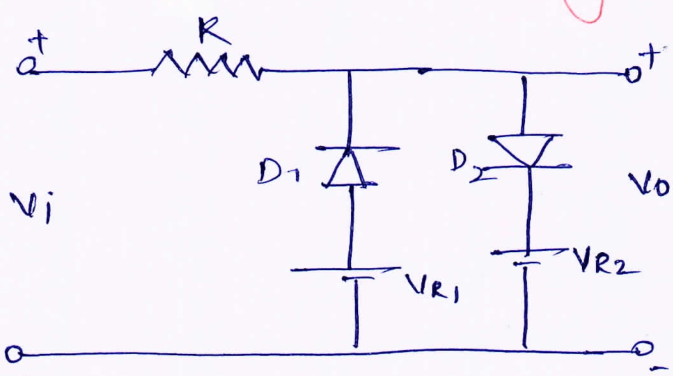
$I_{dc} = 0.636\frac{(V_m - 2V_K)}{R}$.

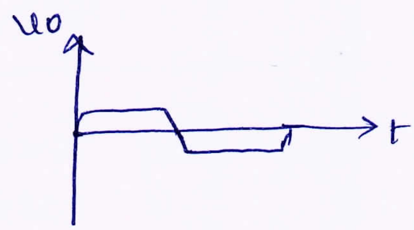
$PIV = V_m - V_K$

for $V_m >> V_K$ $\quad PIV = V_m$.

b) Explain the analysis of double ended clipper ckt which can clip both the peaks of a sinusoidal AC signal.

→





Note that D_1 conducts for $v_i \le V_{R1} - V_K$.

$\therefore v_o = V_{R1} - V_K \quad$ for $v_i \le V_{R1} - V_K$

$$\text{slope} = \frac{\Delta v_o}{\Delta v_i} = 0$$

D_2 conducts for $V_i \ge V_{R2} + V_K$.

$v_o = V_{R2} + V_K \quad$ for $V_i \ge V_{R2} + V_K$.

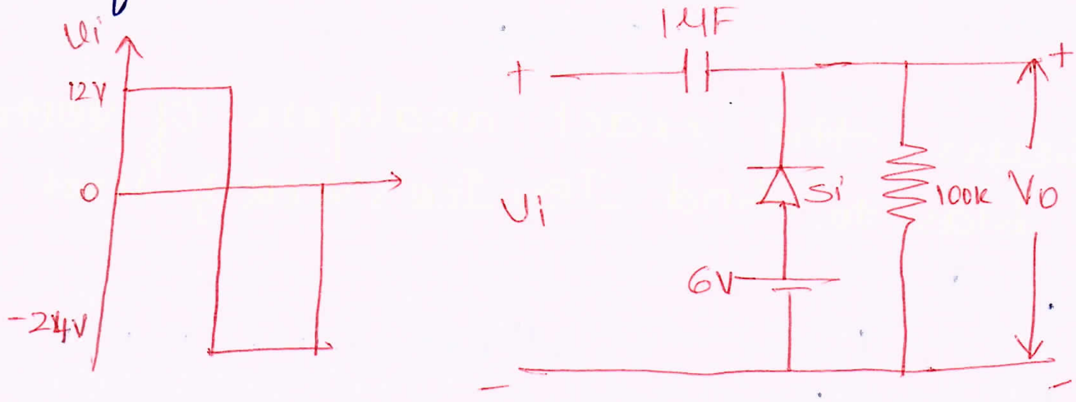
$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 0.$$

for $(V_{R1} - V_K) < v_i < (V_{R2} + V_K)$ neither D_1 or D_2 conducts

$\therefore v_o = v_i$

$$\text{Slope} = \frac{\Delta v_o}{\Delta v_i} = 1$$

1c) For the CKt shown analyse & plot the waveform for v_o for i/p indicated.



→ $v_i + v_c + 0.7 - 6 = 0$.

$v_c = -v_i + 5.3$.

When $v_i = -24V$:

$v_c = -(-24) + 5.3 = 29.3V$

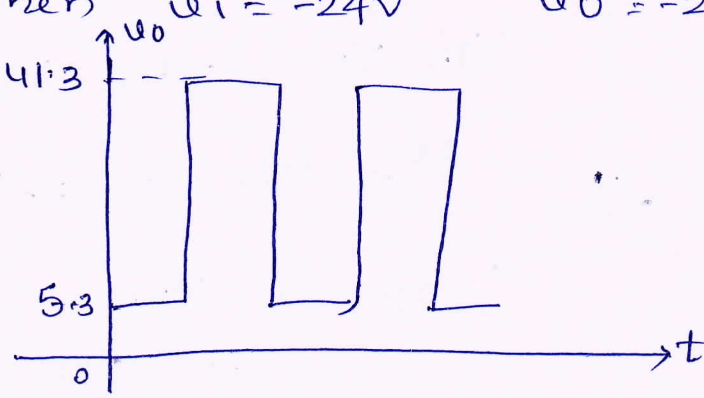
Now, when $v_i = 12V$,

$v_i + 29.3 - v_o = 0$

$v_o = v_i + 29.3$.

∴ when $v_i = 12V$, $v_o = 12 + 29.3 = 41.3V$

when $v_i = -24V$ $v_o = -24 + 29.3 = 5.3V$.



2a) What are the factors that affect the stability of operating point in a transistor.

→ i) variation of Reverse saturation current or leakage current. It increases (or doubles) ~~by~~ for every 10°C rise in temperature

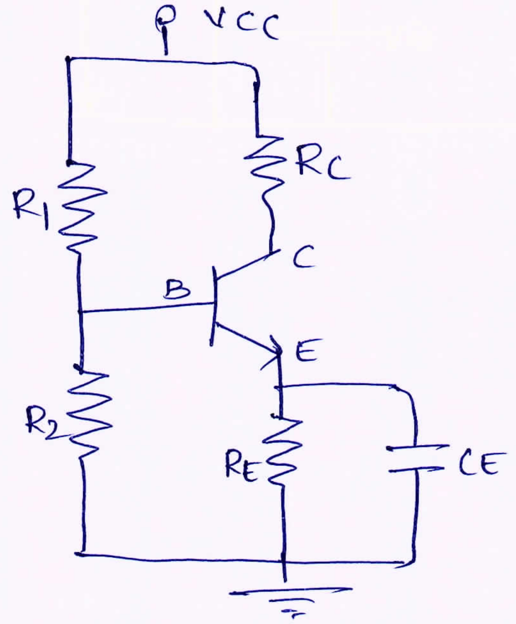
2) Variation of VBE: The Base to emitter

voltage decreases by 2.5 mV for every 1°C rise in temperature.

iii) β varies w.r.t temperature.

2b) Discuss the exact analysis of voltage divider bias to find I_B, I_{CQ}, V_{CEQ} & I_{Csat}.

→



First we find R_{TH}

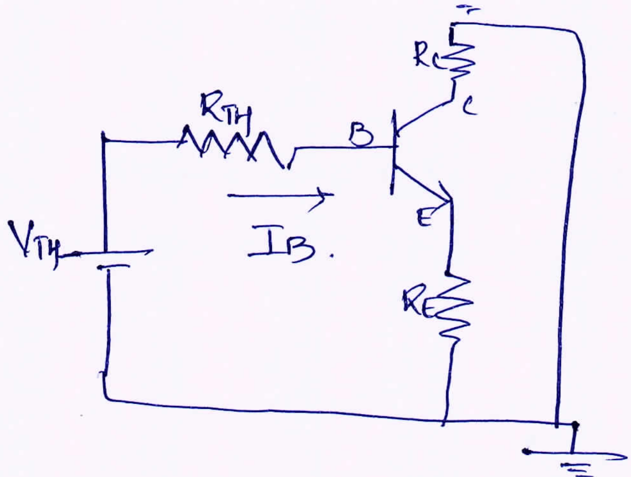
$$R_{TH} = R_1 || R_2$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

To find V_{TH},

$V_{TH} =$ [illegible] $I R_2$

$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$



$\therefore V_{TH} - V_{BE} - I_B R_{TH} - I_E R_E = 0$

$V_{TH} - V_{BE} - I_B R_{TH} - (I_B + I_C) R_E = 0.$

$V_{TH} - V_{BE} - I_B R_{TH} - I_B (1+\beta) R_E = 0.$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta) R_E}$$

$$I_C = \beta I_B = \beta \left[\frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta) R_E} \right]$$

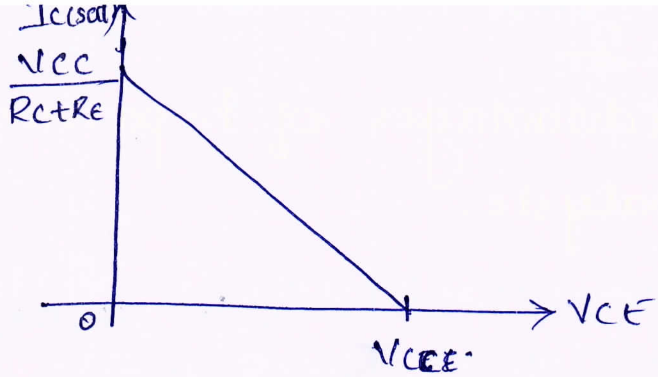
KVL for CE loop

$V_{CE} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$= V_{CC} - I_C R_C - (I_b + I_C) R_E$

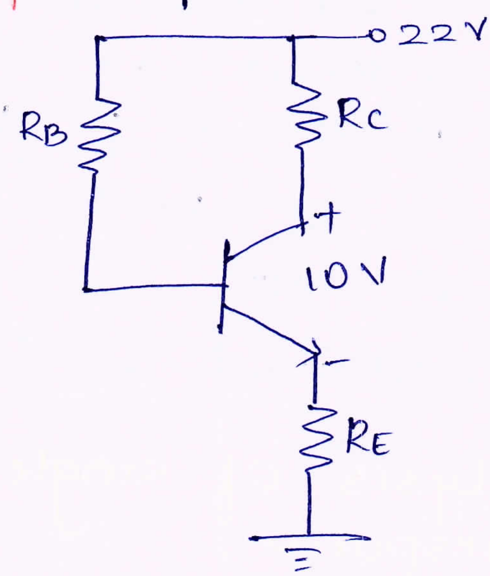
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



$$V_{CE(sat)}\Big/_{I_C=0} = V_{CC}$$

$$I_{C(sat)}\Big/_{V_{CE}=0} = \frac{V_{CC}}{R_C+R_E}$$

2c) Design values of R_B, R_E & R_C for emitter bias ckt shown in fig. Assume Si transistor with $\beta = 100$



$$R_C = \frac{V_{CC} - V_C}{I_C}$$

$$= \frac{12V - 7.6V}{2mA}$$

$$= 2.2k\Omega$$

$$I_E \approx I_C = 2mA$$

$$R_E = \frac{V_E}{I_E} = \frac{2.4V}{2mA} = 1.2k\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{2mA}{100} = 0.02mA$$

$$\therefore R_B = \frac{8.9V}{I_B} = \frac{8.9}{0.02mA}$$

$$= 445k\Omega$$

Module 2

3a. Mention the advantages of h-parameters for transistor analysis.

→ 1) h-parameters are useful in analysis & design of ckts using transistors.

2) At audio frequencies, h-parameter are real nos which makes calculations easy.

3) These parameters can be easily determined using transistor characteristic.

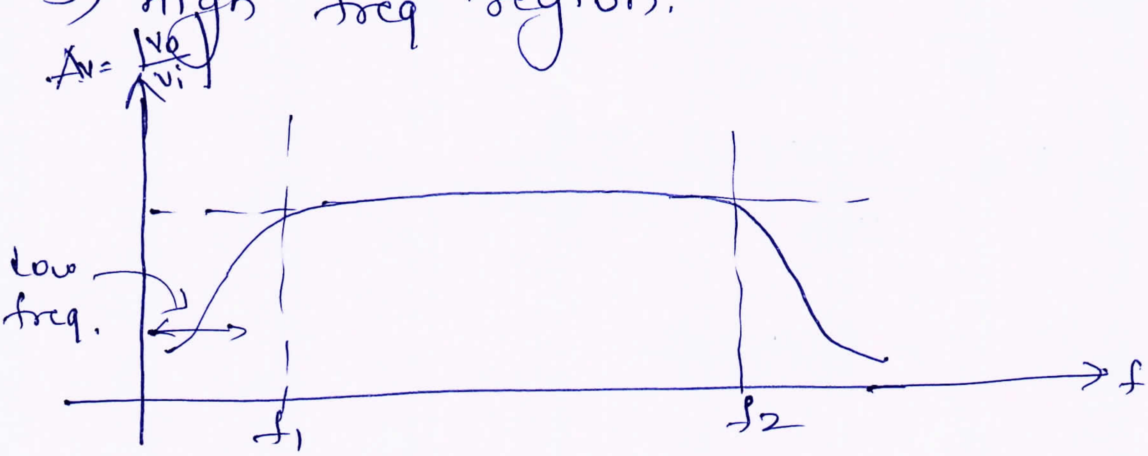
4) The models developed are independent of if transistor is n type or p type.

5) h-parameters are graphically obtained for one configurⁿ, |||ʸ other configurⁿˢ can also be obtained easily.

3b. Discuss Analysis of single stage Amplifier freq response.

→ The freq range is divided into 3 regions.

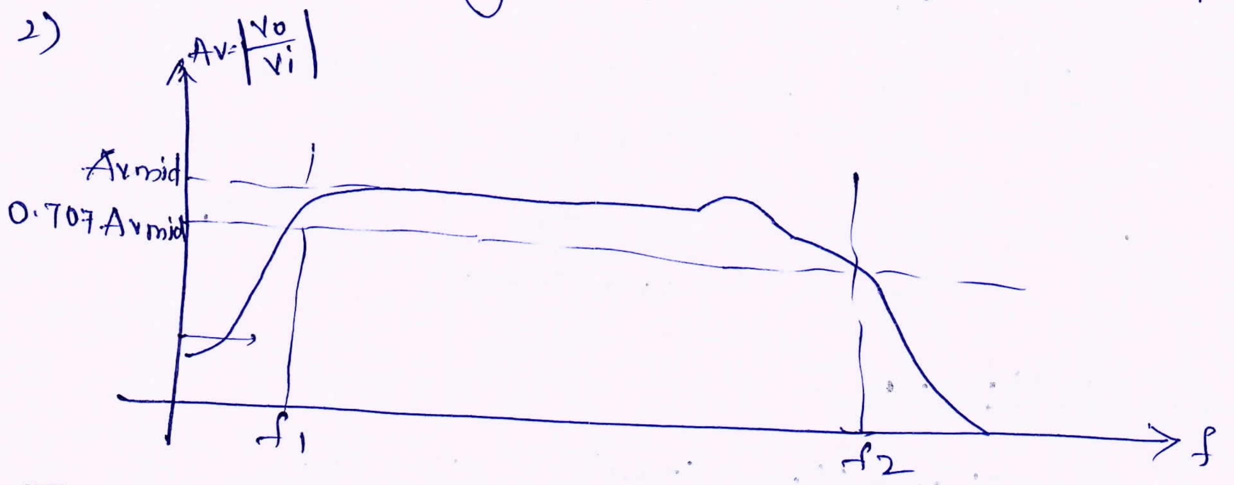
1) low freq region.
2) mid freq region.
3) High freq region.



The drop in gain at low freq is due to the coupling capacitors (Cs & Cs) & CE

At high freq, drop in gain is due to internal wiring capacitance & stray capacitance

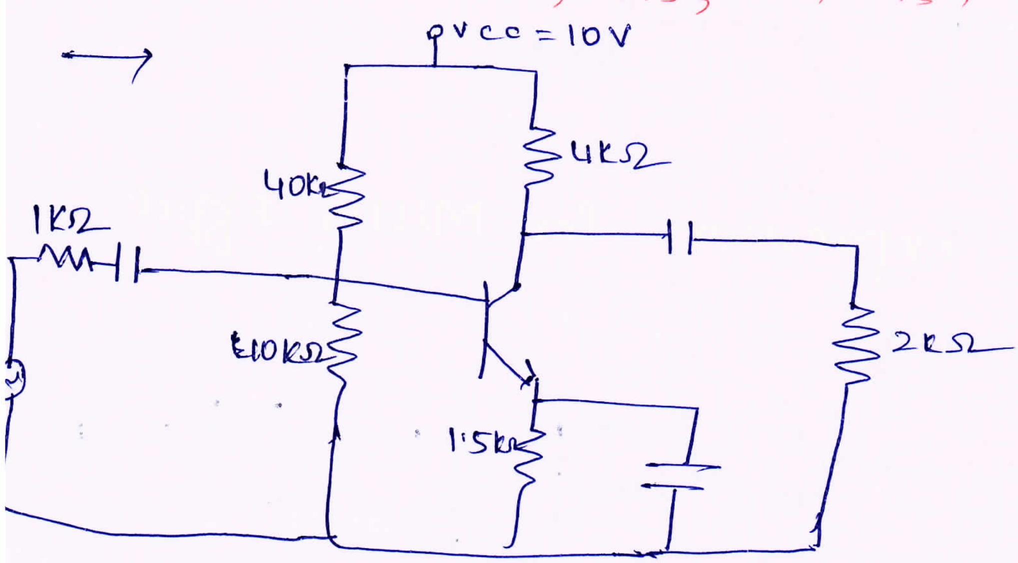
2)



The magnetizing inductive reactance of tfr is $X_L = 2\pi f L$ & at low freq. the gain drops due to small value of X_L. At $f=0$, there is no change in flux in the core.

3c) A transistor with $h_{ie} = 1.1 K\Omega$, $h_{fe} = 50$, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 25 \mu A/V$ is in CE config^n. Calculate A_i, A_{is}, A_V, A_{Vs}, R_i & R_o.

→



$\beta R_E \geq 10 R_2$

$10 R_2 = (10)(10k) = 100 k\Omega$

∴ We can use approximate analysis.

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{(10V)(10k)}{39k + 10k} = 2.04V$$

$$V_E = V_B - V_{BE}$$
$$= 2.04 - 0.7$$
$$= 1.34\,V.$$

$$I_E = \frac{V_E}{R_E} = \frac{1.34\,V}{1.5\,k\Omega} = 0.893\,mA.$$

$$r_e = \frac{26\,mV}{I_E} = \frac{26\,mV}{0.893 \times 10^{-3}} = 29.1\,\Omega$$

→ $R_i = R_1 \| R_2 \| \beta r_e$

$$= 39k \| 10k \| (100)(29.1) = 2.13\,k\Omega.$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_o \| R_L}{r_e}$$

$$R_o = R_C \| r_o = 4\,k\Omega \| 20\,k\Omega = 3.33\,k\Omega.$$

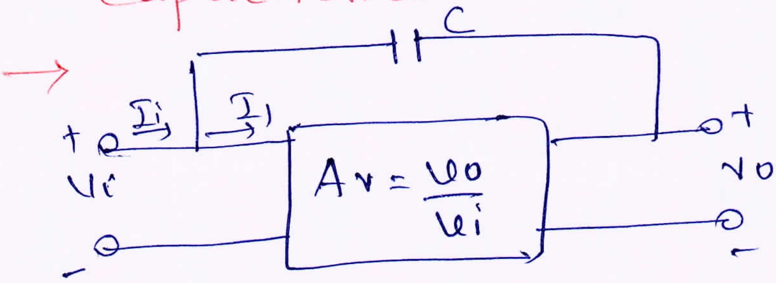
$$A_v = \frac{-2.49\,k}{29.1\,\Omega} = -85.56$$

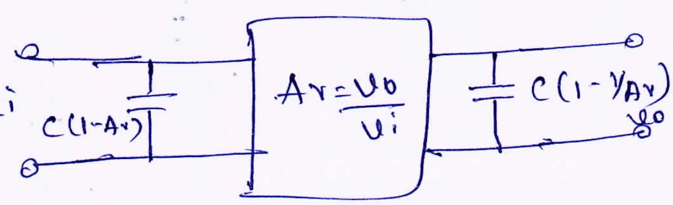
$$A_{vs} = A_v \left[\frac{R_i}{R_i + R_s}\right] = -(85.56) \times 0.68$$

$$= -58.18.$$

~~Ro~~ =

4a) Obtain the expression for Miller Effect Capacitance.

→ 



Let $I_i = I_1 + I_2$.

$$I_i = \frac{v_i}{Z_i} \quad \& \quad I_1 = \frac{v_i}{R_i}$$

$$\therefore I_i = \frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_v)V_i}{X_C}.$$

& $\frac{1}{Z_i} = \frac{1}{R_i} + \frac{(1-A_v)}{X_c}$

$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{CM}}$.

$\frac{1}{2\pi f C_M} = \frac{1}{(1-A_v) 2\pi f C}$.

$\therefore \frac{1}{C_M} = \frac{1}{(1-A_v) C}$.

or $\boxed{C_{M_i} = (1-A_v) C_i}$

Applying KCL we have

$I_o = I_1 + I_2$

$I_1 = \frac{V_o}{R_o}$ & $I_2 = \frac{V_o - V_i}{X_C}$.

$\therefore I_o = \frac{V_o - V_o/A_v}{X_C} = \frac{V_o(1 - 1/A_v)}{X_C}$

& $\frac{I_o}{V_o} = \frac{1 - 1/A_v}{X_C}$

$\therefore X_{CMO} = \frac{X_C}{1 - 1/A_v}$

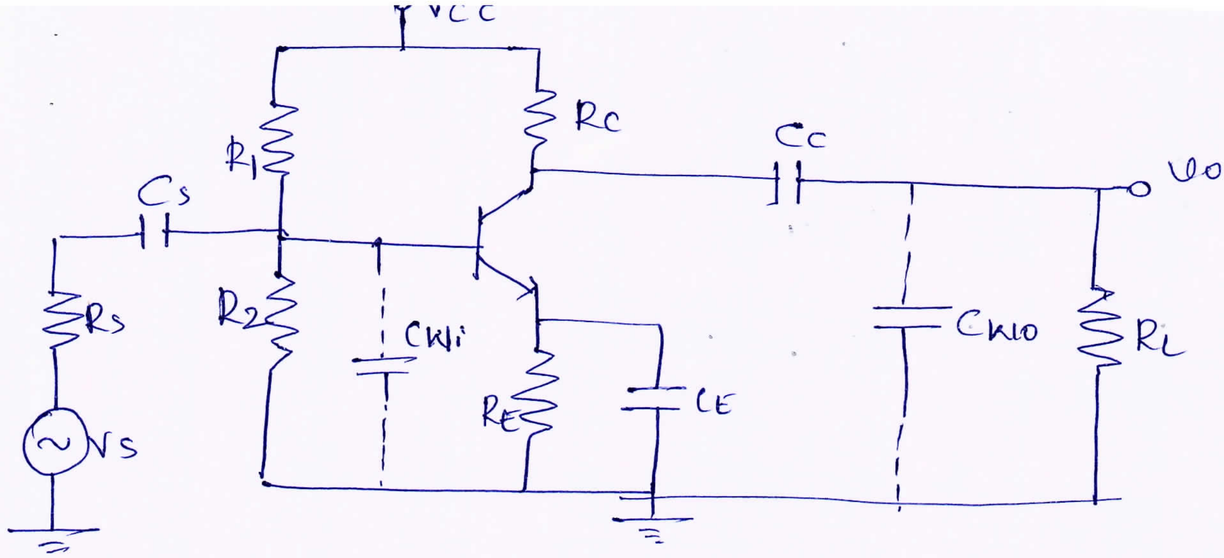
$\therefore \boxed{C_{MO} = C(1 - 1/A_v)}$

4b) Explain the high frequency analysis of BJT amplifier

→ At high freq, there are 2 parameters that define -3dB cut off freq.

1) N/w capacitance.

2) Freq dependent of hfe (β)



The capacitances Cbc, Cbe & Cce are parasitic capacitances & capacitances CWi & CWo are wiring capacitance.

$$f_{Hi} = \frac{1}{2\pi R_{THi} C_i}$$

$$f_{Ho} = \frac{1}{2\pi R_{THo} C_o}.$$

where $C_i = C_{wi} + C_{be} + C_{mi} = C_{wi} + C_{be} + (1 - A_v) C_{bc}$

$$C_o = C_{wo} + C_{ce} + C_{Mo}.$$

4c) Determine lower cut off freq for emitter follower using BJT amplifier with $C_s = 0.1\mu F$, $R_s = 1k\Omega$, $R_1 = 12k\Omega$, $R_2 = 4k\Omega$, $R_E = 1.5k\Omega$, $C = 0.1\mu F$, $\beta = 100$, $V_{CC} = 15V$, $V_{BE} = 0.7V$, $r_o = \infty$ & $h_{ie} = 1.04k\Omega$

→

$$V_B = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$= 15 \times \frac{4K}{12K + 4K} = 3.75V$$

$$V_E = V_B - V_{BE} = 3.75 - 0.7V$$

$$= 3.05V$$

$$I_E = \frac{V_E}{R_E} = \frac{3.05}{1.5k} = 2.03mA$$

$$I_C \approx I_E = 2.03mA$$

$Z_{in} = h_{ie} + (1+\beta) R_E$

$= 1.04 \times 10^3 + (1+100)\, 1.5 \times 10^3$

$= 152.5\,k\Omega$

$Z_{total} = R_s + Z_{in}$

$= 1\,k\Omega + 152.5\,k\Omega$

$= 153.54\,k\Omega$.

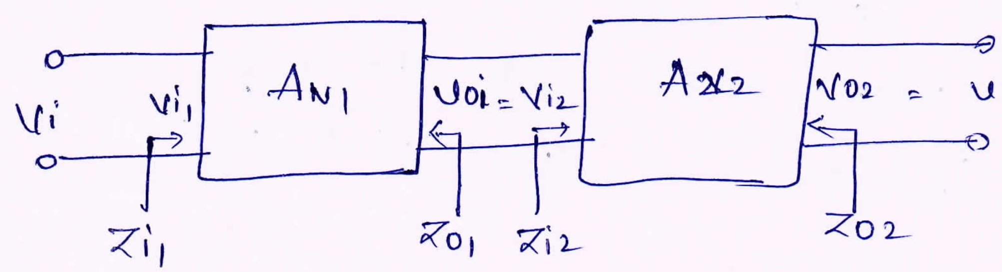
$f_L = \dfrac{1}{2\pi R_s C_s} = \dfrac{1}{2\pi \times 153.5k \times 0.14}$

$= 10.36\,Hz$

Module 3

5a) With two stage cascaded Amplifier, explain the need of Cascading.

→



When amplification from a single stage is not sufficient, then 2 or more amplifier stages need to be connected in series. Such an arrangement is called Cascade Amplifier.

WKT $V_{o1} = V_{i2}$ & $V_{o2} = V_o$

$A_{v1} = \dfrac{V_{o1}}{V_{i1}}$ $\qquad A_{v2} = \dfrac{V_{o2}}{V_{i2}}$

$\therefore A_v = \dfrac{V_{o1}}{V_i} \cdot \dfrac{V_o}{V_{o1}}$

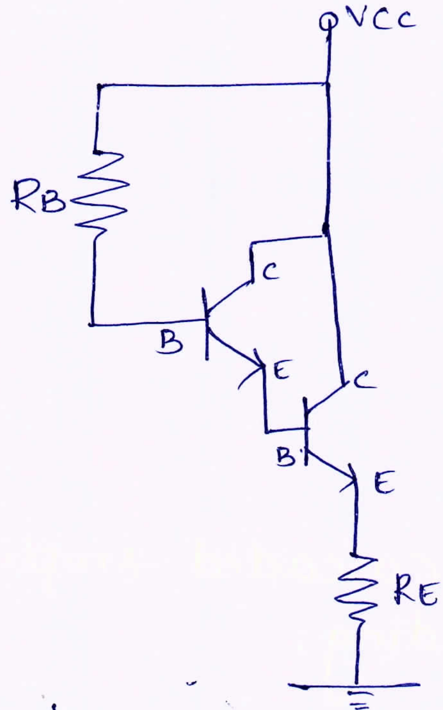
$= \dfrac{V_o}{V_i} = A_{v1} \cdot A_{v2}$.

5b) Write a note on Cascade Connection.

→ Question repeated as previous.

5C. Explain DC Analysis of Darlington Emitter follower.

→



Applying KVL to i/p ckt

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{CC} - I_B R_B - V_{BE} - (I_B + \beta I_B) R_E = 0$

$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$

$\therefore \boxed{I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$

Applying KVL to CE loop.

$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$

Here, $\beta = \beta_D$ & $V_{BE} = 1.6V$ to $1.8V$.

6a) What are the Characteristics of Negative feedback Amplifier.

→ 1) Stability of Transfer Gain:-

Stability of Transfer Gain with feedback is less as compared to without feedback. Hence stability is maintained.

2) Reduction in Noise

3) Reduction in freq distortion.

4) Improves Overall Bandwidth.

5) Negative f/b improves freq response of Amplifier.

6b. An amplifier has mid-band voltage gain of 1000 with $f_L = 50Hz$ & $f_H = 50KHz$. If 5% negative f/b is applied then calculate gain, f_L & f_H with feedback.

→

$$A_f = \frac{A}{1+A\beta} \qquad \beta = 5\% = 0.05$$

$$= \frac{1000}{1+1000\times0.05} = 19.61$$

$$f_{L(f)} = f_L \times (1+A\beta)$$

$$f_{H(f)} = f_H \times (1+A\beta)$$

$$f_{L(f)} = 50 \times (1+0.05\times1000) = 2550\ Hz$$

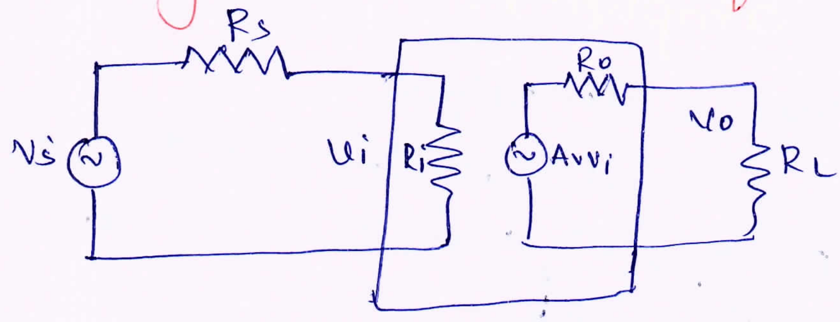
$$f_{H(f)} = 50\times10^3 \times (1+0.05\times1000)$$

$$= 50KHz \times 51$$

$$= 2.55MHz$$

6c) Obtain expression for i/p & o/p resistance of Voltage series Amplifier.

→



By vltg Div rule at i/p side

$$V_i = \frac{V_s \cdot R_i}{R_i + R_s}$$

$$V_i = \frac{V_s}{\frac{R_i + R_s}{R_i}}$$

$$V_i = \frac{V_s}{1 + \frac{R_s}{R_i}}$$

if $R_s/R_i << 1$ or $R_s << R_i$

or $R_i >> R_s$ then $V_i = V_s$.

Ideally $\boxed{R_i = \infty}$

IIIy By vltg Div Rule at o/p side.

$$V_o = \frac{A_v V_i \cdot R_L}{R_o + R_L}$$

$$\therefore V_o = \frac{A_v V_i}{\frac{R_o + R_L}{R_L}}$$

$$V_o = \frac{A_v V_i}{\frac{R_o}{R_L} + 1}$$

$\because R_o/R_L << 1$ or $R_o << R_L$

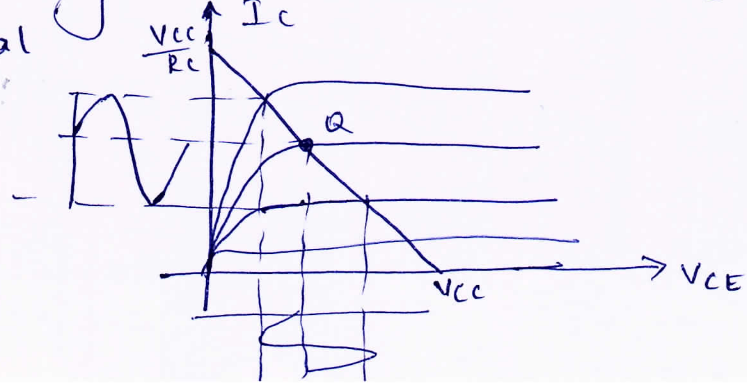
ie, Ideally $\boxed{R_o = 0.}$

Module 4

7. a) With waveforms explain the classification of a power amplifier.

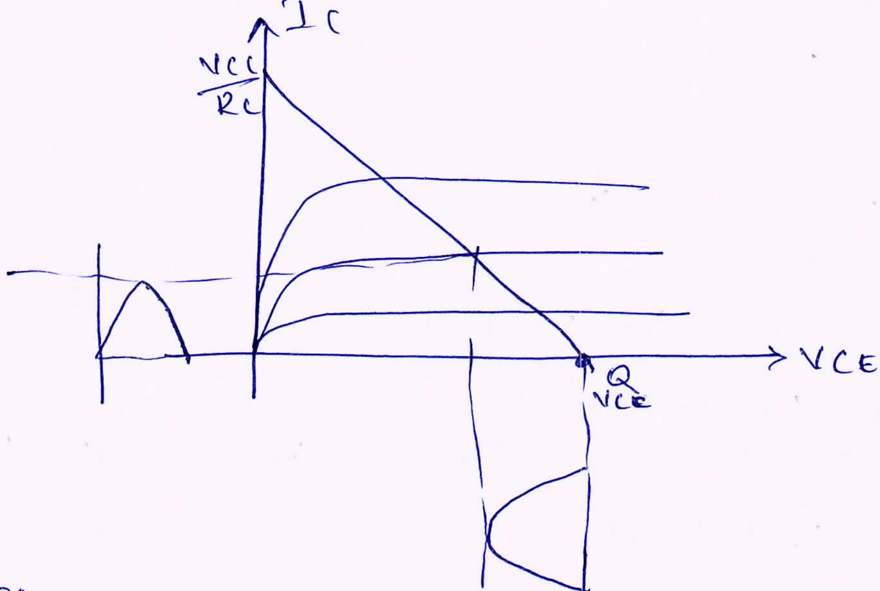
→ i) Class A Power Amplifier :-

→ Q pt is located at the centre of load line. So the o/p signal varies over the full cycle of the i/p signal



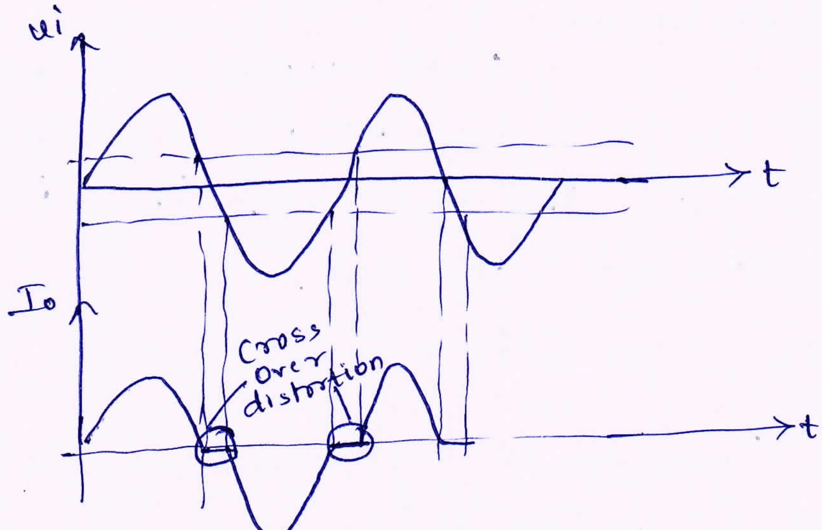
2) Class B Power Amplifier :-

→ Qpt is located at the cut off region of the load line as shown in fig. so o/p signal varies for one half cycle of i/p signal. I_c flows for 180°.



3) Class AB Power Amplifier.

Q-pt & i/p signal are selected such that o/p signal obtained is more than 180° but less than 360°. ie, η of class AB is more than Class A but less than Class B.

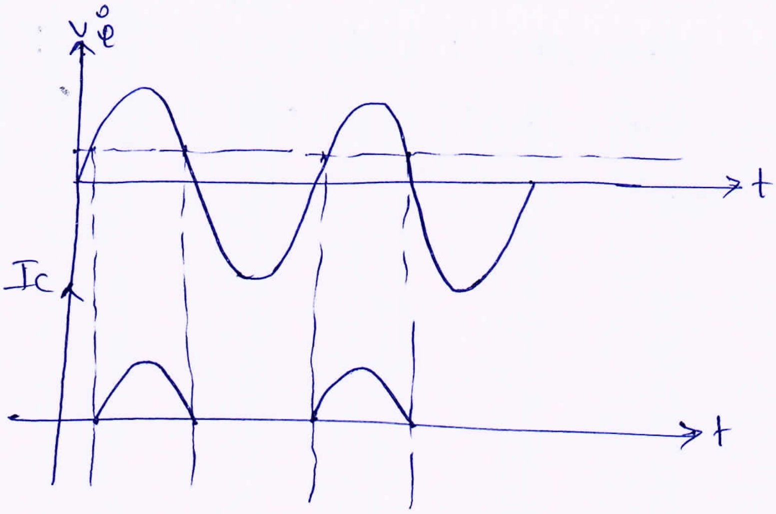


4) Class C power Amplifier :-

Here, the transistor is biased below the cut off region.

Q.pt remains active for less than half a cycle.

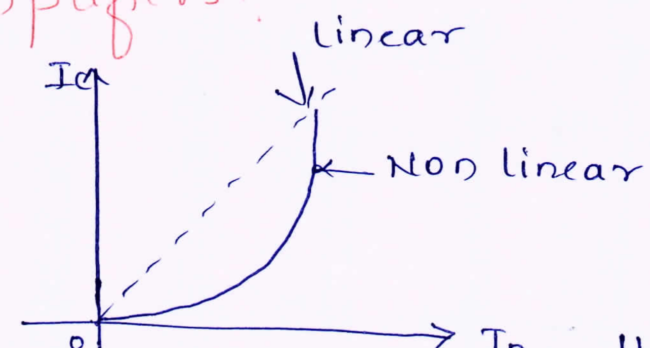
& for remaining, transistor is in Cutoff region.
So, I_C flows for less than 180°



5) Class D power Amplifier →
Designed to Operate as pulse signal which are ON for a short interval & OFF for a longer interval.

7b) Derive an expression for second harmonic distortion using 2 point method for power Amplifiers?

→



∵ $i_b = I_{Bm} \cos \omega t$

Due to this I_C swings around its Q value but the relⁿ b/w. i_b & i_c is non linear as shown in fig.

Mathematically $i_c = G_1 i_b + G_2 i_b^2$

$$= G_1 I_{Bm} \cos \omega t + G_2 I_{Bm}^2 \cos^2 \omega t \quad \text{--- (1)}$$

But, $\cos^2 \omega t = \dfrac{1 + \cos 2\omega t}{2}$

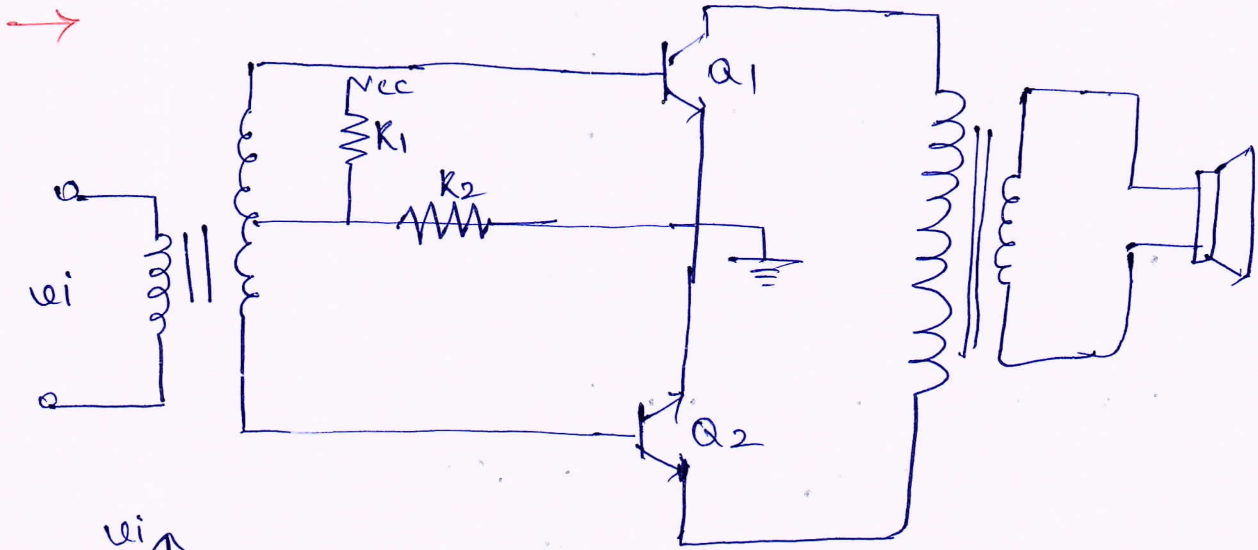
$$\therefore \; i_c = G_1 I_{Bm} \cos \omega t + G_2 I_{Bm} \left(\frac{1 + \cos 2\omega t}{2} \right)$$

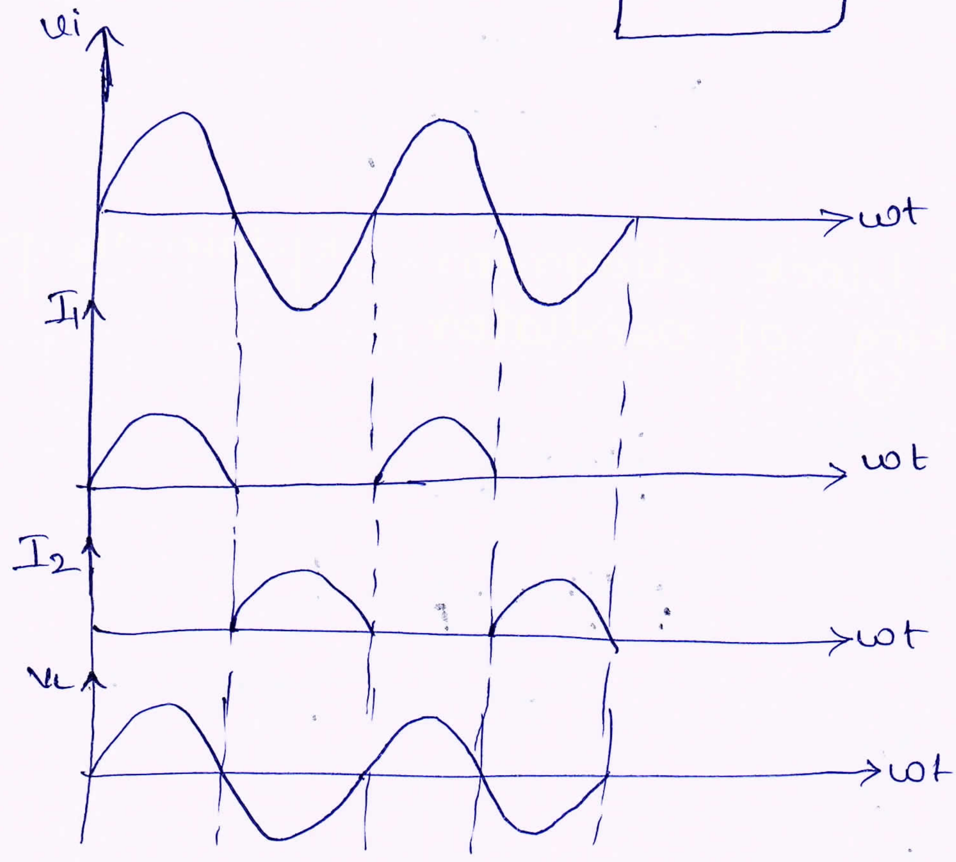
$$i_c = G_1 I_{Bm} \cos \omega t + \frac{1}{2} G_2 I_{Bm}^2 + \frac{G_2 I_{Bm}^2}{2} \cos 2\omega t$$

$$\therefore \; \boxed{i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t}$$

7c) With CKt diagram & waveform, explain working of Class B push pull amplifier. Also show that conversion η is 78.5%.

→





The CKt consist of

1) Two centre tapped tfr (T_1 & T_2)
2) Two identical tfr (Q_1 & Q_2)

During +ve half cycle, Q_1 is +ve & Q_2 is -ve & as a result Q_1 conducts & Q_2 is off. & when i/p signal goes -ve, Q_1 turns off Q_2 is ON. Each transistor handles one half of signal at each instant.

$$I_{dc} = \frac{2I_m}{\pi}$$

$$P_{i(dc)} = V_{cc} I_{dc}$$

$$= V_{cc} \cdot \left(\frac{2I_m}{\pi}\right)$$

$$\boxed{P_{i(dc)} = \frac{2V_{cc} \cdot I_m}{\pi}}$$

$$P_o = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{4V_{cc}}$$

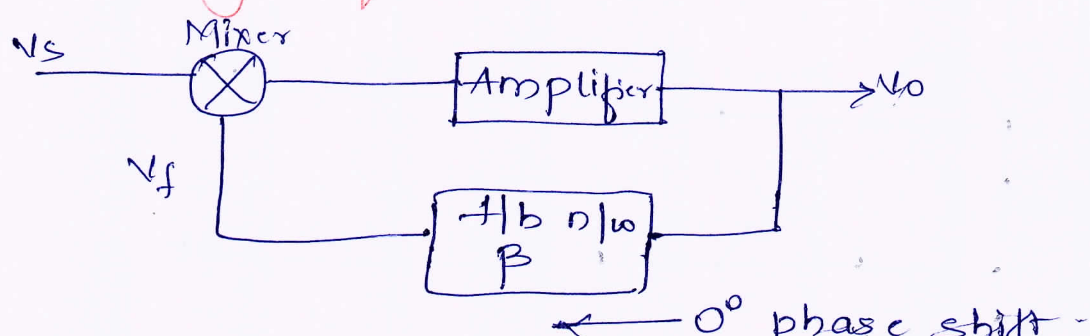
$V_{max} = V_{cc}$ & $V_{min} = 0$.

$$\therefore \eta_{max} = \frac{V_{cc} \cdot \pi}{4V_{cc}} \times 100$$

$$\boxed{\eta = 78.5\%}$$

8 a) With block diagram. explain the principle of working of oscillator.

→



$$A_V = \frac{V_o}{V_i}$$

$$\& \ A_f = \frac{V_o}{V_s}.$$

$\because$ feedback is +ve, vltg 'V_f' is added to V_s to generate i/p of amplifier

$$V_i = V_s + V_f$$

$$\& \ V_f = \beta V_o$$

$$\therefore A_f = \frac{V_o}{V_i - \beta V_o}.$$

Dividing Nr & Dr by V_i we get

$$A_f = \frac{V_o/V_i}{V_i/V_i - \beta V_o/V_i}$$

$$\therefore \boxed{A_f = \frac{A_v}{1 - A_v \beta}}$$

$\because V_f = \beta V_0$

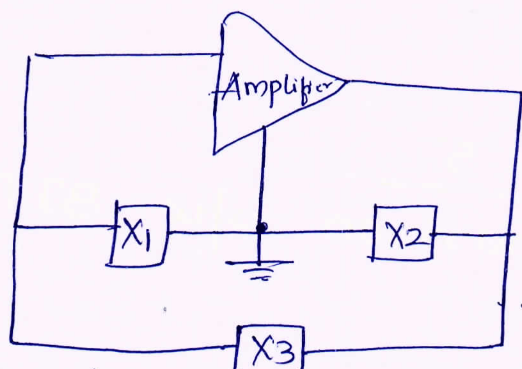
$\therefore V_f = \beta A V_i$

Now if $|A_v \beta| = 1$ then $V_f = V_i$.

so total phase shift should be $0°$ or $360°$.
& they are in same phase, hence satisfies Barkhausen criteria.

8b. Explain the principle of tuned Oscillator. Also obtain expression for freq of Hartley Oscillator.

→



* LC Oscillators employ ||el LC ckts to generate oscillations.
* ||el LC ckt is also called tuned ckt or resonant ckt.

These Oscillators exhibits high Q than RC Oscillators resulting in good freq & stability.

Here X_1 & X_2 may be both L or both C
& X_3 may be ~~either~~ L if both X_1 & X_2 are C
& must be C if both X_1 & X_2 are L.

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}.$$

$L_{eq} = L_1 + L_2$.

& $L_{eq} = L_1 + L_2 + 2M$

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$

& $h_{fe} \geq L_1/L_2$

8c) A Quartz Crystal has L = 50 mH, C_1 = 0.02 pF, R = 500 Ω, C_2 = 12 PF. Determine fs & fp. If ext capacitance across crystal changes from 5 pF to 6 PF. find the change in freq of Osillation

→ $$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{50\times10^{-3}\times5\times10^{-12}}}$$

$$= \frac{1}{2\pi\sqrt{250\times10^{-15}}}$$

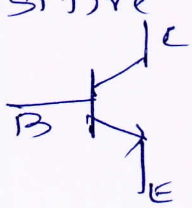
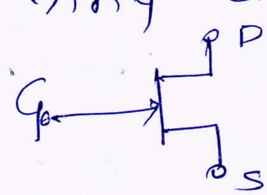
$$= 318.3\,KHz.$$

$$f_p = \frac{1}{2\pi\sqrt{LC_p}}$$

$$C_p = \frac{C_1 C_2}{C_1 + C_2} = 0.0199\times10^{-12}$$

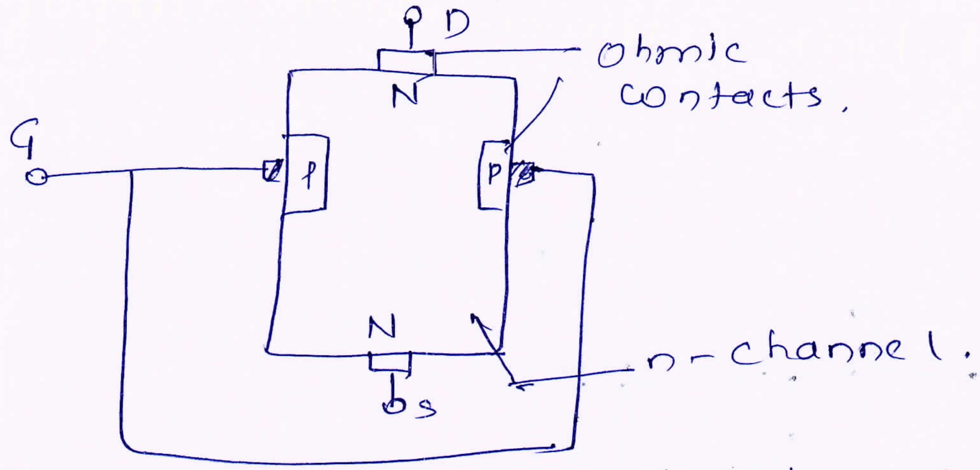
Module 5

9a. Give the Comparison b/w BJT & MOSFET.

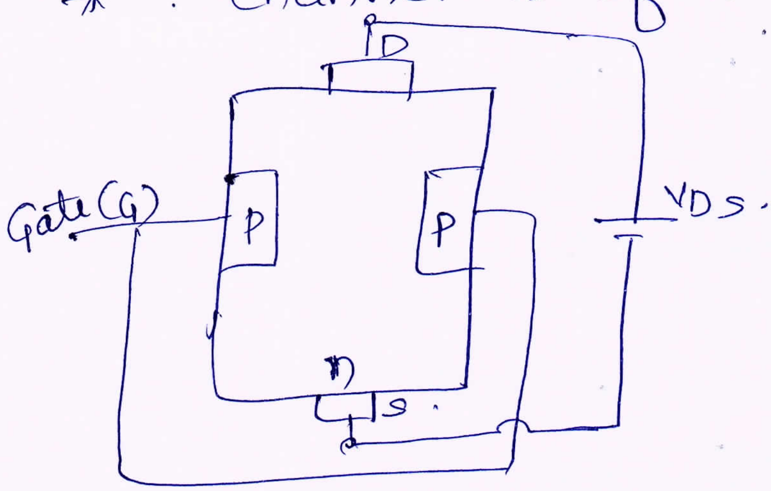
BJT	FET
1) Bipolar	1) Unipolar
2) Current controlled device	2) vltg controlled device.
3) 3 terminals B, E & C	3) 3 terminals G, D & S.
4) Conduction by both charge carriers	4) only majority charge carriers.
5) sensitive to temp	5) Any ambient temp
	

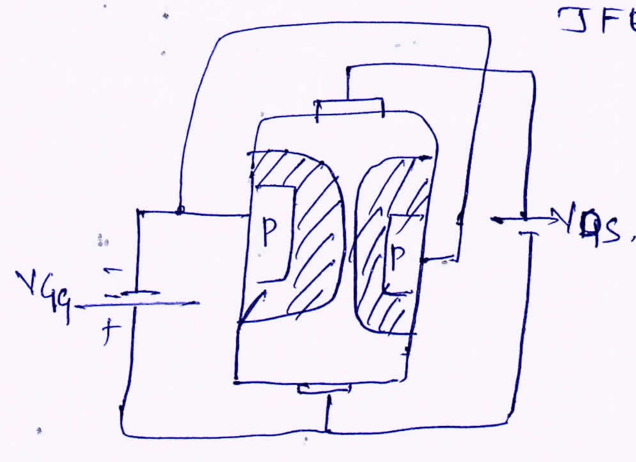
9b. Explain Construction & working of n Channel JFET.

→



* A piece of n type material is required for n-channel.
* It has 2 smaller pieces of ptype materials forming pn junctions.
* Channel ends are designated as Drain & Sour
* 2 p type materials are connected to Gate
* ∵ Channel is of n type it is called n-Channel JFET.

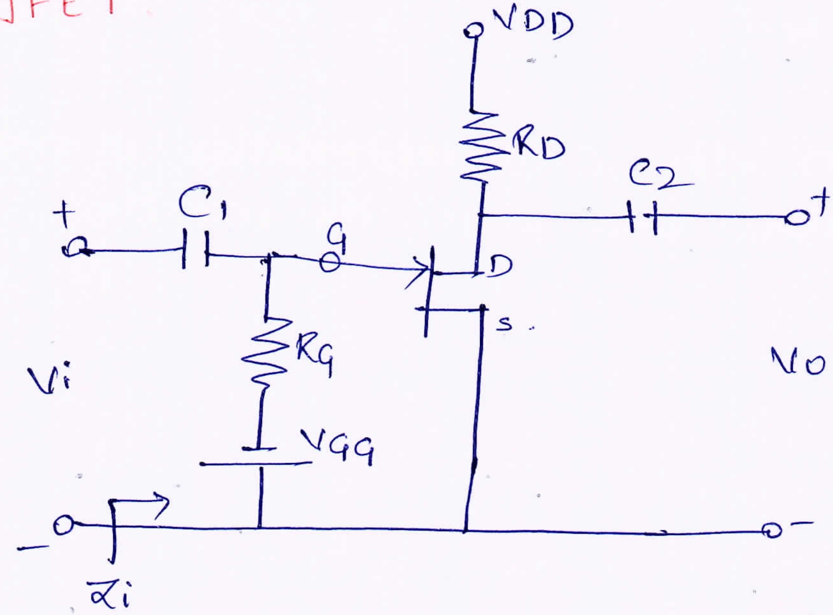




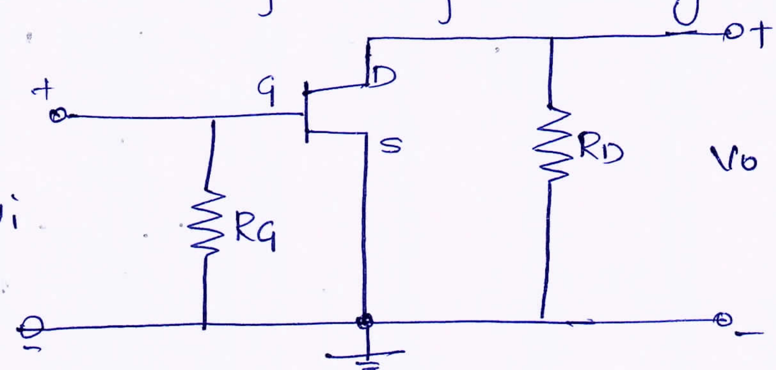
When Gate is not connected,
Vltg is applied +ve at drain & -ve at source.
Id starts flowing.
Now when, Gate is biased -ve w.r.t source PN junctions are reverse biased & depletion regions are formed.
As Channel is light doped, depletion region penetrates deeply & result is ID decreases
Now, when VGS is applied IDS starts to increase

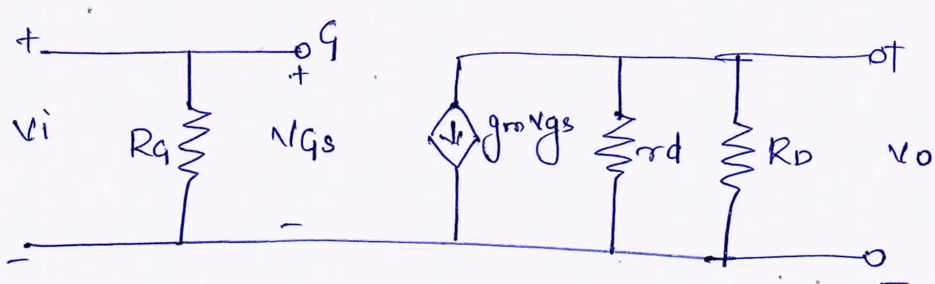
9c. Obtain expression for A_V, Z_i & Z_o for fixed bias common source amplifier using JFET.

→



A C equivalent ckt is obtained by S.C the Capacitors C1 & C2 & reducing VDD & VGG to zero.





from fig, i) $Z_i = R_G$.

ii) $Z_o = r_d \parallel R_D$.

iii) Applying KCL $g_m V_{GS} + I_1 + I_2 = 0$.

$I_1 = \frac{V_o}{r_d}$ & $I_2 = \frac{V_o}{R_D}$.

$$g_m V_{GS} + \frac{V_o}{r_d} + \frac{V_o}{R_D} = 0.$$

$$g_m V_{GS} = -V_o\left[\frac{1}{r_d} + \frac{1}{R_D}\right]$$

$$g_m V_{gs} = -V_o \left[\frac{r_d + R_D}{r_d R_D} \right]$$

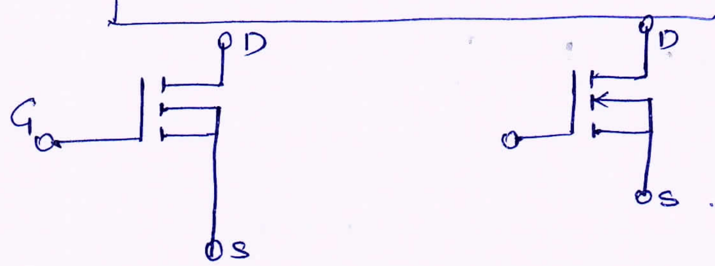
$$\therefore \boxed{\frac{V_o}{V_i} = -g_m (r_d \| R_D)}$$

10 a) Explain the characteristics of n-Channel EMOSFET & also describe its working.

→ * E. MOSFET is fabricated to Operate only in Enhancement mode.

* Hence, V_{GSQ} can only be positive for n channel
* & negative for p-channel device.

$$\therefore \boxed{I_D = k\left[V_{GS} - V_{GS(TH)}\right]^2}$$



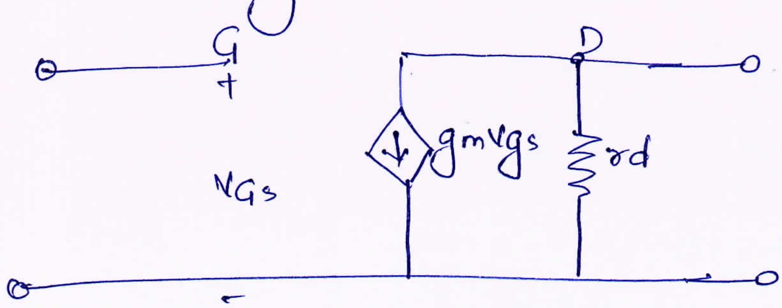
$V_{GS(TH)}$ → Threshold vltg.

It is Important to note that Drain Current is zero for $V_{GS} > V_{GS(TH)}$ & it significantly increases for $V_{GS} \geq V_{GS(TH)}$

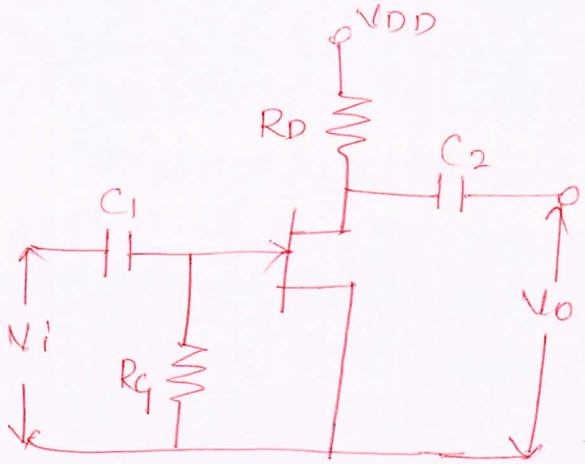
k → constant.

$$\therefore g_m = 2k\left[V_{GS(Q)} - V_{GS(TH)}\right].$$

* Small signal AC Model of EMOSFET.



10 b) Design the fixed bias FET Common source amplifier shown in fig to meet the foll requirements $A_V = 12$, $Z_i = 10M\Omega$, $V_{DD} = 40V$



$I_{DSS} = 10mA$

$V_P = -5V$

$y_{os} = 25\mu s$.

→ $g_m = \frac{2 I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$

$= \frac{2 \times 10mA}{5}\left[1 - \frac{0}{-5}\right]$

$g_m = 4ms$.

$r_d = 1/y_{os} = 1/25\mu s. = 40K\Omega$

$Z_i = R_G = 10M\Omega$.

$Z_o = r_d || R_D$.

$A_v = -g_m [r_d || R_D]$

$12 = -4 \times 10^{-3}\left[\frac{40K \times R_D}{40K + R_D}\right]$

$\frac{-3 \times 10^{-3}}{40 \times 10^3} = \frac{R_D}{40K + R_D}$.

$\therefore Z_o = 40K || 3K$

$= 2.79K\Omega$.

$R_D = (-75 \times 10^{-9})\, 40K + R_D$.

$= (-3 \times 10^{-3}) + (-75 \times 10^{-9} R_D)$

$1 R_D = 3 \times 10^{-3}$

$\boxed{R_D = 3K\Omega}$