KLS Vishwanathrao Deshpande Institute of Technology

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(Recognized Under Section 2(f) by UGC, New Delhi)
Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada
Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813
www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper Scheme & Solution

Faculty Name	:	Deepak Sharma
Course Name	:	VLSI Design and Testing
Course Code	:	21EC63
Year of Question Paper	:	June/July 2024
Date of Submission	:	03/09/2024

Faculty Member HoD Dean (Acad.)

Head of the Department
Dept. of Electronic & Communication Engg.
K.L.S.V.D.I.T., HALIYAL (U.K.)

CBCS SCHEME

USN | | | | | | | | | | |

21EC63

Sixth Semester B.E. Degree Examination, June/July 2024
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. State Moore's law, elaborate with graph. **(04 Marks)**

b. Derive the expression for drain current in linear and saturation regions. **(10 Marks)**

c. Explain the following non-ideal characteristics:
i) Body effect ii) Channel length modulation. **(06 Marks)**

OR

2 a. Explain working of nMOS enhancement mode transistor operation with neat sketches and relevant equations. **(08 Marks)**

b. Draw inverter circuit and explain its DC transfer characteristics. **(08 Marks)**

c. Draw the schematic of
i) $F = \overline{A + BC}$ ii) $F = \overline{AB + CD}$. **(04 Marks)**

Module-2

3 a. Explain CMOS fabrication process with necessary diagrams. **(10 Marks)**

b. With relevant equations explain transient response of CMOS inverter. **(05 Marks)**

c. With neat diagrams explain layout design rules. **(05 Marks)**

OR

4 a. Draw the stick diagram and layout of three input NAND gate. **(06 Marks)**

b. Find maximum and minimum rise time and fall time delays of two input NAND gate. **(06 Marks)**

c. Estimate the minimum delay of the path from A to B in Fig.Q.4(c) and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width.

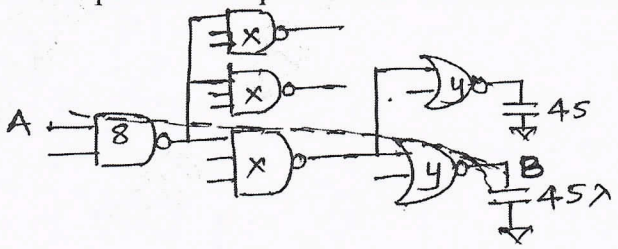


Fig.Q.4(c)

(08 Marks)

Module-3

5 a. Explain the operation of three transistor DRAM cell with necessary timing diagrams. **(08 Marks)**

b. Draw the structure of NAND flash memory cell and explain the operation. **(06 Marks)**

c. Explain ferroelectric RAM with necessary diagrams. **(06 Marks)**

OR

6 a. Explain read and write operations of SRAM cell with necessary diagrams. **(08 Marks)**

b. What is row decoder? Explain with an example. **(06 Marks)**

c. Explain data programming and erasing methods of flash memory. **(06 Marks)**

Module-4

7 a. Briefly explain different types of faults in digital circuits. **(08 Marks)**

b. Consider the logic circuit shown in Fig.Q.7(b) find Boolean difference with respect to x_3.

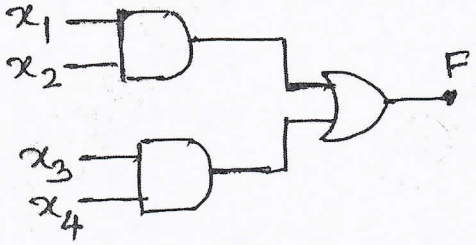


Fig.Q.7(b)

(06 Marks)

c. Explain detection of multiple faults in combinational logic circuits. **(06 Marks)**

OR

8 a. With neat sketch, explain path oriented decision making algorithm. **(10 Marks)**

b. For a given logic network determine tests for checking all single node faults (Fig.Q.8(b))

$F = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$ **(10 Marks)**

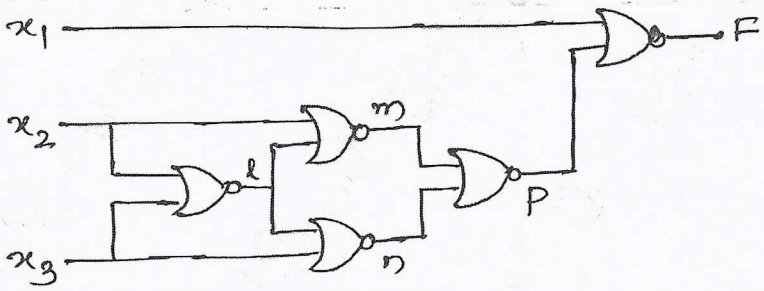


Fig.Q.8(b)

Module-5

9 a. Briefly explain :

i) Controllability ii) Observability. **(06 Marks)**

b. Explain adhoc design rules for improving testability. **(06 Marks)**

c. With neat diagram explain partial scan. **(08 Marks)**

OR

10 a. List LSSD design rules. **(10 Marks)**

b. Explain test generation based on functional fault models. **(10 Marks)**

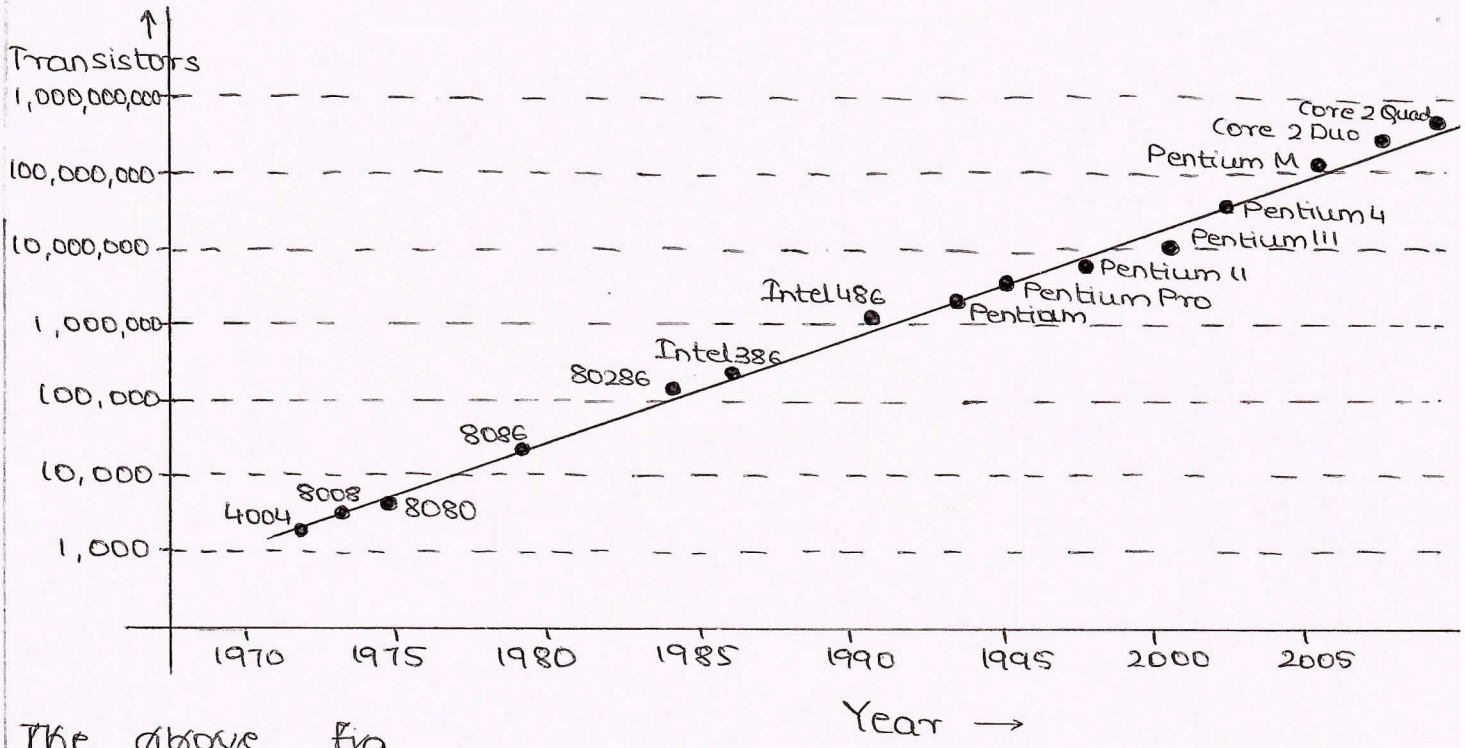
* * * * *

Module - 1

1.a. State Moore's law, elaborate with graph.

⇝ Moore's law states that the number of transistors on a microchip doubles every two years, while the cost of manufacturing a transistor drops by half.

This was observed by Gordon Moore in the year 1965.



The above fig

The above graph shows that the number of transistors in Intel microprocessors has doubled every 26 months since invention of 4004.

Moore's law is driven primarily by scaling down the size of transistors and to a minor extent, by building larger chips.

1.b. Derive the expression for drain current in linear and saturation regions.

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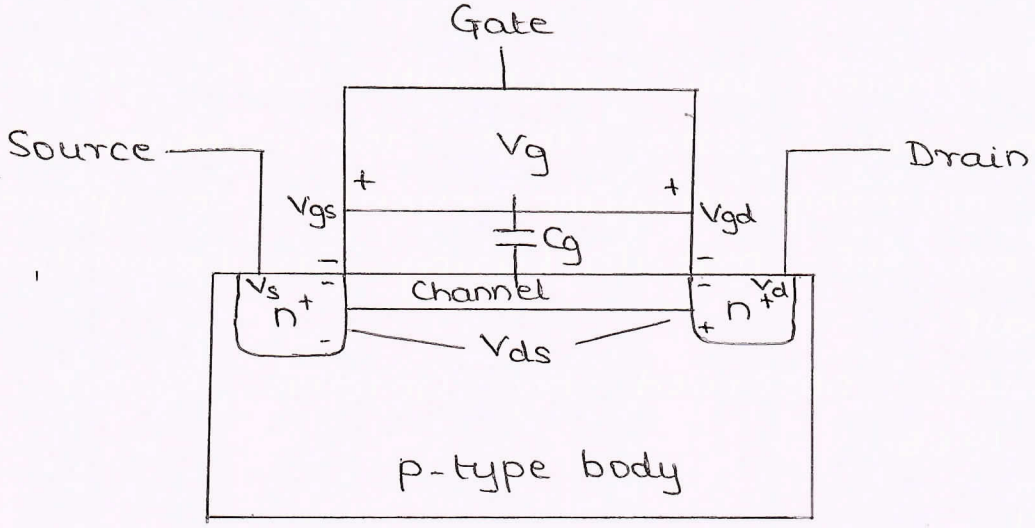
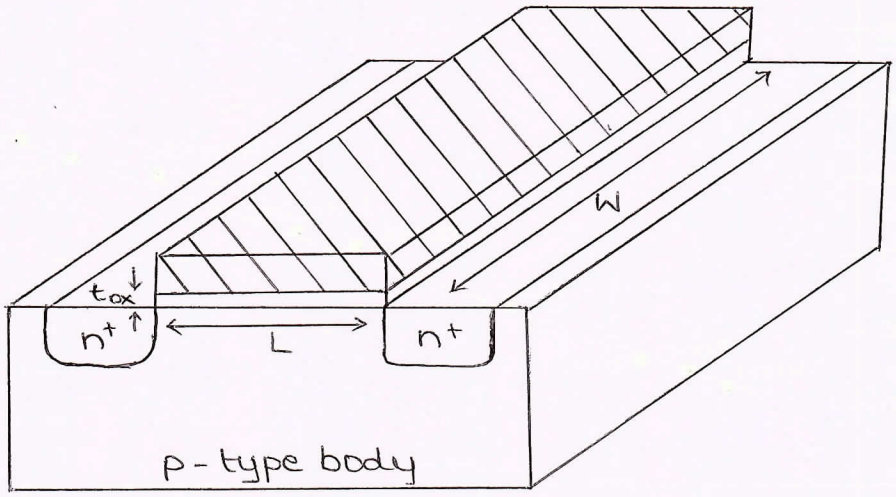




Charge on plate of capacitor

$$Q = CV$$

Charge in the channel is

$$Q_{channel} = C_g (V_{gc} - V_t) \rightarrow (1)$$

where, C_g : capacitance of gate to channel

V_{gc} : Minimum voltage for inversion

$$C_g = \frac{\varepsilon_{ox}}{t_{ox}} (W.L) \rightarrow (2)$$

But, $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \rightarrow (3)$$

For Si, $\varepsilon_{ox} = 3.9\ \varepsilon_0$

Every charge carrier is accelerated to velocity which is directly proportional to lateral electric field between drain & source.

i.e, $V \propto E \Rightarrow V = \mu E \rightarrow (4)$

where, μ : mobility of charge carrier

E : electric field.

$$E = \frac{V_{ds}}{L} \longrightarrow (5)$$

Time required for carriers to cross channel is

$$\text{Time} = \frac{\text{Distance}}{\text{Speed}}.$$

$$t = \frac{L}{V} \longrightarrow (6)$$

where, L : channel length

V : velocity

Current between drain and source.

$$I_{ds} = \frac{Q_{ch}}{t}$$

$$I_{ds} = \frac{Q_{ch}}{(L/V)} \quad | \because \text{eq (6)}$$

$$I_{ds} = \frac{C_g (V_{gc} - V_t)}{(L/V)} \rightarrow (8) \quad | \because \text{eq (1)}$$

$$I_{ds} = \frac{\varepsilon_{ox}}{t_{ox}} \frac{W.\cancel{K}(V_{gc} - V_t)}{\cancel{K}} \times \mu \frac{V_{ds}}{L}$$

$$| \because V = \mu E = \mu \frac{V_{ds}}{L}$$

Voltage between gate and channel.

$$V_{gc} = \frac{(V_{gs} + V_{gd})}{2}$$

$$= \frac{(V_{gs} + V_g - V_d)}{2}$$

$$= \frac{V_{gs}}{2} + \frac{V_{gs}}{2} - \frac{V_{ds}}{2} \quad | \because V_g = V_{gs} = V_g - V_s = V_g$$
$$V_d = V_{ds} = V_d - V_s = V_d$$

$$V_{gc} = V_{gs} - \frac{V_{ds}}{2} \rightarrow (9)$$

$$\therefore I_{ds} = \mu C_{ox} \frac{W}{L} \left[V_{gs} - V_t - \frac{V_{ds}}{2} \right] V_{ds} \rightarrow (10)$$

Taking $\mu C_{ox} \frac{W}{L} = \beta \rightarrow (11)$

$$\boxed{I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}}$$ (Linear Region)

In saturation region:

For $V_{ds} > V_{gs} - V_t$, pinch off occurs.

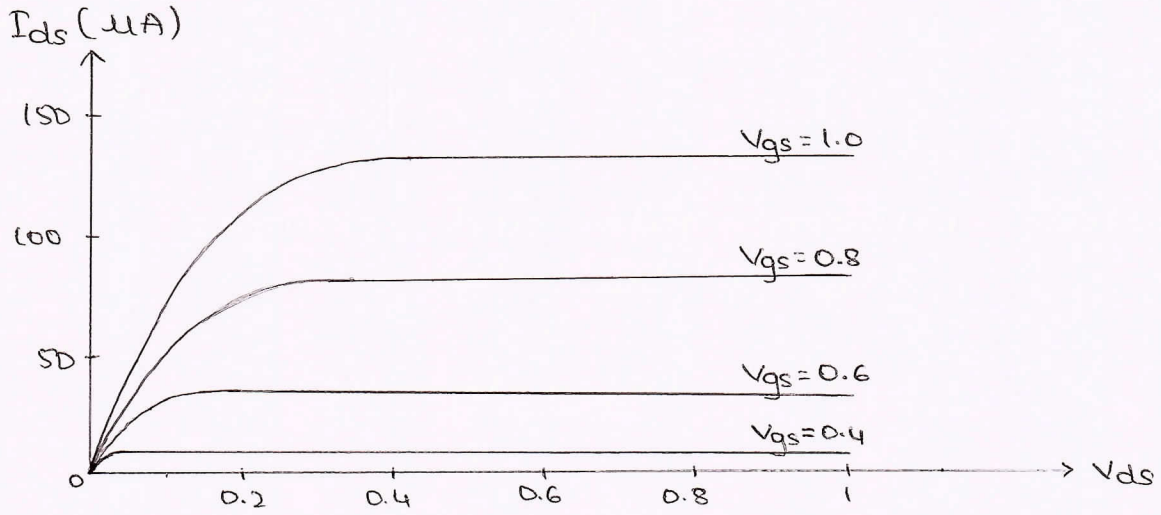
$\therefore$ Replacing V_{ds} by $V_{gs} - V_t$ (i.e, $V_{ds} = V_{gs} - V_t$)

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{(V_{gs} - V_t)}{2} \right) (V_{gs} - V_t)$$

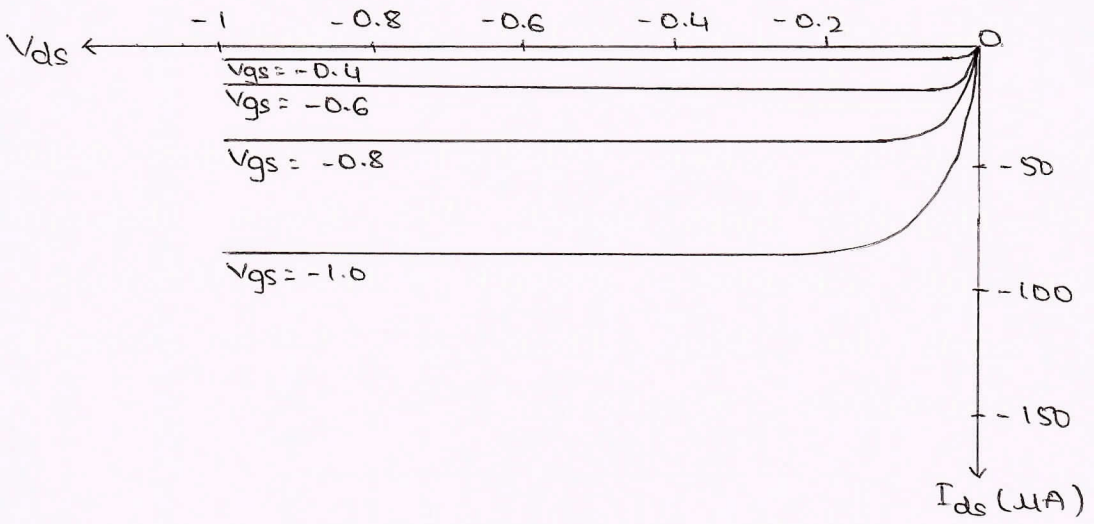
$$= \frac{\beta}{2} (2V_{gs} - 2V_t - V_{gs} + V_t)(V_{gs} - V_t)$$

$$= \frac{\beta}{2} (V_{gs} - V_t)(V_{gs} - V_t)$$

$$\boxed{I_{ds} = \frac{\beta (V_{gs} - V_t)^2}{2}}$$ (Saturation Region)



I - V characteristics of ideal nmos transistor



1.c. Explain the following non-ideal characteristics

i. Body effect

⇝ The threshold voltage of MOSFET will change because the voltage of bulk is not equal to voltage of source (or voltage difference between body and source) is called body effect.

$$V_t = V_{tno} + \gamma \left[\sqrt{2\phi + V_{SB}} - \sqrt{2\phi_b} \right]$$

when, $V_{SB} = 0$,

$$V_t = V_{tno}$$

where, V_{tno} : threshold voltage at $V_{SB} = 0$

γ : body effect parameter

V_{SB} : potential difference between source & substrate.

ϕ_b : bulk potential.

ii. Channel length modulation

⇝ Due to channel length modulation, the current changes and width of the channel reduces.

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

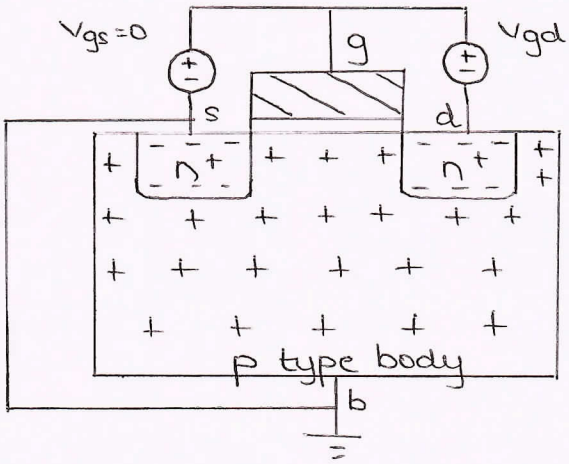
We know that, when MOSFET is under saturation part of channel gets pinch off. Even though 'L' is taken as channel length, the effective channel length will be less than L, when transistor is in saturation region,

$$L_{effective} = L - L_{short}$$

where, L_{short} is channel segment being pinch off. With increase in V_{ds}, L_{short} also increases and hence $L_{effective}$ gets reduced.

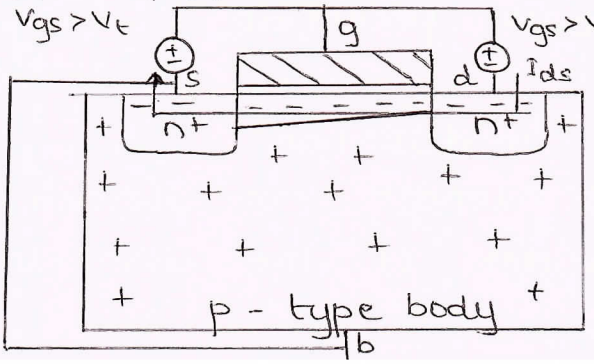
2.a. Explain working of nMOS enhancement mode transistor operation with neat sketches and relevant equations.

~> Cutoff region operation



→ $V_{gs} = 0$
→ No channel formed.
→ No current flow
→ $\therefore I_{ds} = 0$.

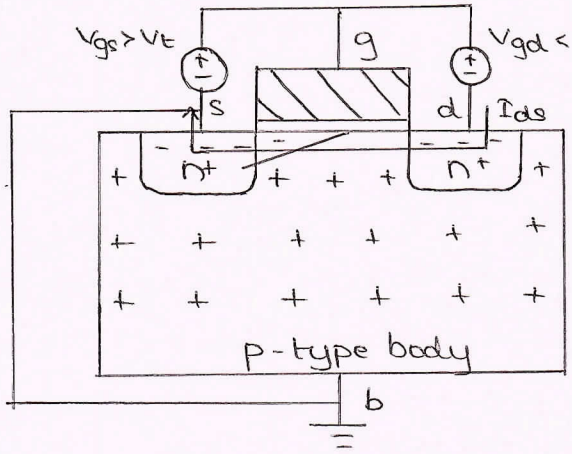
Linear region operation



$0 < V_{ds} < V_{gs} - V_t$

→ $V_{gs} > V_t$
→ Channel formed.
→ If $V_{gs} = V_{gd} \Rightarrow V_{ds} = 0$ hence no current flows between drain and source.
→ If $V_{gs} > V_{gd} > V_t$, I_{ds} current flows between source and drain.
→ I_{ds} increases with V_{ds}.

Saturation Region operation



→ V_{ds} increased further
→ pinch off happens due to increased depletion region
→ I_{ds} saturates.

2.b. Draw inverter circuit and explain its DC transfer characteristics

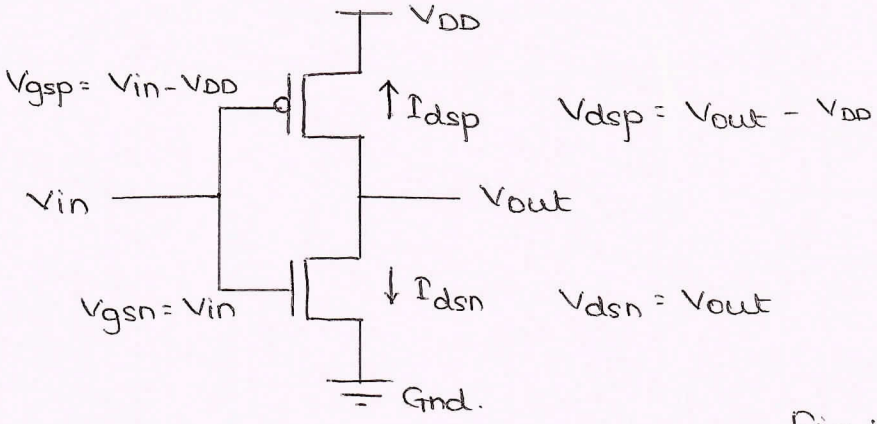


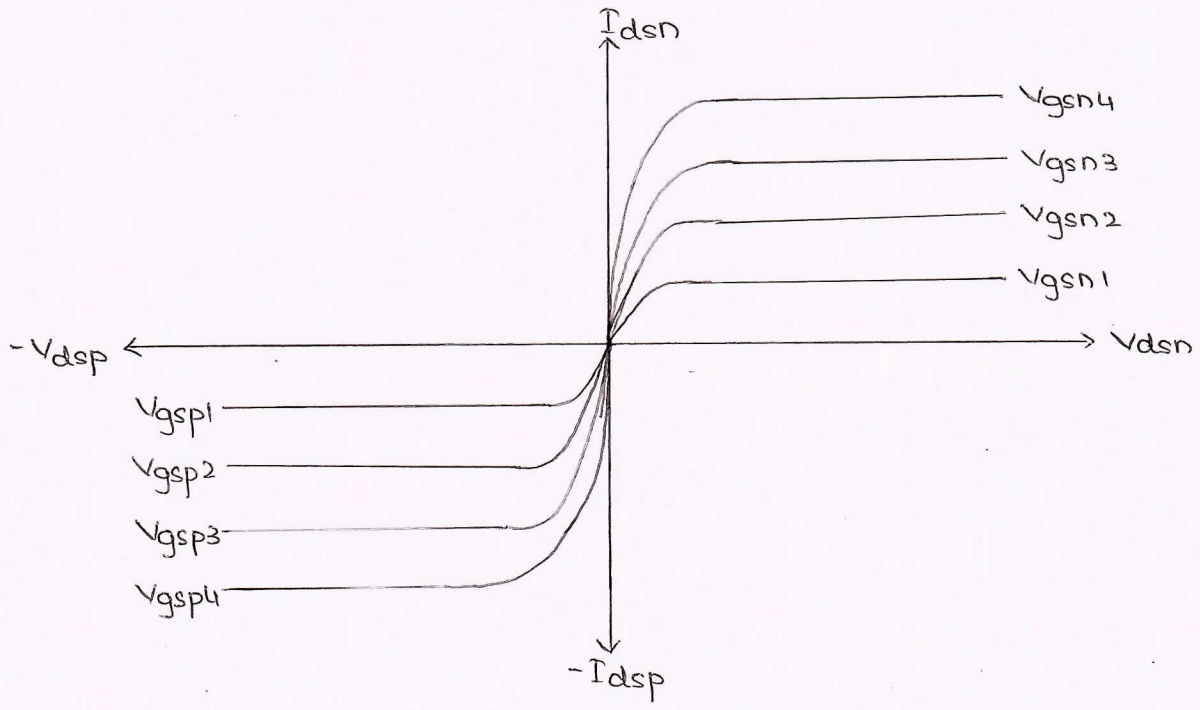
Fig: CMOS inverter.

- CMOS inverter consists of pmos and nmos transistors, the gate and drain terminals are connected.
- V_{DD} is connected to pmos source. Gnd is connected to nmos source
- V_{tn} is threshold voltage for nmos and V_{tp} is

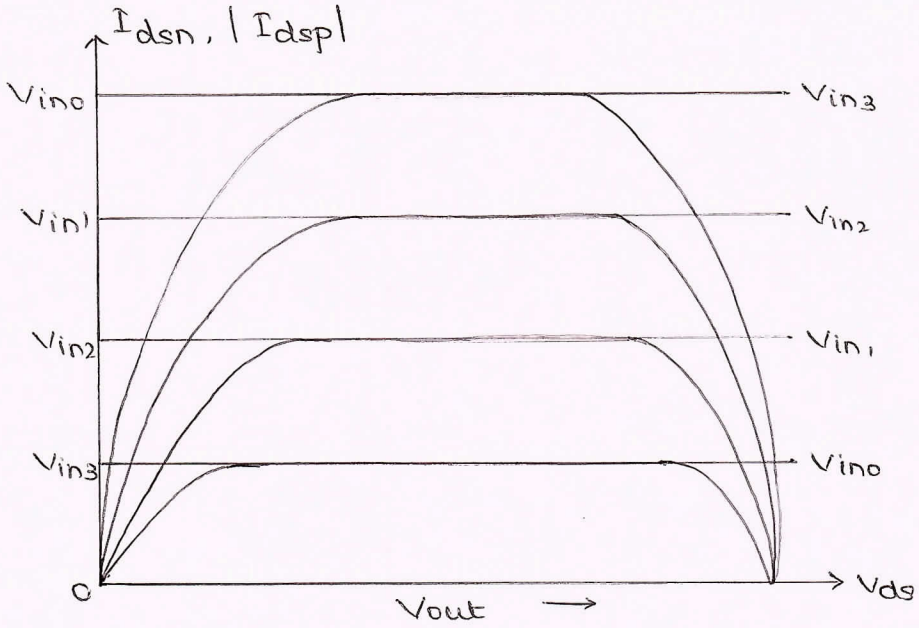
threshold voltage for pMOS.

- V_{tp} is -ve for pMOS.
- $V_{gsn} = V_{in}$; $V_{gsp} = V_{in} - V_{DD}$
- $V_{dsn} = V_{out}$; $V_{dsp} = V_{out} - V_{DD}$

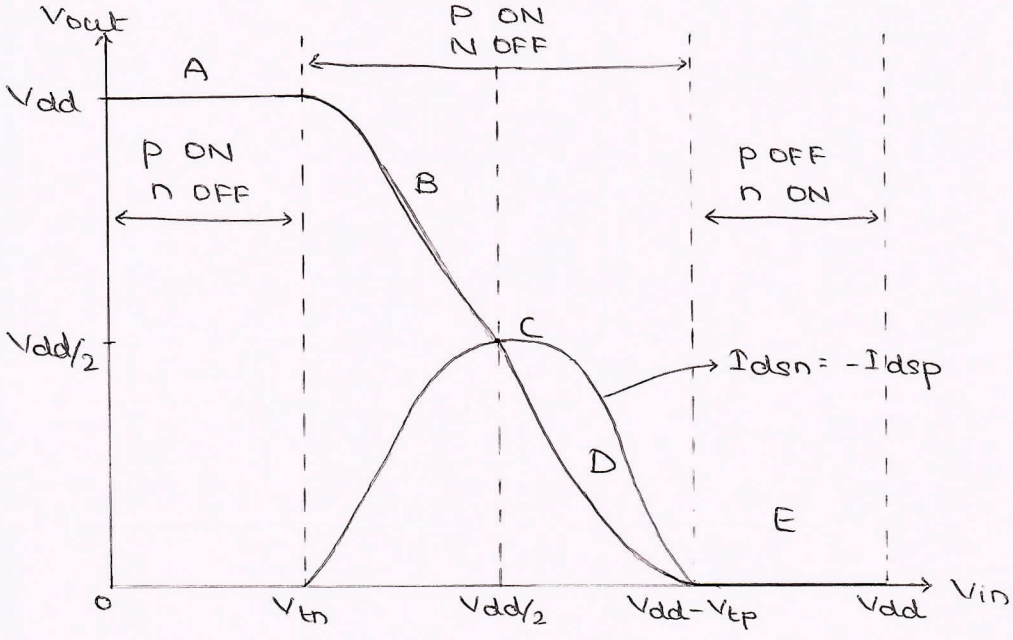
MOSFET	Cutoff	Linear	Saturation
nMOS	$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$ $V_{in} > V_{tp} + V_{DD}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{dd}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{dd}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$.



Plot shows I_{dsn} and I_{dsp} in terms of V_{dsn} & V_{dsp} for various values of V_{gsn} and V_{gsp}.



Plot shows Idsn and Idsp in terms of Vout for various values of Vin

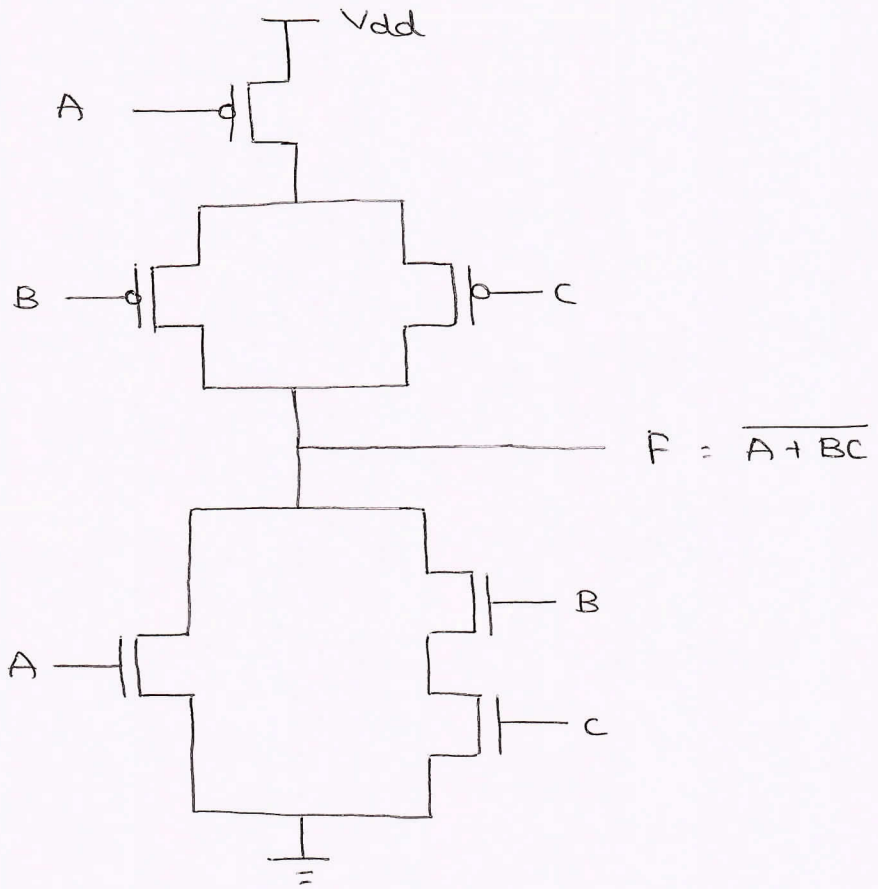


DC transfer characteristics of Inverter.

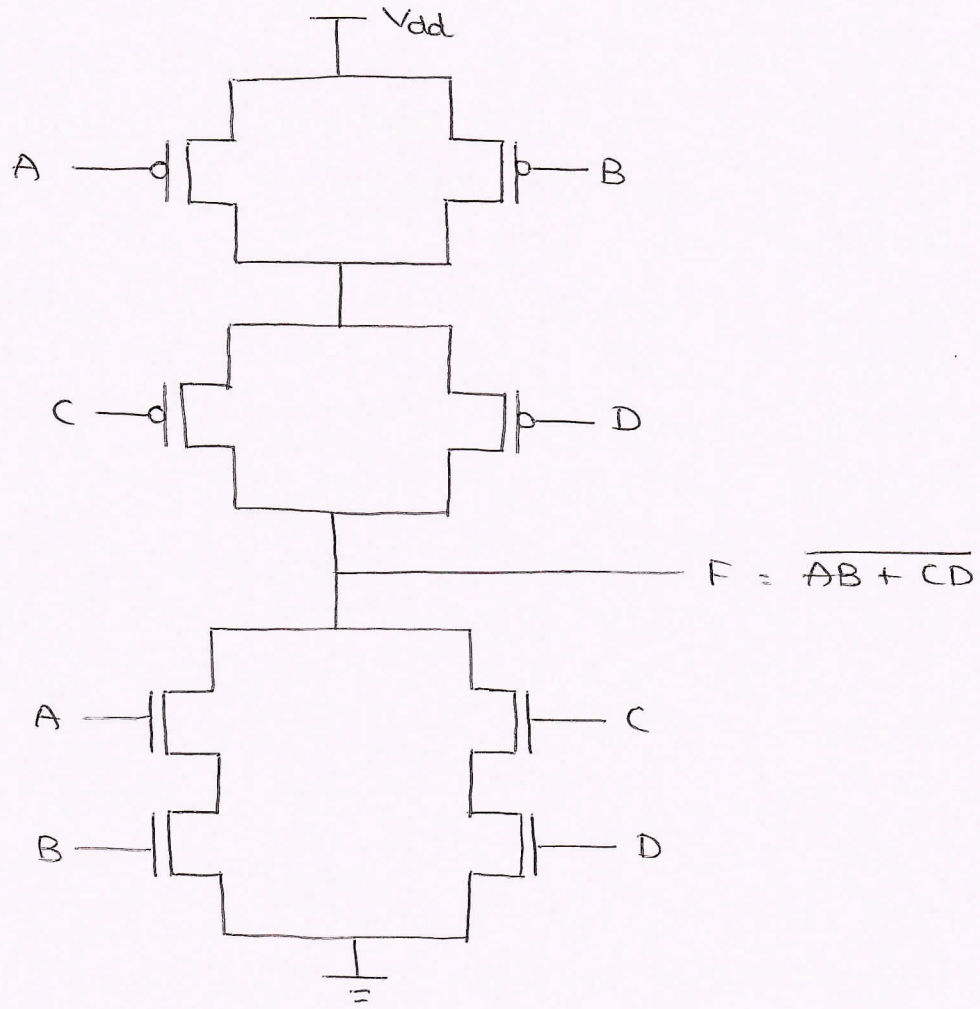
Region	Condition	pMOS	nMOS	Output
A	$0 \leq V_{in} \leq V_{tn}$	Linear	Cut-off	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} \leq \frac{V_{DD}}{2}$	Linear	Saturation	$V_{out} > \frac{V_{DD}}{2}$
C	$V_{in} = \frac{V_{DD}}{2}$	Saturation	Saturation	$V_{out} = \frac{V_{DD}}{2}$
D	$\frac{V_{DD}}{2} \leq V_{in} \leq \frac{V_{DD}}{2} - \lvert V_{tp} \rvert$	Saturation	Linear	$V_{out} < \frac{V_{DD}}{2}$
E	$V_{in} > \frac{V_{DD}}{2} - \lvert V_{tp} \rvert$	Cut-off	Linear	$V_{out} = 0$.

2.c. Draw the schematic of

i. $F = \overline{A + BC}$



ii. $F = \overline{AB + CD}$



Module - 2

3.a. Explain CMOS fabrication process with necessary diagrams.

⇝ Fabrication of CMOS can be done using following methods.

- n - well process
- p - well process
- twin - well process
- triple - well process.

Making of CMOS using n-well process

In this process, an n-type well is diffused on a p-type substrate

Step 1: Choose a p-substrate as base for fabrication

Step 2: Develop a protective layer of oxide over entire wafer.

Step 3: An organic photoresist is placed on the SiO_2 layer.

Step 4: The photoresist is exposed to n-well mask.

Step 5: The softened photoresist is removed to expose oxide.

Step 6: The oxide is etched with hydrofluoric acid

Step 7: Remaining photoresist is stripped away using mixture of acids.

Step 8: The well is formed where substrate is not covered with oxide

Step 9: The remaining oxide is stripped

Step 10: A thin layer of oxide and polysilicon is placed over the wafer.

Step 11: The wafer is patterened with photoresist and polysilicon mask leaving polysilicon gates atop the thin gate oxide.

Step 12: A protective layer of oxide is formed and patterned with n diffusion mask.

Step 13: The n^+ regions are introduced for transisto active area

Step 14: Finally the protective oxide is stripped.

Step 15: The process is repeated for p-diffusion mask.

Step 16: The process is repeated for p-diffusion

Step 16: The field oxide is grown to insulate wafer from metal and patterned with contact mask to leave contact cuts where metal should attach to diffusion or polysilicon.

Step 17: The metal is patterned with metal mask and plasma etched to remove metal everywhere except where wires should remain.

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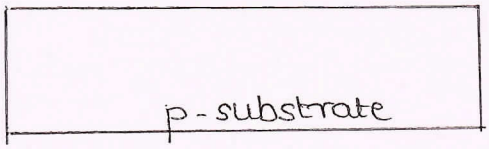

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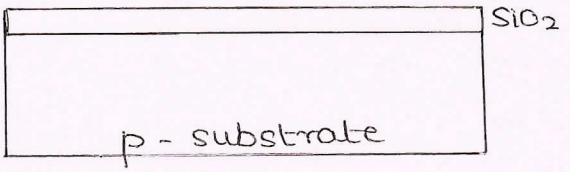

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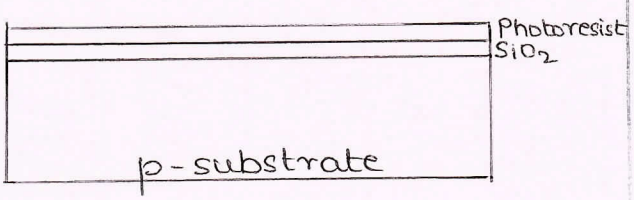

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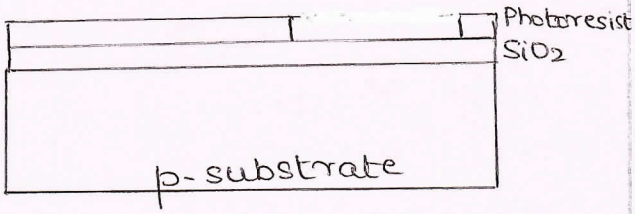

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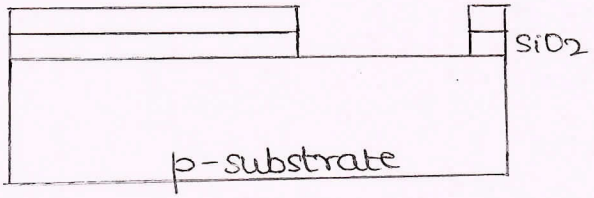

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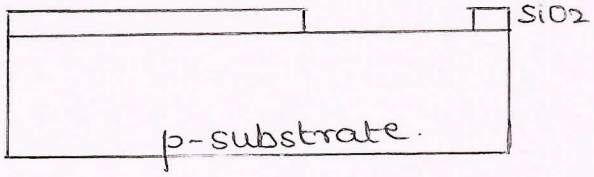

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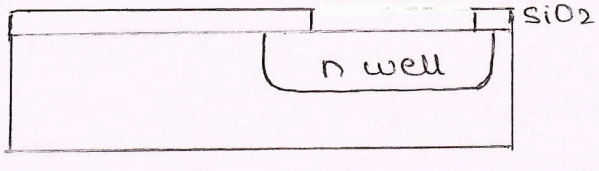

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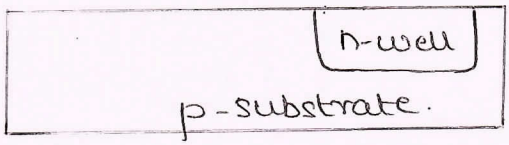

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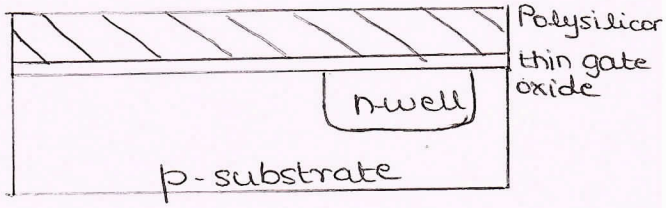

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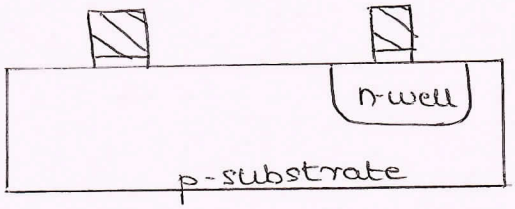

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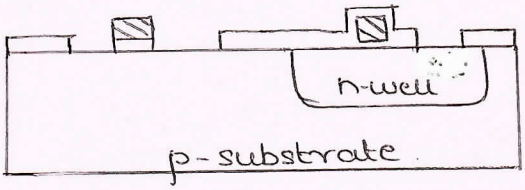

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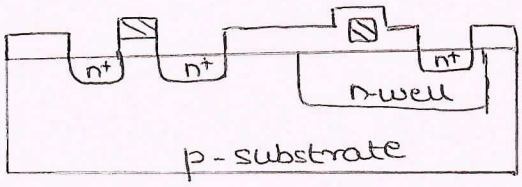

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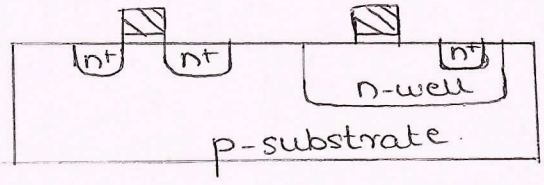

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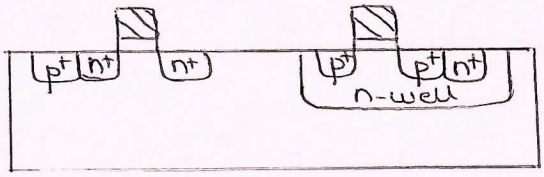

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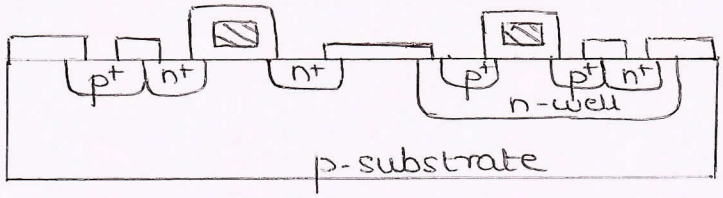

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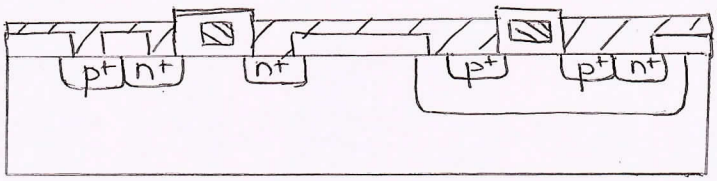


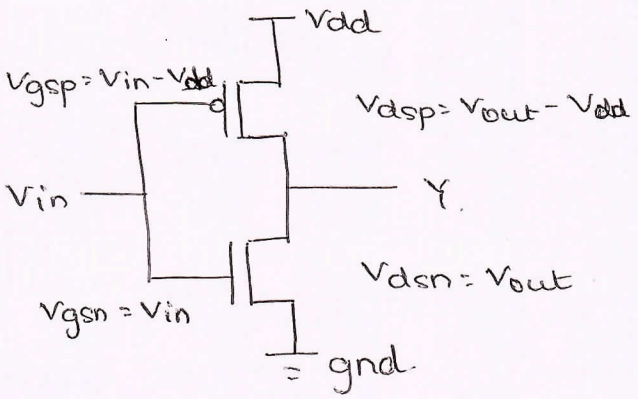
Making of CMOS using p-well process.

The p well process is similar to n well process except that n-type substrate is used and p-type diffusions are carried out.

In case of twin-well process, only one mask need to be defined because the other well by definition is its complement.

Triple well process have to define at least two masks, one for deep well and the other for either n-well or p-well.

3.b. With relevant equations, explain transient response of CMOS inverter.



nmos:

Cut-off: $V_{gsn} < V_{tn}$

Linear: $V_{gsn} > V_{tn}$

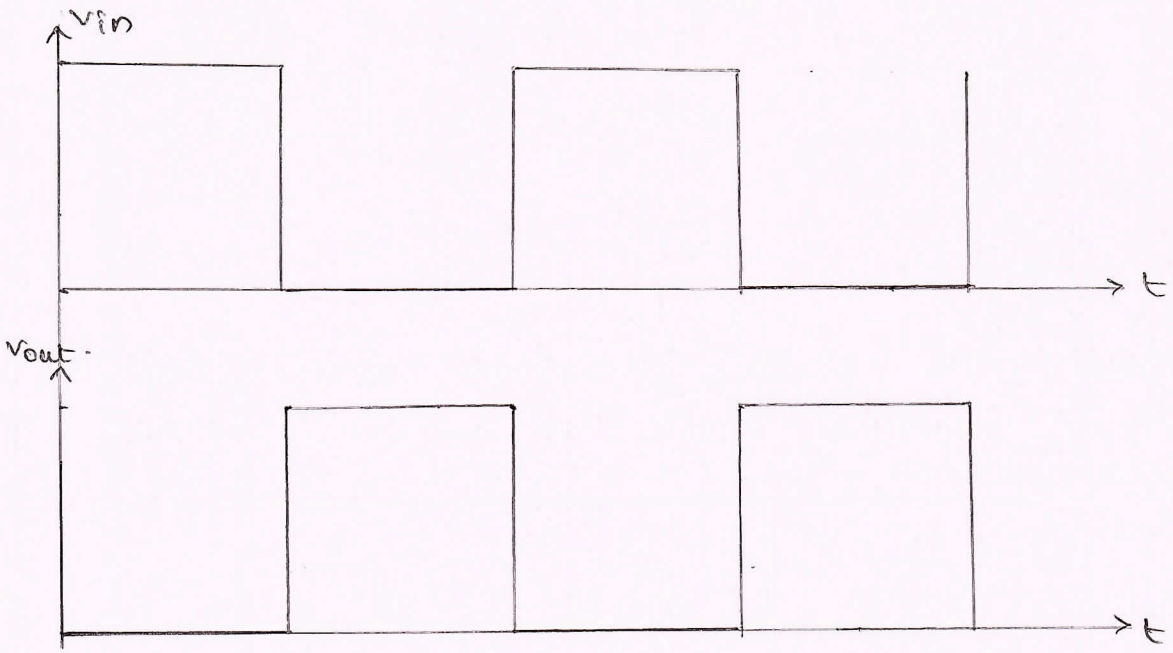
Saturation: $V_{gsn} > V_{tn}$

pmos:

Cut-off: $V_{gsp} > V_{tn}$

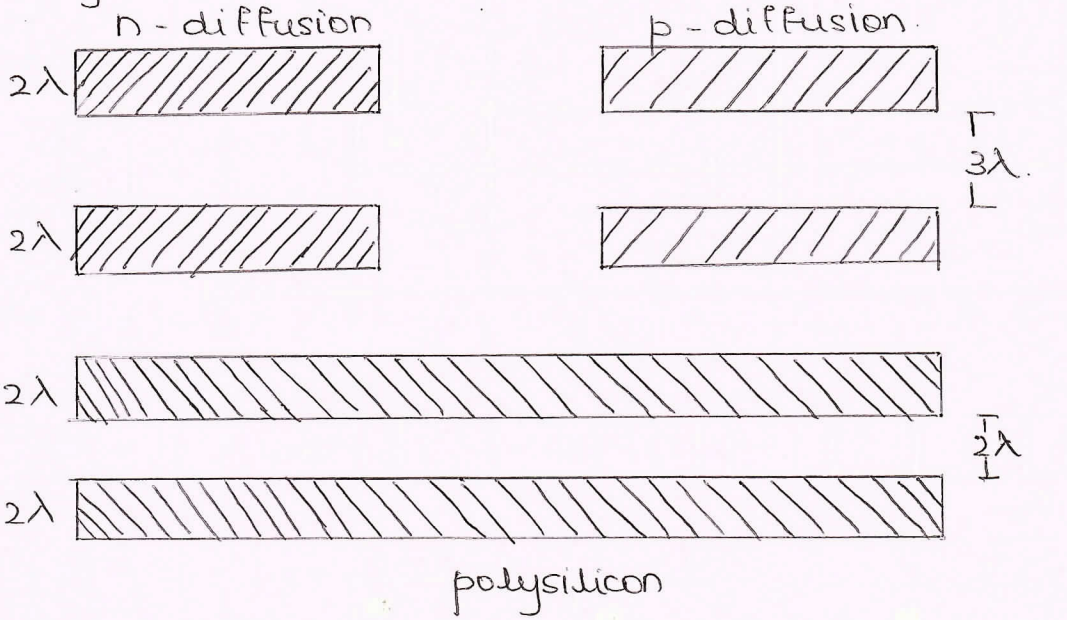
Linear: $V_{gsp} < V_{tp}$

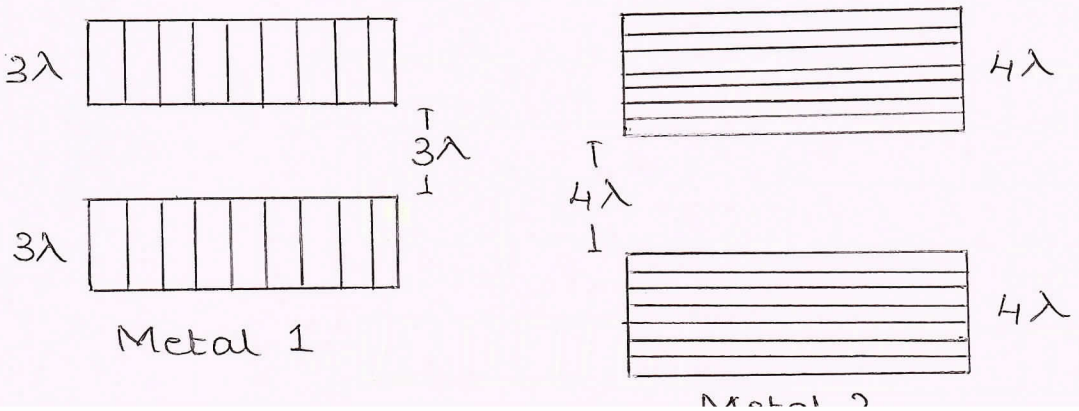
Saturation: $V_{gsp} < V_{tp}$

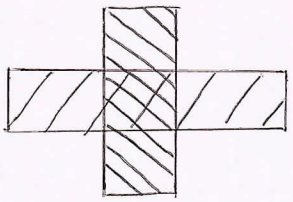


3.c. With neat diagram explain layout design rules

~> Design rules for wires.

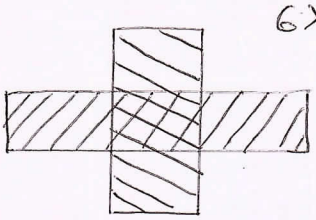






6λ×6λ.

pmos

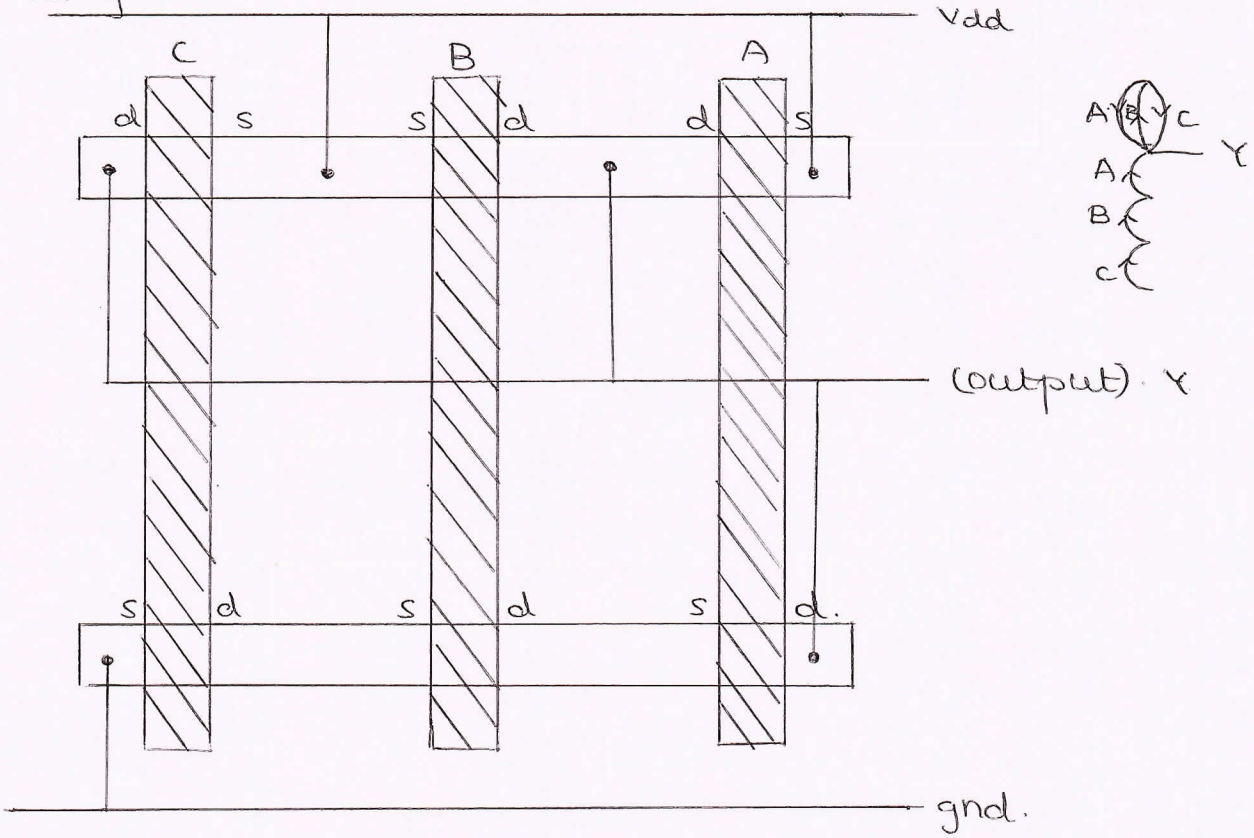


6λ×6λ.

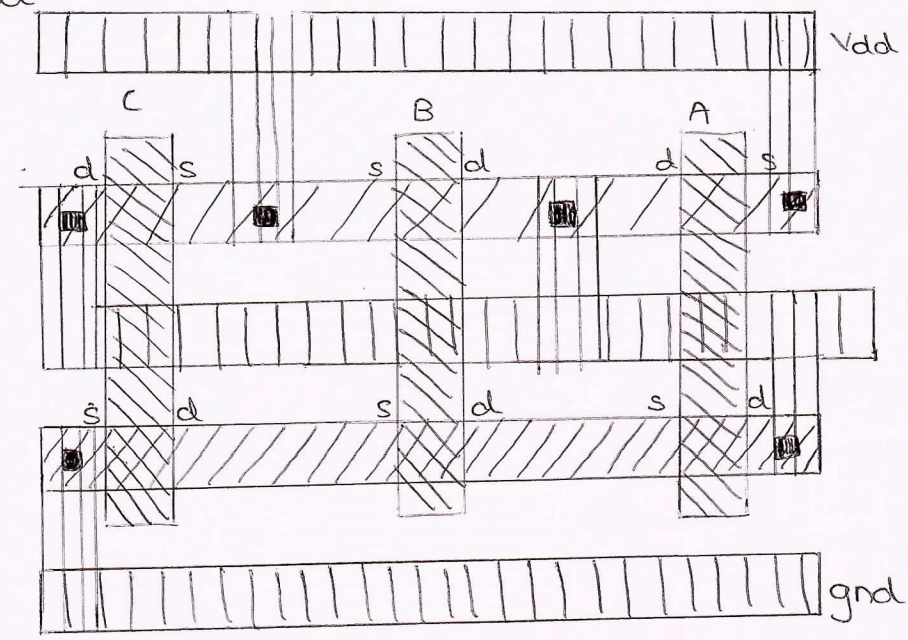
nmos

4.a. Draw the stick diagram and layout of three input NAND gate

⇝ Stick diagram

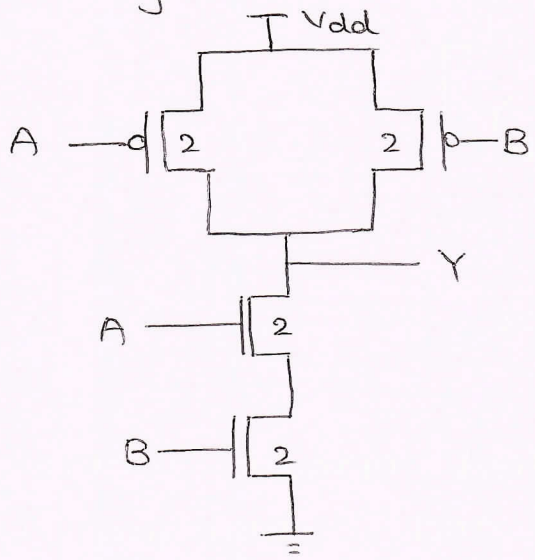


Layout



4.b. Find maximum and minimum rise time and fall time delays of two input NAND gate.

~>

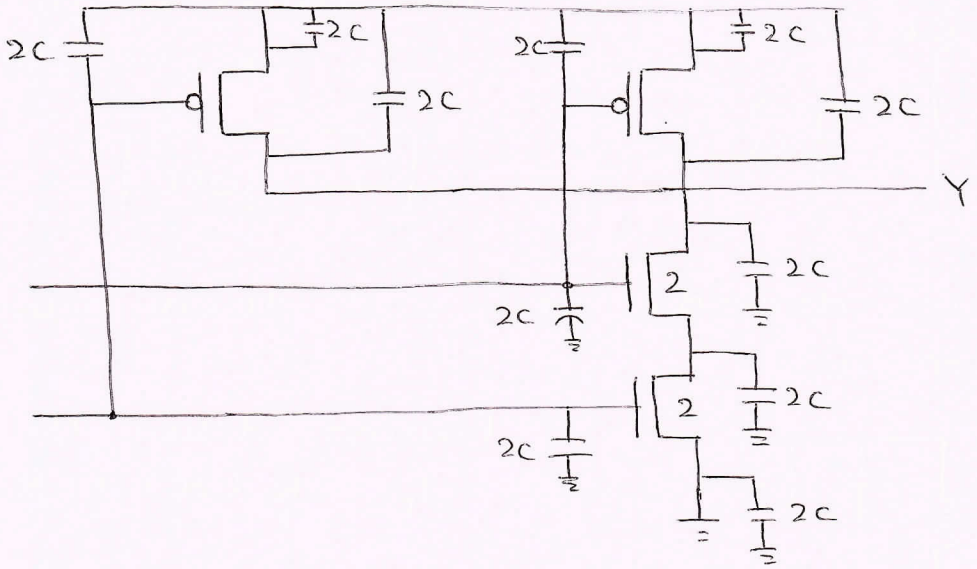


→ Fig shows 2 i/p NAND gate.

→ Two nMOS transistors are in series, the resistance is 2 times that of single transistor

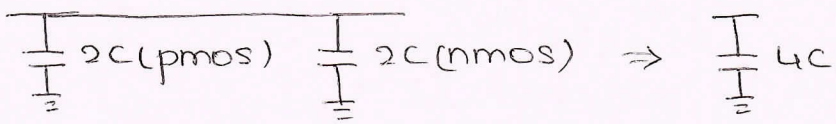
→ Each transistor has resistance R/2 and series combination has resistance R.

→ Two pMOS transistor are parallel. In worst case only 1 pmos transistor is ON. Therefore each transistor has resistance 2R to have resistance R.

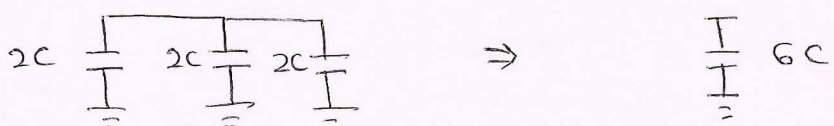


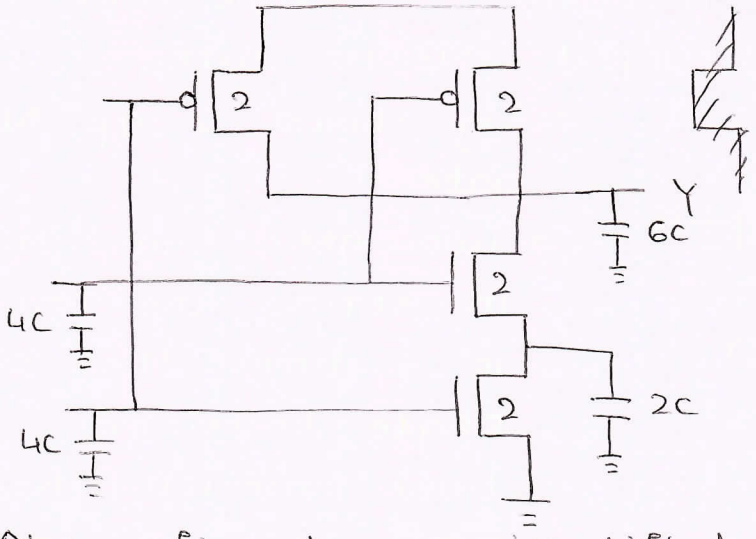
→ Above fig shows the capacitance of capacitors.

→ At each input



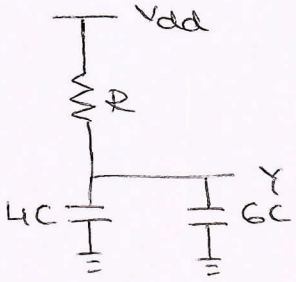
At node Y





Above fig shows simplified circuit where irrelevant capacitors are deleted and remaining capacitors are lumped to ground.

Rise time depends on pull-up network which is given by

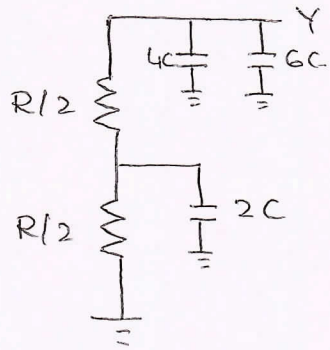


The rising delay is

$$T_r = R\,[4C + 6C]$$

$$\boxed{T_r = 10RC}$$

Fall time depends on pull down network which is given by



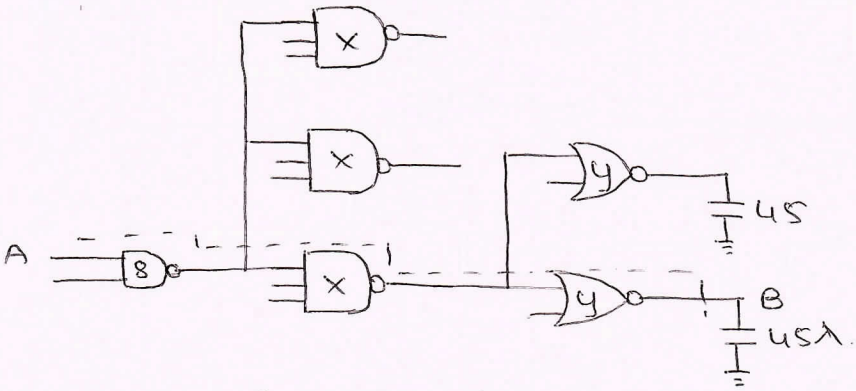
Falling delay is

$$T_F = \frac{R}{2}(2C) + \left(\frac{R}{2} + \frac{R}{2}\right)(4C + 6C)$$

$$= RC + R(10C)$$

$$\boxed{T_F = 11RC}$$

4.c. Estimate the minimum delay of the path from A to B in fig & choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on input and the output load is equivalent to 45λ of transistor width.



⇝ $G = (4/3) \times (5/3) \times (5/3) = 100/27$.

$H = 45/8$.

$B = 3 \times 2 = 6$.

$F = GBH = 125$.

$f = \sqrt[3]{F} = \sqrt[3]{125} = 5$.

$P = 2 + 3 + 2 = 7$

$D = 3 \times 5 + 7 = 22$ in units of τ.

The gate sizes are:

$y = 45 \times (5/3) / 5 = 15$

$x = (15 + 15) \times (5/3) / 5 = 10$.

Initial NAND gate has specified size of

$(10 + 10 + 10) \times (4/3) / 5 = 8$.

The transistor size are choosen to given desired amount of input capacitance while achieving equal rise & fall delays.

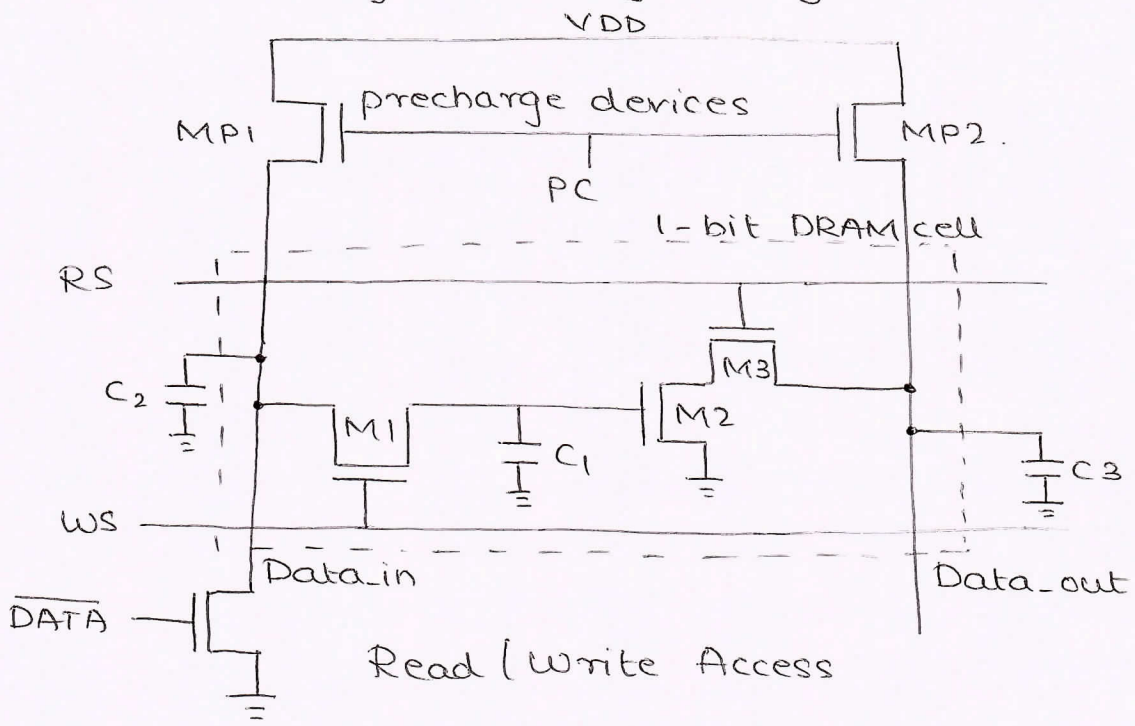
The NAND2 gate delay is

$d_1 = g_1 h_1 + p_1 = (4/3) \times (10 + 10 + 10) / 8 + 2$

$d_1 = 7$

Module - 3

5.a. Explain operation of three transistor DRAM cell with necessary timing diagrams.



→ Circuit works on 2 non-overlapping clocks.
→ Circuit has 3-transistor basic DRAM for storing data, 2 transistors MP1 and MP2 for precharging capacitor C2 & C3.
→ During precharge phase, PC is made high.

Writing data 1

→ When data = 1, $\overline{data}$ = 0. Transistor MP is OFF. data_in = HIGH.
→ During write operation : WS signal = HIGH which turns on transistor M1.
→ Charge is shared between C2 & C1. C1 charges upto V_{DD}.

Reading data 1

→ RS is made HIGH. Which turns on transistor M3
→ HIGH voltage at C1 turns ON M2. and discha

-ge path is opened for C3.
→ Capacitor C3 discharges via M3 & M2 & this discharge is sensed at output of the circuit.

Writing data 0
→ When data = 0, $\overline{data}$ = 1 transistor MP = ON.
Data_in = low.
→ WS signal = HIGH. which turns ON M1.
→ C1 will hold charge 0.

Reading data 0
→ RS = HIGH which will turn ON M3.
→ 0V at C1 turns OFF M2.
→ There is no flow of current from C3 which completes reading 0 operation.

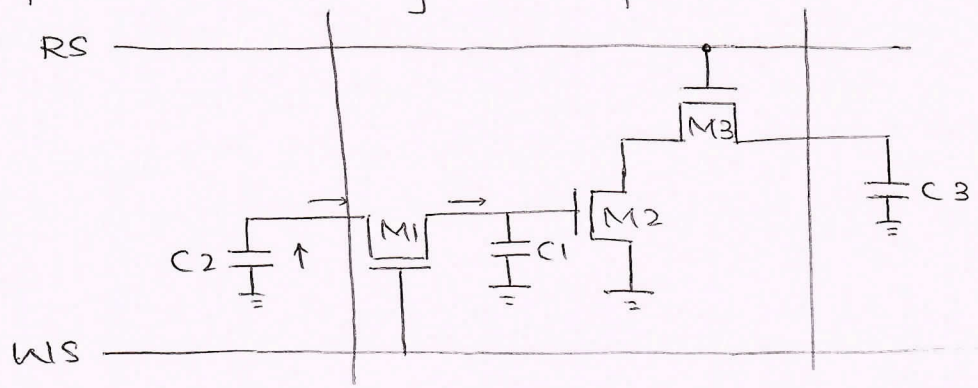


Fig: charge sharing between C1 & C2 during write 1

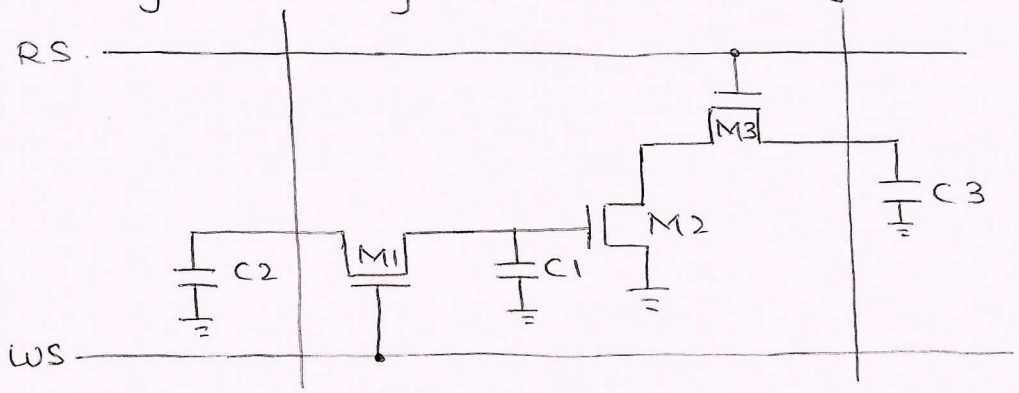
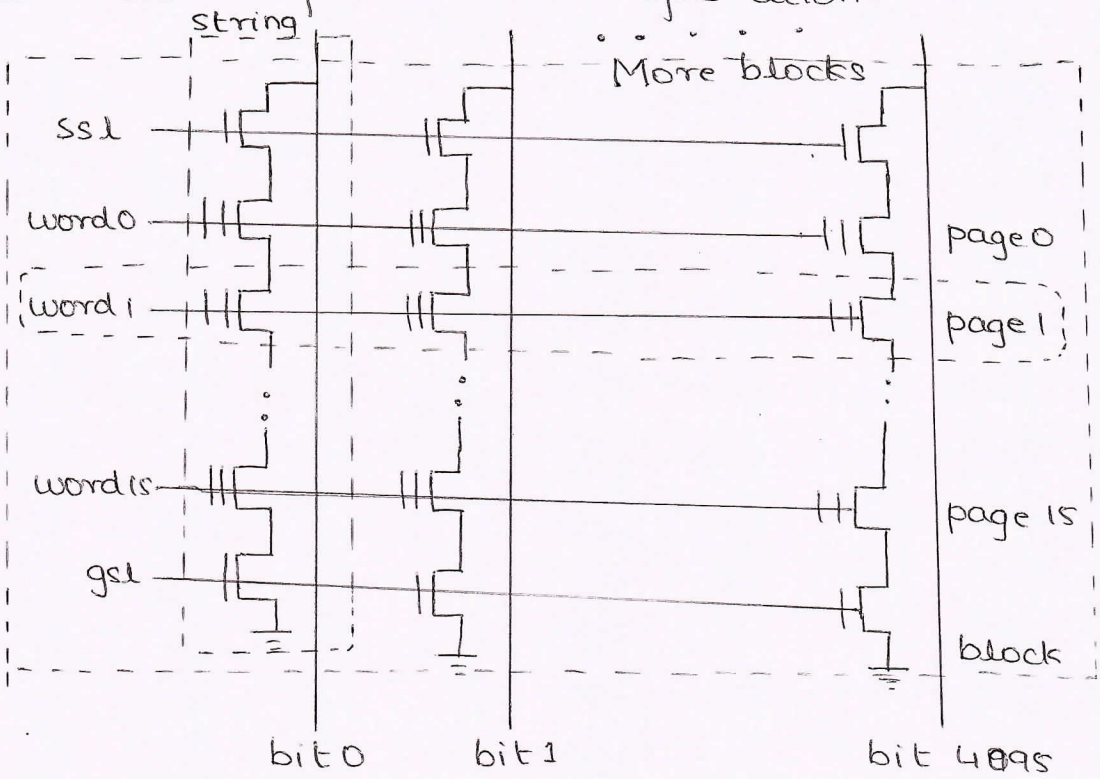


fig: C3 discharged through M2 & M3 during read 1.

5.b. Draw the structure of NAND flash memory cell and explain the operation.



NAND flash is organized into blocks, which are further divided into pages. Each memory cell in NAND flash is a floating gate transistor. Charge on floating gate affects transistors threshold.

In NAND ~~gate~~ flash, floating gate transistors are connected in series to form a string. A typical string might have 16 cells connected in series with string select transistor at one end and ground select transistor at the other. These strings are organized into columns, with each column corresponding to a bit in a page.

Operations

1. Erase operation: Erases data by setting all cells in a block to logic 1 using a high voltage to remove electrons from floating gates.
2. Program operation: Write data by changing selected cells from logic 1 to logic 0 using high

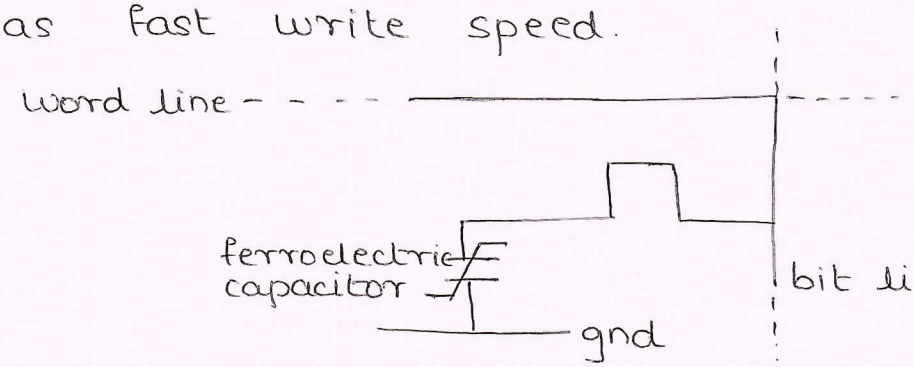
voltage to add electrons to the floating gates.

3. Read operation : Reads data by checking threshold voltage of cells to determine if they store 1 or 0.

S.C. Explain ferroelectric RAM with necessary diagrams

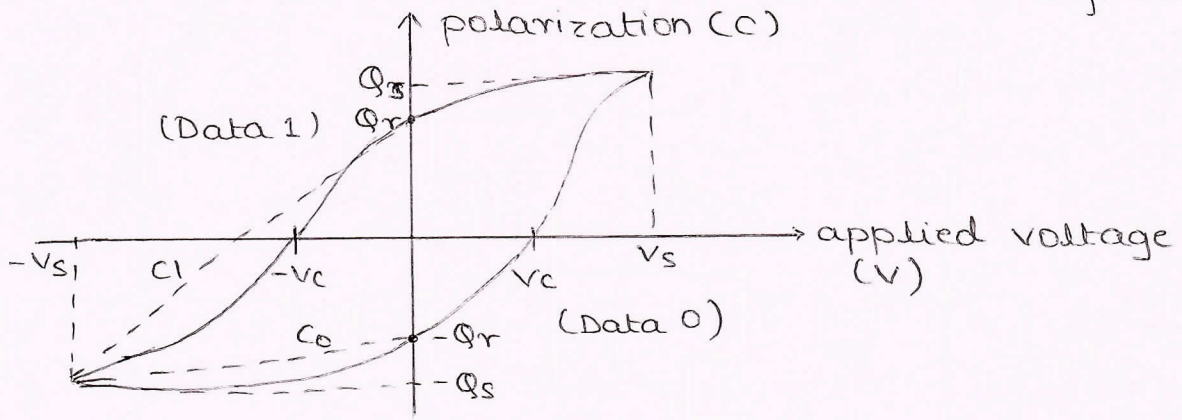
~> • Ferroelectric memories use ferroelectric capacitor.

• It is non volatile memory & consumes less power & has fast write speed.



• Read and write operation takes place by switching state of capacitor.

Hysteresis characteristics of ferroelectric capacitor



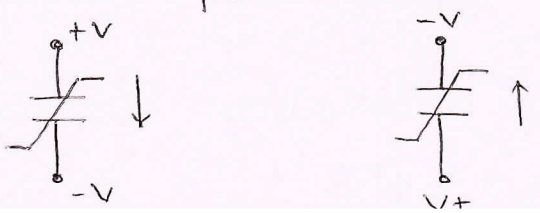
Q_r & $-Q_r$: remnant charge

Q_s & $-Q_s$: saturation charge.

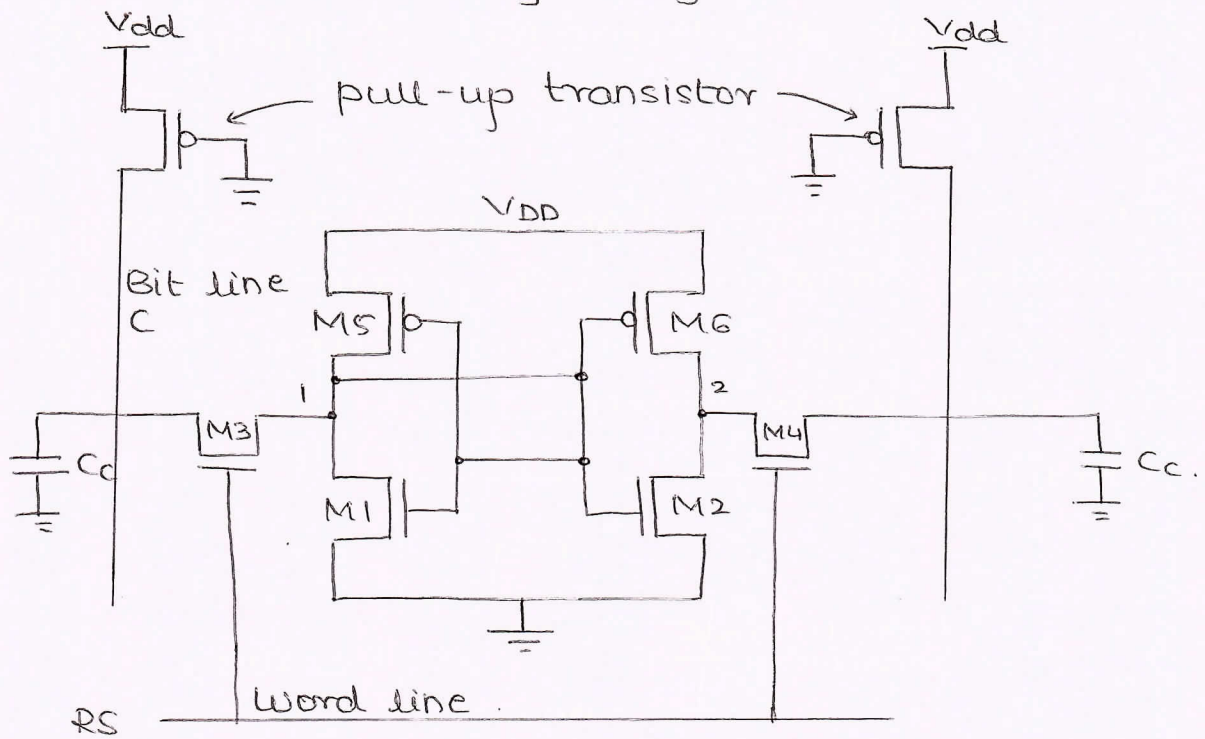
V_c : saturation voltage.

C_0 & C_1 : linear capacitance for data 0 or 1

Two states of polarization

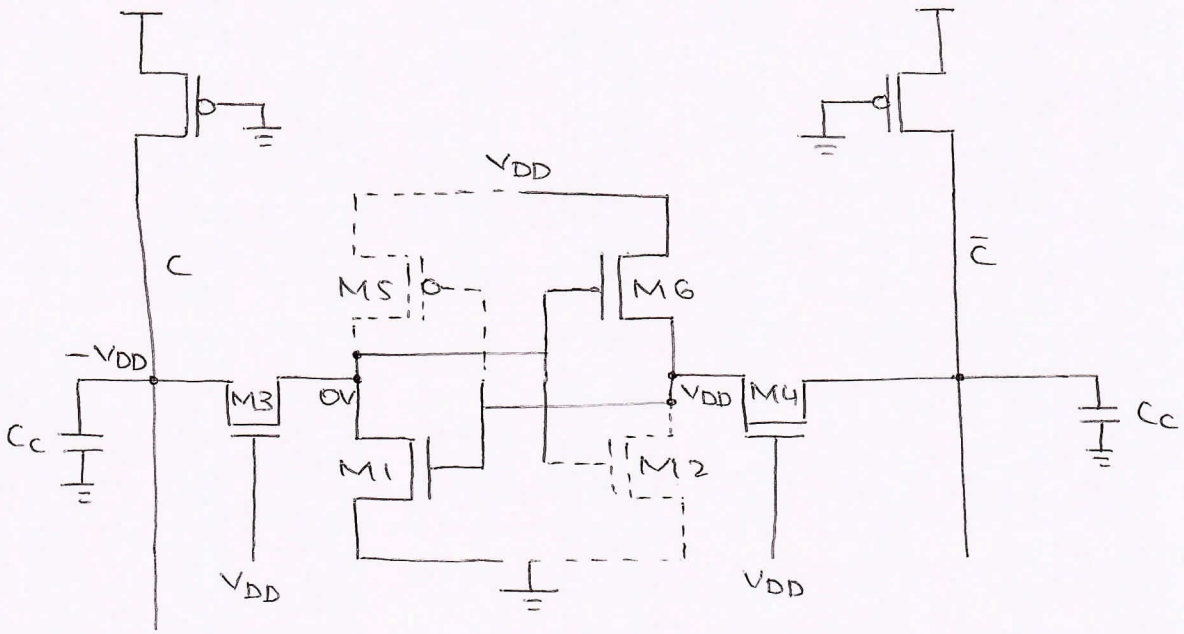


6.a. Explain read and write operation of SRAM cell with necessary diagrams.



Data Read Operation (Read 0)

- Assume logic 0 is stored in the cell.



Voltage level in SRAM cell at beginning of read operation.

- M2 & M5 are OFF, M2 & M6 are ØN in linear mode. Internal node voltage $V_1 = 0$ & $V_2 = V_{DD}$.
- Before cell access, transistor M3 & M4 are turned ON.

- After M3 & M4 turn ON by row selection circuitry voltage level of column $\bar{C}$ will not show any significant variation.
- On other half M3 & M1 will conduct non-zero current. C will begin to drop slightly.
- M1 & M3 discharge through C_c. V_1 will increase from initial value.

Data Write Operation (write 0)

- Assuming logic 1 is stored in cell.
- M1 & M6 are OFF while M2 & M5 operate in linear mode.
- Internal node voltages are $V_1 = V_{DD}$ & $V_2 = 0V$.
- Before cell access M3 & M4 turn ON.
- Column voltage is forced to 0.
- When M3 & M4 are ON, V_{th} of M1.
- Consequently voltage level at node 2 would not turn ON M1.
- To change stored information, force V_1 to 0V & V_2 to V_{DD}. V_1 must be reduced below V_{th}. of M_2, so that M_2 turns OFF first.
- M2 will be forced into cut-off during write 0. If above condition is satisfied, M1 turns ON changing stored information

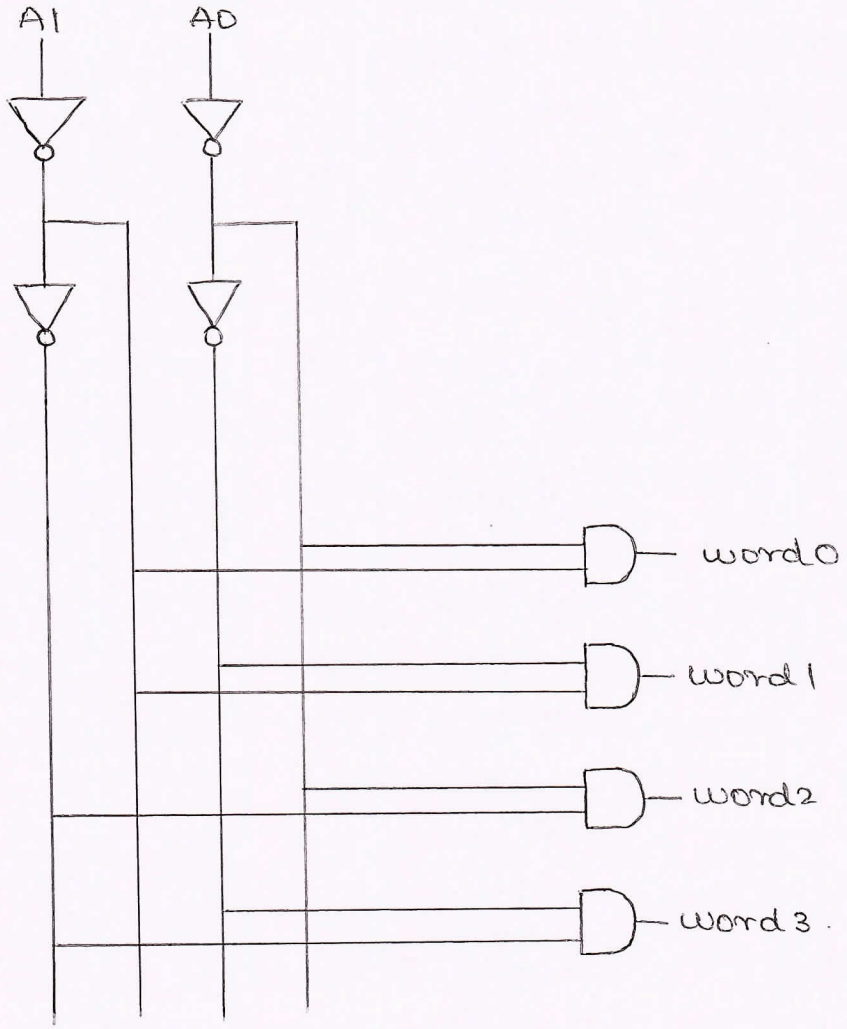
6.b. What is row decoder ? Explain with an example

⇝ A row decoder is a crucial component in memory array like SRAMs and ROMs. It is responsible for selecting specific rows that is to be accessed based on address input.

Simplest form of row decoder is collection of AND gates which can be used to decode the input address bits. Each output of AND gate corresponds to a unique row in the memory array.

For example, in 4-word memory array decoder would have two address lines (A0 and A1) and four outputs (word 0, word 1, word 2, word 3). Output line would activate based on the combination of address bits:

- When A0=0 and A1=0, word0 is activated.
- When A0=0 and A1=1, word1 is activated.
- When A0=1 and A1=0, word2 is activated.
- When A0=1 and A1=1, word3 is activated.



6.c. Explain data programing and erasing methods of flash memory

~> Programming flash memory

- Flash memory is programmed by tunneling electrons onto the floating gate of memory cell.
- To program a cell, the control gate is raised to high voltage while source is left floating & drai

is held at low voltage. This causes electron to tunnel from substrate into floating gate, changing its charge state and threshold voltage.

- Programming flash memory cell sets V_{th} high, representing logical 0.

Erasing Flash Memory

- Flash memory cells are erased by removing electro-ns from floating gate. This is done using tunneling in opposite direction.
- During erasing, high electric field causes electron to tunnel from floating gate back to substrate, effectively resseting cells to logical 1.

Module - 4

7.a. Briefly explain different types of faults in digital circuit.

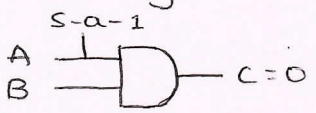
⇝ Types of faults.

1. Stuck at fault.
2. Bridging fault.
3. Stuck open fault and stuck on faults.
4. Delay faults.

1. Stuck at fault.

In fault in a logic gate results due to one of its input or output being fixed at logic 0 (sa0) or logic 1 (sa1)

Ex: NAND gate s-a-1



line A is always s-a-1 hence output C=0. always.

- But when A=0, B=1, $C = \overline{A.B} = \overline{0.1} = \bar{0} = 1$

1 should have been the answer.

2. Bridging faults

- Unintended shorts between lines form a class of permanent faults known as bridging faults.

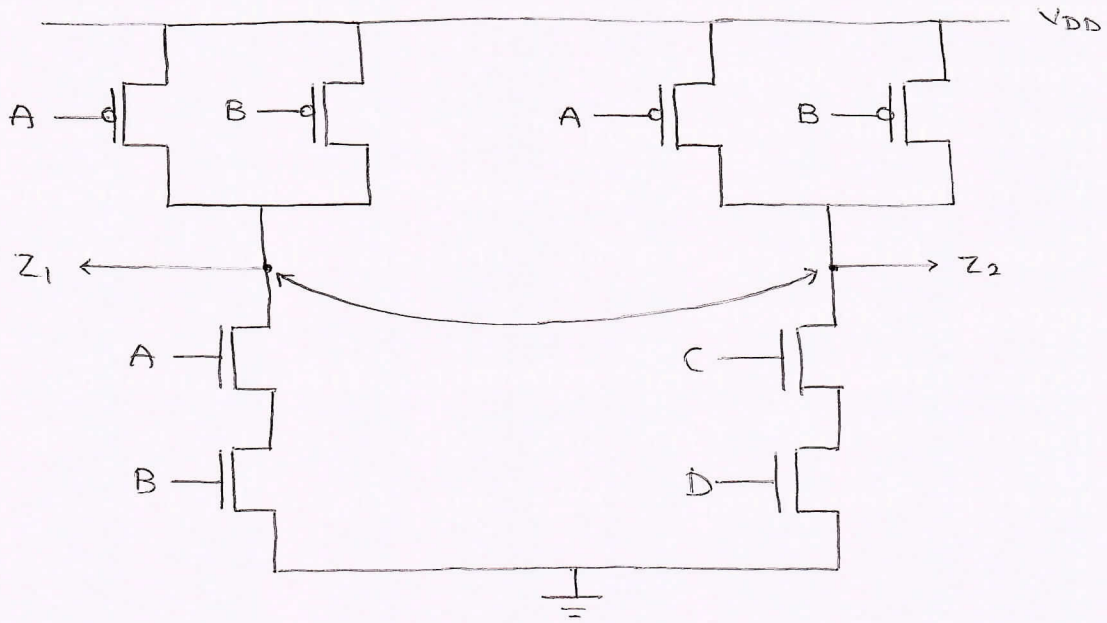


fig: Short between outputs Z_1 and Z_2.

- 3 types of bridging faults.

1. Input bridging: Shorting of certain primary i/p lines.
2. Feedback bridging: If short between i/p & o/p lin
3. Non-feedback bridging: If short is not between i/p bridging or feedback bridging.

3. Stuck open faults and stuck on faults

- Stuck on faults implies permanent closing of path between source & drain of transistor.
- Stuck open faults implies permanent opening of connection between source & drain of transistor

4. Delay faults

2 types of delay faults

i. Gate delay faults: used to model defects that cause actual propagation delay.

ii. Path delay faults: used to model isolated as wel as distributed defects.

7.c. Explain detection of multiple faults in combinatorial logic circuits.

~> • Fault collapsing

• Procedure.

1. Assign fault to every gate input line if that is primary i/p or fanout branch line. Fault is s-a-1 for AND/NAND gate inputs and s-a-0 for OR/NOR gate input.
2. Identify every gate that has faults assigned to all i/p lines as primary gate.

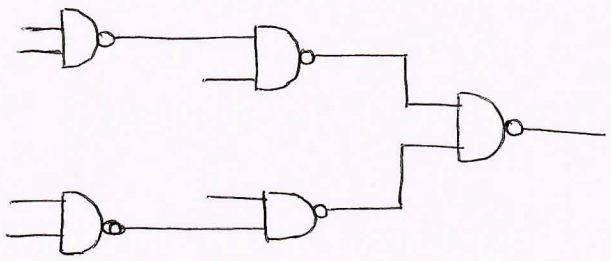
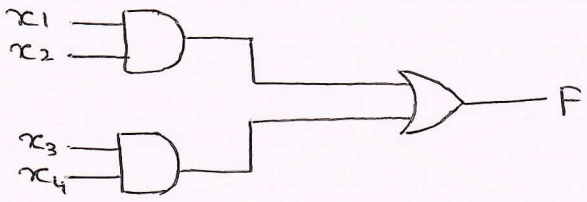


fig: multi level fan out free network.

• Restricted fan out free network: every single fault detection test set is also a multiple fault detection test set.

7.b. Consider logic circuit shown in fig. Find boolean difference w.r.t x_3



~> $F = x_1 x_2 + x_3 x_4$

$$\frac{dF(x)}{dx_3} = F_3(0) \oplus F_3(1)$$

$$= (x_1 x_2) \oplus (x_1 x_2 + x_4)$$

$$= (x_1 x_2)\,\overline{(x_1 x_2 + x_4)} + \overline{x_1 x_2}\,(x_1 x_2 + x_4)$$

$$= (x_1 x_2)\,(\overline{x_1 x_2} \cdot \overline{x_4}) + \overline{x_1 x_2}\, x_4$$

$$\frac{dF}{dx_3} = \overline{x_1 x_2} x_4$$

Test for x_3 s-a-0

$$x_3 \cdot \frac{dF(x)}{dx_3} = x_3 \overline{x_1 x_2} x_4$$

$$= x_3 (\overline{x_1} + \overline{x_2}) x_4$$

$$= \overline{x_1} x_3 x_4 + \overline{x_2} x_3 x_4$$

The test are : $\{0\phi 11\}$ $\{\phi 011\}$

Test for x_3 s-a-1

$$\overline{x_3} \cdot \frac{dF(x)}{dx_3} = \overline{x_3}\ \overline{x_1 x_2} x_4$$

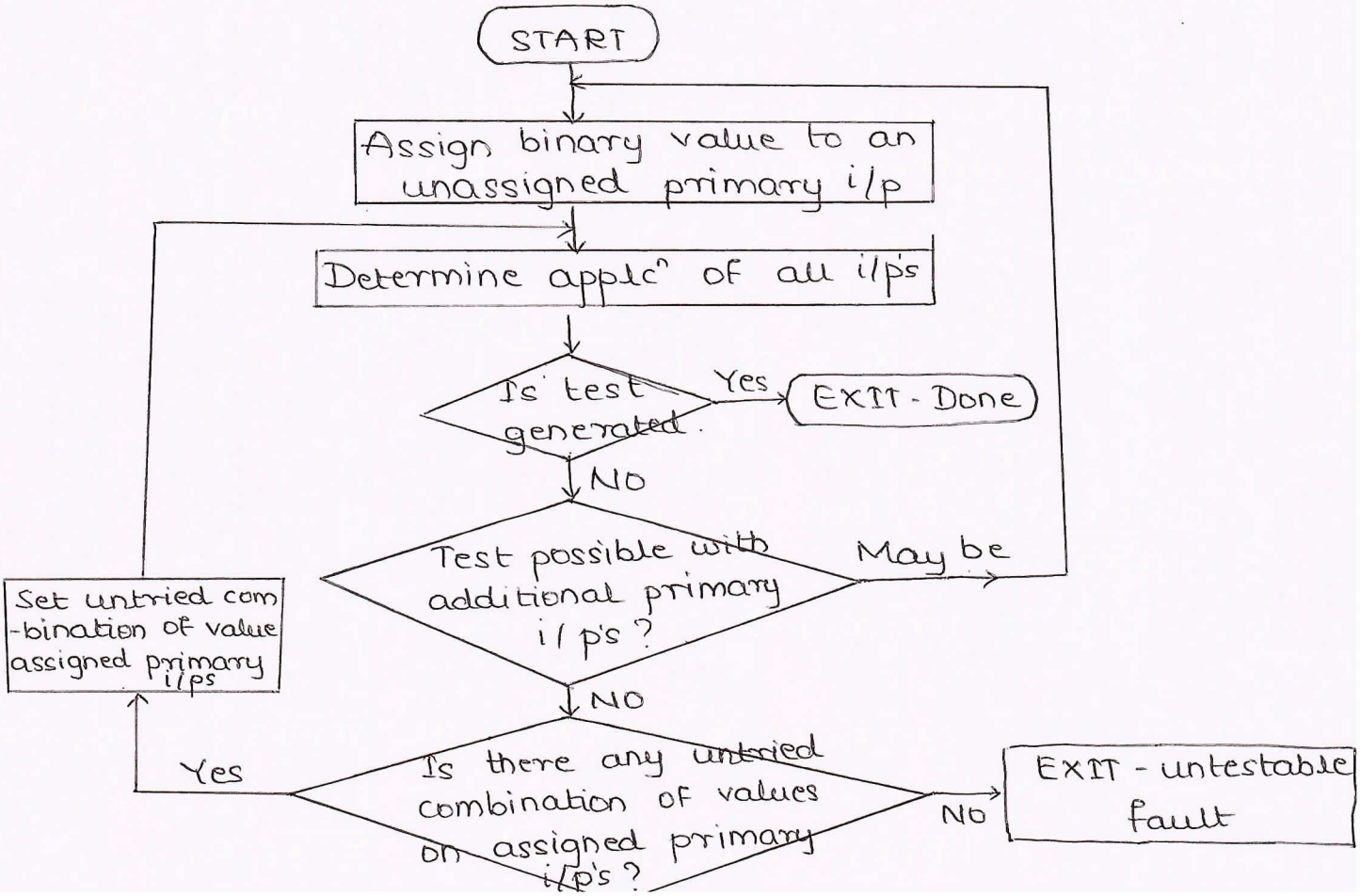
$$= \overline{x_3} (\overline{x_1} + \overline{x_2}) x_4$$

$$= \overline{x_1} \overline{x_3} x_4 + \overline{x_2} \overline{x_3} x_4$$

The test are : $\{0\phi 01\}$ $\{\phi 001\}$

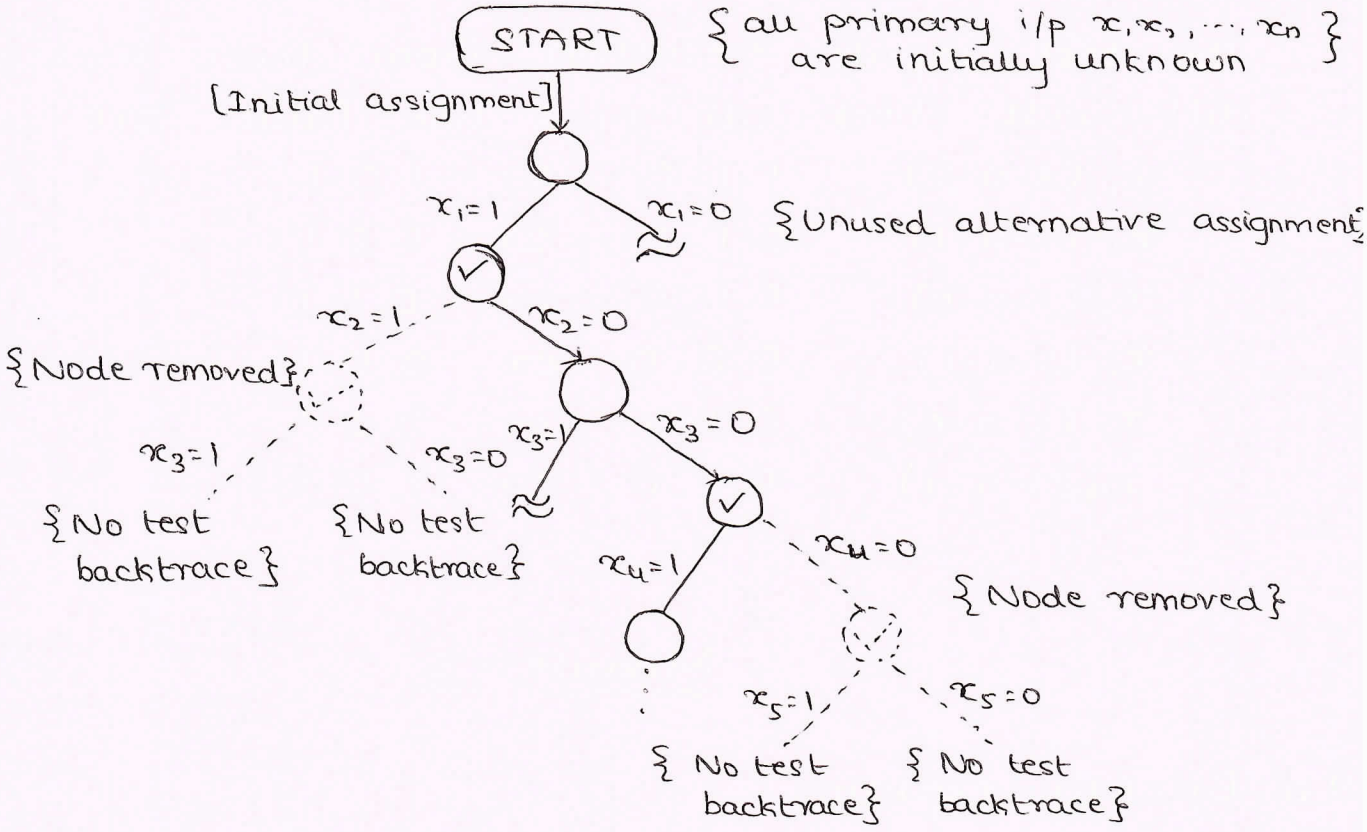
3.a. With neat sketch, explain path oriented decision making algorithm.

⇝ • It is enumeration algorithm in which all input patterns are examined as test for given fault.

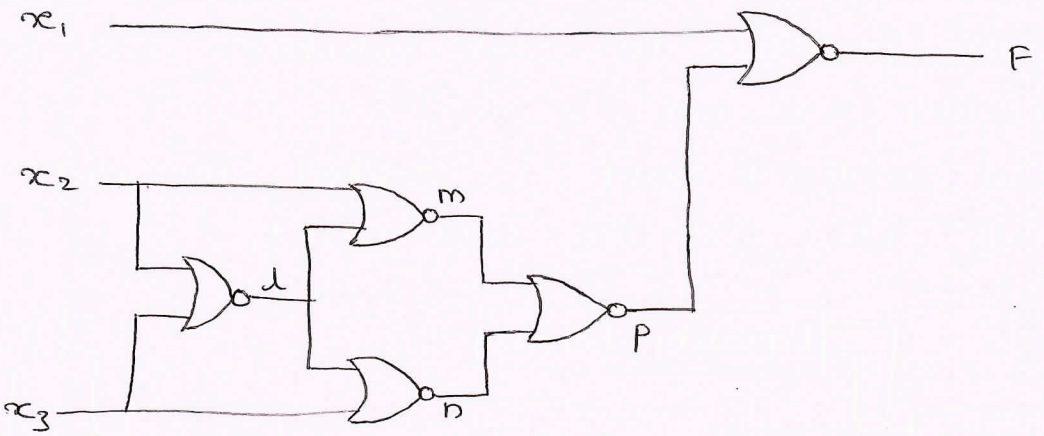


Decision tree is list of nodes having

1. Each node identifies current assignment of 0 or 1 to primary i/p.
2. Ordering reflects sequence in which the current assignment have been made.



8.b. For given logic network determine tests for checking all single node faults. $F = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$



⇝ Network function is given by

$$F = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$$

$$\frac{dF}{dx_1} = x_2\bar{x}_3 + \bar{x}_2 x_3$$

$$\frac{dF}{dx_2} = \bar{x}_1\bar{x}_3 + \bar{x}_1 x_3$$

$$\frac{dF}{dx_3} = \bar{x}_1 x_2 + \bar{x}_1\bar{x}_2$$

The test inputs resulting from these boolean diff. will check all input line faults are as follow

x_1 (s-a-0)	1	1	0	or	1	0 1
x_1 (s-a-1)	0	1	0	or	0	0 1
x_2 (s-a-0)	0	1	0	or	0	1 1
x_2 (s-a-1)	0	0	0	or	0	0 1
x_3 (s-a-0)	0	1	1	or	0	0 1
x_3 (s-a-1)	0	1	0	or	0	0 0

Module - 5

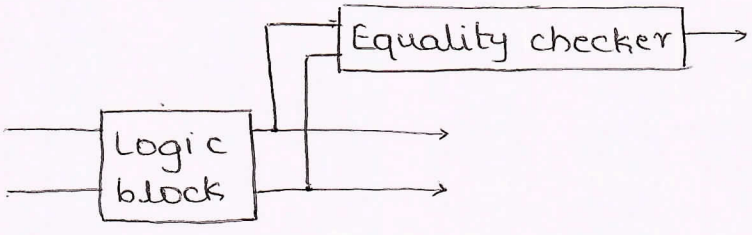
9.a. Briefly explain:

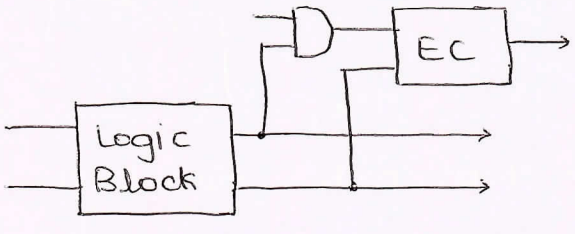
i. Controllability

~> Ability to apply test patterns to the i/ps of subcircuit via primary i/ps of the circuit.

Ex: • If o/p of EC ckt is always equal then it is not possible to test whether EC is operating correctly or not.

• If a control gate is added to ckt the operation of EC can be controlled.

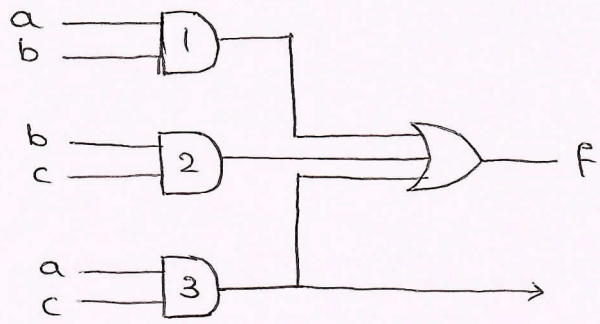




ii. Observability

⇝ Ability to observe response of subcircuit via primary o/p of ckt or at some other o/p points.

Ex:



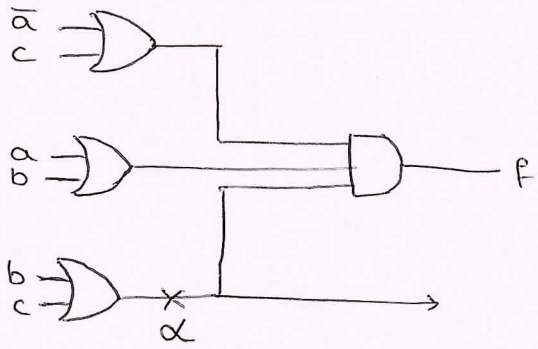
If there is s-a-0 fault at AND3 then it is not detectable.

Hence circuit o/p is pulled seperately ⟶

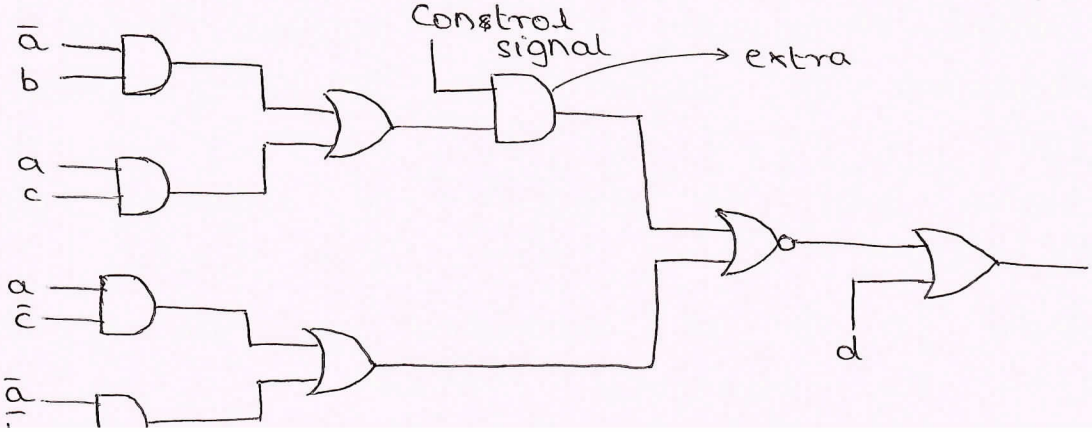
9.b. Explain adhoc design rules for improving testability.

⇝ → Include additional control & observation points in a circuit.

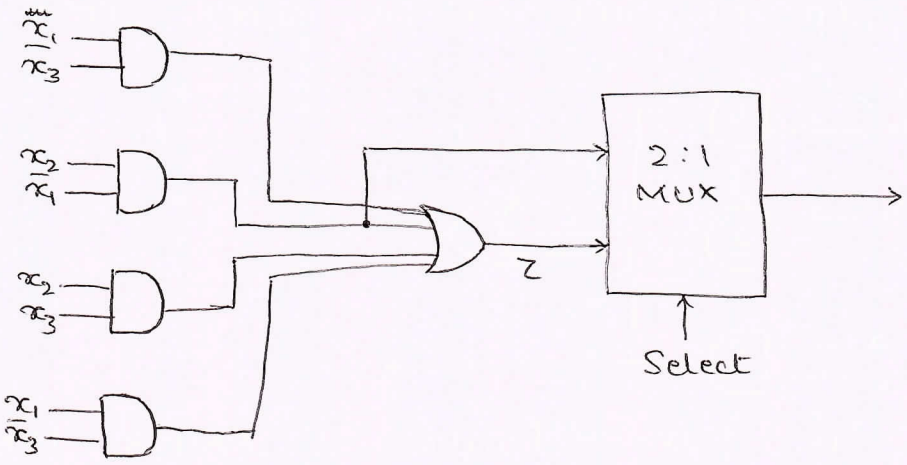
Ex: Fault α s-a-1 ckt is undectable at ckt o/p and extra line makes it detectable.



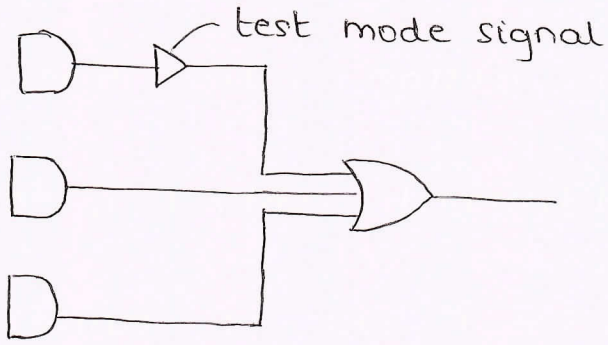
→ Adding extra control point is useful.



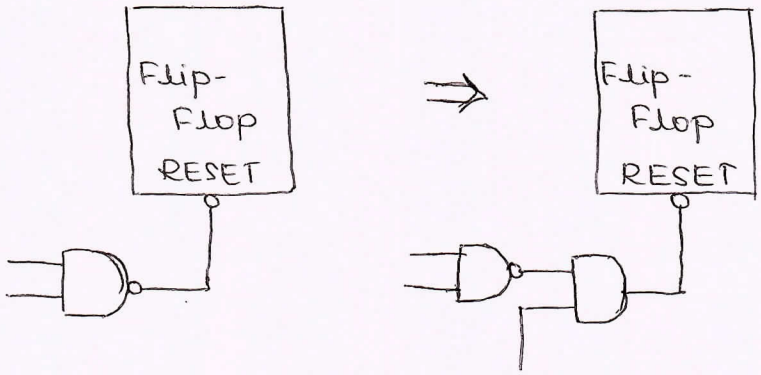
→ Including MUX in the circuit to increase no. of internal points.



→ Including tristate drivers.



→ Circuit Initialization.



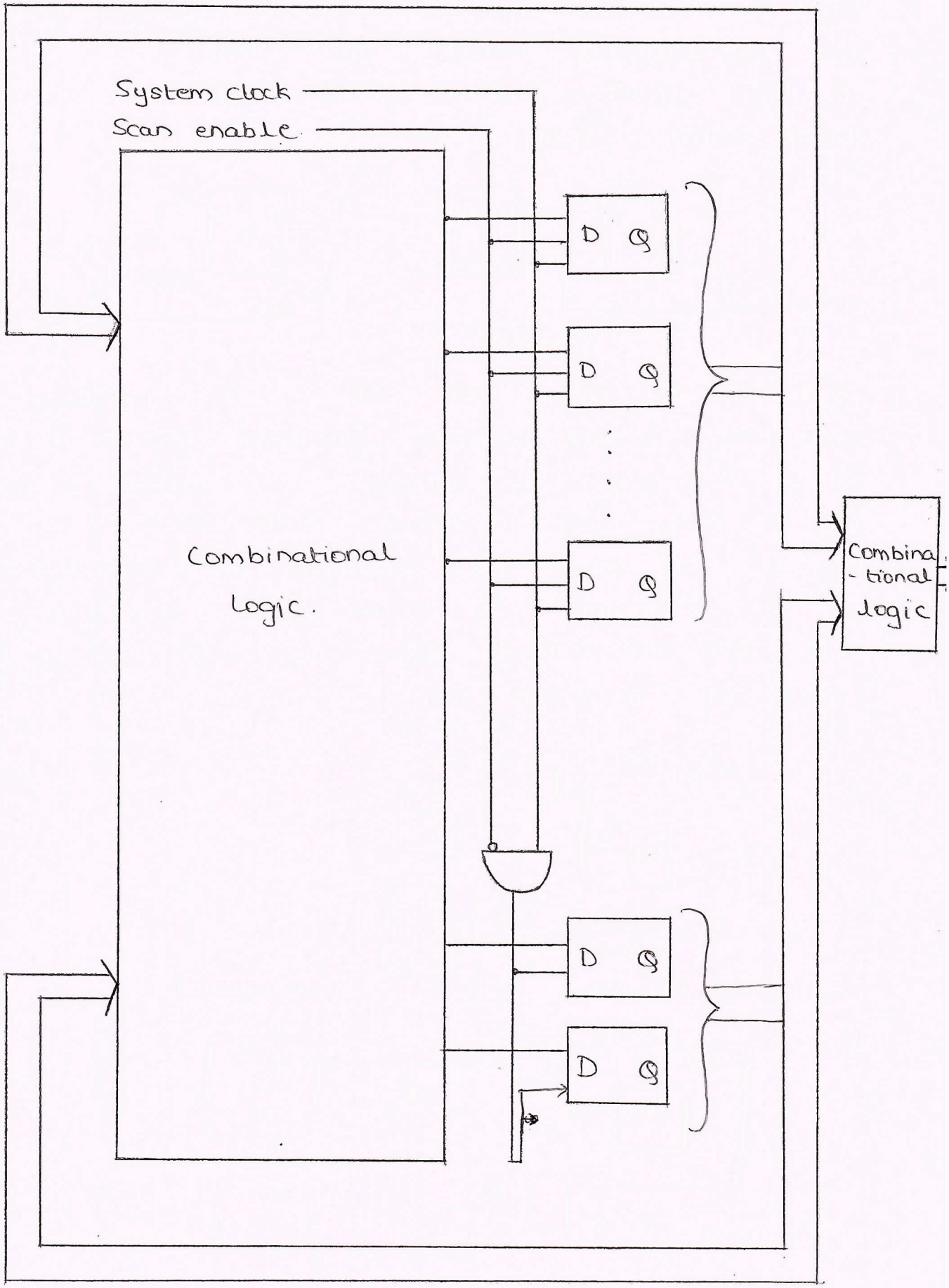
9.c. With neat diagram explain partial scan.

~> • Test sequence is derived by shifting data into scan FF.

• Remaining bits of states i.e, contents of required circuit states.

• Selection FF to be included in the partial scan is done by heuristic methods.

• Fault coverage can be increased to as high as 95% by including less than 65% of FF in partial scan.

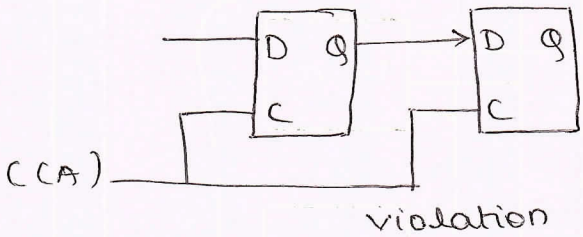


10a. List LSSD design rules.

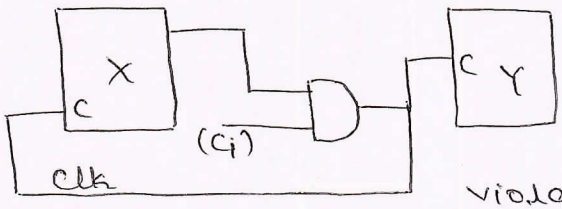
⇝ Rule 1 : All internal storage is implemented in Hazard free polarity hold latches.

Rule 2 : Latches are controlled by two or more non overlapping clocks such that.

a. Two latches where one feeds the other can't have same clock.



violation

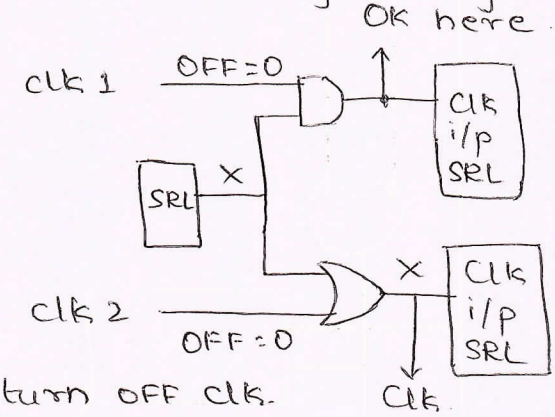


violation.

b. Latch X may get clk Ci to produce a gated clk Cig which drives another latch Y if & only if clk. Cig doesn't clk latch X, where Cig is only clk derived from Ci

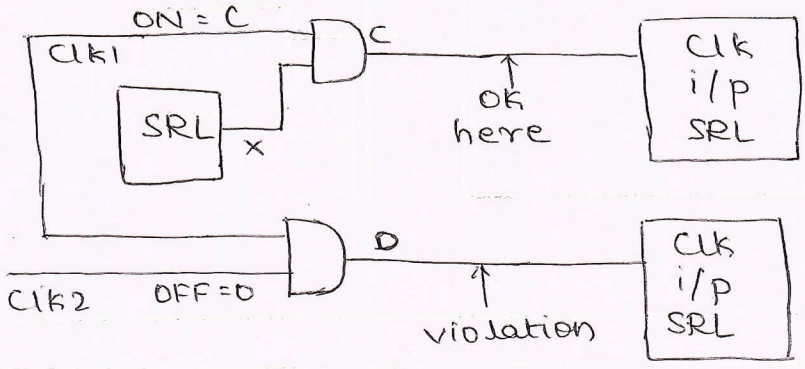
Rule 3 : It must be possible to identify a set of clk primary i/p from which the clk i/ps to SRL's are controlled either through simple powering trees or through logic

a.



Can't turn OFF clk. (violation)

b.



c. No clk can be ANDed with either true value or complement value of another clk.

Rule 4: Clk primary i/p may not feed data i/p to latches either directly or through combinational logic.

Rule 5: All SRLs must be connected into one or more shift registers, each of which has an i/p, an o/p and clks available at terminal of the module.

Rule 6: There must be primary i/p such that

a. Each SRL or scan out primary o/p is function of only preceeding SRL or primary i/p in its shift reg during shift operation.

b. All clks except shift clks are held OFF at SRL i/ps.

c. Any shift clk to an SRL may be turned ON & OFF by changing corresponding clk primary i/p for each clk.

10.b Explain test generation based on functional fault models.

~> • State group differentiating (SGD) is applied to differentiate between expected state and faulty state.

• A reduced n-state sequential circuit has a collection of n-1 SGD sequences, each of which distinguishes between a state S and one other state in the circuit.

	x=0	x=1
A	C/D, 0	B, 0
B	D, 0	C, 0
C	A, 1	D, 1
D	B, 0	A, 1

• Below is another state table which doesn't have distinguishing sequence

• I/p $x=1$ can be distinguished between state A and state C.

	$x=0$	$x=1$
A	B, 0	C, 0
B	C, 0	D, 1
C	A, 1	D, 1
D	B, 0	A, 1

	$x=0$	$x=1$
A	C/D, 0	B, 0
B	D, 0	C, 0
C	A, 1	D/A, 1
D	B, 0	A, 1

i	A	B	C	D	C/D	A/B	D/A
0	1	0	0	0	0	0	0
1	0	1	0	0	1	0	0
2	0	0	1	1	0	1	1

• Detect state table fault

A → C/D is 2

sequence is

$$A \xrightarrow{0} C/D \xrightarrow[1/0]{0} A/B$$