KLS Vishwanathrao Deshpande Institute of Technology

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper Scheme & Solution

Faculty Name	:	Prof. Deepak Sharma
Course Name	:	Basic Electronics for EEE stream
Course Code	:	BBEE103
Year of Question Paper	:	2023 Jan-Feb
Date of Submission	:	15-07-2024

Faculty Member

HoD

Head of the Department
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Dean (Acad.)

CBCS SCHEME

USN | | | | | | | | | | |

BBEE103

First Semester B.E./B.Tech. Degree Examination, Jan./Feb. 2023
Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. VTU Formula Hand Book is permitted.
3. M : Marks , L: Bloom's level , C: Course outcomes.

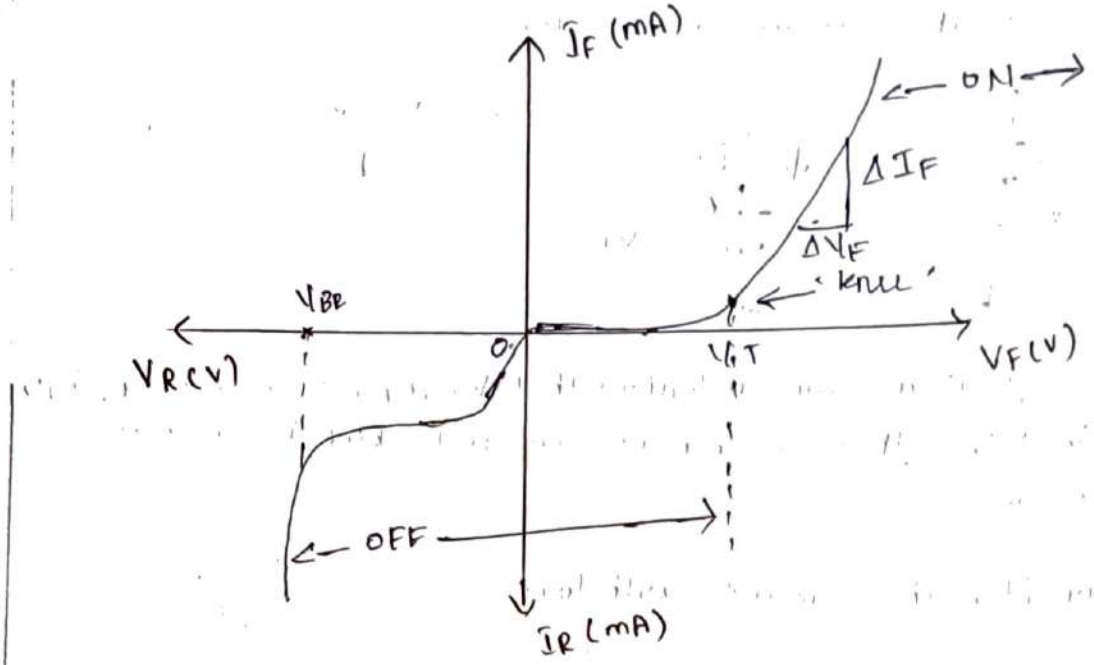
		Module – 1	M	L	C
Q.1	a.	Explain V-I characteristics of a PN junction diode for both forward and reverse characteristics.	4	L1	CO1
	b.	With appropriate circuit diagram, explain the DC load line analysis of semiconductor diode.	8	L2	CO1
	c.	The input voltage to a half wave rectifier is V = 200 Sin 50t. If R_L = 1kΩ, and forward resistance of the diode is 50Ω, find : i) The dc current through the diode ii) The ac or RMS value of current through the circuit iii) The dc output voltage iv) The ac power input v) Rectifier efficiency.	8	L3	CO1
		OR			
Q.2	a.	Explain the working of Full-wave rectifier with neat circuit diagram and waveforms.	8	L2	CO1
	b.	Explain the operation of RC π - Filter sign full waver rectifier.	8	L2	CO1
	c.	What is zener doide? With neat circuit diagram, explain the operation of voltage regulator with and without load.	4	L1	CO1
		Module – 2			
Q.3	a.	Describe with neat circuit diagram of BJT amplification for both voltage and current.	8	L2	CO2
	b.	With neat diagram, explain the input and output characteristics of transistor in common base configuration.	8	L2	CO2
	c.	A transistor has β = 150 and I_E is 12mA. Calculate the approximate collector current (I_E) and Base current (I_β).	4	L3	CO2
		OR			
Q.4	a.	Explain the construction and operation of N-channel JFET.	8	L2	CO2
	b.	Explain Depletion type MOSFET along with the transfer and Drain characteristics.	8	L3	CO2
	c.	Briefly explain common collector input characteristics.	4	L2	CO2

		Module – 3			
Q.5	**a.**	Explain block diagram representation of typical op-amp.	**8**	**L2**	**CO2**
	b.	Explain the following op-amp parameters i) CMRR ii) Spew Rate iii) Input offset voltage iv) Input Bias current.	**8**	**L2**	**CO2**
	c.	Design an adder circuit using an op-amp, to give the output $V_0 = (3v_1 + 4v_2 + 5v_3)$. Assume $R_f = 120k\Omega$.	**4**	**L3**	**CO2**
		OR			
Q.6	**a.**	Explain op-amp as an integrator circuit with a neat input and output waveforms using square wave as input.	**8**	**L2**	**CO2**
	b.	Explain op-amp as an inverting and non-inverting amplifier.	**8**	**L2**	**CO2**
	c.	Briefly explain op-amp as an voltage follower.	**4**	**L2**	**CO2**
		Module – 4			
Q.7	**a.**	Convert the following numbering system. i) $(11101.01)_2 = (?)_{10}$ ii) $(ABC \cdot D)_{16} = (?)_{10}$ iii) $(11011011110)_2 = (?)_8$ iv) $(734)_{10} = (?)_2$	**8**	**L3**	**CO3**
	b.	Explain NAND and NOR gate called as universal gates.	**8**	**L2**	**CO3**
	c.	State and prove Demorgan's theorem.	**4**	**L1**	**CO3**
		OR			
Q.8	**a.**	Briefly explain minterm, maxterm, SOP and POS forms, with examples.	**8**	**L1**	**CO3**
	b.	Design the working of full adder using basic gates.	**8**	**L2**	**CO3**
	c.	Reduce the expression i) $ABC + A\bar{B}C + AB\bar{C}$ ii) $AB + \overline{AC} + A\bar{B}C(AB + C)$	**4**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Describe the working of a linear variable differential transducer (LVDT) with neat diagram.	**8**	**L2**	**CO5**
	b.	With neat diagram, explain the operation of a piezoelectric transducer.	**8**	**L2**	**CO5**
	c.	Briefly explain with diagram of a resistance thermometer.	**4**	**L2**	**CO5**
		OR			
Q.10	**a.**	Describe with diagram of an AM superheterodyne receiver, explain each block.	**8**	**L2**	**CO5**
	b.	Explain the various blocks involved in communication block diagram.	**8**	**L2**	**CO5**
	c.	The coil in a variable reluctance transducer has a 1mH inductance, when the total air gap length is 1mm. Calculate the inductance change when the air gap is reduced by 0.2mm.	**4**	**L3**	**CO5**

Module-1

1. a. Explain V-I characteristics of a PN junction diode for both forward & reverse characteristics. -4M

Ans:-



-1M

-1M

V-I Characteristics of a p-n junction diode is a plot of voltage applied across the pn junction & the current flowing through the pn-junction.

A diode conducts a large forward biased with its anode at a positive potential w.r.t cathode. If conducts a comparetively much smaller current (reverse current) in a reverse baised.

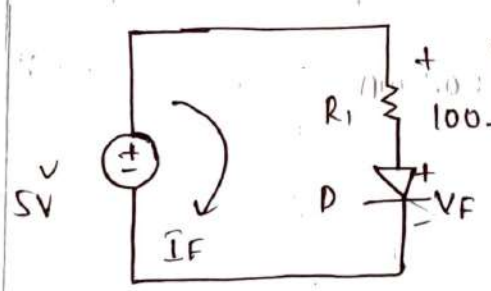
In forward biased the forward current I_F remains very low until the forward bias voltage across the diode exceeds 0.7V, beyond which the current rapidly increases & the diode is said to be "ON". This voltage of 0.7 V is called the cut-in or threshold voltage $V_f \simeq V_T$. Thus diode turns 'on' for $V_F > V_T$.

When reverse biased, a very small current 'I_R' which flows through the silicon diode until the p-n junction breaks down at a reverse voltage. The diode is said to be "OFF" for forward voltage less than V_T. This voltage at which the pn junction breaks down is called the "reverse breakdown voltage" & $I_R << I_F$. — 2 M

b. With appropriate circuit diagram, explain the DC load line analysis of Semiconductor diode — 8 M

A: DC load line is the graphical analysis in which a straight line drawn over the forward characteristics of diode, From this straight line we will be able to determine the Q-point (operating point of the diode) which intersects with the forward characteristics of the diode

Example:- consider the following circuit, for understanding the Procedure of DC load line — 4M



KVL to fig gives

$V = I_F R_1 + V_F$ - (1)

When $V_f \to 0$, then $V = I_F R_1$, $\therefore I_F = \frac{5}{100} = 50mA$

let this point (B)

when $I_F \to 0$, $V = V_F = 5V$, let this be point (A) — 4 M

then Q. point is (1.2 V, 40mA).

c. The input Voltage to a half wave rectified is $V = 200 \sin 50t$. If $R_L = 1k\Omega$ & forward resistance of the Diode is 50Ω, find: — 8 M

(i) The dc current through the diode.

(ii) The ac or RMS value of current through the circuit.

(iii) The dc output voltage

(iv) The ac power i/p.

(v) Rectifier efficiency.

Ans:-

(i) $I_{DC} = \frac{V_{rms}}{2R} =$

Given:- I/p Voltage = 200 V (peak)

$R_L = 1k\Omega$ — 1 M

$R_F = 50\Omega$

(i) $I_m = \frac{V_m}{R_L + R_F}$

$= \frac{200}{1000 + 50}$

$= \frac{200}{1050}$

$= 0.190\,A$ or $190\,mA$

$\therefore$ DC current $I_{DC} = I_m / \pi$

$= \frac{190\,mA}{\pi} = 60.5\,mA$ — 2 M

(ii) $I_{rms} = \frac{I_m}{2}$

$= \frac{190\,mA}{2}$

$= 95\,mA$. — 2 M

(iii) $V_{DC} = I_{DC} \times R_L$

$= 60.5 \times 1000$

$= 60.5\,V$. — 1 M

(iv) $P_{AC} = V_m \times \frac{I_{rms}}{2}$

$= \frac{100}{200} \times \frac{95}{2}$

$= 9.5\ W.$

— 1 M

(v) $\eta = (P_{DC}/P_{AC}) \times 100\%$

$= \frac{V_{DC} \times I_{DC}}{P_{AC}} \times 100$

$= \frac{60.5 \times 60.5}{9.5} \times 100$

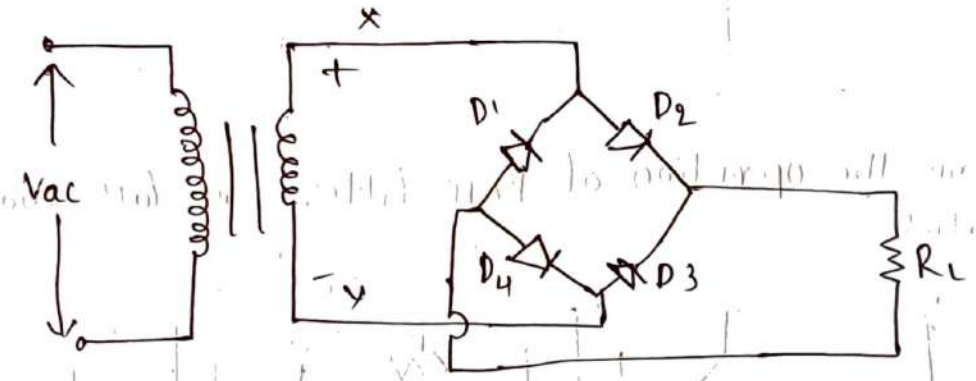
$= 40.4\ \%.$

— 1 M

2. a. Explain the working of full-wave rectifier with neat circuit diagram & wave forms. — 8 M

∴ Full wave rectifier.

Circuit Diagram :- It uses 4 diodes for rectification process

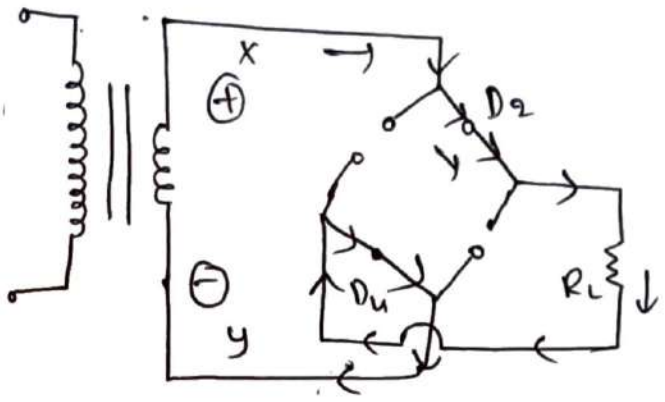


— 2 M

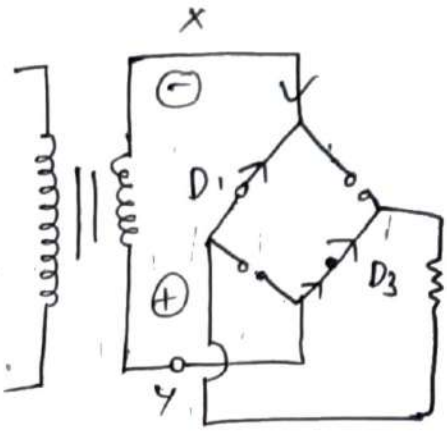
During the +ve half of the input signal, point X will be +ve w.r.t Y. Hence Diode D_2 & D_4 will be forward biased whereas Diode D_1 & D_3 will be reverse biased, hence current flows through. X - D_2 - R_L - D_4 - Y as shown below, Similarly During -ve half of i/p takes X will be -ve w.r.t Y, hence condition takes place form Y - D_3 - R_L - D_1 - X.

— 2 M

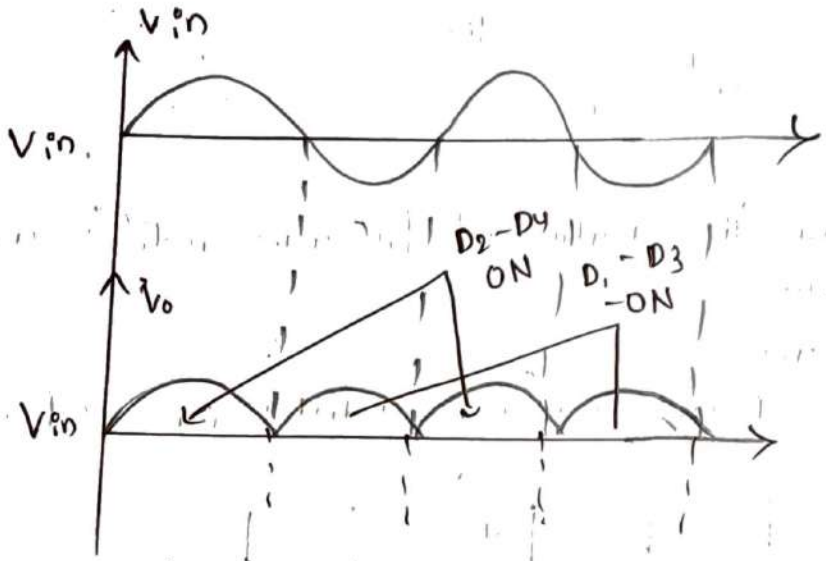
During +ve half cycle



During -ve half cycle



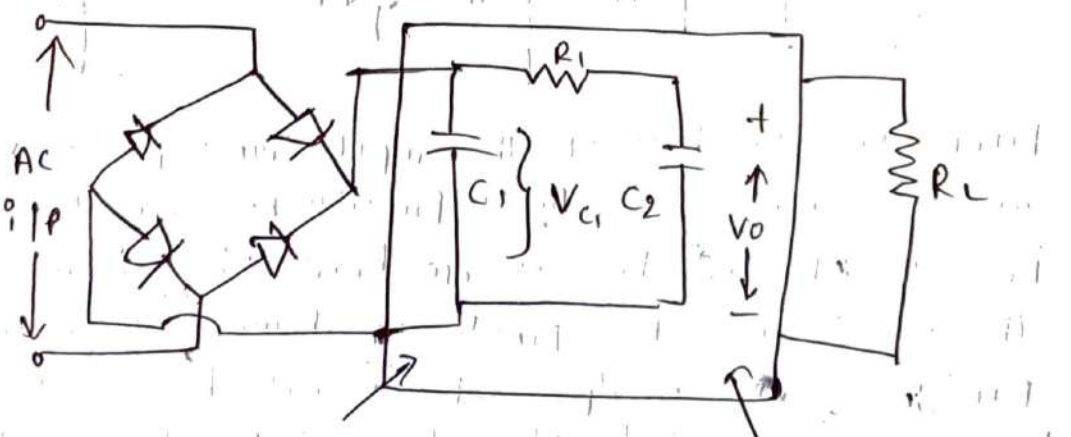
-2 M



-2 M

2b. Explain the operation of RCπ-filter sign full wave rectifier -8M

Ans:-



-4M

Here additional capacitor C_1 & R, will attenuate the ripple contents from transformer o/p.

the shape of C_1, R_1, C_2 is like π symbol.

hence the name RC - π filter

The harmonic components are more severly attenuated by voltage division across R_1 & C_2

$\therefore$ Peak voltage is $V_p = \frac{V_r}{\pi}$

$$\therefore V_{DC_2} \text{ (ac)} = \frac{V_i X_{C_2}}{\sqrt{R_1^2 + X_{C_2}^2}}$$

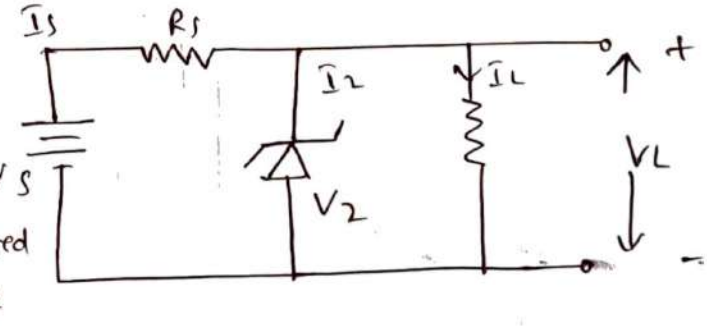
$$X_{C_2} = \frac{R_1}{\sqrt{(V_i/V_o)^2 - 1}}$$

$$\boxed{X_{C_2} \simeq R_1/(V_i/V_o)}$$

– 4 M

2c. What is zener diode? With neat circuit diagram, explain the operation of zener voltage regulator with & without load. – 4 M

A: Zener diode can be used as a voltage regulator, since it maintains a constant output voltage even though the current through zener changes

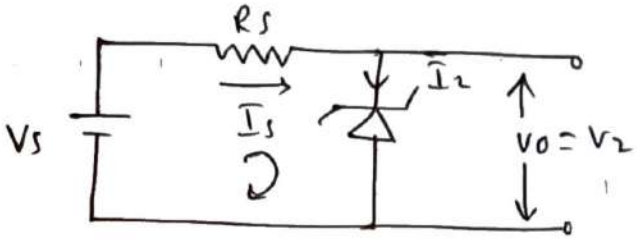


– 2 M

- The fig. shows the zener diode as voltage regulator, zener is connected in parallel with the load therefore the circuit is also known as shunt regulator.
- A resistance Rs is connected in series with zener to limit current in the circuit. through Rs is also known as series current limiting resistor.

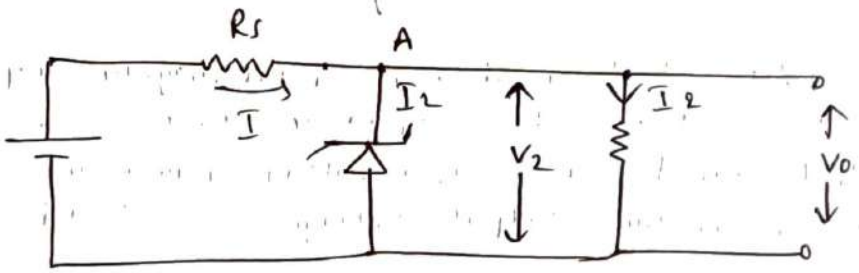
Regulator with no load:-

- The resistor R_S is used to limit the zener diode current to desired value



Regulator with load:-

- Consider the circuit as shown in fig. the current through R_S is sum of load current & zener current, but care must be taken to ensure that I_Z (minimum) is greater to keep zener under breakdown region.



– 2 M

Module - 2.

3.a. Describe with neat circuit diagram of BJT amplification for both Voltage & current — 8 M

A: Amplication means enhancing or increasing. Amplication with respect to current & voltage.

~~Voltage~~ current Amplication.

we have two factors α & β which are current gain or current amplication factors.

(i.e; α & β can be current gain factors or current amplification factors).

If we consider, α then w.k.t.

$$\alpha_{ac} \text{ or } \alpha_{dc} = \frac{I_C}{I_E}$$

it implifies that small change in emitter current may cause large or maximum change in collector current.

but the range of α is 0.95 to 0.99 $\simeq 1$.

$$\alpha \Delta I_C \simeq \Delta I_C \text{ or } I_E = I_C.$$

Therefore no amplication is possible

But we have another amplification factor β ranging between 2 s to 300.

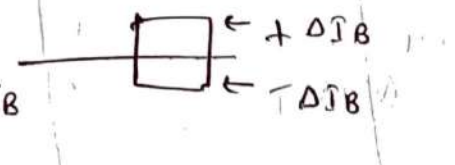
we know $\beta_{ac} = \frac{I_C}{I_B}$.

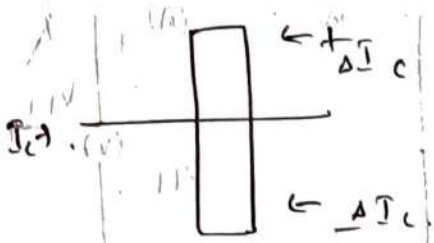
i.e; a small change in base current (ΔI_B) produces large change in collector current (ΔI_C).

$$\text{So } \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\therefore \Delta I_B = \beta \Delta I_C$$

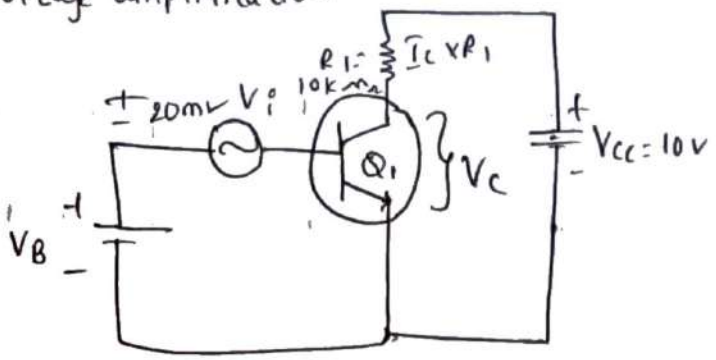
— 4M





Base & Collector currents
Hence β can be choosed for amplification factor.

Voltage amplification.



Assume transistor Q_1 has $\beta_{DC} = 50$, $V_B = 0.7V$.

Ac signal V_i having ± 20mv peak to peak Sinosoidal signal

$I_B = 10\mu A$

then $I_C = \beta I_B$

$= 50 \times 10 \times 10^{-6} = 0.5mA$

$V_C = V_{CC} - I_C R_1$

$= 10 - 0.5 \times 10^{-3} \times 10 \times 10^3 = 5V$.

i.e; when AC i/p signal $V_i = 0$, then collector voltage is 5V, now when V_i changes to ± 20mv, then base current changes by ± 5μA

$\therefore \Delta I_C = \beta_{dc} \Delta I_B$

$= 50 \times 5 \times 10^{-6}$

$\Delta I_C = 0.25mA$

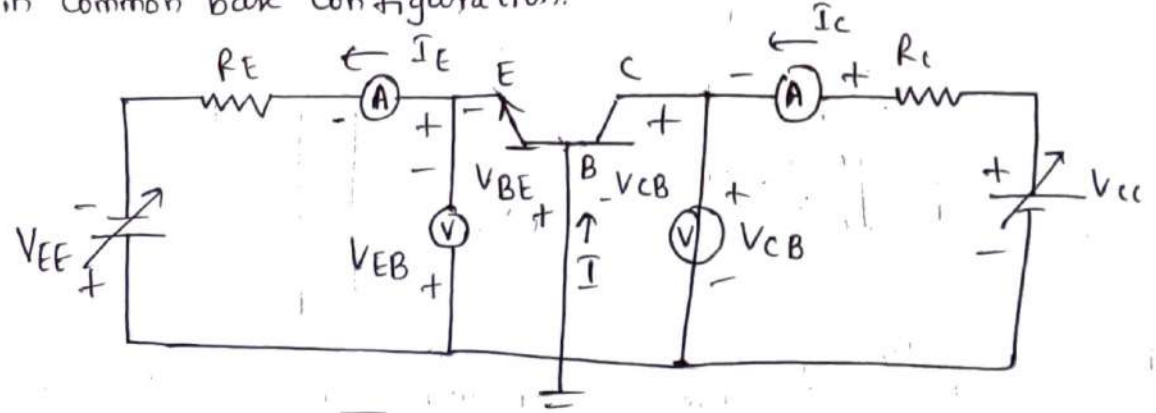
therefore Voltage gain A_V is defined as ratio of change in collector voltage to change in base voltage

$$A_V = \frac{\Delta V_C}{\Delta I_B} = \frac{\pm 2.5V}{\pm 20mV} = 12\Omega$$

for a small change in input voltage there is a large change in o/p voltage hence Voltage amplification is achieved. – 4 M

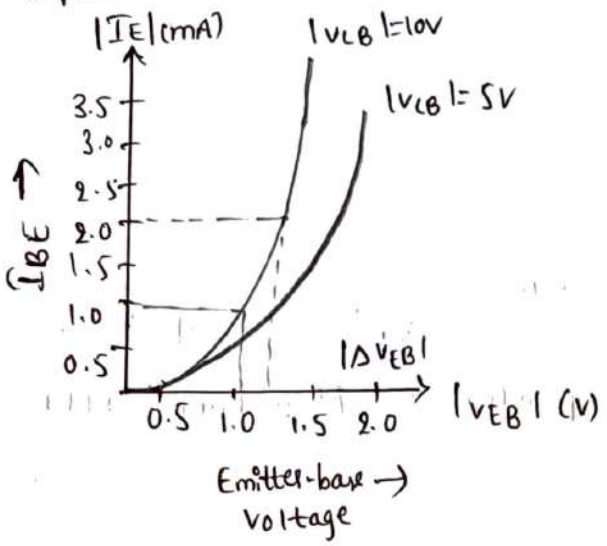
3 b. With neat diagram, explain the i/p & o/p characteritics of transistor in Common base Configuration. – 8 M

A:-

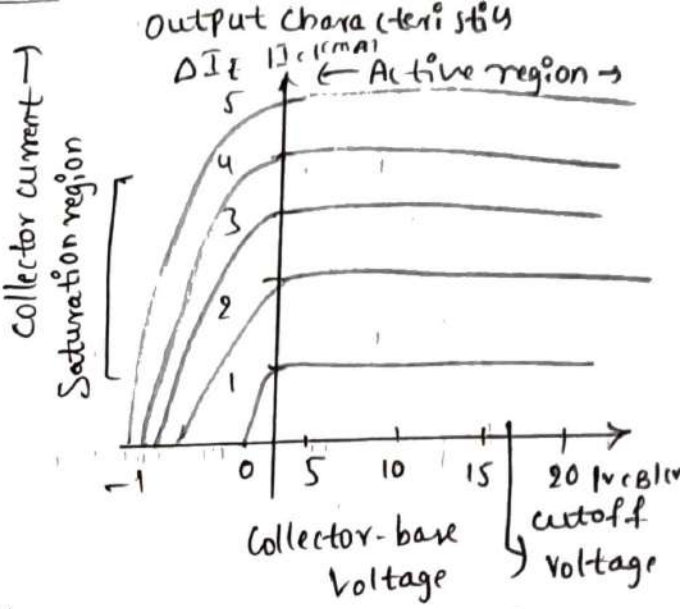


– 3

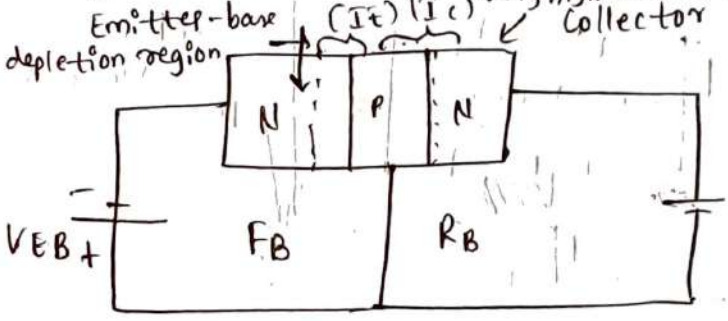
Input characteristics.



Output characteristics



Punch through effect or base width modulation or Early effect.



– 5M

3c. A transistor has $\beta = 150$ & $I_E = 12\,mA$. Calculate the approximate Collector current (I_E) & Base current (I_B). – 4 M

Ans: Given: $\beta = 150$

$I_E = 12\,mA$

w.k.t

$\beta = I_C / I_B$

$I_C = \beta \times I_B$

we also know that

$I_E = I_C + I_B$. – 2M

Substituting the expression for I_C, we get.

$I_E = \beta \times I_B + I_B$

$I_E = (\beta + 1) * I_B$.

$\therefore 12 = (150 + 1) \times I_B$

$12 = 151 \times I_B$

$I_B = \frac{12}{151} = 0.0795\ mA$ — 1 M

to find I_C.

$I_C = \beta \times I_B$.

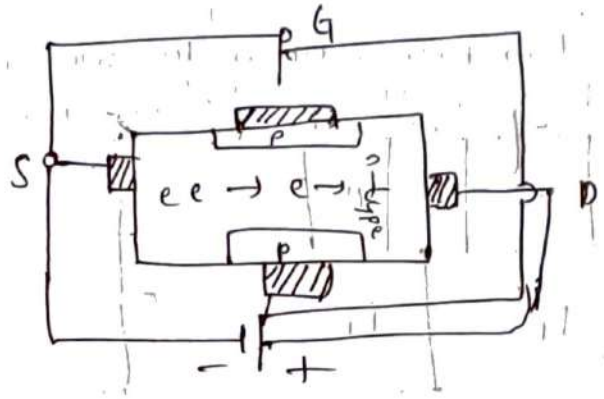
$= 150 \times 0.0795$

$= 11.925 mA$

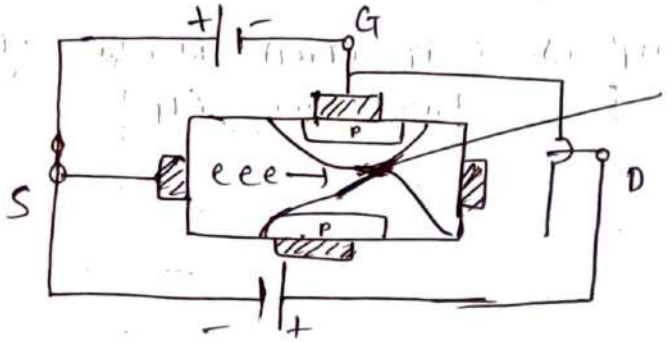
$\therefore I_B = 0.0795_{mA}$ & $I_C = 11.925 mA$ — 1 M

4.a. Explain the construction & operation of N-Channel JFET — 8 M

A:- Construction.



when $V_{GS}=0$ & $V_{DS}=+ve$



Pinch off

when

V_{GS} = -ve

V_{DS} = more +ve

Pinch off.

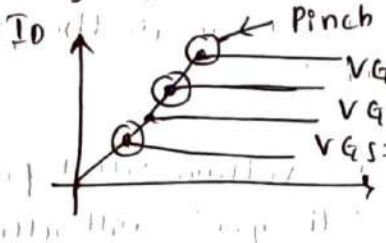
— 4 M

The working of n-channel JFET can be understand by considering the following cases

Case(i):- When $V_{GS}=0$ & $V_{DS}=+ve$

In this condition, as source is connected to -ve terminal, more number of electrons will be replaced towards the drain, hence the drain current increases, but as drain in +ve, after reacting the certain voltage level (V_{DS}) the reverse bias at drain increases, hence it extends the Depletion region more towards the Drain. hence the flow of electrons from Source to drain, is going to be limited as result of which I_D decrease slowly

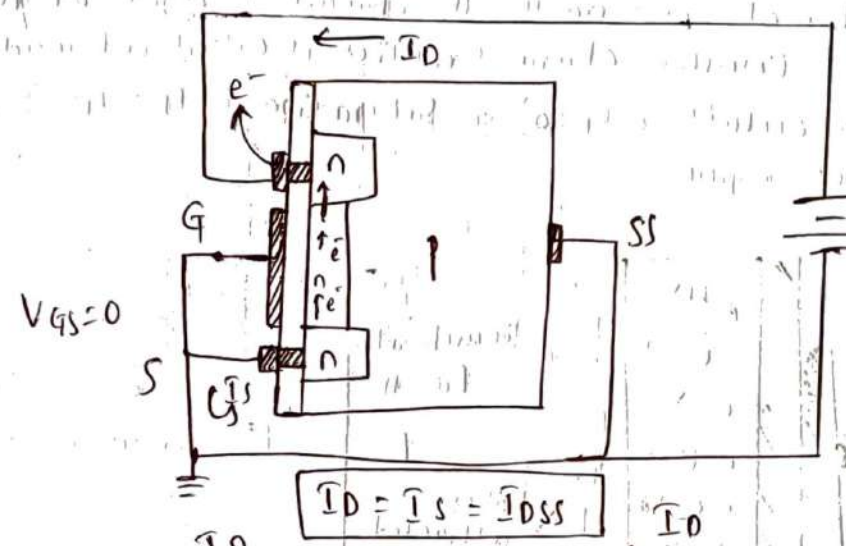
Case(ii):- V_{GS} = -ve, V_{DS} is more +ve. Under these conditions as reverse bias increases more towards drain, hence blocking the path of flow of electrons, this condition is known as pinch off condition at this stage I_D remains constant. — 3 M



— 1 M

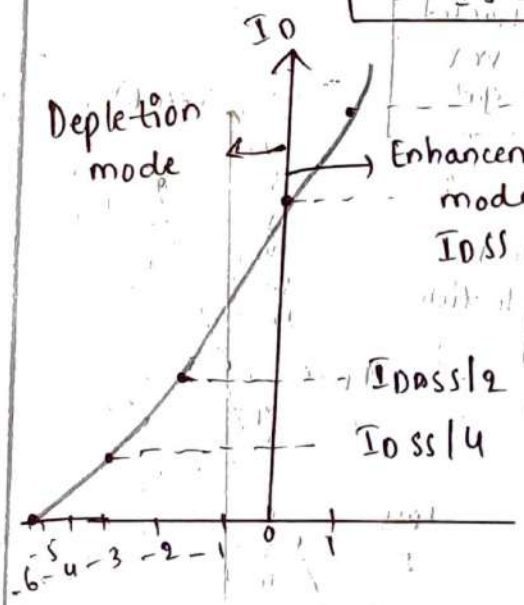
4.b. Explain Depletion type MOSFET along with the transfer & Drain characteristics. — 8 M

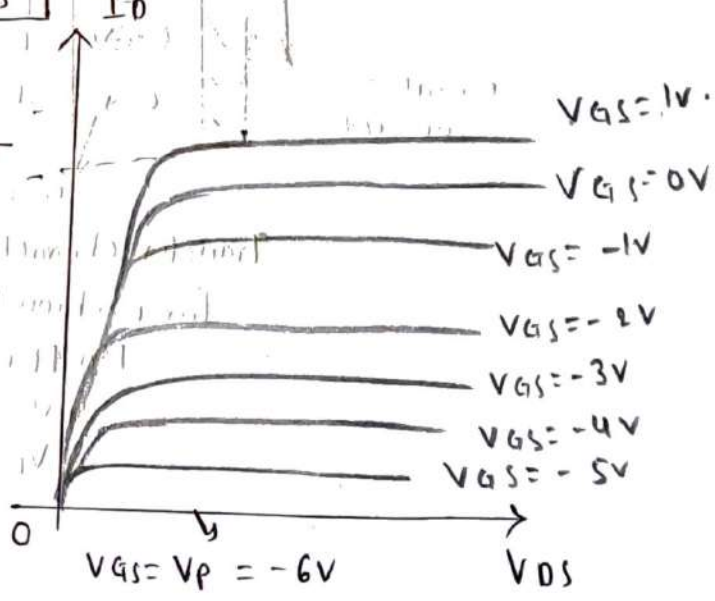
Δ:-



— 1 M

$I_D = I_S = I_{DSS}$

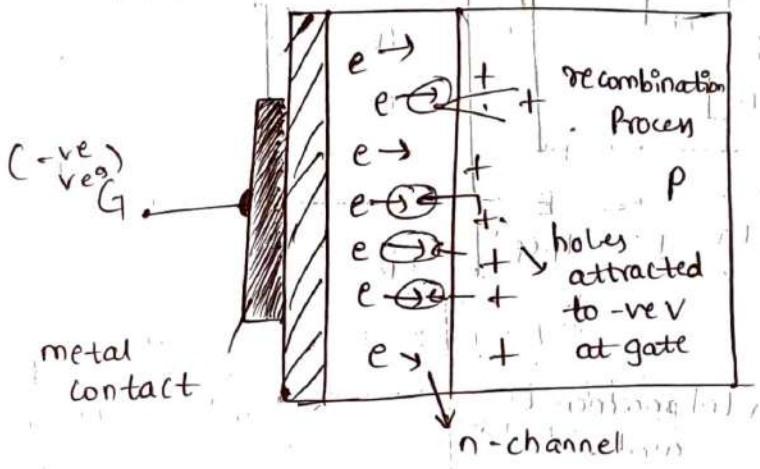




— 2 M

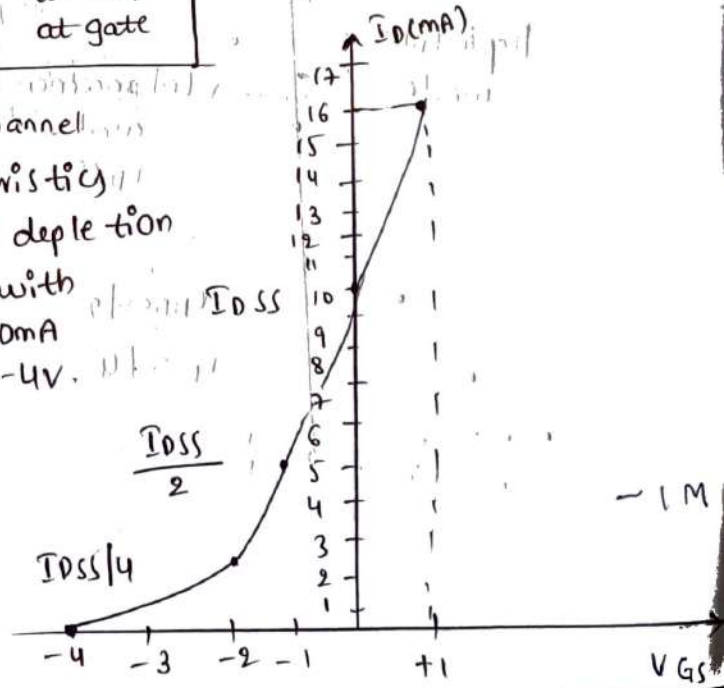
* If $V_{GS} = -Ve$ potential at gate will push electrons towards p-type substrate & attract the holes from p substrate.
* Recombination of holes & electoons happens due to this & free $e^{\ominus}$ gets reduced
* More the applied V_{GS} in -ve direction more is the effect leading to decrease in na of $e^{\ominus}$ in n-channel
* Hence current goes reduced
* Finally current reaches 0 at some voltage called pinch off voltage
* If $V_{GS} = +1V$, +ve potential at the gate will attract $e^{\ominus}$ towards the channel & holes are repelled.
* Electron strength increases in n channel thus increasing the current as shown in ~~fi~~ graph.
* +ve V_{GS} enhanced $e^{\ominus}$ na in the channel ∴ region of the gate voltages on the transfer characteristics is called enhanced region
* Region between cutoff ($I_D = 0$) & Saturation ($I_D = I_{DSS}$) is called depletion region

- 3 M



- 1 M

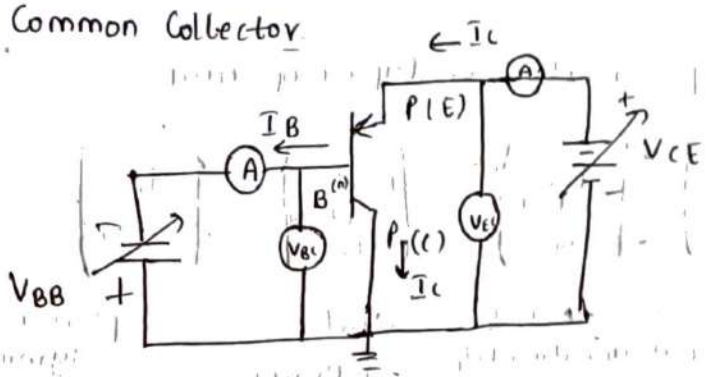
Transfer characteristics for n-channel depletion MOSFET with $I_{DSS} = 10mA$ & $V_P = -4V$.



- 1 M

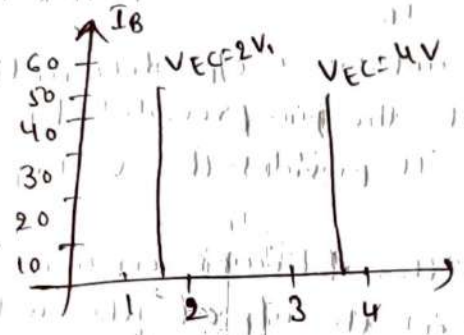
4.C Briefly Explain Common Collector i/p Characteristics. -4M

A:- Common Collector



-1M

Input characteristics:- I_B i/p voltage V_{BC} keeping o/p voltage V_{CE} constant



-1M

with respect to circuit diagram J_2 junction Base collector junction is forward baised & emitter is connected to positive terminal of P supply at the o/p side & base is connected to -ve terminal of power supply for E-B junction i.e; J_1 is also forward biased

Therefore,

Change $V_{EC}=2V$ vary V_{BC} from 0.

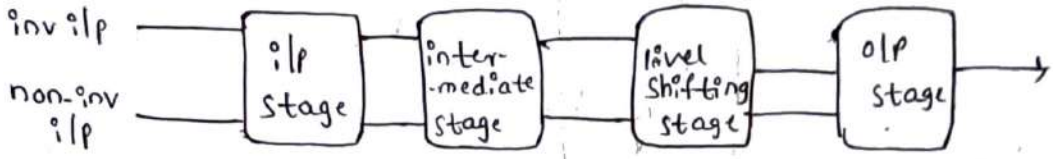
the transistor i/p current is 0 ∴ B C junction is going to become reverse baised w.r.t E-B junction therefore when $V_{BC}=2V$, J_2 also becomes forward baised & their is sudden raise in I_B

-2M

Module - 3

5.a. Explain block diagram representation of typical op-Amp — 8 M

A:-



— 2 M

dual i/p balanced o/p differential amplifier | dual i/p unbalanced o/p differential amplifier | emitter follower | Complementary symmetry Push or pull amplifies

* i/p stage:- It is dual i/p balanced o/p differential amplifier used for providing a high gain of order of 60dB.
* intermediate stage:- It is dual i/p unbalanced o/p differential amplifies stage which provides the half of the gain provided by the first stage & has two i/p terminals. It provides the voltage gain for the op-Amp.
* Level Shifting stage:- It is an emitter follower circuit which is used for shift the dc level at the o/p of the intermediate stage of the op-Amp to zero (0) volts w.r.t ground
* Output stage:- It is the low i/p impedence, large AC o/p voltage swing stage it consists of push pull complimentary amplifies that meets the required levels. — 6 M

5b. Explain the following op-Amp parameters. — 8 M

(i) CMRR (ii) Slew rate (iii) input offset voltage (iv) Input bias current

A:-(i) CMRR:- It is the ratio of Differential Voltage gain to the common mode voltage gain.

$$CMRR = \frac{Ad}{Acm} = \frac{Vo}{V_{inv} - V_{noninv}} = \frac{Vocm}{Vicm}$$

* Ideally it is ∞.

(ii) Slew rate:- The rate of change of o/p w.r.t to time is slew rate ideally it is ∞.

(iii) Input offset voltage:- It is the voltage that must be applied between the two i/p terminals of the op-Amp to make o/p zero

* Ideally it is 0.

* (iii) input bias current:- It is the average of the current flowing into inverting & non-inverting terminals of the op-Amp

4 × 2M = 8M

* Ideally it is zero (0).

5.c. Design an adder circuit using an op-Amp, to give the output $V_o = (3V_1 + 4V_2 + 5V_3)$. Assume $R_f = 120k\Omega$. — 4 M

Ans:

$$V_o = (3V_1 + 4V_2 + 5V_3) \quad - (1)$$

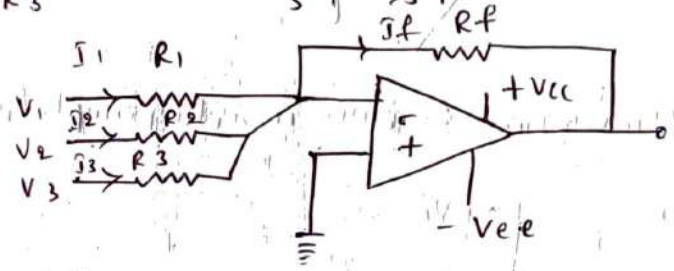
$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right] \quad - (2)$$

Comparing eqn (1) & (2) — 1 M

$$\frac{R_f}{R_1} = 3 \Rightarrow R_1 = \frac{R_f}{3} = \frac{\cancel{120}^{40}}{\cancel{3}_1} = 40k\Omega$$ — 1 M

$$\frac{R_f}{R_2} = 4 \Rightarrow R_2 = \frac{R_f}{4} = \frac{\cancel{120}^{30}}{\cancel{4}_1} = 30k\Omega$$ — 1 M

$$\frac{R_f}{R_3} = 5 \Rightarrow R_3 = \frac{R_f}{5} = \frac{\cancel{120}^{24}}{\cancel{5}_1} = 24k\Omega$$ — 1 M

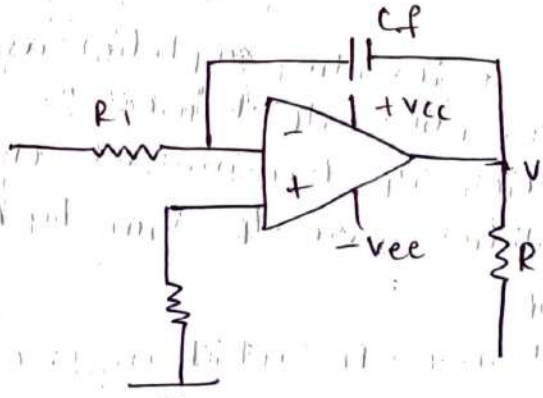


— 1 M

$R_1 = 40k\Omega$
$R_2 = 30k\Omega$
$R_3 = 24k\Omega$
$R_f = 120k\Omega$

6a. Explain op-Amp as an integrator circuit with a neat i/p & o/p waveforms using square wave as i/p. — 8 M

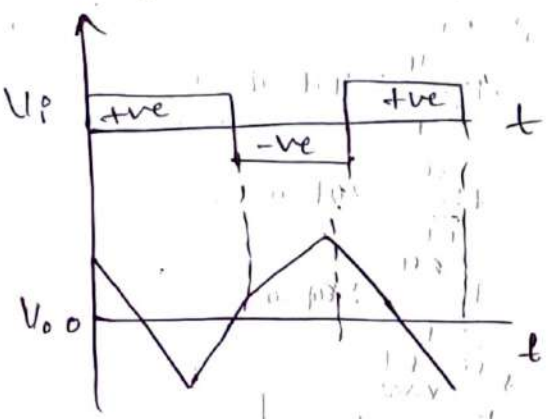
Ans:



7.2 M

* The above circuit is integrated using op-Amp.
* V_i is i/p signal applied at inverting i/p terminals through resistor R_1
* Non-inverting i/p terminal is grounded
* A capacitor Cf is connected in the feeback path between o/p terminal & inverting i/p terminal. — 2 M
* The o/p is given by

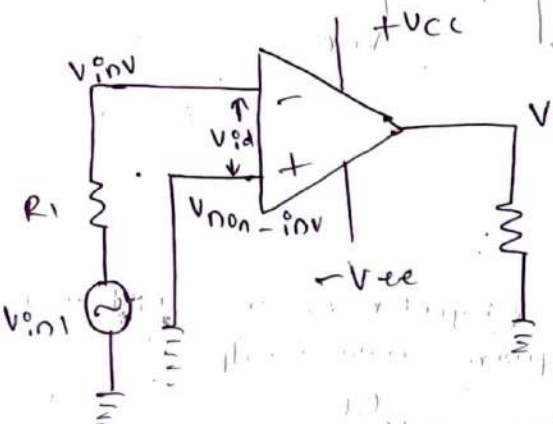
$$V_o = -R_1 C_f \int_0^t v_i dt + C$$ — 2 M



— 2 M

6.b. Explain op-Amp as inverting & non-inverting amplifier. — 8 M

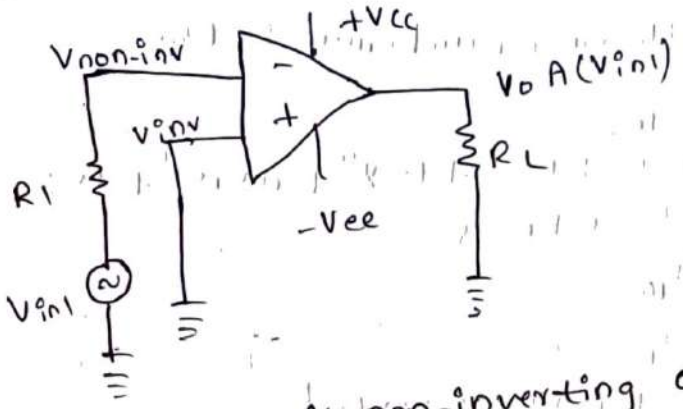
Ans:



— 2 M

* The above circuit is inverting amplifier using op-Amp.
* i/p is given to inverting i/p terminal of the op-Amp.
* At the non-inverting i/p terminal of the op-Amp. is 0V
* the inverting amplifier given o/p V_{in1} by A times where A is gain of op-Amp
* the o/p is measured across R_L which is given by $V_o = -A(V_{in1})$
* (-) sign indicates 180° phase shift (or) change in the angle of the op-Amp Compare with the i/p — 4 M

* Non-inverting Amplifier.



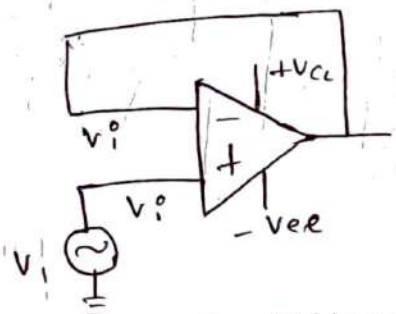
— 2 M

* The above circuit is non-inverting amplifier using op-Amp.
* i/p is given to non-inverting amplifier of op-Amp.
* At the inverting i/p terminal of the op-Amp is 0v given
* the non-inverting amplifier amplifies the given Vin1 by A times where, A is gain of op-Amp.
* the o/p is measured across RL which is given by $V_o = A(V_{in1})$

— 4 M

6.C. Explain Op-Amp as Voltage follower

A:-



— 2 M

* The above circuit is Voltage follower.
* The i/p Vi is applied at non-inverting i/p terminal
* Virtual ground concept says that inverting terminal follows the non-inverting i/p terminal in closed loop.
* Hence the o/p voltage is = i/p voltage . i.e; Vo = Vi.
* Hence this is Voltage follower

— 2 M

Module - 4.

7.a. Convert the following numbering system. — 8M

(i) $(11101.01)_2 = (?)_{10}$.

A:- $1\times2^0 + 0\times2^1 + 1\times2^2 + 1\times2^3 + 1\times2^4 + 0\times2^{-1} + 1\times2^{-2}$

$1+0+4+8+16+0+0.25$

$(29.25)_{10}$.

(ii) $(ABC.D)_{16} = (?)_{10}$.

A:- $10\times16^2 + 11\times16^1 + 12\times16^0 + 13\times16^{-1}$

$2560 + 176 + 12 + 0.8125$

$= (2748.8125)_{10}$.

(iii) $(110111011110)_2 = (?)_8$.

A:- $1\times2^0 + 1\times2^1 + 1\times2^2 + 1\times2^3 + 0\times2^4 + 1\times2^5 + 1\times2^6 + 0\times2^7 + 1\times2^8 + 1\times2^9$

$1+2+4+8+0+32+64+0+256+512$.

$= 879$

$879 \div 8 = 107$

8	879
8	109 - 7
8	13 - 5
8	8 - 15
	1 - 0

$(1577)_8$.

(iv) $(734)_{10} = (?)_2$

2	734
2	367 - 0
2	183 - 1
2	91 - 1
2	45 - 1
2	22 - 1
2	11 - 0
2	5 - 1
2	2 - 1
	1 - 0

$(1011011110)_2$

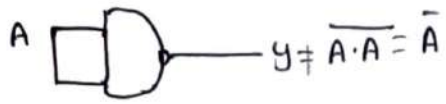
4 × 2M = 8M

7b. Explain NAND & NOR gate called as Universal gates. - 8M

A: Both NAND & NOR gates are called universal gates because all the logic gates NOT, AND & OR can be constructed using only NAND or NOR gate.

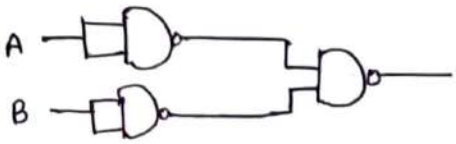
(i) Construction of NOT, AND or OR gates using NAND only.

NOT gate



AND gate

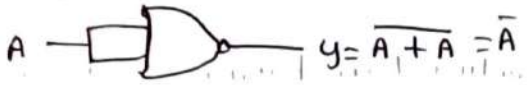
OR gate.



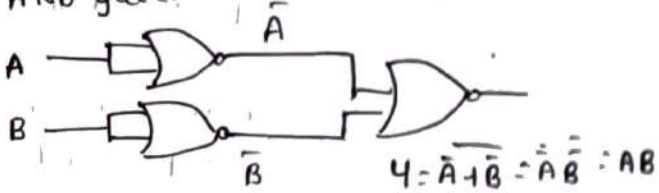
- 4M

(ii) Construction of NOT, AND & OR gates using NOR gate.

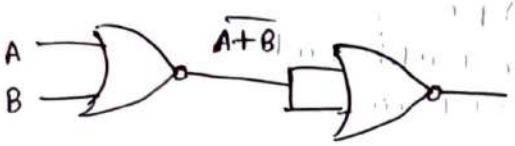
NOT gate.



AND gate.



OR gate.



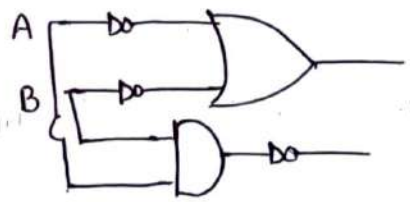
- 4M

7c. State & prove De-morgan's theorem. - 4M

A: $\overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$	$\overline{A \cdot B}$
0	1	1	0	0	1	0
0	0	1	1	1	0	1
1	0	0	1	0	1	0
1	1	0	0	0	1	0

LHS = RHS

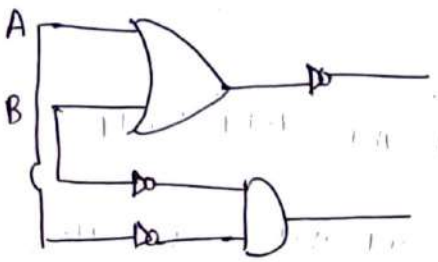


- 2M

(iii) $\overline{A \cdot B} = \bar{A} + \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	$\overline{A \cdot B}$	A + B	$\overline{A+B}$
1	0	0	1	1	0	1
0	0	1	1	01	0	1
0	1	1	0	1	0	1
1	1	0	0	0	1	0

LHS = RHS



– 2M

8a. Briefly explain minterm, maxterm, SOP & POS forms with example – 8M

A:- 1) minterm :- A minterm is a product term having are the literals in it either in complimented or uncomplimented form. It evaluates for 1

Ex:- $a + \bar{b}c$

$a(b+\bar{b})(c+\bar{c}) + (a+\bar{a})\bar{b}c$

$abc + a\bar{b}c + a\bar{b}c + a\bar{b}\bar{c} + a\bar{b}c + \bar{a}\bar{b}c$

$111 + 101 + 101 + 100 + 101 + 001$

$= m_7 + m_6 + m_5 + m_4$

$\Sigma m(4,5,6,7)$

2) Max term :- A max term is a sum of area the literate in it either in compliment or uncomplimented form. It evaluates for 0.

Ex :- $(a+b\bar{b}+c\bar{c})(b+c+a\bar{a})$

$: (a+b+c)(a+b+\bar{c})(a+\bar{b}c)(a+\bar{b}+\bar{c})$

$= [b+c+a][\bar{a}+b+c]$

$= M_0 M_1 M_2 M_3 M_0 M_4$

$= \Pi M(0,1,2,3,4)$

3. SOP :- A Sum of products is a logical or of multiple literals

$y = AB + BC + AC$

4. POS :- A product of Sum is the logical & of multiple Sum term. It evaluates for '0'

Ex :- $F(A,B,C) = AB + BC + AC$

4 x 2M = 8M

8.b. Design the working of full adder using basic gates. — 8M

A: A full adder is a 1-bit adder which can add 3-1 bit numbers i/p say A, B & C. & produces 2-1 bit results sum(S) & Cout (carry)

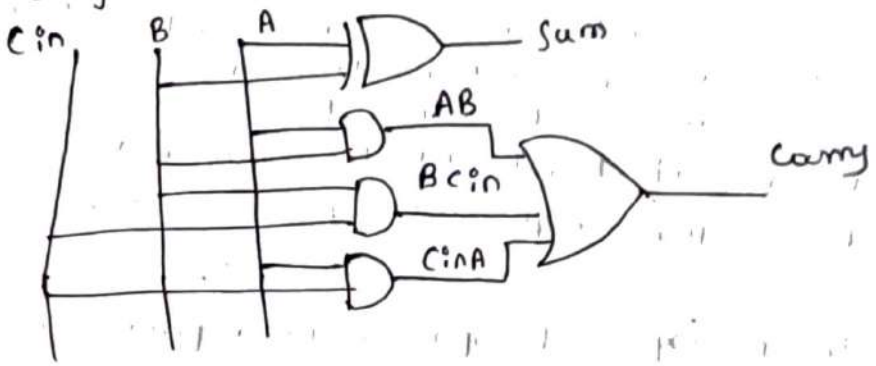
A	B	Cin	Sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	1	0	0

A	B	Cin	S	C.
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

— 4M

$Sum = A \oplus B \oplus C_{in}$.

$Carry = AB + BC_{in} + C_{in}A$



— 4M

— 4M

8c. Reduce the expression

(i) $A+B+C + A\bar{B}C + AB\bar{C}$

A: $AB(C+C') + ABC$

$AB(1) + ABC$

$AB + ABC$

$AB(1+C) = AB$

$AB(1) = AB$

— 2M

(ii) $AB + \bar{A}\bar{C} + A\bar{B}C(AB+C)$.

using De morgan's rule.

$\bar{A}\bar{C} = \bar{A} + \bar{C}$

$AB + \bar{A} + \bar{C} + A\bar{B}C(AB+C)$

$= AB + \bar{A} + \bar{C} + A\bar{B}CAB + CC$

$AB + \bar{A} + \bar{C} + A\bar{B}CAB + 0$

$A\bar{B}CAB = A\bar{B}CAB$

$AB + \bar{A} + \bar{C} + A\bar{B}CAB$

$AB(C1 + \bar{C}A) + \bar{A} + \bar{C}$

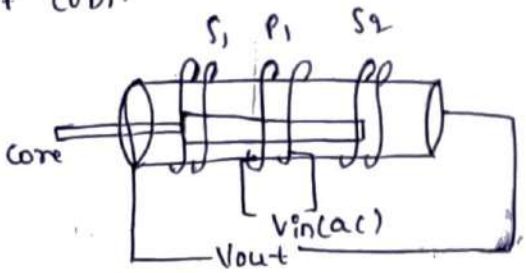
$= AB + \bar{A} + \bar{C}$

— 2M

Module-5

9.a Describe the working of a linear Variable differential transducer (LVDT) with neat diagram — 8 M

A:- working of LVDT.



— 4M

It consists of 2 secondary windings S_1 & S_2 & primary winding P_1 movable core, If core is moved towards S_1 then,

$V_{out} = V_{S1} - V_{S2}$; if core is towards S_1 then,

$V_{out} = V_{S2} - V_{S1}$ which indicates the change in Voltage w.r.t change in distance, Here displacement is converted to voltage.

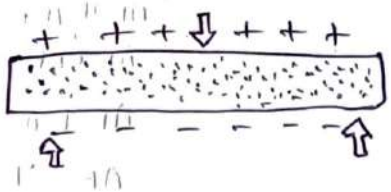
— 4M

9b. With neat diagram, explain the operation of a pizoelectric transducer. — 8 M

A:- Pizoelectric transducer:

Pizoelectric transducers are a type of electrostatic transducer that convert the electrical charges produced by some forms of solid materials into energy.

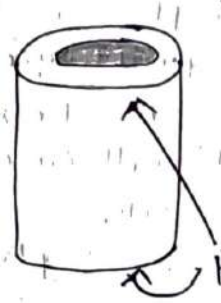
If a mechanical stress is applied to a water of quartz crystal, a Voltage proportional to the stress appears at the surfaces of the crystal as shown.



— 4M

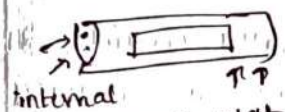
The properties are the result of the crystal structure of the quartz and all materials that behave in this way are termed pizoelectric. Because the crystal resonance frequency is extremely stable pizoelectric crystals are widely used to stabilizing the freq of oscillators. They are also used on pressure transducers.

Cylindrical transducers:



cylindrical-shaped synthetic piezoelectric device consisting of electrical constant plates at an each end. one application of this device is a pressure transducer for listening to sea noises with a preamplifier inverted inside the cylinder ends are sealed and the device is suspended at the end of a long cable from a board. The pressure variations due to ship engine noise for example generate electrical signals at the transducer terminals. These are amplitude and fed to the surface for processing.

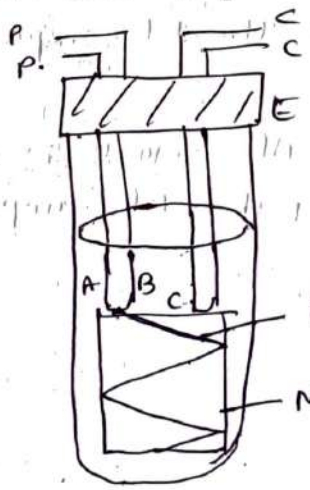
Bimorph:



A ceramic device known as bimorph when supported at one end, electrical signals are generated at the internal and external electrodes by vibrations applied to the other end. This type of device is to a record player cartidge. The minute vibrations are generated as the stylus moves in a record tracks are converted into electrical signal which are then amplified & applied to speakers. — 4M

9C. Briefly explain with Diagram of a resistance thermometer. — 4M

A:



— 2M

* It consists of a mica crossed frame, inside which a platinum in coil from is present. The whole arrangement is placed in an evacuated tube of a stainless steel. The coil from arrangement generates the least strain when the temperature rises. As tension increases with an increase in the strain. So, this will cause an undesirable change in the resistance of the wire.

* we can have better electrical insulation when mica is placed between the evacuated tube & platinum coil.

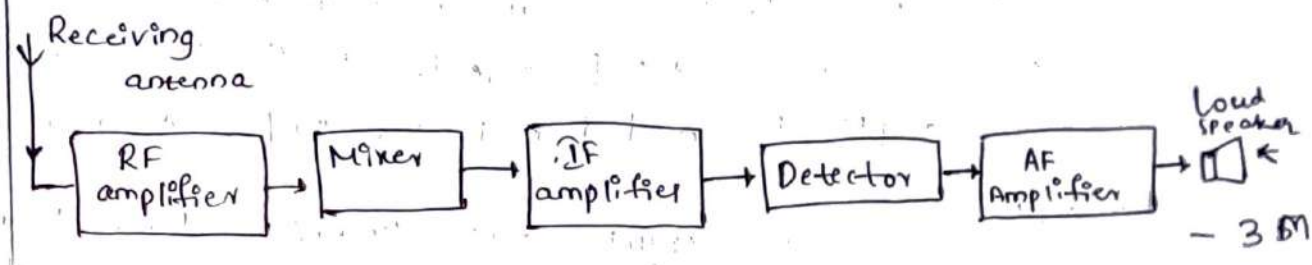
- 2M

*

10.a Describe with Diagram an AM Superheterodyne receiver. explain each block.

- 8 M

A:-



- 3 M

(i) RF amplifier: The RF amplifier uses a tuned parallel circuit. The radiowaves form various broadcasing stations are intercepted by the receiving antenna & are coupled to this stage

(ii) Mixer & local oscillator:- The amplified output of RF amplifier is fed to the mixer stage, where it is combined with the output of a local oscillator.

(iii) IF amplifier:- The output of the mixer circuits is fed to the tuned if amplifier. This amplifier. This amplifier, This amplifiers is tuned to one frequency. (i.e; 455kΩ) & is amplified.

(iv) Detector:- The output from the I.F amplifier is coupled with input of a detector.

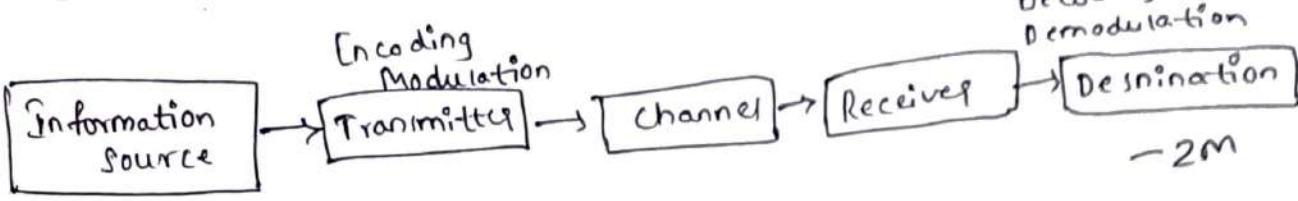
(v) AF Amplifier:- The detected AF signal is usually weak & so it is further amplified by the AF amplifier.

-5M

10.b. Explain the various blocks involved in communication block. — 8 m

diagram.

A:



— 2M

1) Source
2) Destination
3) Transmitter
4) Channel
5) Receiver.

for electrical communication purpose, first we need to convert to message signal to electrical form, which achieved using a suitable transducer. Transducer is a device which converts energy in one form to other

Transmitter:- High frequency signal is essential for carrying out an important occupation called modulation. The high frequency signal called carrier. The carrier signal is characterized to three parameters amplitude, frequency & phase

* Channel:- Channel is the physical medium which connects the transmitter with that of the receiver.

* Receiver:- Receiver block receives the incoming modified version of the message signal from the channel & processes it to secreate the original form of the message signal.

* Demodulation:- is the most important one which converts the message signal avaiable in the modified form to the original electrical version of the message

* Destination:- Destination is the final block in the communication sim which services the message signal & processes it to comprehend the information present it

10 c. $L = \frac{k}{g}$ $\therefore k = 1m \times 0.001 = 1 \times 10^{-6}$, $g_{new} = 1mm - L_{new} = k/g_{new}$ — 6 M — 4M

$g_{new} = \frac{1}{8} \times 10^{-2}$ Now, $\Delta L = L_{new} - L_{initial} = 1.25mH - 1mH$

$= 0.25\ mH$ — 4M