KLS Vishwanathrao Deshpande Institute of Technology

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(Recognized Under Section 2(f) by UGC, New Delhi)
Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada
Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813
www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper Scheme & Solution

Faculty Name	:	Prof. Plavin f Dias.
Course Name	:	Basic Electronics for EEE Stream
Course Code	:	BBEE103/203
Year of Question Paper	:	Dec 2024 / Jan 2025
Date of Submission	:	14.07.2025

Faculty Member

HoD
14.07.2025

Dean (Acad.)

Dean Academics
KLS VDIT, HALIYAL

Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T., HALIYAL (U.K.)

CBCS SCHEME

USN | | | | | | | | | | |

BBEE103/203

First/Second Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025

Basic Electronics for EEE Stream

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the VI characteristics of PN junction diode.	06	L2	CO1
	b.	Explain the operation of center tapped full wave rectifier.	08	L2	CO1
	c.	Design the zener diode regulator for the following specification. I_L = 10 mA , V_0 = 5 V, I_{zmin} = 1 mA , I_{zmax} = 25 mA and V_i = 10 V.	06	L3	CO1
		OR			
Q.2	a.	Explain the halfwave rectifier with 'C' filter.	07	L2	CO1
	b.	Explain the operation of zener voltage regulator.	07	L2	CO1
	c.	With relevant circuit explain the concept of Load line analysis of a diode.	06	L2	CO1
		Module – 2			
Q.3	a.	Explain common emitter input and output characteristics of a BJT.	08	L2	CO2
	b.	Explain various voltages and currents of BJT.	07	L1	CO2
	c.	With neat circuit diagram, explain DC line concept of a transistor amplifier to fix the Q point.	05	L2	CO2
		OR			
Q.4	a.	Explain the construction and operation of a JFET.	08	L2	CO2
	b.	Explain the construction and operation of a enhancement MOSFET.	08	L2	CO2
	c.	Mention any four differences between BJT and JFET.	04	L1	CO2
		Module – 3			
Q.5	a.	Define (i) CMRR (ii) Slew rate (iii) Input offset voltage (iv) Input offset current.	08	L1	CO2
	b.	Design a op-Amp circuit to get output voltage $V_0 = -(3V_1 + 2V_2 + 0.5V_3)$. Assume R_f = 10 kΩ.	06	L1	CO2
	c.	Derive the expression for the output voltage of a non-inverting amplifier.	06	L2	CO2

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		OR			
Q.6	**a.**	Mention any six ideal characteristics of an opamp.	**06**	**L1**	**CO2**
	b.	Derive the expression for output voltage of a differentiator circuit.	**07**	**L2**	**CO2**
	c.	Derive the expression for the output voltage of a three input inverting summing amplifier.	**07**	**L2**	**CO2**
		Module – 4			
Q.7	**a.**	Convert : (i) $(23.25)_{10} = (\quad)_2 = (\quad)_{16}$ (ii) $(3250)_{10} = (\quad)_8 = (\quad)_{16}$	**06**	**L2**	**CO3**
	b.	Given the two binary numbers X = 1010100 and Y = 1000011 , perform the subtraction (i) X – Y (ii) Y – X , using two's complement.	**08**	**L2**	**CO3**
	c.	Design Half adder using basic gates.	**06**	**L2**	**CO3**
		OR			
Q.8	**a.**	Prove Demorgan's theorem for two variables.	**06**	**L2**	**CO3**
	b.	Design full adder using basic gates.	**08**	**L2**	**CO3**
	c.	Express the Boolean function $F = xy + \bar{x}z$.	**06**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Explain the operation of LVDT.	**08**	**L2**	**CO4**
	b.	Explain breifly block diagram of a communication.	**08**	**L2**	**CO5**
	c.	Mention the applications of optoelectric transducer.	**04**	**L1**	**CO2**
		OR			
Q.10	**a.**	Explain the operation of photodiode transducer.	**06**	**L2**	**CO4**
	b.	Explain briefly Thermistor transducers.	**08**	**L2**	**CO4**
	c.	Define Modulation. Explain the need for modulation.	**06**	**L1**	**CO5**

* * * * *

1 a. VI characteristics of PN Junction diode (6M)

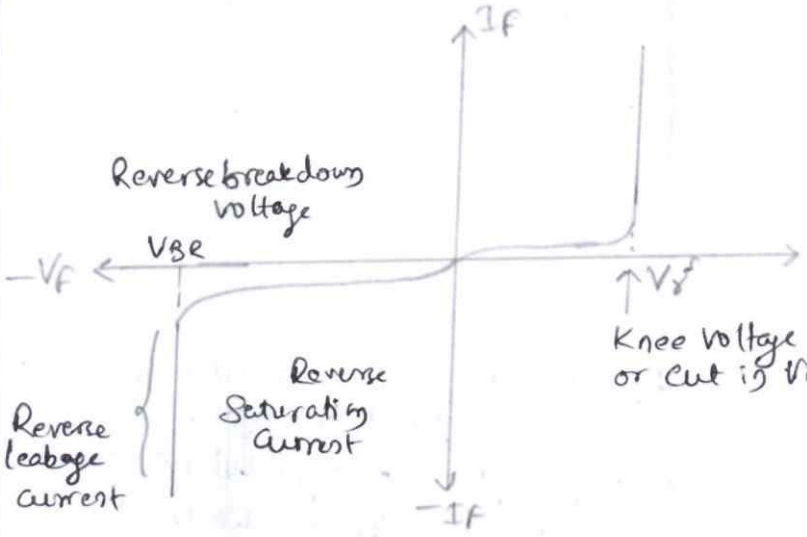
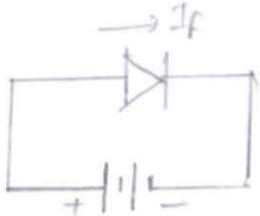
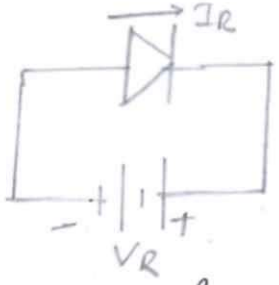


fig (a) VI characteristics of PN Diode



If → forward current
Vf → forward voltage

fig(a) forward bias of PN Junction diode



IR → Reverse current
VR → Reverse voltage.

fig.b. Reverse bias of PN Junction Diode.

forward and Reverse characteristics of diode are referred as VI characteristics of PN Junction Diode.

1. Knee voltage or cut in voltage V_γ: It is the amount of forward biased voltage needed to be applied across the diode at which current increases linearly. Typical values are 0.6 to 0.8V, for silicon diode and 0.3 to 0.4 V for Germanium diode.
2. Forward voltage: V_f. It is the voltage applied across the diode under forward biased condition or amount of voltage needed to get current to flow across a diode.
3. forward current I_F: It is the amount of current that flows through the diode from P to N under forward biased condition.
4. Reverse saturation Current (I_r): It is very small amount of reverse current that flows through the diode from N to P under reverse bias condition, typically it remains constant for a range of reverse biased voltage.
5. Reverse Breakdown voltage (V_{BR}): It is the reverse biased voltage value at which maximum reverse current is seen initially. Typical value are -75V for Si and -35 for Ge. (3+3)

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b. Center tapped full wave rectifier: (8M)

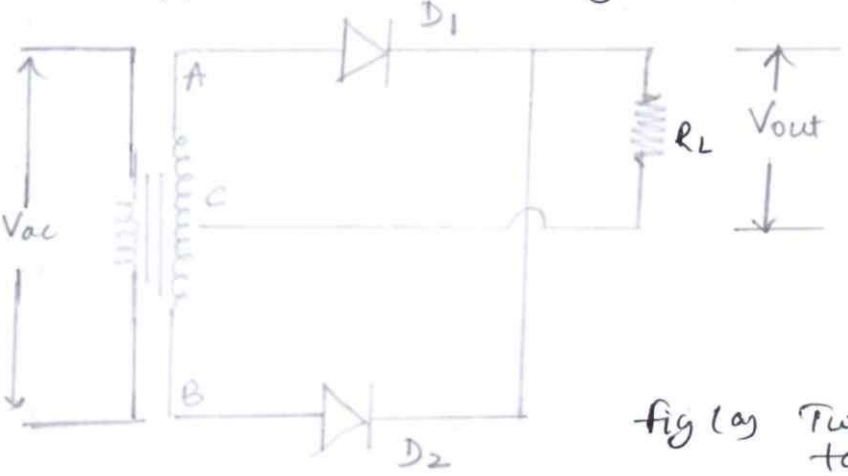
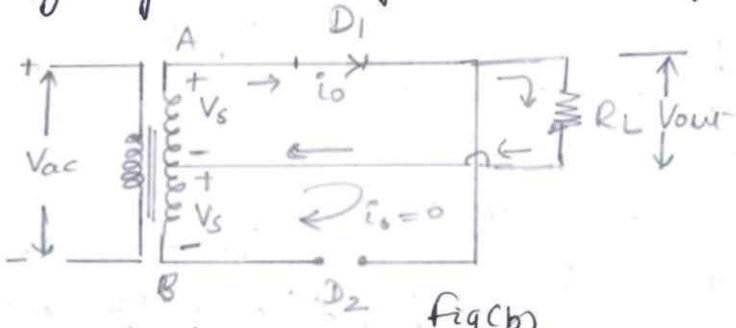


fig (a) Two diode model or center tapped rectifier.

Consider the circuit in positive half cycle of input. End A will be positive and End B will be negative. Hence diode D_1 is forward biased and D_2 is reverse biased. Hence the current flows from secondary to load via D_1 where as no current flow through Diode D_2 via R_L. Hence only D_1 is "ON" in positive half of the input, the equivalent circuit is shown in fig(b)



fig(b)

$$\therefore i_o = \frac{V_{out}}{R_L}$$

$$I_m = \frac{V_m}{R_L}$$

if Internal resistance is taken,

$$I_m = \frac{V_m}{R_f + R_L} \quad \text{or} \quad i_o = \frac{V_s}{R_f + R_L}$$

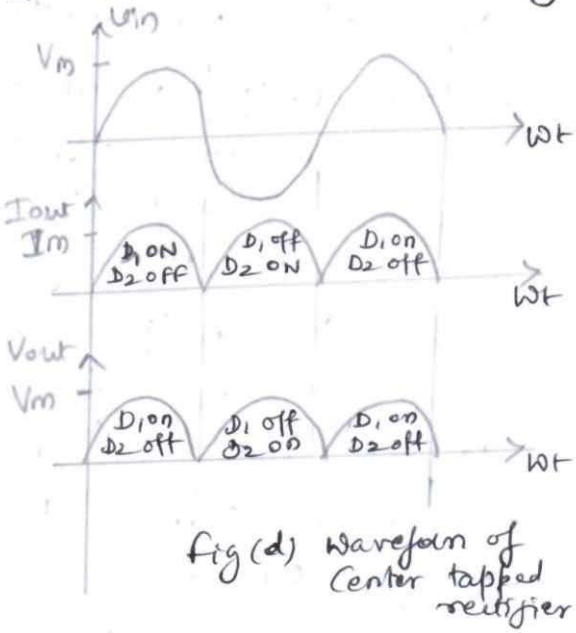


fig (d) Waveform of Center tapped rectifier

During negative half cycle of input signal the polarity of A will be negative and polarity of B will be +ve. hence D_2 is forward bias and D_1 is reverse bias. Hence D_2 only conducts. The equivalent circuit is shown in fig (c)

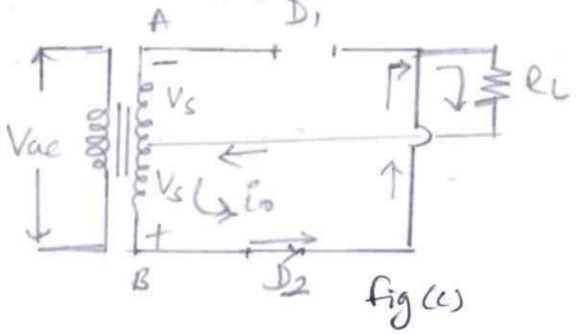


fig (c)

$$i_o = \frac{V_{out}}{R_L}$$

$$i_o = \frac{V_s}{R_f + R_L}$$

3+5

1c Zener diode regulator (6M)

(1+3+2)

Given $I_L = 10\ mA$

$V_o = 5V$

$I_{Z min} = 1\ mA$

$I_{Z max} = 25\ mA$

$V_i = 10\ V$

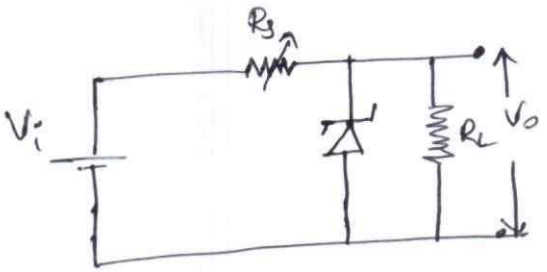
$$R_L = \frac{V_o}{I_L} = \frac{5}{10 \times 10^{-3}} = 500\ \Omega$$

$$R_{S min} = \frac{V_i - V_o}{I_{S max}} = \frac{10-5}{26 \times 10^{-3}} = 192\ \Omega$$

$I_{S max} = 26\ mA$

$I_{S min} = 11\ mA$

$$R_{S max} = \frac{V_i - V_o}{I_{S min}} = \frac{5}{11 \times 10^{-3}} = 455\ \Omega$$



2a. Half wave rectifier with 'c' filter (07)

(03+02+02)

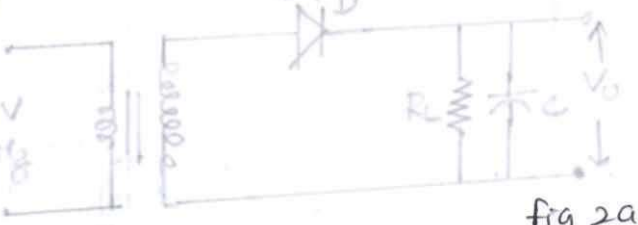


fig 2a. Half wave rectifier with 'c' filter

During positive half cycle of sinewave or input signal the diode D is forward biased and thus capacitor charge toward the peak of the applied input signal. When the applied input signal becomes less than the peak voltage, the capacitor stops charging because voltage across it is more than incoming and, when the input signal reaches the negative half cycle diode becomes reverse bias and thus capacitor starts to discharge through the load resistance R_L. The choice of C is high value so that discharging rate of the capacitor is controlled.

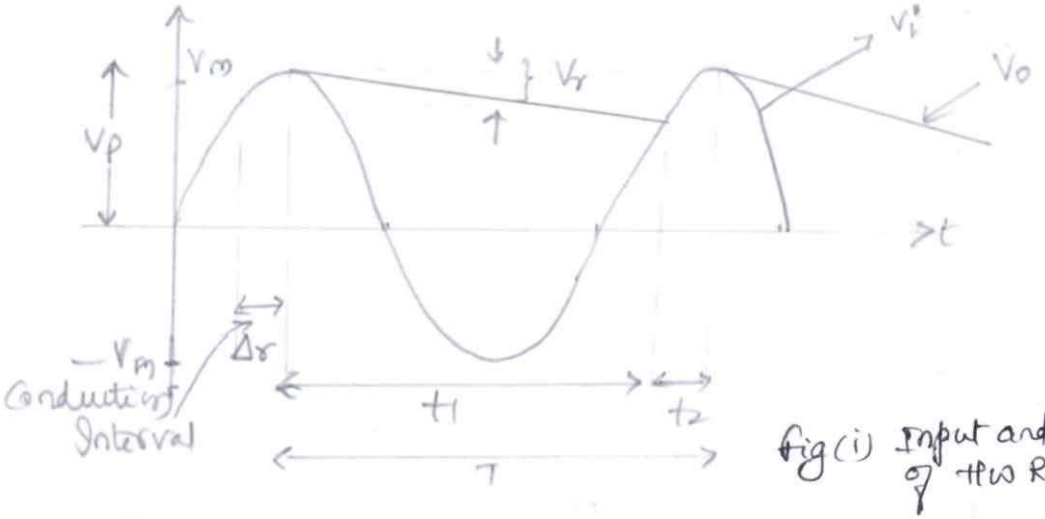


fig (i) Input and Output waveform of the Rectifier with 'C' filter

V_r → DC voltage with ripple
t_1 → discharging of capacitor
t_2 → charge of capacitor

2b. Zener voltage Regulator

(07)
(3+2+2)

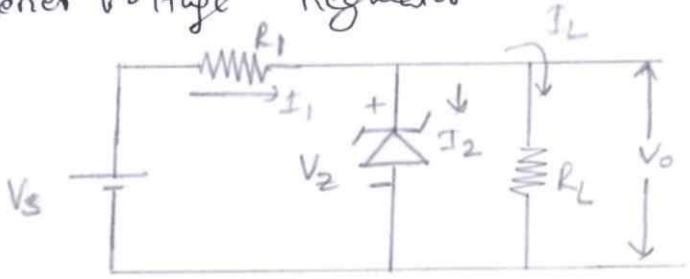


fig 2b. Voltage Regulator with load.

In the circuit current through R_1 is I_1 and it can see two path further to flow that is through zener diode and through load

$$\therefore I_1 = I_Z + I_L$$

Let $I_Z = I_{Zk}$ (I_{Zmin} → minimum current to keep the diode in reverse biased condition)

$I_L = I_{L\,max}$ (I_L → current through load. Assume it as maximum

$$\therefore I_1 = I_{Zk} + I_{L\,max}$$

Apply KVL to the circuit

$$-V_S + I_1 R_1 + V_Z = 0$$

$$I_1 R_1 = V_S - V_Z$$

$$\therefore I_1 = \frac{V_S - V_Z}{R_1} \quad \text{where } I_1 = I_{Zk} + I_{Zmax}$$

We know, as V_Z = constant, V_o is also constant.

$$I_1 = I_Z + I_L$$

$$I_2 = I_1 - I_L$$

$$\therefore I_2 = \left(\frac{V_S - V_2}{R_1}\right) - I_L$$

The load current varies between no load (zero) and maximum $I_{L\max}$
ie $I_L = 0$ to $I_{L\max}$.

i) When load current is maximum,

$$I_L = I_{L\max}$$

then $$I_2 = I_{2\min}$$

Care must be taken that, $I_{2\min}$ is large enough to keep the diode in reverse breakdown. —①

$$\therefore I_1 = I_2 + I_L \quad —②$$

$$\therefore I_1 = I_{2\min} + I_{L\max}$$

(ii) When load current is zero, $I_L = 0$

then entire I_1 flows through the zener diode.

Ensure, The total current does not exceed maximum zener diode current I_{2m},

$$\therefore I_1 = I_2 + \cancel{I_L}^{0}$$

$$\therefore I_1 = I_{2m} \quad —③$$

Substitute ③ in ②

$$I_{2m} = I_{2\min} + I_{L\max}$$

$$\therefore R_1 = \frac{V_S - V_2}{I_{2m}}$$

2c) Load line analysis of diode. (06) (03+03)

A DC loadline is a straight line on the diode forward characteristics, which describes all the dc conditions that exist in the operation of the circuit.

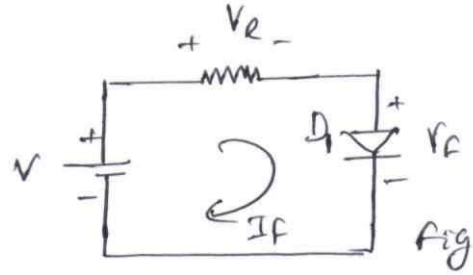


Fig 1. Diode resistor series circuit

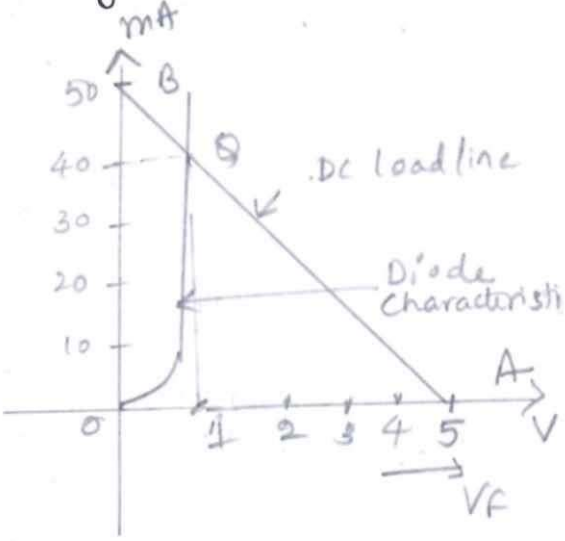


fig 2. Plot of DC load line

Consider Diode resistor series circuit, as shown in fig (1)

where I_F → Current through diode

V_F → Voltage across the diode.

DC load line is drawn on the diode forward characteristics.

The load line is plotted with any two values of circuit current voltage pair,

Apply Kirchhoff's voltage law to the circuit,

$$-V + V_R + V_F = 0$$

$$V = I_F \cdot R_1 + V_F \quad \text{—(1)}$$

(1) is the Equation of dcload line.

Calculate V_F when $I_F = 0$ & I_F when $V_F = 0$

from (1), when $I_F = 0$

$V = V_F$

$\therefore V_F = V$

from fig (2) at $V_F = 5V$, $I_F = 0\,mA$.

from (1) when $V_F = 0$

$V = I_F \cdot R_1$

$\therefore I_F = \frac{V}{R_1}$

$\therefore V_F = 0, \quad I_F = \frac{V_1}{R_1}$

$V_F = 0, \quad I_F = \frac{5}{100} = 50\,mA.$

Join AB to get DC loadd line.

Assume $R_1 = 100\Omega$, $V = 5V$.

DC load line intersects the diode characteristics at the point Q.

$$I_F = \frac{V - V_F}{R_1}$$

Let $V_F = 1\,V$

$$\therefore I_F = \frac{5-1}{100\Omega}$$

$$= 40\,mA //$$

Q. (V_F, I_F) DC bias point

3 a. Common Emitter input and output characteristics of a BJT (08)

(2+2+2+2)

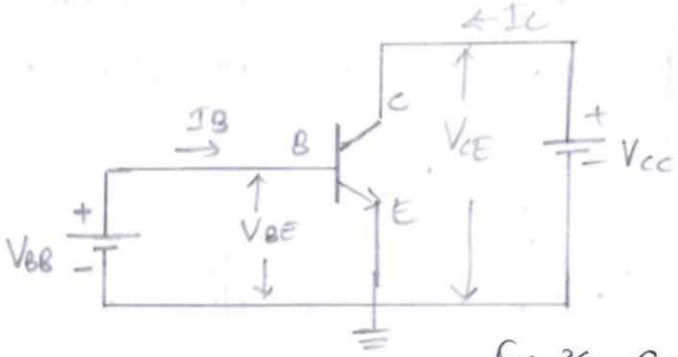
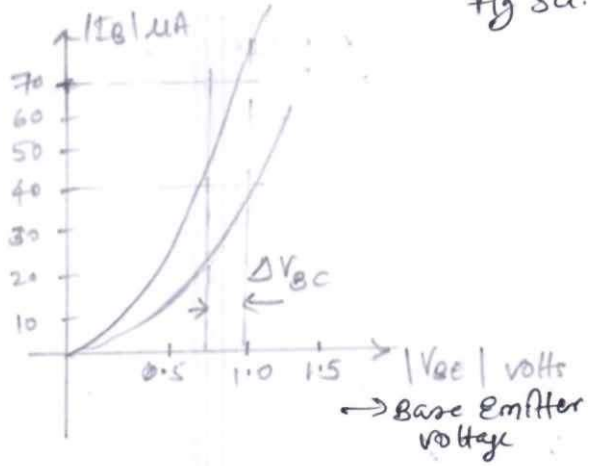
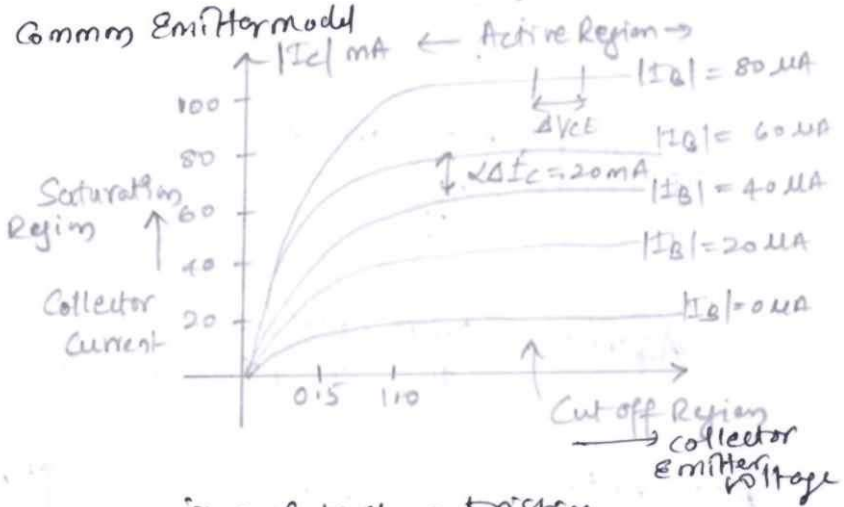


fig 3a. Common Emitter model



(i) Input characteristics of Transistor in CE configuration



(ii) Output Characteristics

Input resistance is the ratio of change in base emitter voltage, to the resulting change in base current, at constant emitter voltage V_{CE}

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

As transistor is in CE configuration, input to a transistor is between base to emitter junction, the CE input characteristics resembles forward biased diode curves.

After the cut in voltage, base current (I_B) increases rapidly with small increase in base emitter voltage V_{BE}, Thus the dynamic input resistance is small in CE configuration.

For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased

The input voltage is applied between the base and emitter terminals and the output is taken at the collector and emitter terminals so that the emitter terminal is common to both input and output.

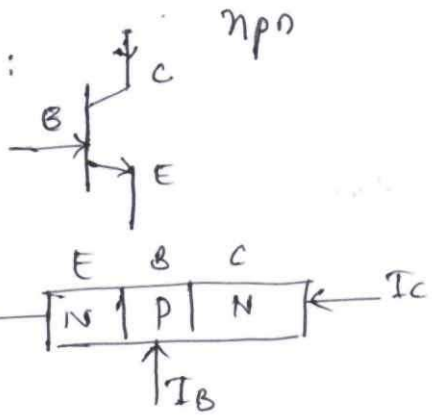
The slope of the output characteristics is termed as Early Effect.

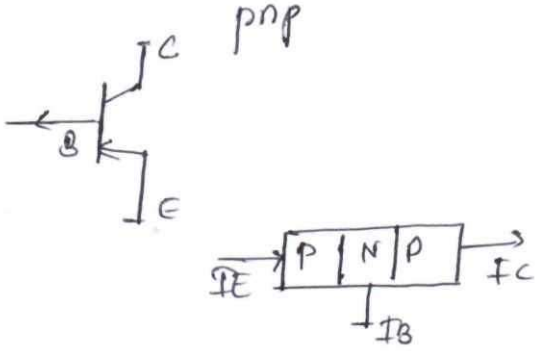
3 b. Voltages and Currents of BJT (07) (3+4)

BJT Stands for Bipolar Junction Transistor,

It is a 3 layer, 3 Terminal and two junction semiconductor device.

BJT current :

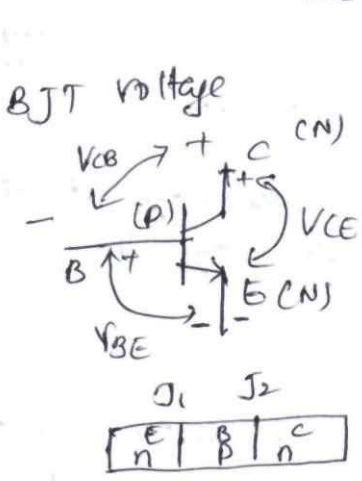


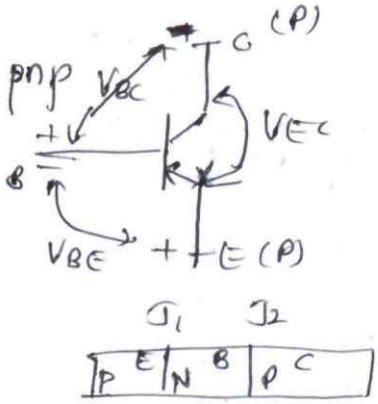


Assume NPN, PNP as node,

$$I_E = I_B + I_C \quad \longleftarrow (1)$$

BJT voltage





$$\alpha dc = \frac{I_C}{I_E}$$

αdc → Emitter to Collector dc current gain

I_C → dc collector current

I_E → dc emitter current

$$\beta dc = \frac{I_C}{I_B}$$

βdc → Base to collector dc current gain

I_B → dc base current.

It is referred as h_{FE}.

3c. DC line concept of transistor amplifier to fix the Q point. (05) (2+3)

When a diode is forward biased, then to determine the corresponding precise level of diode voltage and diode current a graphical analysis is employed it is known as DC load line analysis.

If we have the diode forward characteristics, as shown in fig 3c(i) and (ii)

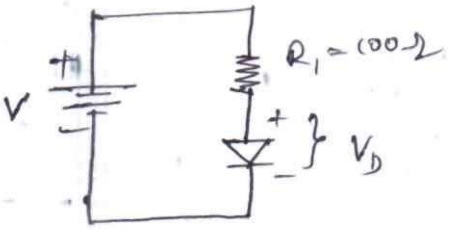


fig 3c(i)

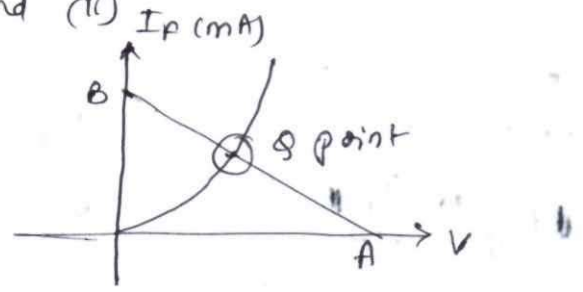


fig 3c (ii)

From fig 3c(i)

$$-V + I_F R_1 + V_D$$

or $$V = I_F R_1 + V_D$$

from ①,

Q can be obtained when $V_D = 0$

A can be obtained when $I_F = 0$

Point Q is referred to as Q point (Quiscent Point) or Operating point

The intersection of diode forward characteristics and the ① load line is called the Q point also referred as dc bias point.

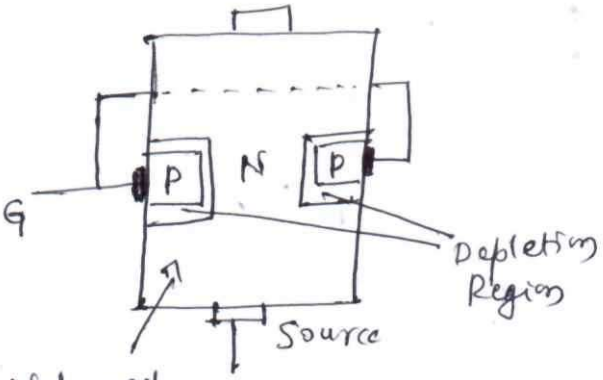
Q : (V_F, I_F)

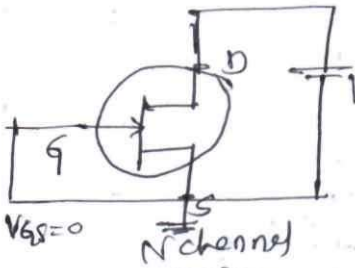
$V = I_F R_1 + V_F$ //

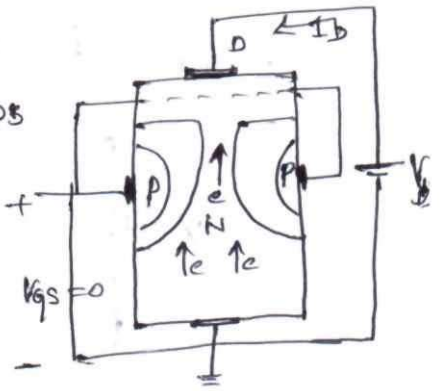
The external resistor is called load resistor & denoted as R_L

4 a. Construction and Operation of JFET. (8m) (4+4)

JFET is a type of FET that operates with a reverse biased pn junction to control current in a channel. Depending on the structure JFET are classified into n channel and p channel JFET. If the channel is of N type semiconductor then it is 'N' channel JFET. If channel is of P type semiconductor, then it is p channel JFET.







In a N channel JFET an N type semiconductor material forms a channel between two embedded layers of p type material. The two pN junctions are formed between semiconductor channel and two semiconductor layer. Ohmic contacts are made at the top and bottom of channel, referred as drain (d) and source (S). Both P layers connected together to form gate (G) terminal.

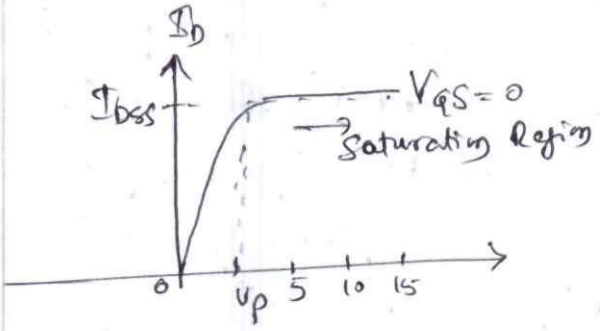
When V_{DS} is applied and $V_{GS}=0$,

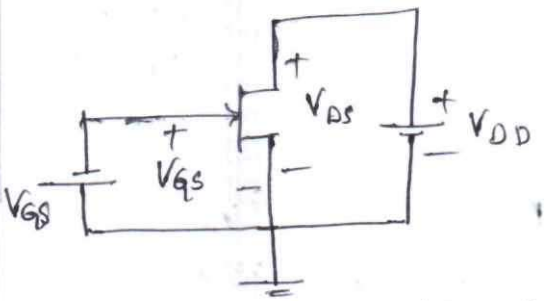
When the drain source voltage is applied, positive of power supply is connected to source. Due to negative potential at source, the electrons starts to repel and move toward drain terminal, establishing the flow of drain current (I_D). The value of I_D is determined by the value of V_{DS} applied and channel resistance, width of the depletion region increases near the drain region than near the source region because electrons starts to combine with holes present in the p type material. Thus there is increase in width of the depletion region due to this, there is decrease in channel width. Therefore I_D increases linearly with increase in V_{DS} later it reaches a saturation point & called as I_{DSS} (Drain source saturation current). For V_{DS} positive & $V_{GS}=0$, where saturation effect sets that voltage of is termed as Pinch off voltage, denoted by V_p.

In case of N-channel JFET, voltage V_{GS} is negative $V_{GS}=-V$ ie gate terminal is made more negative than source terminal ie p type material is connected negative of power supply this makes reverse bias condition, thus I_D decreases for V_{GS} = -ve voltage that is it makes reverse bias condition Therefore Pinch off phenomenon occurs at lower value of V_{DS} when $V_{GS} = -V_p$ then $I_D = 0$

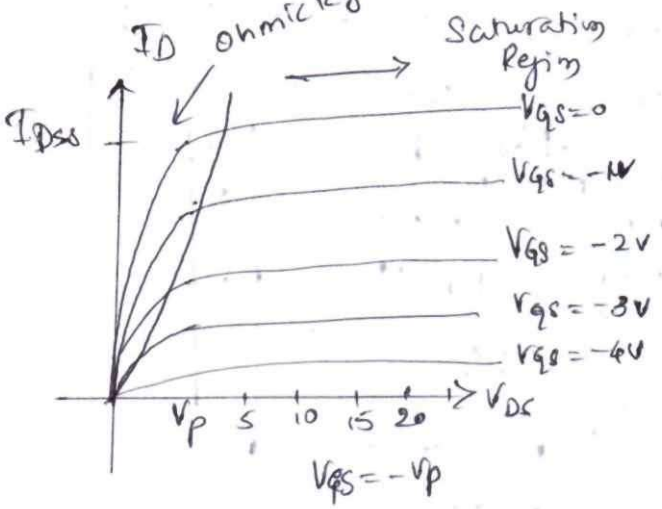
Output current I_D in the saturation for given value of input V_{GS} is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

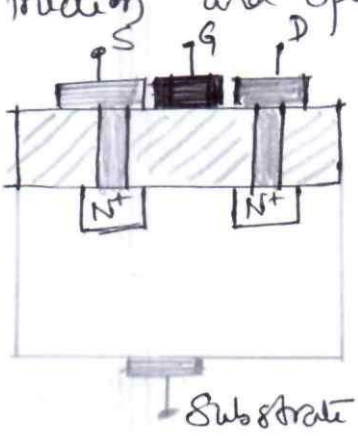


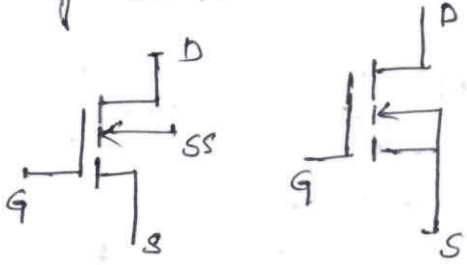


-ve gate voltage applied



*6. Construction and operation of enhancement MOSFET: (08) (4+4)



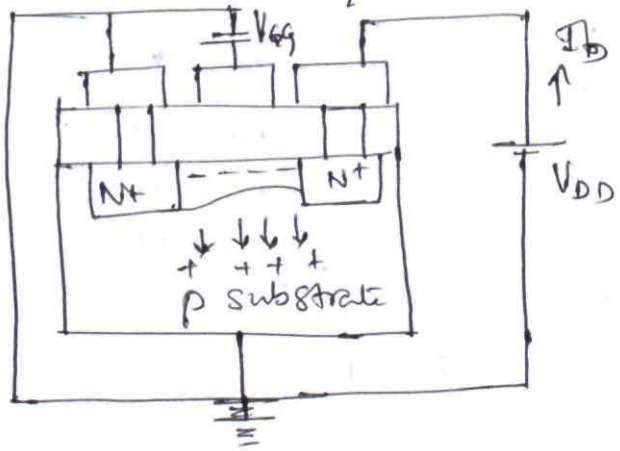


There is no physical channel between source and drain terminals in E-MOSFET.

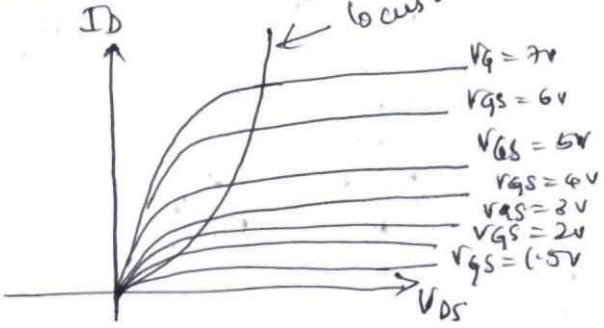
Principle of operation:

When gate source voltage is zero and V_{DS} = +ve is applied there is no drain current because there is no channel available for flow of drain current. When $V_{GS} = 0V$ E-mosfet is called as off mosfet.

When V_{GS} = +ve voltage which is applied to gate terminal electrons which are the minority carriers in p type substrate are attracted near the SiO_2 layer and the holes in the p type substrate are repelled and moved away from SiO_2 layer. The electrons that are attracted near the SiO_2 layer forms the required N channel. Anyway electrons do not get accumed by gate terminal because of SiO_2 presence. The minimum gate voltage that causes significant flow of drain current, that voltage is called as threshold voltage and denoted by V_T, for increase in V_{GS} there is increase in the flow of drain current



N channel E-mosfet with V_{GS} = +ve



$V_{GS} = V_T = 1.5$ V

O/p characteristics of N channel E-mosfet.

$V_{DS} = V_{GS} - V_T$

after V_T there is increase in I_D.

$I_D = 0$ for $V_{GS} < V_T$

I_D for $V_{GS} > V_T$ is given by

$$I_D = k\,(V_{GS} - V_T)^2$$

k is constant term which is function of construction of the device.

4c four difference between BJT and JFET: (4m)

JFET	BJT
1. It is a Unipolar device	1. It is bipolar device
2. It is voltage controlled device, input voltage controls the output current	2. It is current controlled device, output current is controlled by input current.
3 It exhibits high input resistance, many mega ohms	3. It exhibits low input resistance, few kilo ohms.
4. It is less noisy due to carriers crossing single junction.	4. It is too noisy due to carrier crossing two junction
5. Voltage gain low	5. Voltage gain High.
6. Output resistance is low	6. Output resistance is moderate.

(8m)

5a. (i) CMRR (ii) Slew Rate (iii) Input offset voltage (iv) Input offset current

(i) CMRR : CMRR is a metric used to measure the ability of the op-amp to suppress/reject the common signals. (2+2+2+2)

$$CMRR = \frac{A_d}{A_{cm}} \quad \text{or} \quad CMRR = \frac{A_d}{A_c}$$

A_d ← Gain obtained due to differential input voltage

A_{cm} ← Gain obtained due to common input voltage.

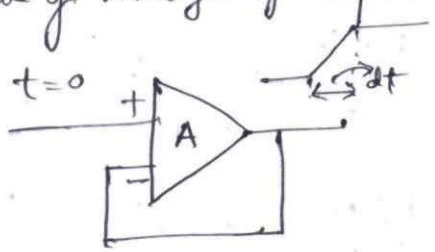
CMRR is large & expressed in dB.

$$\therefore CMRR = 20 \log\left(\frac{A_d}{A_{cm}}\right)$$

(ii) Slew Rate : It is the maximum rate of change of output voltage with respect to time.

It is denoted by SR.

$$SR = \frac{dV_0}{dt} \text{ volts/sec}$$



(iii) Input offset voltage : It is the voltage that must be applied to the input terminals of the op-amp such that it produces zero output voltage.

(iv) Input offset current : It is the difference between the current in the input terminal. It is given by

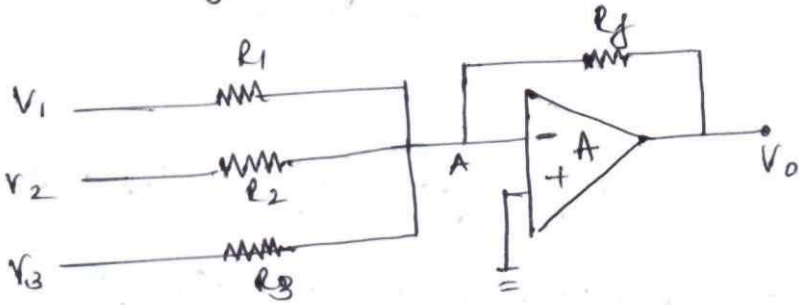
$$I_{io} = I_2 - I_1$$

where, $I_1 \rightarrow$ Current into the inverting terminal
$I_2 \rightarrow$ Current into the noninverting terminal.

5b. Op-amp circuit : (06) (3+3)

$$V_o = -(3V_1 + 2V_2 + 0.5V_3)$$

$R_f = 10\ k\Omega$ //



$$V_o = -(V_1 + V_2 + V_3)$$

$$\text{or } V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_o}{R_f}$$

$V_A = 0$ //

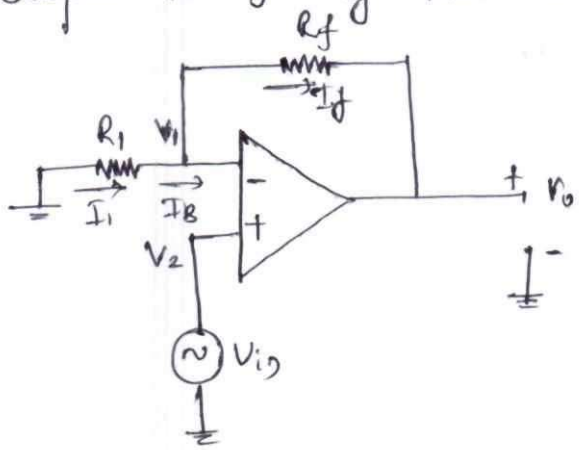
$$\therefore V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

(i) $\frac{R_f V_1}{R_1} = 3V_1$ $\quad \therefore R_1 = \frac{R_f}{3} = \frac{10\ k\Omega}{3} = 3.33\ k\Omega$

(ii) $\frac{R_f V_2}{R_2} = 2V_2$ $\quad \therefore R_2 = \frac{R_f}{2} = \frac{10\ k\Omega}{2} = 5\ k\Omega$

(iii) $\frac{R_f \cdot V_3}{R_3} = 0.5V_3$ $\quad \therefore R_3 = \frac{R_f}{0.5} = \frac{10\ k\Omega}{0.5} = 20\ k\Omega$ //

5C. Output voltage of Non Inverting Amplifier (06) (3+3)



The input signal V_{in} is applied at the non inverting input terminal of op-amp. Inverting terminal is connected to ground via resistor. Feedback resistor 'Rf' appears between output terminal and inverting input terminal.

As V_{in} is connected to non inverting terminal of op-amp.

Hence $V_2 = V_{in}$

Due to virtual ground, $V_1 = V_2$

$\therefore V_1 = V_2 = V_{in}$

Applying KCL, current entering the node is equal to current leaving the node.

ie $I_1 = I_B + I_f$

$I_B = 0$ due to $R_i = \infty$

$\therefore I_1 = I_f$

$$\frac{0 - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

Substitute $V_1 = V_{in}$

$$-\frac{V_{in}}{R_1} = \frac{V_{in} - V_o}{R_f}$$

$$\therefore V_o = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{in}$$

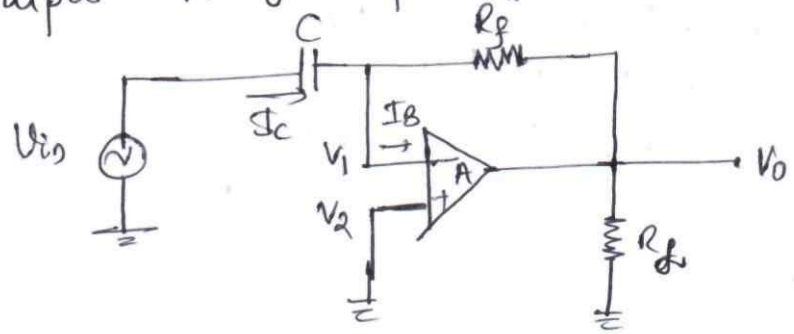
6a. Six Ideal characteristics of op-amp (06)

(1×6=6)

1. Infinite input impedance or $R_i = \infty$.
2. Output resistance $R_o = 0$.
3. Infinite Bandwidth : $BW = \infty$.
4. Infinite voltage gain
5. CMRR = ∞
6. Slew Rate = ∞.

6b. Output voltage of differentiator circuit. (07)

(3+4)



The circuit performs the mathematical operation of differentiation.
The output waveform is derivative of input waveform.

Due to virtual ground concept $V_1 = V_2 = 0$ & $I_B = 0$

Applying Kirchoff's current law at node V_1

$$I_C = I_B + I_f$$

$$\therefore I_C = I_f$$

$$C \cdot \frac{dV}{dt} = \frac{V_1 - V_o}{R_f}$$

$$C \cdot \frac{d(V_{in} - V_1)}{dt} = \frac{V_1 - V_o}{R_f}$$

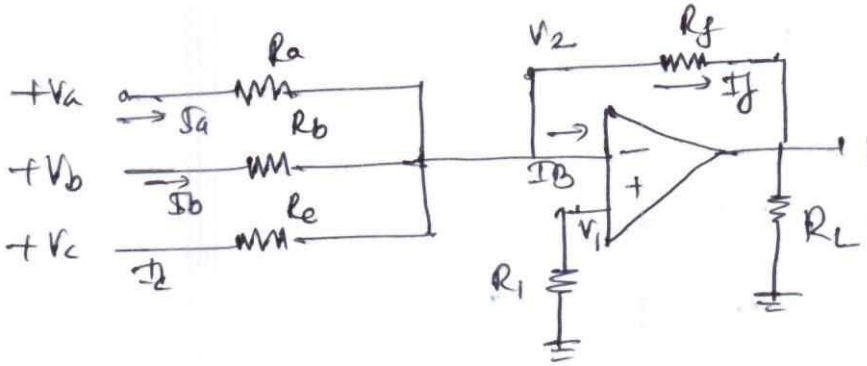
$$V_1 = 0$$

$$\therefore C \cdot \frac{dV_{in}}{dt} = \frac{-V_o}{R_f}$$

$$\therefore V_o = -\frac{1}{R_f C} \frac{dV_{in}}{dt}$$ //

6c. Output voltage of three input inverting summing amplifier (07) (3+4)

Circuit Diagram for Inverting configuration with three inputs V_a, V_b and V_c.



Inverting configuration with three inputs can be used as Summing Amplifier, Scaling amplifier, Averaging Amplifier. The circuit function can be verified by examining the expression for the output voltage V_o which is obtained from Kirchoff's current equation written at node V_2

$$\therefore I_a + I_b + I_c = I_B + I_f$$

Due to Virtual ground

$$V_1 = V_2 = 0\ V \quad \therefore I_B = 0$$

$$\frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_c - V_2}{R_c} = \frac{V_2 - V_o}{R_f}$$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_f}$$

$$\therefore V_o = -\left(\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b + \frac{R_f}{R_c} \cdot V_c\right)$$

i) Summing Amplifier $R_a = R_b = R_c = R$ $\therefore V_o = -\frac{R_f}{R}(V_a + V_b + V_c)$

If $R_f/R = 1$ $V_o = -(V_a + V_b + V_c)$

ii) Scaling or Weighted Amplifier $V_o = -\left(\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b + \frac{R_f}{R_c} V_c\right)$ where $R_f/R_a \neq \frac{R_f}{R_b} \neq \frac{R_f}{R_c}$

iii) Averaging Circuit: $V_o = -\left(\frac{V_a + V_b + V_c}{3}\right)$ $R_a = R_b = R_c = R_f$ $\frac{R_f}{R_a} = \frac{1}{n} = \frac{1}{3}$

7a. Convert (i) $(23.25)_{10} = (\quad)_2 = (\quad)_{16}$ (06) (3+3)

(ii) $(3250)_{10} = (\quad)_8 = (\quad)_{16}$

(i)

2	23	$0.25 \times 2 = 0.50$
2	11 – 1	$0.50 \times 2 = 1.0$
2	5 – 1	
2	2 – 1	
2	1 – 0 ↑	

$(23.25)_{10} = (10111.01)_2$

$= (17.4)_{16} = (17.4)_{H}$

(ii) $(3250)_{10}$

8	3250
8	406 – 2
8	50 – 6
8	6 – 2

$(6262)_8 = (6262)_0$

$(3250)_{10} = (\quad)_{16}$

16	3250
16	203 – 2
	12 – 11

12 11 2 → C B 2

$(CB2)_{16}$ //

(08 m)

7b. $X = 1010100$

$Y = 1000011$

* Perform subtracting
(i) $X - Y$
(ii) $Y - X$ Using 2's complement.

2's complement of X = 0101011 (1's complement) + 1

$$\begin{array}{r} 0101011 \\ +\quad\quad 1 \\ \hline 0101100 \end{array}$$

2's complement of Y = 0111100 (1's complement) + 1

$$\begin{array}{r} 0111100 \\ +\quad\quad 1 \\ \hline 0111101 \end{array}$$

* Invert each bit for given value

$X - Y$ = 1 0 1 0 1 0 0

0 1 1 1 1 0 1 — 2's complement of Y

1 1 1 1

(1) 0 0 1 0 0 0 1 → 0 0 1 0 0 0 1

discard

$Y - X$ 1 0 0 0 0 1 1

0 1 0 1 1 0 0 — 2's complement of X

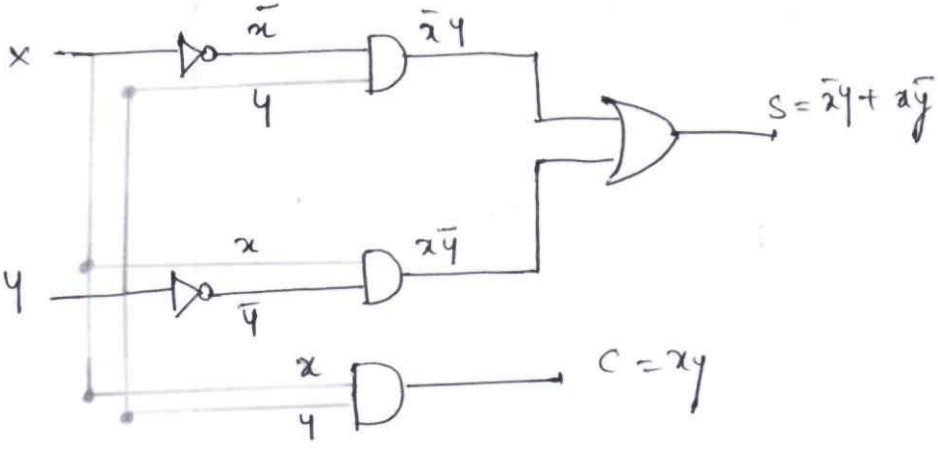
1 1 0 1 1 1 1

7c. Half adder using basic gates (06) (3+3)

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{x}y + x\bar{y}$

$C = xy$



8a. Demorgan's Theorem for Two Variables: (06)

(i) $\overline{xy} = \bar{x} + \bar{y}$ (ii) $\overline{x+y} = \bar{x} \cdot \bar{y}$

x	y	$\bar{x}$	$\bar{y}$	xy	$\overline{xy}$	$\bar{x}+\bar{y}$	$x+y$	$\overline{x+y}$	$\bar{x} \cdot \bar{y}$
0	0	1	1	0	1	1	0	1	1
0	1	1	0	0	1	1	1	0	0
1	0	0	1	0	1	1	1	0	0
1	1	0	0	1	0	0	1	0	0

8 b. full adder Using Basic Gates. (8m)

a	b	C_{in}	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

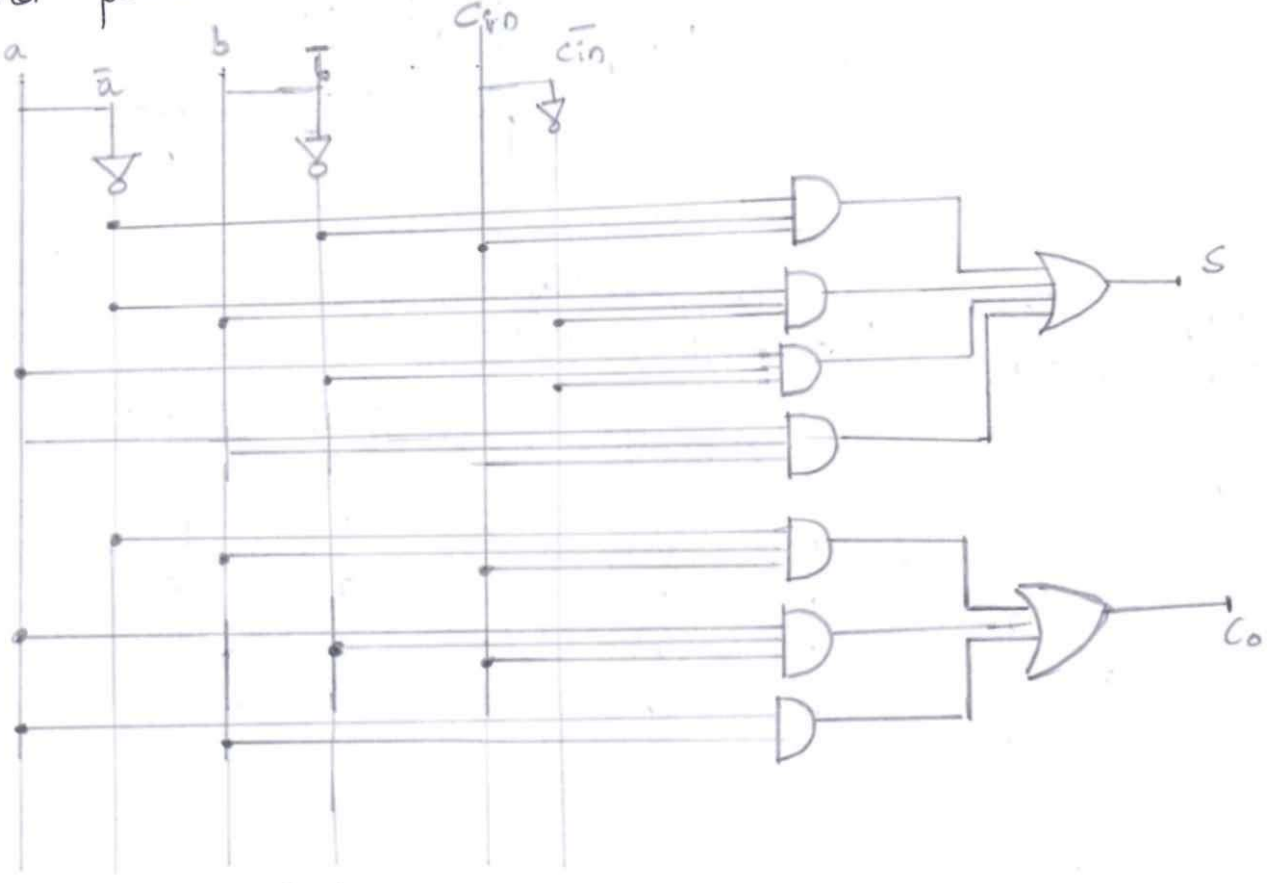
$$S = \bar{a}\bar{b}C_{in} + \bar{a}b\bar{C}_{in} + a\bar{b}\bar{C}_{in} + abC_{in}$$

$$C_o = \bar{a}bC_{in} + a\bar{b}C_{in} + ab\bar{C}_{in} + abC_{in}$$

$$= \bar{a}bC_{in} + a\bar{b}C_{in} + ab(\bar{C}_{in} + C_{in})$$

$$C_o = \bar{a}bC_{in} + a\bar{b}C_{in} + ab$$

Full adder is a combinational circuit that adds three inputs and produces two outputs.



8c. $f = xy + \bar{x}z = (xy + \bar{x})(xy + z)$ (6m)

$= (x + \bar{x})(y + \bar{x})(x + z)(y + z)$

$= (\bar{x} + y)(x + z)(y + z)$

$(\bar{x} + y) = \bar{x} + y + z\cdot\bar{z} = (\bar{x} + y + z)(\bar{x} + y + \bar{z})$

$(x + z) = (x + z + y\bar{y}) = (x + y + z)(x + \bar{y} + z)$

$(y + z) = (x\bar{x} + y + z) = (\bar{x} + y + z)(x + y + z)$

$f = (x + y + z)(x + \bar{y} + z)(\bar{x} + y + z)(x + y + z)$

9a. Operation of LVDT: (08)

(Linear Variable Differential Transducer)

The transducer is essentially a transformer with one primary winding, two secondary winding and adjustable iron core.

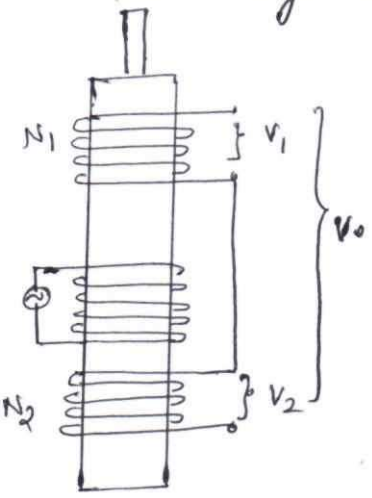
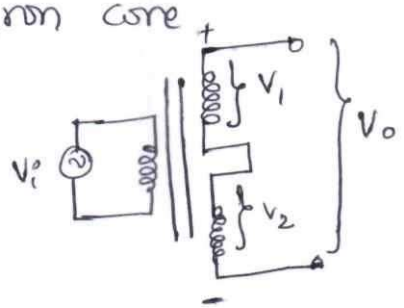


Fig 9a. LVDT has a primary winding, two secondary winding and movable iron core



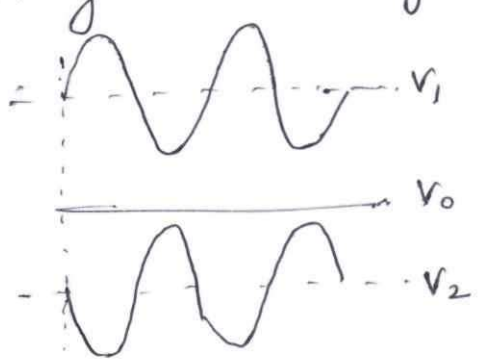
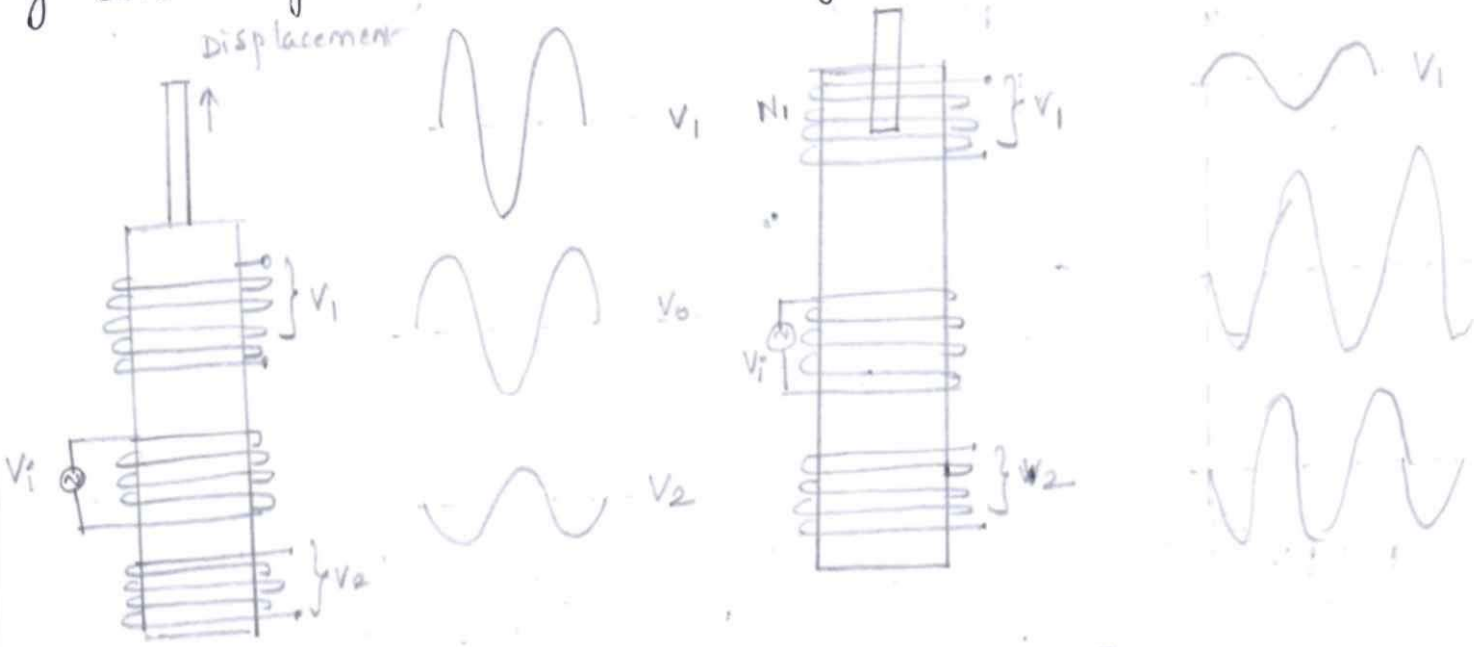


fig 9(i) Circuit diagram and waveforms.

The two waveforms are in antiphase. (out of phase)
The secondary output voltages V_1 and V_2 are equal in magnitude when the movable core is placed with equal sections of core. The output voltage V_1 is in phase with the primary input (V_i) and output V_2 is in outphase to V_i
The secondary windings are connected in series, so that the voltages cancel to produce zero output from the transducer.

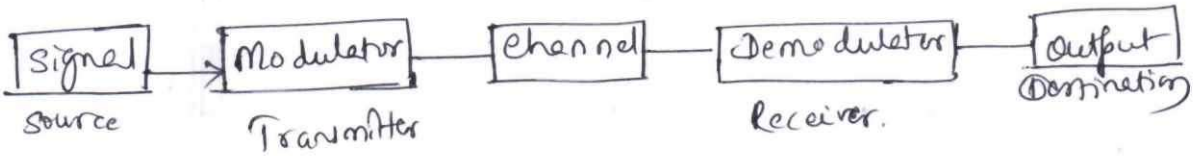
When the LVDT core is displaced upward, there is increase in the flux from the primary linking to secondary N_1 and decrease in linking with respect to secondary N_2. This causes an increase in amplitude of V_1 and decrease in V_2. Thus produces difference output voltage (V_o)

Similarly, when the core is displaced in a downward direction, V_2 increases and V_1 decreases. In this case V_o increases but with 180° phase shift from the input.
Thus the output voltage, amplitude and phase give a measure of core displacement and direction of motion.



Q5. Block Diagram of communication: (08)

Communication system include generation, storage and transmission of information. Basic elements of communication system are transmitter, receiver and communicating channels.



Communication systems are used to transfer information from a generation point to place where it is needed / processed. The information at the generation point is not in the form that can travel long distance through the channel. So device called modulator and transmitter is needed. In the receiving end the information must undergo the reverse process such as decoding or demodulation. Source is analog or digital signal. common examples of sources are analog audio, video signal, digital data.

Communication channel can be pair of conductors, optic fibre or just free space. Transducer converts any physical parameter such as temperature, pressure, flow rate into electrical signal like voltage or current or vice versa.

Applications:

- Telecommunication
- Broad casting
- Satellite communication
- Data communication
- Wireless communication

Q6. Applications of Optoelectric transducer:

- Optical communication systems : fiber optic communication
- Light detection and Ranging (LiDAR) : Robotics
- Solar Energy system : Solar panels (Photovoltaic cells)
- Barcode Scanners and optical Readers: Barcode or QR codes

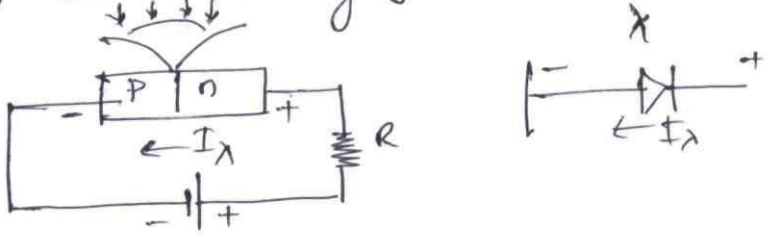
10 a. Operation of Photodiode transducer: (6m)

Photo diode is semiconductor device that converts light into electric current. It is also called Photo detector light detector, photo sensor.

Photo diode is PN junction diode that operates in reverse bias region. the reverse saturating current I_λ in uA, is limited by the availability of thirmally generated minority carrier.

As light is made to strikee on the junction, the light (photon) imparts energy to the valence electron causing more electron hole pairs to be released.

Thus reverse saturating current increases with increase in light intensity. If there is no light, then reverse saturation current is negligible.



Photodiode is a type of optoelectric transducer that converts light energy into electrical current.

Applications:

- Optical fiber receivers
- Light meters & safety sensors
- Pulse oximeters.
- Bar code readers.

10 b. Thermistor transducers. (8m)

Thermistor or thermal resistor is type of resistor whose electrical resistance varies with changes in temperature. A thermistor is a passive transducer, meaning it requires an external power source to operate and produces an output signal (change in resistance) in response to a change in temperature. These are used in temperature measurement and control applications.

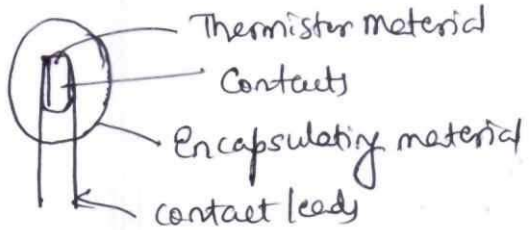
When temperature increases, the atoms in the material vibrate more vigorously leaving more electrons free to conduct electricity.

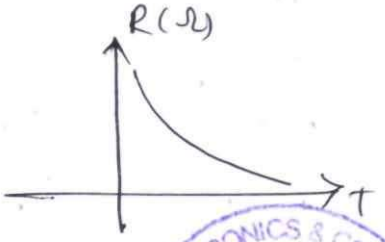
Two main types of Thermistors

- NTC : Negative Temperature Coefficient : R↓ T↑
- PTC : Positive Temperature Coefficient : R↑, T↑

Applications:

- Over current protection : PTC
- Temperature sensing : Digital Thermometer, AC,
- Automotive sensor: Temperature monitoring





Symbol

$$\ln \frac{R_1}{R_2} = \beta\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

(06 M)

10c Modulation is defined as changing the characteristics of carrier wave according to modulating or message signal.

Need for Modulation:

(i) Reduces the height of an antenna
(ii) Travelling for long distance.
(iii) Allows multiple channels on single medium
(iv) Improves signal quality and reduces noise.
(v) Enables Wireless Communication.

Modulation is essential in communicating systems for the efficient and reliable transmission of signals.

Modulation is the process of modifying a carrier signal in order to transmit information like audio video or data over a communication channel such as air cables or optical fibres.

Types of Modulation:

1) Analog Modulation
   Used for analog signals like voice, radio, TV
   Amplitude Modulation
   Frequency modulation
   Phase Modulation.

2. Digital Modulation
   Used for digital data
   Amplitude shift keying
   Frequency shift keying
   Phase shift keying

Head of the Department
Dept. of Electronic & Communication Engg.
KLS V.D.I.T., HALIYAL (U.K.)