KLS Vishwanathrao Deshpande Institute of Technology

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper
Scheme & Solution

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Course Name	:	Electronic Principles and Circuits
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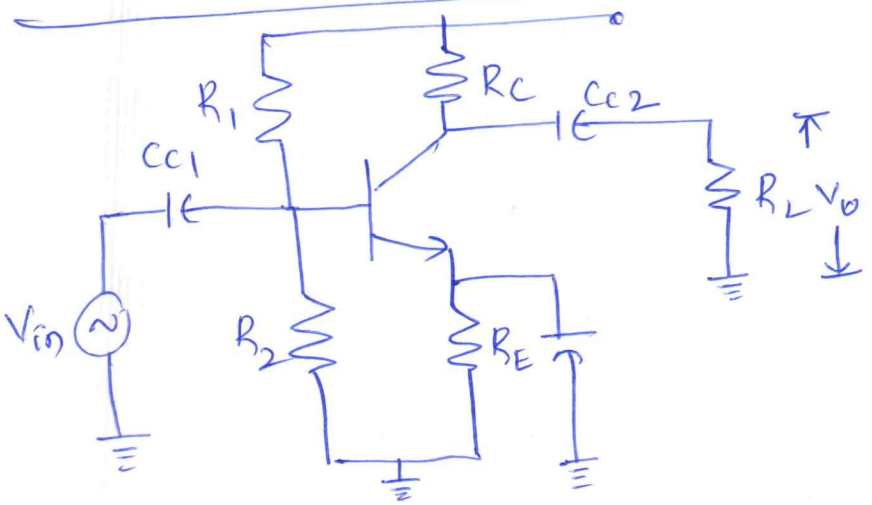
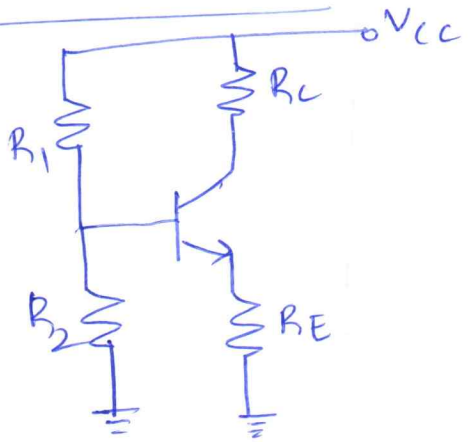
Module 1

1)a) Derive expressions V_{in}, V_{out} and A_v for common emitter circuit with AC equivalent circuit with π model. [12 Marks] L1, CO2

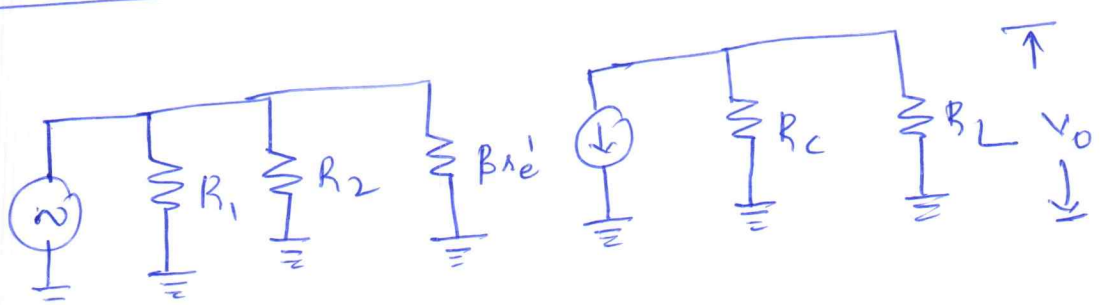
Soln: common Emitter Amplifier:



DC equivalent Circuit:



AC equivalent circuit (π - model)



To generate, Ac equivalent model, start with DC Equivalent model.

Procedure:

1) Short all coupling and Bypass capacitors
2) Visualize all DC supply voltages as Ac grounds
3) Replace the transistor by its π or T model.
4) Draw the Ac equivalent Circuit.

→ At i/p side, $V_{in} = i_b \cdot \beta r_e'$ — (1) By ohm's Law

At o/p side, $V_{out} = i_c (R_C \| R_L)$

as $i_c = \beta i_b$

$$V_{out} = \beta i_b (R_C \| R_L) \quad — (2)$$

Voltage gain, $A_V = \frac{V_{out}}{V_{in}}$

$$= \frac{\beta i_b (R_C \| R_L)}{i_b (\beta r_e')}$$

$$= \frac{\beta i_b (R_C \| R_L)}{\beta i_b (r_e')}$$

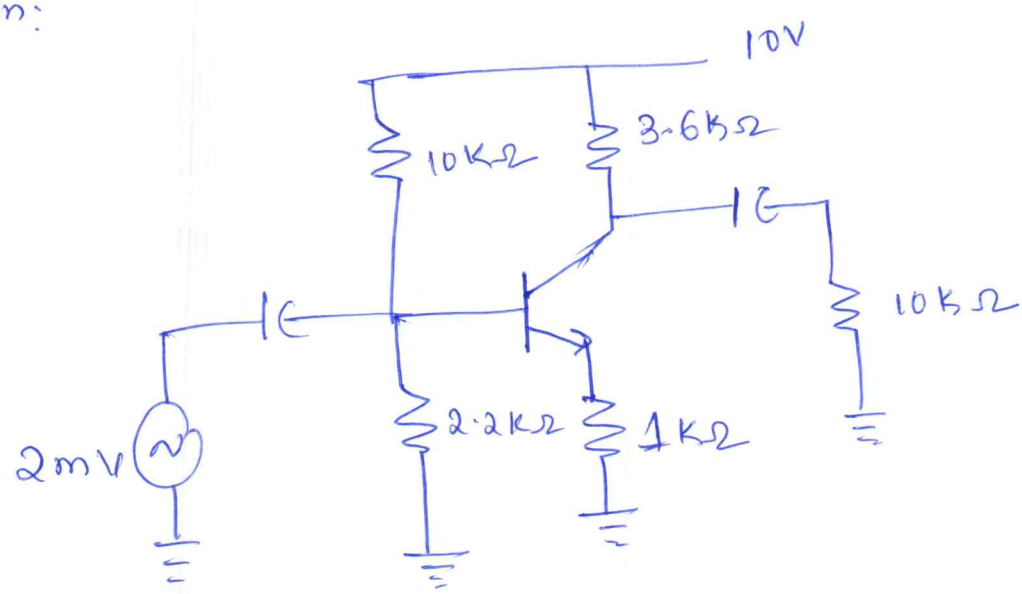
$$\boxed{A_V = \frac{R_C \| R_L}{r_e'}}$$

1)6) What is the voltage gain and output voltage across the load resistor of V_{DB} amplifier?

$R_1 = 10K\Omega$, $R_2 = 2.2K\Omega$, $R_C = 3.6K\Omega$, $R_E = 1K\Omega$, $R_L = 10K\Omega$, $V_{CC} = 10V$, $V_{BE} = 0.7V$ and $V_{in} = 2mV$.

[08 Marks] L1 CO2

Soln:



$$V_{th} = V_B = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$= 10 \cdot \frac{2.2K}{2.2K + 10K} = 10 \cdot \frac{2.2}{12.2} = 1.80V$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 2.2}{10 + 2.2} = \frac{10 \times 2.2}{12.2}$$

$$= 1.80K\Omega$$

$$V_E = V_B - V_{BE}$$

$$= 1.8 - 0.7$$

$$V_E = 1.1V$$

$$I_E = \frac{V_E}{R_E} = \frac{1.1}{1K} = 1.1mA$$

$$g_m = \frac{I_c}{V_{th}} = \frac{1.1\,mA}{25mV} = 0.044\ A/V$$

$$R_c' = \frac{3.6K + 10K}{3.6K + 10K}$$

$$= \frac{36000}{13.6} = 2.65\,K\Omega$$

Voltage gain, $A_V = \frac{-g_m R_i'}{1 + g_m - 1}$

$$A_V = \frac{-0.044(2650)}{1 + 0.044 \times 1000}$$

$$\boxed{A_V = -2.59}$$

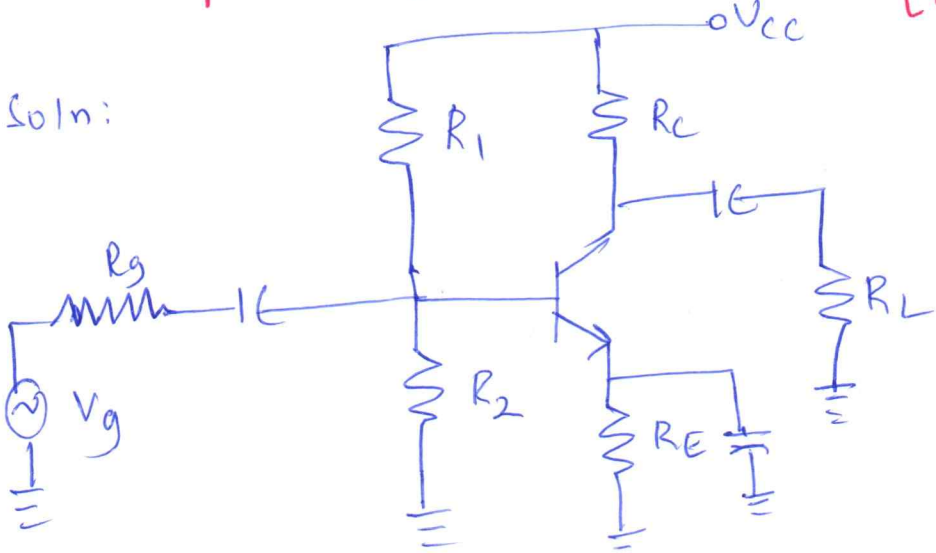
$$V_{out} = A_V \cdot V_{in}$$

$$= -2.59 \times 2\,mV = -5.2\,mV$$

$$\boxed{V_{out} = -5.2\,mV}$$

2)a) with a neat diagram, explain loading effect of input impedance. [10 marks] L1 CO1

Soln:

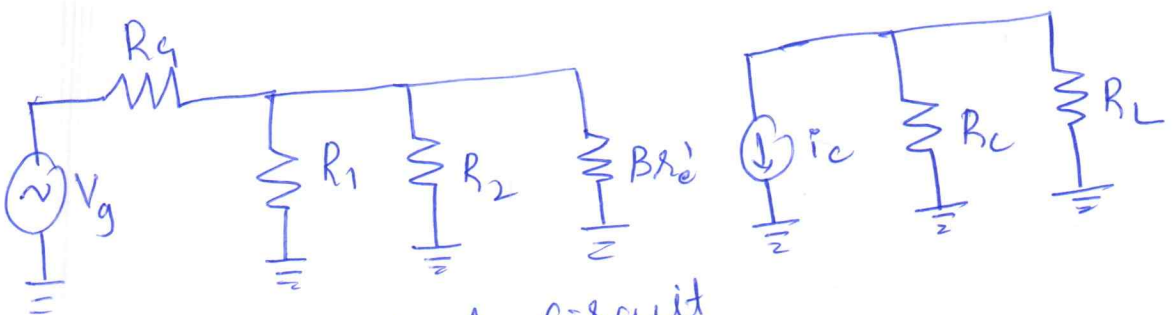


(x) In this circuit, we assume an ideal Ac voltage source with zero source resistance.

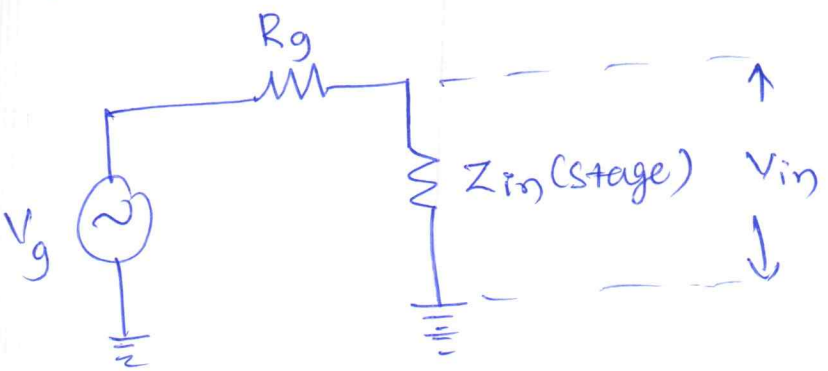
(x) But practically the Ac voltage source has some resistance

(x) This resistance reduces the Ac voltage appearing across the Emitter diode

(x) This is known as the loading effect of input imp-edance on Ac source.



Ac equivalent circuit



using voltage divider rule,

$$V_{in} = \frac{Z_{in(stage)}}{R_g + Z_{in(stage)}} \times V_g$$

2) b) Explain three types of Bias Circuit,

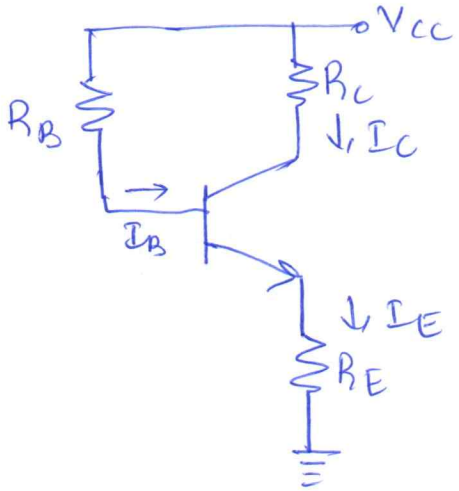
i) Emitter feed back bias

ii) collector feed back bias

iii) collector and emitter feed back

[10 Marks] L1 CO1

Soln: i) Emitter feed back Bias:



The Circuit above shows emitter feedback bias, which is used to stabilize the Q-point

→ The emitter resistance is added to the circuit to provide more stability

If I_e increases, V_E increases causing V_B to increase

$\because V_E = I_E R_E$

$\& V_B = V_E + 0.7V$

→ More V_B means less voltage across R_B and less I_B which opposes the increase of I_c.

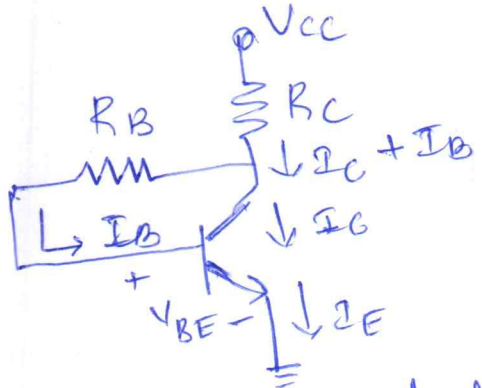
$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{dc}}$$

$$V_{CE} = V_{CC} - I_C R_C$$

if $R_E >> R_B/\beta_{dc}$

$$I_E = \frac{V_{CC} - V_{BE}}{R_E}$$

ii) collector feed back bias:



→ Figure shows collector feed back - it is another way of stabilizing the Q-point.

→ Feed back a voltage to base to neutralize any change in collector current.

→ If collector current increases, there is decrease in the collector voltage, which in turn decreases base current, which opposes the original change in collect -or current, I_C.

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta}$$

$$V_B = 0.7V$$

$$V_C = V_{CC} - I_C R_C$$

If $R_B = \beta R_C$, then Q-point will be near the middle of the load line.

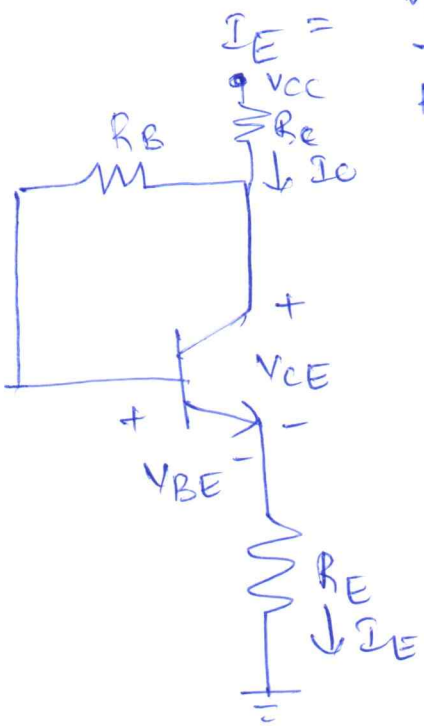
→ It is more efficient than emitter follower bias in Q-point stability.

iii) collector and emitter feedback bias:

→ collector bias and emitter bias does not have enough negative feed back.

→ Hence collector - Emitter biasing is used as shown in figure

It is combination of both collector feedback and Emitter feedback biasing.



$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_E + R_B/\beta}$$

$$V_E = I_E R_E$$

$$V_B = V_E + 0.7V$$

$$V_{CC} = V_{CC} - I_C R_C$$

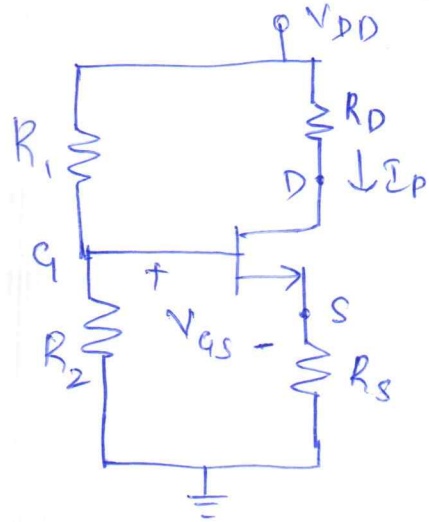
3)a) Explain the three biasing methods to bias MOS amplifiers with neat circuit diagram.

[10 Marks] L2 CO2

3)a) Explain the three biasing methods to bias Mos amplifies with neat circuit diagrams.

[10 Marks, L_2 CO_2]

Soln: Biasing by fixing V_{GS}:



(*) V_{GS} is fixed so that we can get required amount of drain current.

(*) V_{GS} is increased until required amount of I_D is obtain once I_D is sufficient then, V_{GS} is maintained constan

(*) This can be achieved by using suitable voltage divider circuit as shown in figure.

Drain current, $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

where

I_D = Drain current,

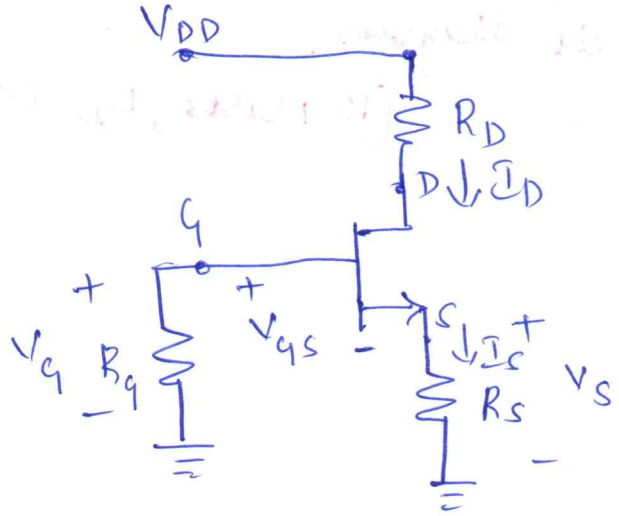
C_{ox} → oxide capacitance

V_{GS} → voltage between gate and source

V_t → threshold voltage

W/L → transistor aspect ratio

Biasing by Fixing V_G :-



Applying KVL to i/p side,

$$+V_G - V_{GS} - I_D R_S = 0$$

$$V_G = V_{GS} + I_D R_S \quad \text{—— (1)}$$

V_G → constant or fixed

→ If I_D increased, due to temperature change, then V_{GS} should decrease.

→ If V_{GS} decreases, then i/p decreases, hence the drain current will also decrease

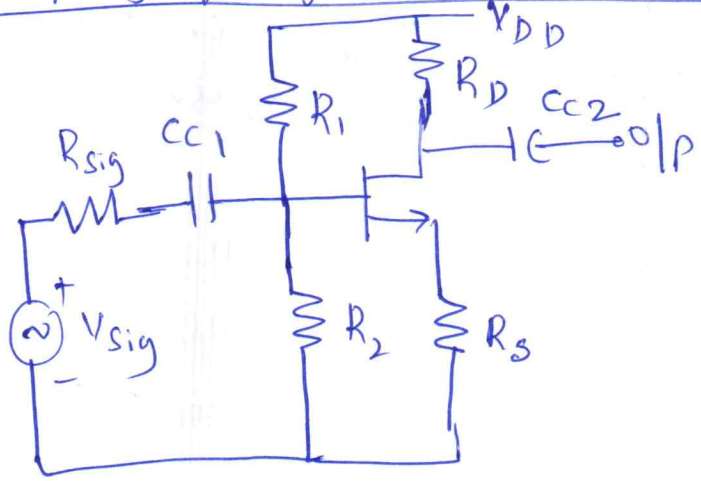
→ R_S is the resistance that employs negative feedback Thats why it is known as Degenerative resistance.

$$V_G = V_{GS} + I_D$$

i) if $V_G >> V_{GS}$ → Drop V_{GS} → negligible → constant I_D

then $\boxed{I_D = \frac{V_G}{R_S}}$

Coupling of Signal Source to the amplifier



The above figure shows how to connect Signal source to the gate through a coupling capacitor

→ Here CC_1 blocks DC and allows the signal V_{sig} to gate without affecting biasing point.

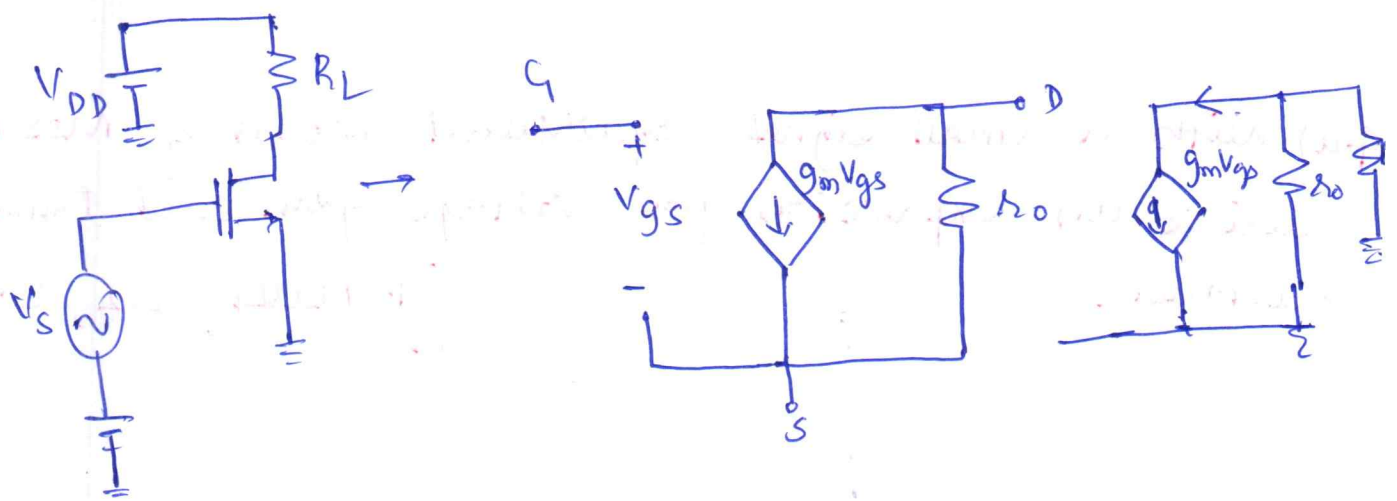
→ CC_2 blocks all DC and allow o/p signal to couple with other circuits.

→ CC_1 should be large enough to provide sufficient voltage gain.

3)b) Explain the T-equivalent Circuit model of MOSFET.

[10 Marks] L_3, CO_2

Soln:



The MOSFET T-equivant circuit is a small signal model that represents the MOSFET as a voltage controlled current source at the drain terminal, with an equivalent resis-tance $1/g_m$ at the source terminal.

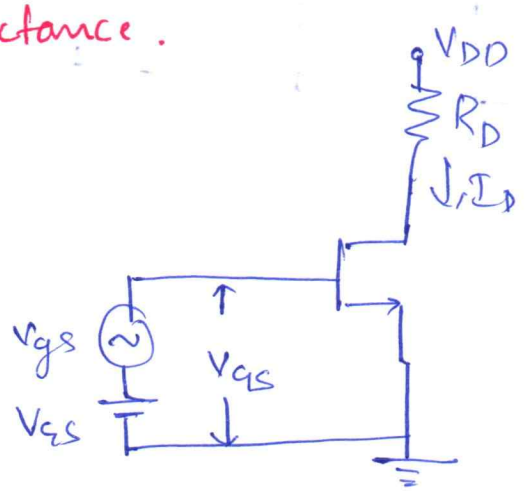
→ The core of the T-model is the $G_m V_{gs}$ current source. The gate to source voltage controls the current at the drain terminal, making it a voltage controlled current source.

→ The resistance $R_s = 1/g_m$ at the source terminal accounts for the internal resistance of the source.

→ The O/p resistance, R_o is added to the basic T-model to include the effect of channel length modul-ation, which causes the drain current to change with drain source voltage.

→ This model is used for analyzing the small signal behaviours of a MOSFET, where the small AC signals are superimposed on the DC bias conditions of the transistor.

4a) With a small signal Equivalent model of MOSFET, derive an expression for voltage gain and transcond-uctance. [10 Marks, L2, CO2]



Total voltage = AC + DC

$$V_{GS} = V_{gs} + V_{GS}$$

Total current = AC + DC

$$i_D = i_d + I_D$$

DC current, $I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$

Total current, $i_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) \left[(V_{GS} + V_{gs}) - V_t\right)^2]$

apply $(a+b-c)^2$ formula

$$= a^2 + b^2 + c^2 + 2ab - 2bc - 2ca$$

$$\therefore i_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) \left[V_{GS}^2 + V_{gs}^2 + V_t^2 + 2V_{gs} \cdot V_{gs} - 2V_{gs} V_t - 2V_t V_{GS} \right]$$

AC current,

$$\boxed{i_D = K_n' \frac{W}{L} \left(V_{gs} (V_{GS} - V_t)\right)}$$

Above eqn is the expression for signal current in drain terminal.

Trans conductance: g_m

$$g_m = \frac{i_d}{V_{gs}}$$

$$\boxed{g_m = K_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)}$$

Voltage gain, A_V:

$$A_V = \frac{\text{O/P Voltage}}{\text{I/P Voltage}}$$

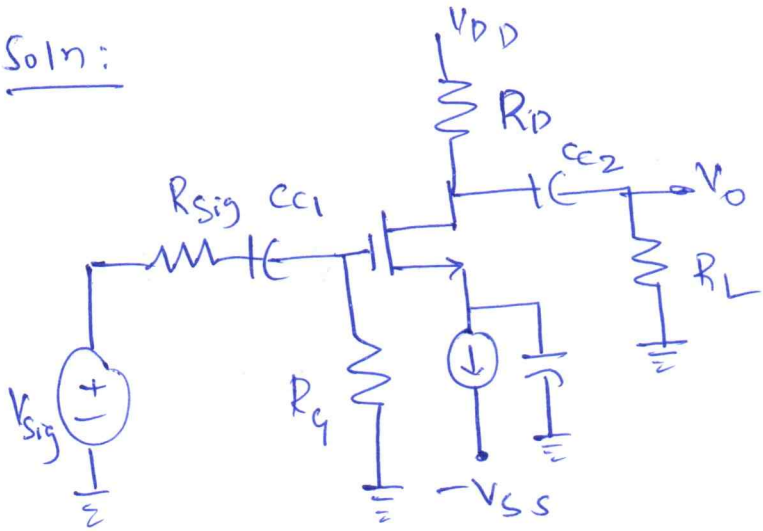
$$A_v = \frac{V_{ds}}{V_{gs}} = \frac{i_d R_D}{V_{gs}}$$

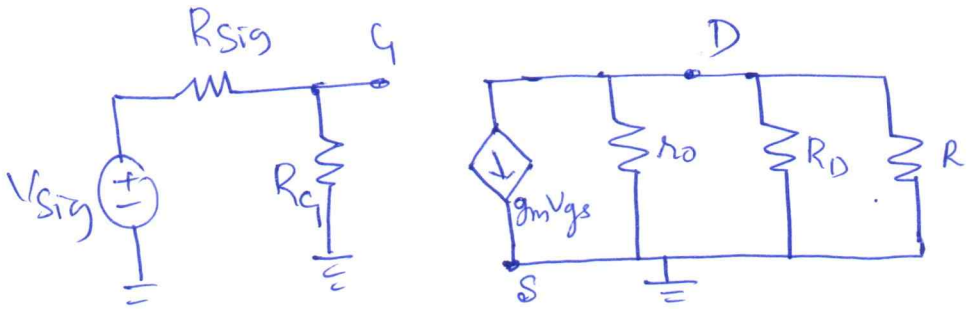
$$\boxed{A_v = g_m R_D}$$

4) b) Explain common source follower and derive the expression of voltage gain with necessary equation.

[10 Marks, L2, CO2]

Soln:





A Source follower is an field effect transistor (FET) configuration where the input is applied to the gate and output is taken from the source, making the drain common to Ac signals.

$$V_o = -g_m V_{gs} (R_D \| R_L)$$

Applying KVL from input around the gate source loop

$$V_i = V_{gs} + (g_m V_{gs}) R_s$$

The R-2R ladder D/A converter is shown in figure above

→ It is used to overcome the limitations of binary weighted D/A converter.

→ Since only two resistor values are required, this method lends 8-bit or higher binary inputs and produces high degree of accuracy.

→ The above figure shows 4-bit D/A Converter.

→ The switches $D_0 - D_3$, connect the 4 inputs to ground (logic 0) or $+V_{ref}$ (logic 1)

→ This network converts binary inputs 0000 to 1111 to one of 16 unique output voltage levels.

where D_0 → Least Significant Bit

D_3 → Most Significant Bit

To determine the o/p voltage, first change the binary input values to decimal equivalent, B_{in}.

$$B_{in} = (D_0 \times 2^0) + (D_1 \times 2^1) + (D_2 \times 2^2) + (D_3 \times 2^3)$$

Then o/p voltage can be found by,

$$V_{out} = -\left(\frac{B_{in}}{2_N} \times 2 V_{ref}\right)$$

where N → Number of inputs.

$$V_i = V_{gs}(1 + g_m R_s)$$

$$V_{gs} = \frac{V_i}{1 + g_m R_c}$$

Small signal voltage gain is,

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(R_D \| R_L)}{V_{gs}(1 + g_m R_s)}$$

$$A_v = \frac{-g_m (R_D \| R_L)}{1 + g_m R_s}$$

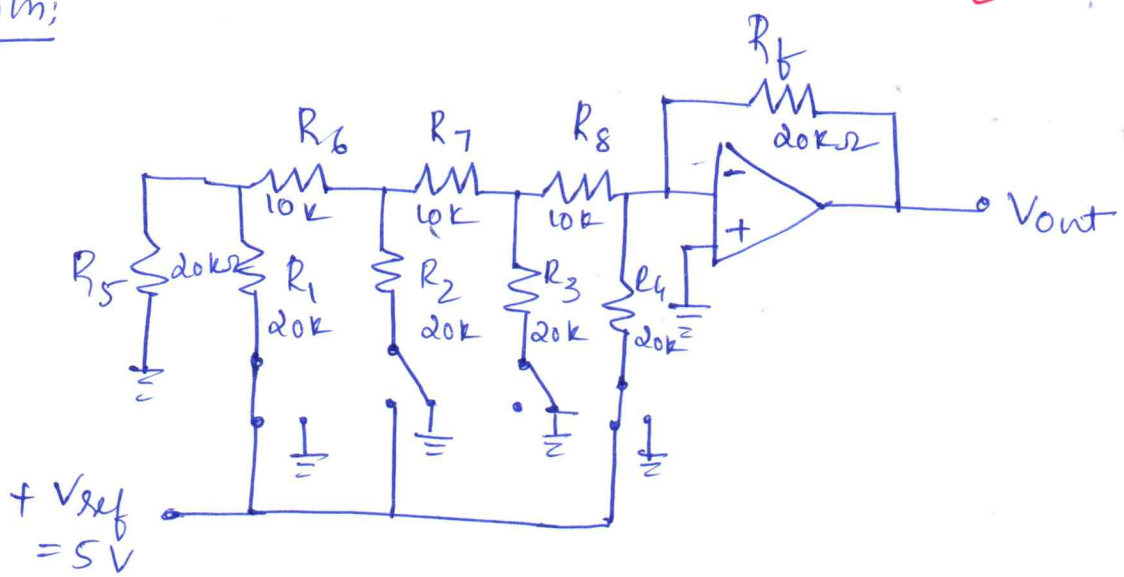
The overall Small Signal voltage gain,

$$G_v = A_v \times \frac{R_G}{R_G + R_{sig}}$$

5)a) Explain R-2R resistor Digital to Analog converter and also derive the expression of output voltage.

[10 Marks, L2 CO3]

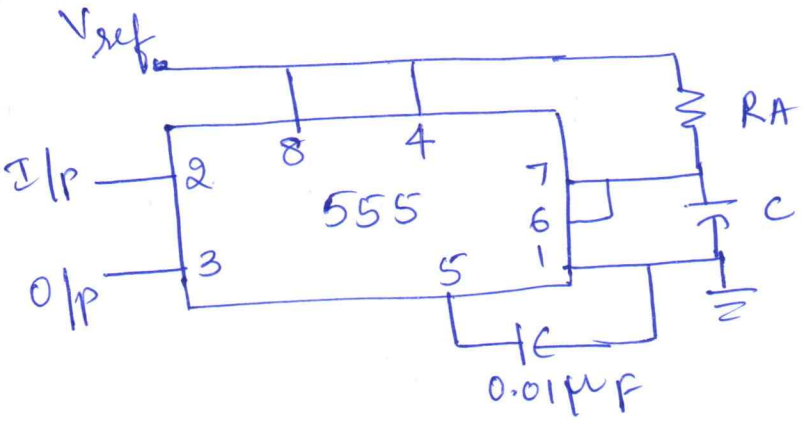
Soln:

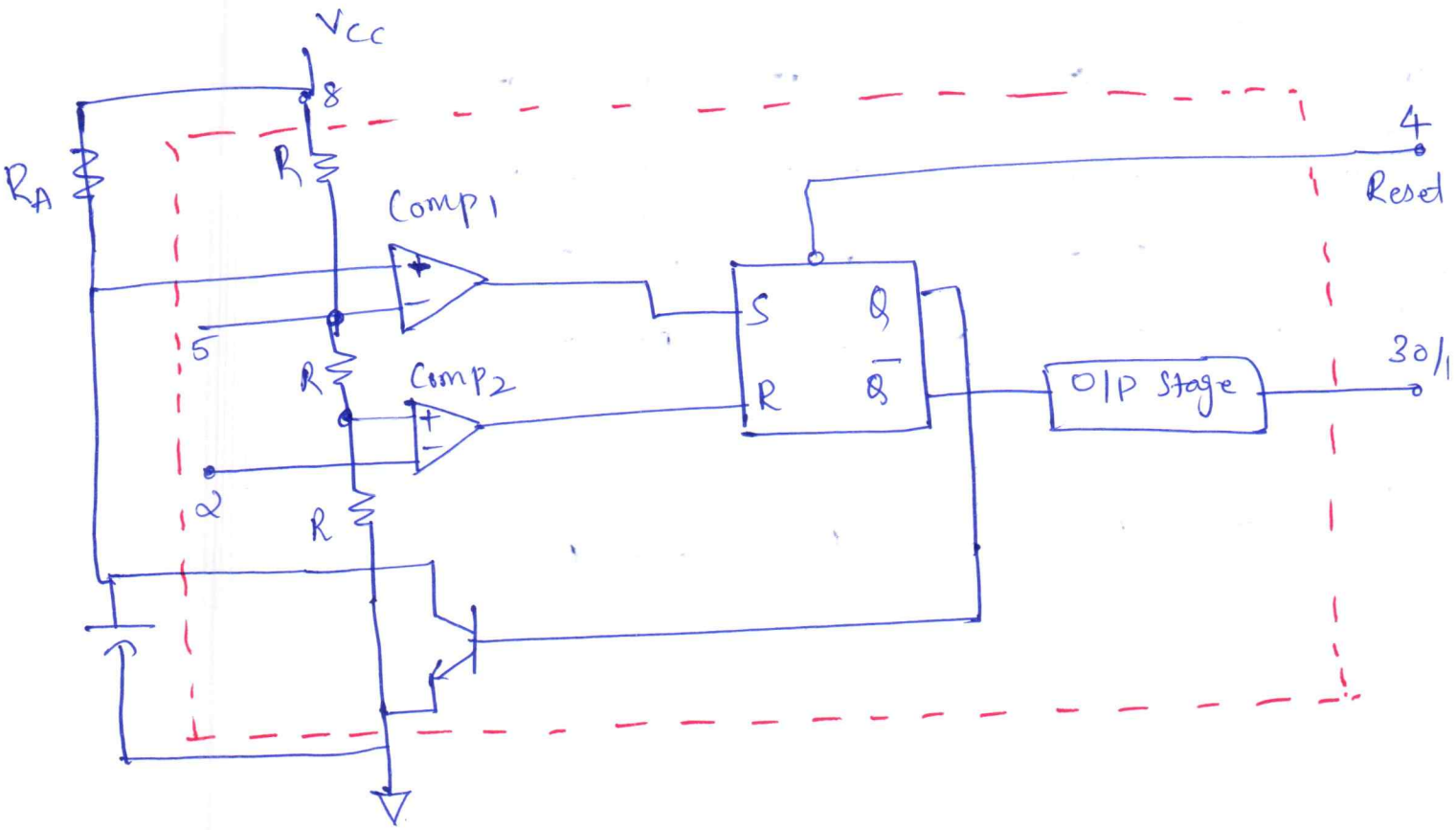


5)b) With a neat circuit diagram, explain the operation of Monostable multivibrator.

[10 Marks, L2, CO3]

Soln:





Initially, the o/p is low,

trigger pulses is applied across input of comparator 2

then $trig << 1/3\ V_{cc}$.

then the o/p of comp 2 is high. SR flipflop is reset

$Q = 0$ & $\bar{Q} = 1$

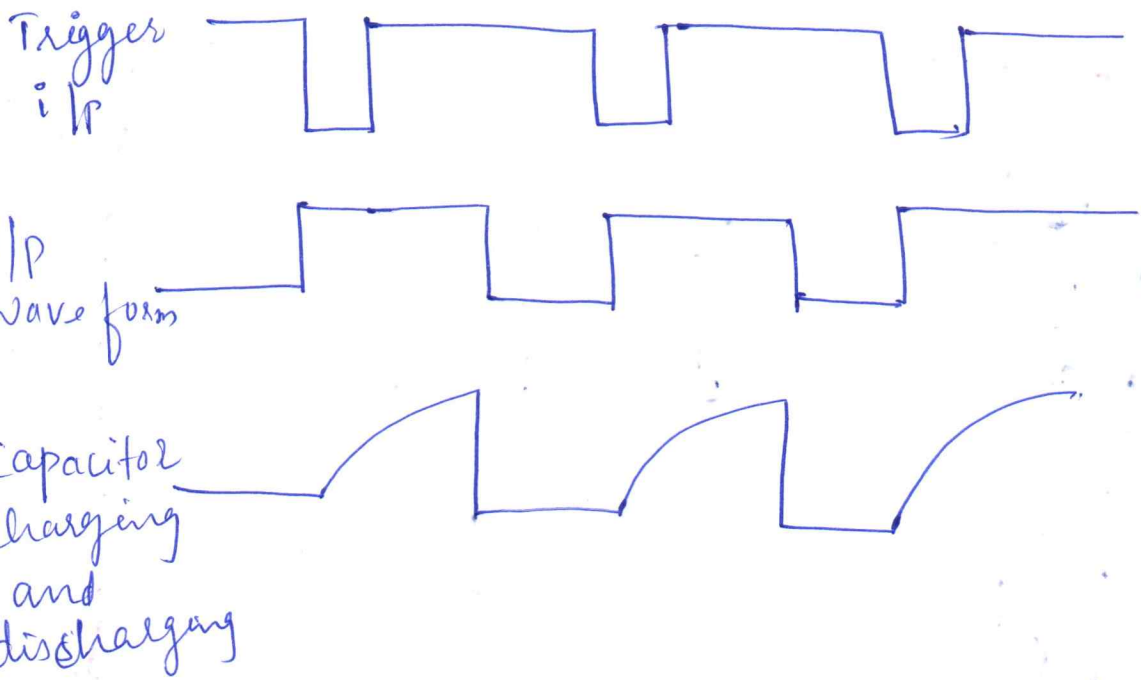
→ 1 is the i/p to the o/p stage and the o/p will be high for some time.

→ when $Q = 0$, it will set transistor Q_1 to off condⁿ and acts as open circuit.

→ then capacitor starts charging with V_{cc}.

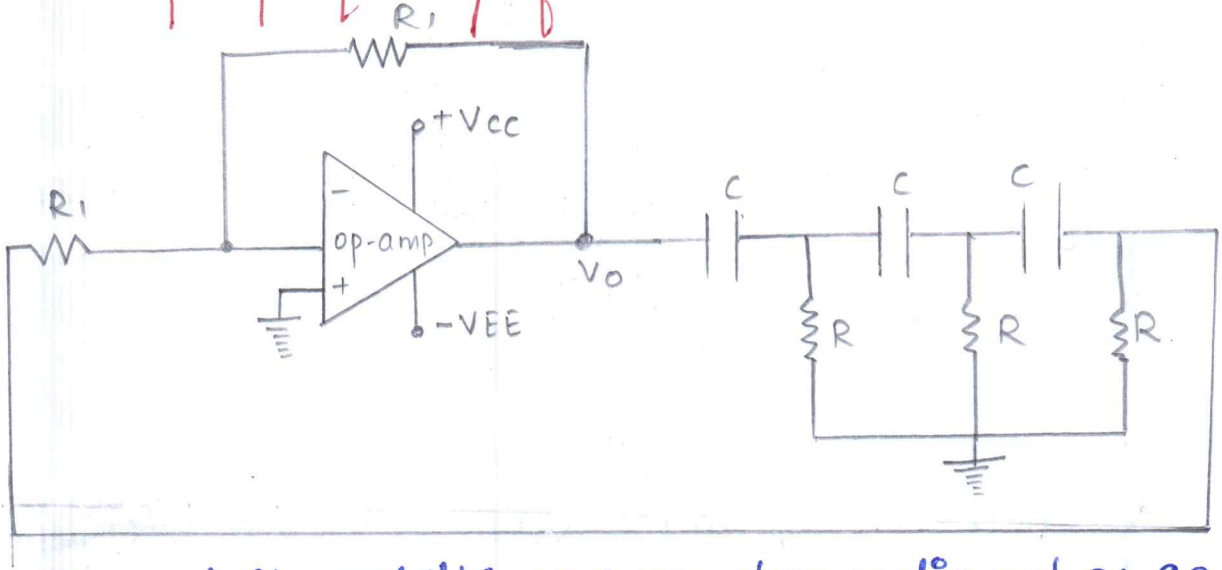
→ At pin no 6, i/p is equal to $2/3 V_{cc}$ then o/p of comp 1 is high, SR flip flop is set then $Q = 1$ and $\bar{Q} = 0$.

→ Since $\bar{Q} = 0$, the o/p will be low, the capacitor starts discharging since Q_1 acts as short circuit



6 a) With a neat diagram, explain operation of RC-phase shift oscillator using op-amp. Write the expression for frequency of oscillations. (8M, L2, CO3)

Sol:



1. Amplifier and phase shift: op-amp when configured as an inverting amplifier, provides a 180° phase shift b/w its input and output signals.

2. Feedback network: Cascaded RC network produce a specific phase shift at particular frequency. In typical three-stage network, each RC section shifts the phase by 60°.

3. Total phase shift: The total phase shift around the feedback loop must be 360°. The 180° shift from op-amp, combined with the 180° shift from the three-stage RC network, results in the necessary 360° phase shift.

4. Gain Requirement: The product of amplifier gain and feedback network's gain must be unity $a * \beta = 1$.

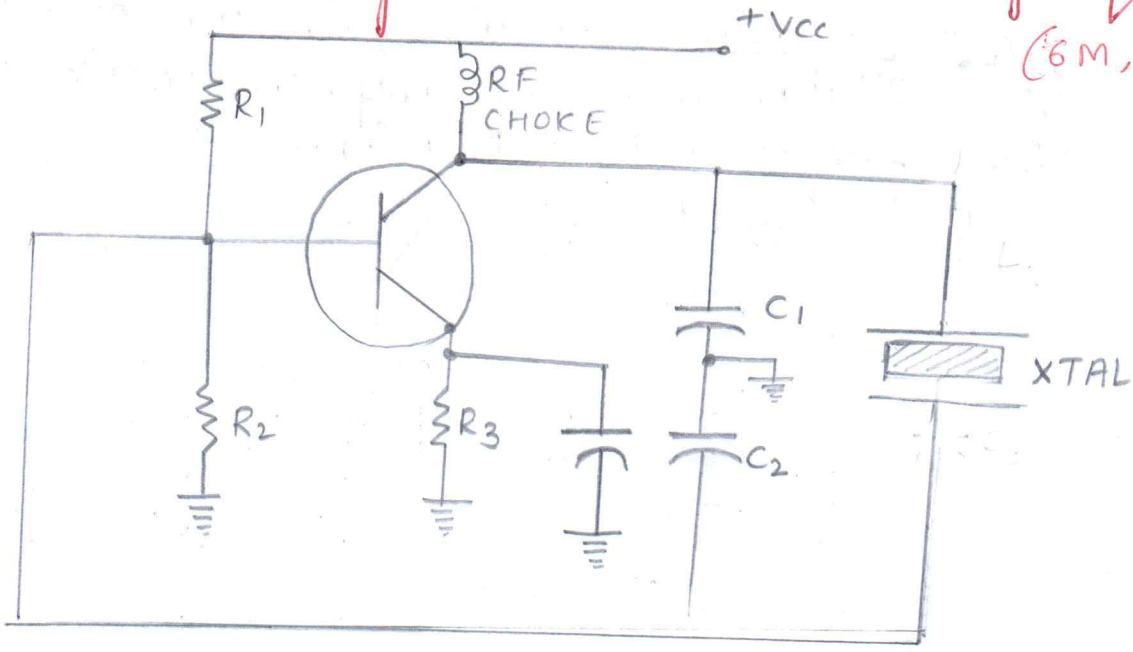
5. Oscillation: At the frequency where the total phase shift is 360°, the circuit oscillates, producing a continuous sinusoidal output.

Frequency of Oscillation = $f = \frac{1}{2\pi RC}$

6b) With a neat diagram, explain operation of crystal oscillator using BJT and write necessary equations

(6M, L2, C03)

Sol:



When accuracy and stability of the oscillation frequency are important, a quartz-crystal oscillator is used.

* The feedback signal comes from a capacitive tap.
* The Crystal (abbreviated XTAL) acts like a large inductor in series with a small capacitor (similar to the clapp).
* Because of this, the resonant frequency is almost totally unaffected by transistor and stray capacitance

$$f = \frac{1}{2\pi\sqrt{LC}}$$

6 c) A Crystal has these values $L = 3H$, $C_S = 0.05\,pF$, $R = 2k\Omega$ and $C_m = 10PF$, what are the series and parallel resonant frequencies of the Crystal? (6M, L3, CO3)

Soln:

$C = 0.05\,pF = 0.05 \times 10^{-12}\,F$

$R = 2k\Omega = 2000\Omega$

$C_m = 10\,pF = 10 \times 10^{-12}\,F$

The series resonant frequency is given by:

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$f_s = \frac{1}{\left(2\pi\sqrt{3 \times 0.05 \times 10^{-12}}\right)}$$

$$f_s = \frac{1}{2.433 \times 10^{-6}}$$

$$f_s = 411\,kHz$$

The parallel resonant frequency is given by formula:

$$f_p = f_s \times \sqrt{\left(1 + \frac{C}{C_0}\right)}$$

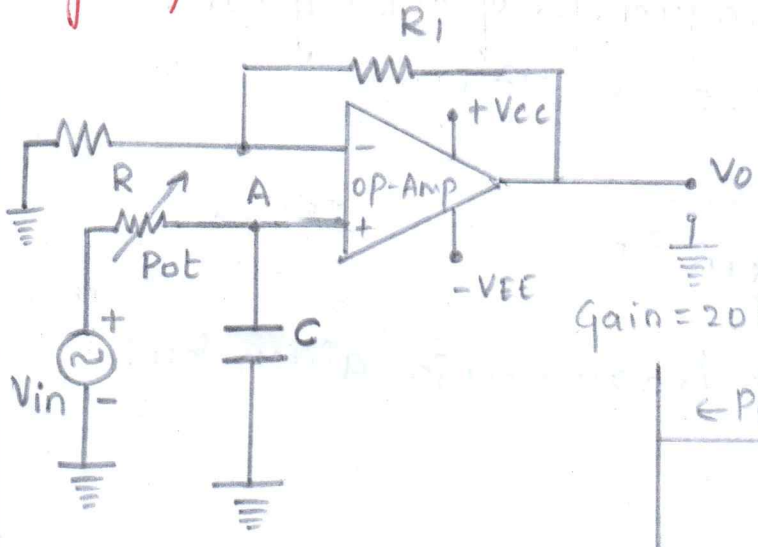
$$f_p = 411\,kHz \times \sqrt{1 + \frac{0.05}{10}}$$

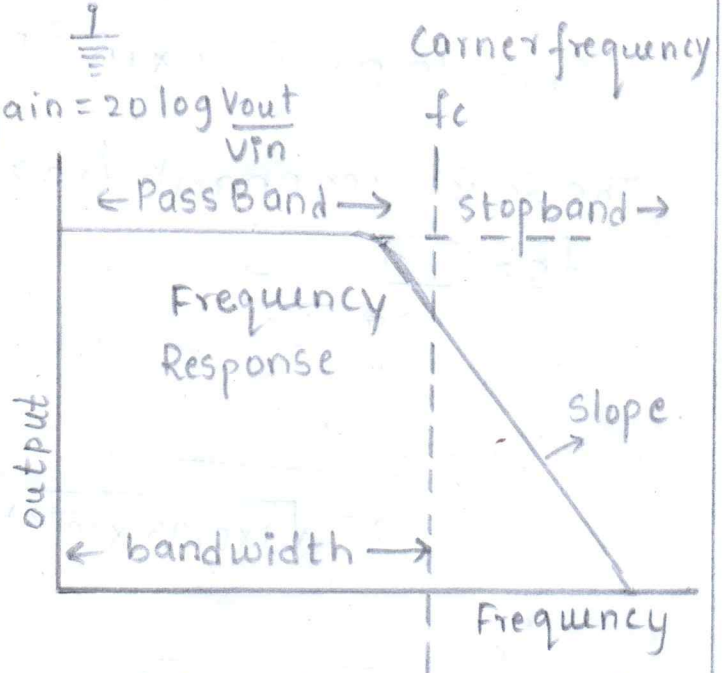
$$f_p = 411\,kHz \times 1.0025$$

$$f_p = 412\,kHz.$$

7a) Explain the first order low Pass filter with frequency response (10 M, L2, CO4)

Sol:





The simplest first order low-pass filter consist of R in series with the input and C in parallel with the output. At very low frequencies the $X_C = \frac{1}{\omega C}$ is very high, so it essentially acts as a open circuit. The input voltage passes through the resistor to the output with little attenuation.

As the input frequency increases, the capacitor's impedance decreases. It begins to act more like a short circuit diverting the signal to ground instead of output.

This is the point where the filter's output signal has dropped to 70.7% of the input signal.

7b) Explain the two types of Band Pass Filters (10 M, L2, CO1

→ **Wideband filters**: bandpass filter with a lower cutoff frequency of 300 Hz and an upper cutoff frequency of 3.3 Hz

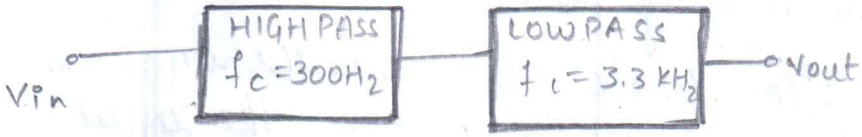
The center frequency of filter $f_0 = \sqrt{f_1 f_2} = 995 Hz$

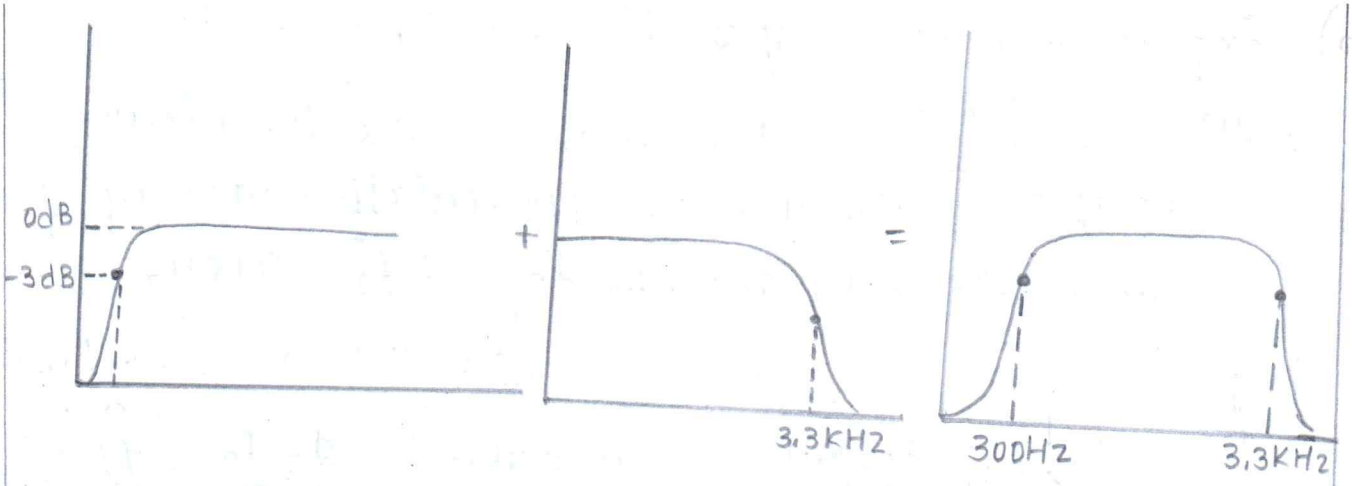
$= \sqrt{(300 \times 3.3)}\ Hz$

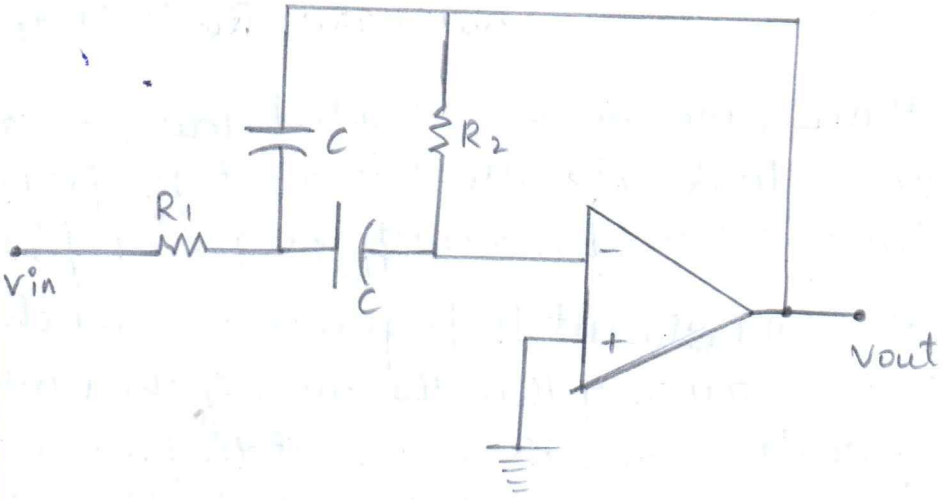
$BW = f_2 - f_1 = 3.3 KHz - 300 Hz = 3 KHz$ $\quad Q = \frac{f_0}{BW} = \frac{995 Hz}{3 KHz} = 0.332$

Since Q is less than 1, we can use cascaded low-pass and high pass stages. The high pass filter has a cutoff frequency of 300 Hz and low pass filter has a cutoff frequency of 3.3 KHz. Since Q is greater than 1, the cutoff frequencies are much closer than that. Because of this, the sum of the passband attenuations is greater than 3dB at the cutoff frequencies.

NarrowBand filters: When Q is greater than 1 we can use MFB, the input signal goes to inverting input rather than the noninverting input. The Circuit has two feed back paths one through a capacitor and another through a resistor. At low frequencies the Capacitors appear to be open. The input signal cannot reach the op-amp, the output is Zero.
At high frequencies the capacitors appear to be shorted. Voltage gain is Zero because the feedback capacitor has Zero impedence. $A_V = \frac{-R_2}{2R_1}$ $\quad Q = 0.5\sqrt{\frac{R_2}{R_1}}$ $\quad f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}}$







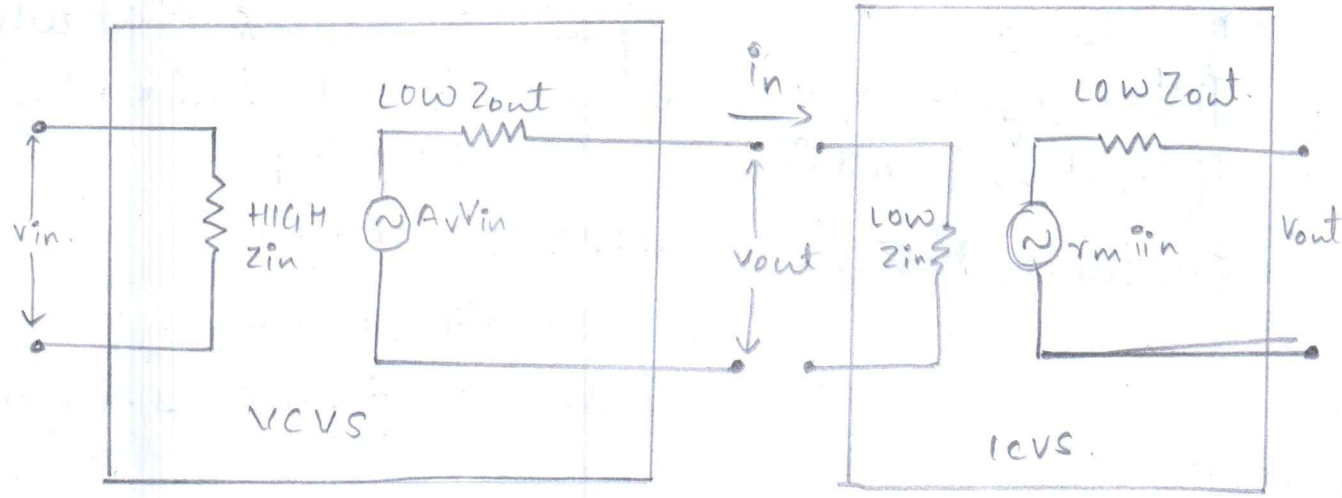
8a) Explain the four types of Negative feedback circuits (10 M, L2, CO4)

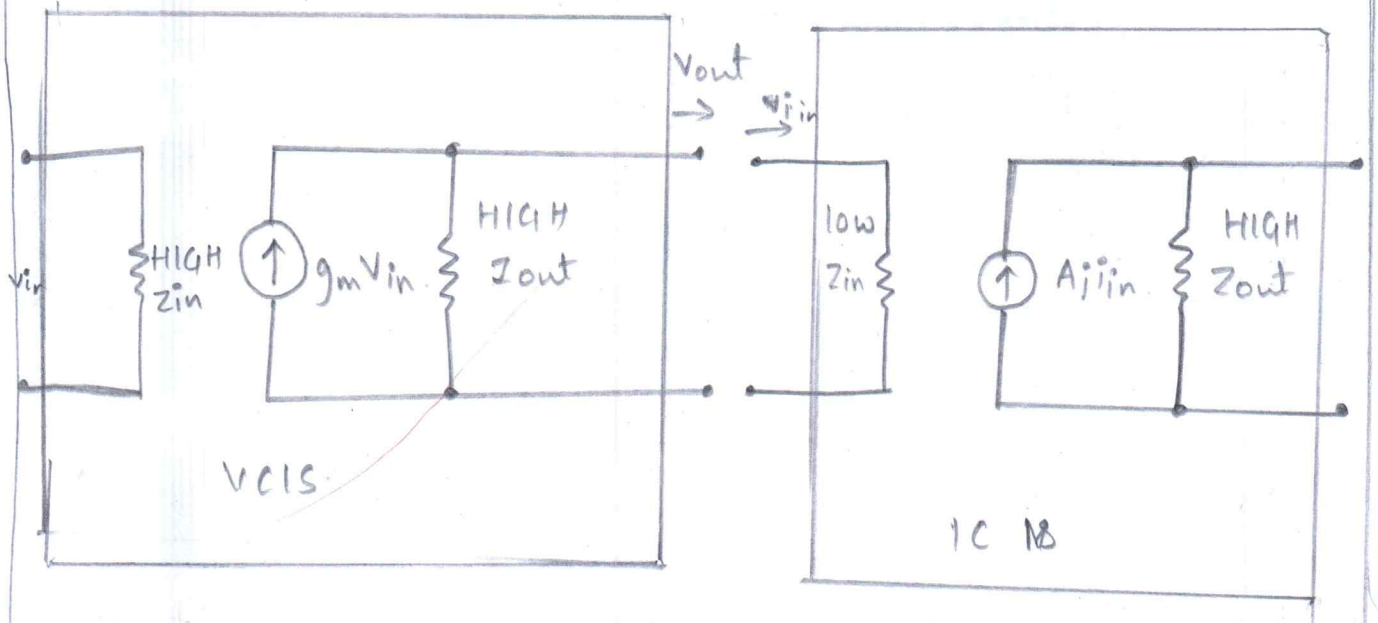
→ 1. Voltage-Series: feedback network samples the output voltage. connected in series with input Voltage. This configuration increases the input impedance and decreases the output impedance and decrease the output impedance. acting as VCVS.

2. Voltage-Shunt: The feedback connected in parallel with the input. The Configuration increases the output impedance, acting as VCCS.

3. Current-Series: The feedback is connected in series with the input. This configuration decreases the input impedence and also decreases the output impedence, acting as a current-controlled voltage source. The Feedback network samples the output current.

4. Current - Series : The Feedback is connected in Parallel with the input. This Configuration decreases the input impedence and increases the output impedence, acting as a Current - Controlled Current Source.





8b) Explain the Working of 2nd order high pass filter with a neat circuit and frequency response. (10 M, L2, CO4)

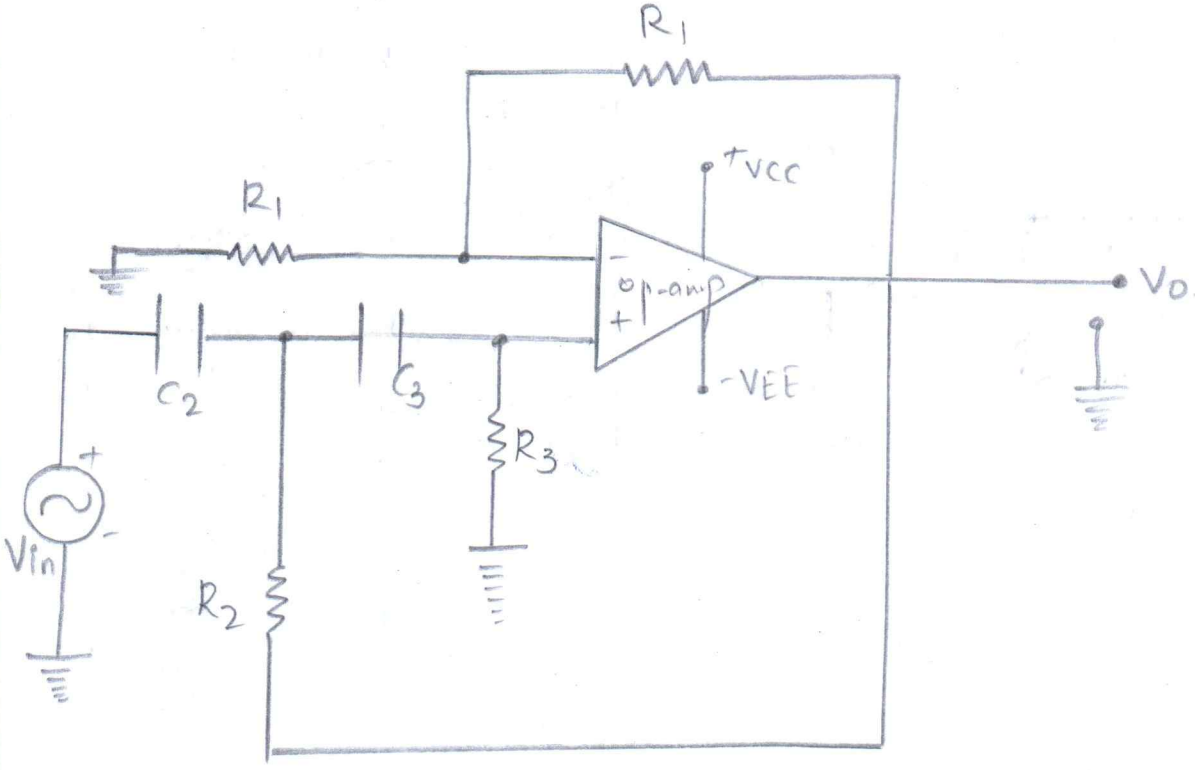
→ At low frequencies X_C is high acting as an open circuit. This blocks most of low-frequency input signal from reaching the op-amp. As the frequency increases the X_C decrease. allows the high-frequency signal to pass through to the op-amp's non-inverting

Input

* The non-inverting op-amp amplifies the passed signal. The passband gain is determined by feedback and is greater than 1

* The lower cutoff frequency is the point at which the filter begins to pass the signal and determined by values of R_1, R_2, C_1 and C_2.

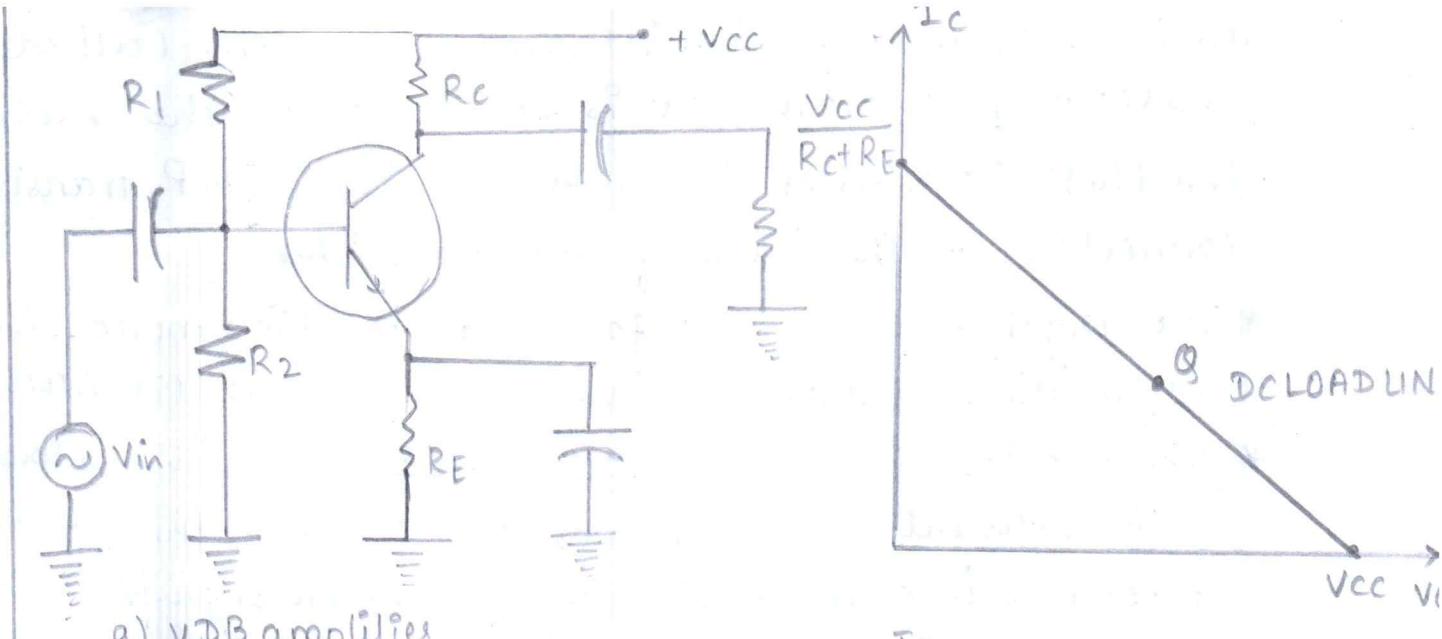
Frequency Respones : stop band ($F < FL$)
Pass band ($F > FL$)
Bode Plot (dB versus frequency)

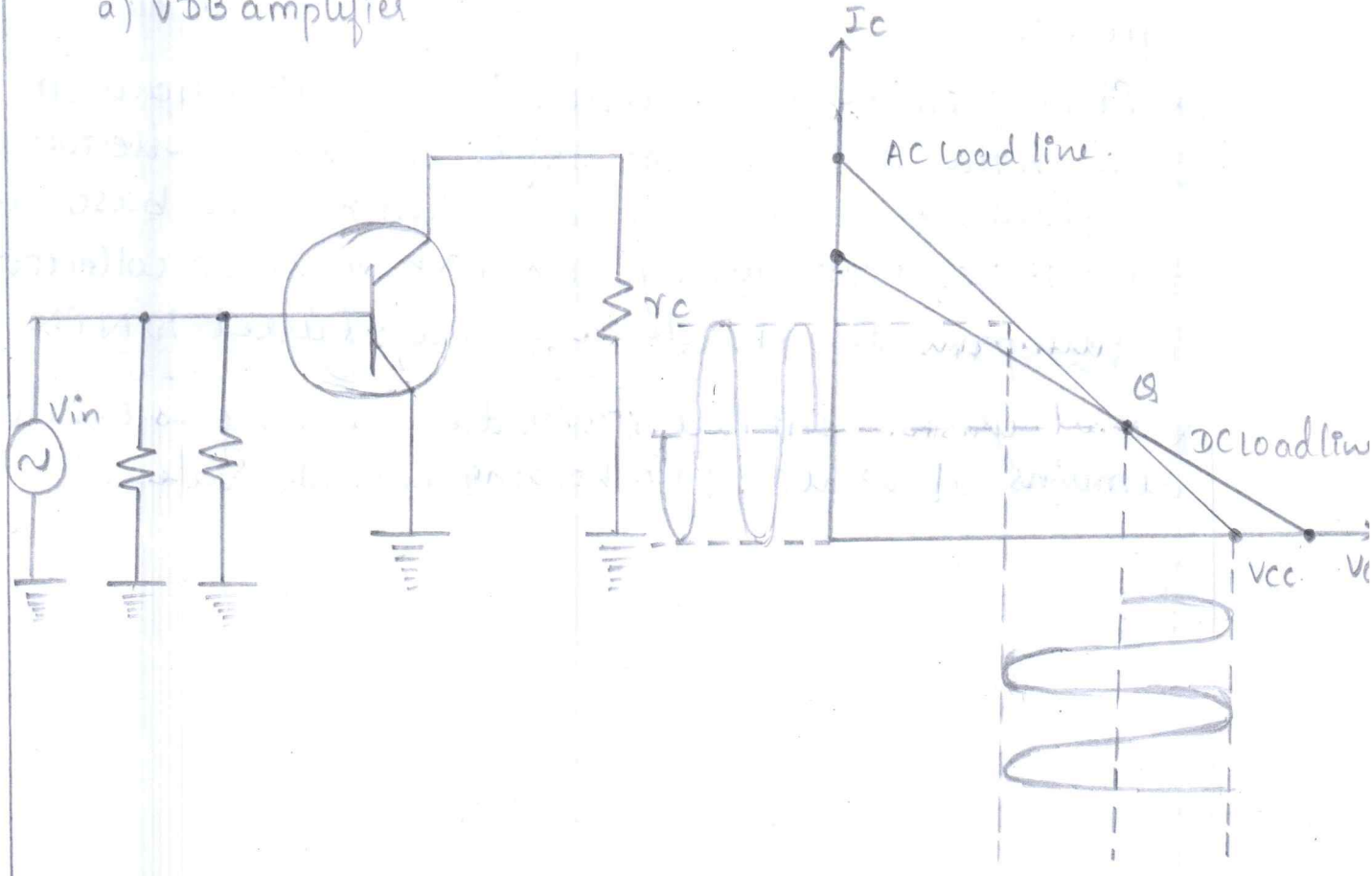


9a) Explain two load lines with necessary circuit diagram and equation. (10 M, L2, CO5)

→ DC load line : Move the Q point is by varying the value of R_2. For very large of R_2, the transistor goes into saturation and its current $I_{c(sat)} = \frac{V_{cc}}{R_c + R_E}$.

Very small values of R_2 will drive the transistor into cut off and its voltage is : $V_{CE(cutoff)} = V_{cc}$





9b) ~~With a diagram, explain the working~~

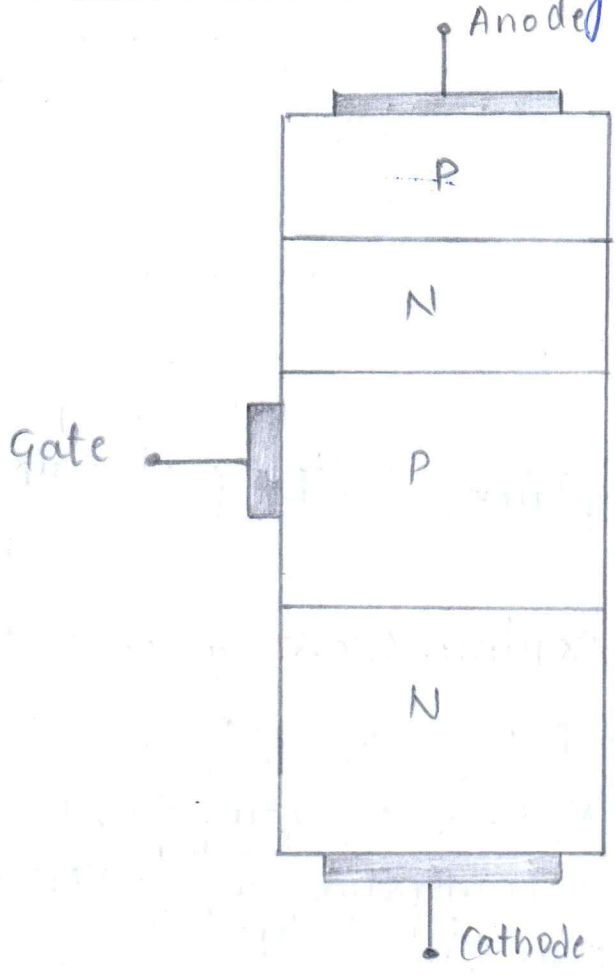
(10 M, L2, C05)

9b) With a diagram, explain working of a thyristor.

→ A thyristor is a P-N-P-N structure with three terminals. The P-N-P-N structure can be viewed as two interconnected transistors as a PNP transistor with its emitter as the Anode.

an NPN transistor with its Emitter as the Cathode. The Collector of NPN transistor is connected to the base of the PNP transistor. The collector of the PNP transistor is connected to the base of NPN transistor.

* The Thyristor is in the forward-blocking mode. The inner P-N junction is Forward-biased, but the two transistors are off.
* The collector currents of both transistors are very low, acting as base Current, keeping both transistors in the off-state. it behaves like an open switch, and no significant current flows.
* Signal provides base Current to the NPN transistor, this turns on the NPN transistor, which causes its collector current to flow. This collector current then becomes base Current for PNP transistor, turning it on. PNP transistor collector Current in turn provides a much larger base Current to NPN.
* The thysistor continues to conduct as long as the Current remains above a certain holding current value.

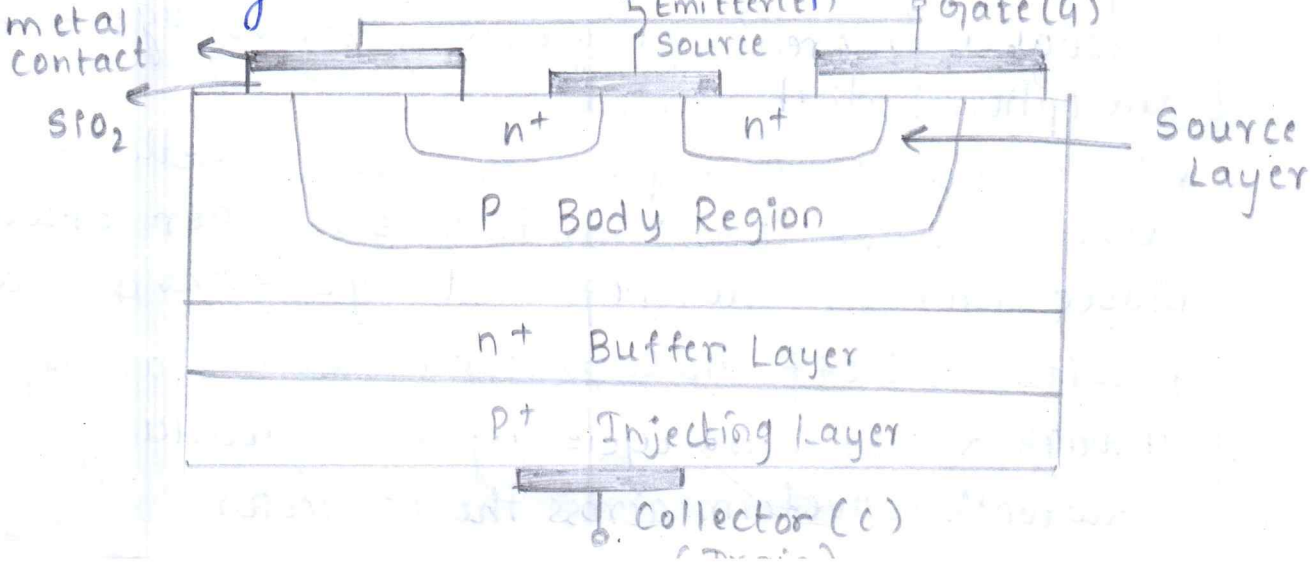


10a) Explain Basic Construction and Working of IBGTs with fi
(10 M, L2, CO5

→ **Construction:** The base layer is a P+ doped Substrate, serv as collector. A high resistivity N- drift layer is grown on P+ Substrate. A P-layer is diffused into the N- drift region. This is the body region where the gate is formed. N+ region is diffused into the P- body. Serves as emitter terminal. A metal gate terminal is placed on the top of the P- body region. A metal laye is deposited on P+ substrate to form the collector terminal.

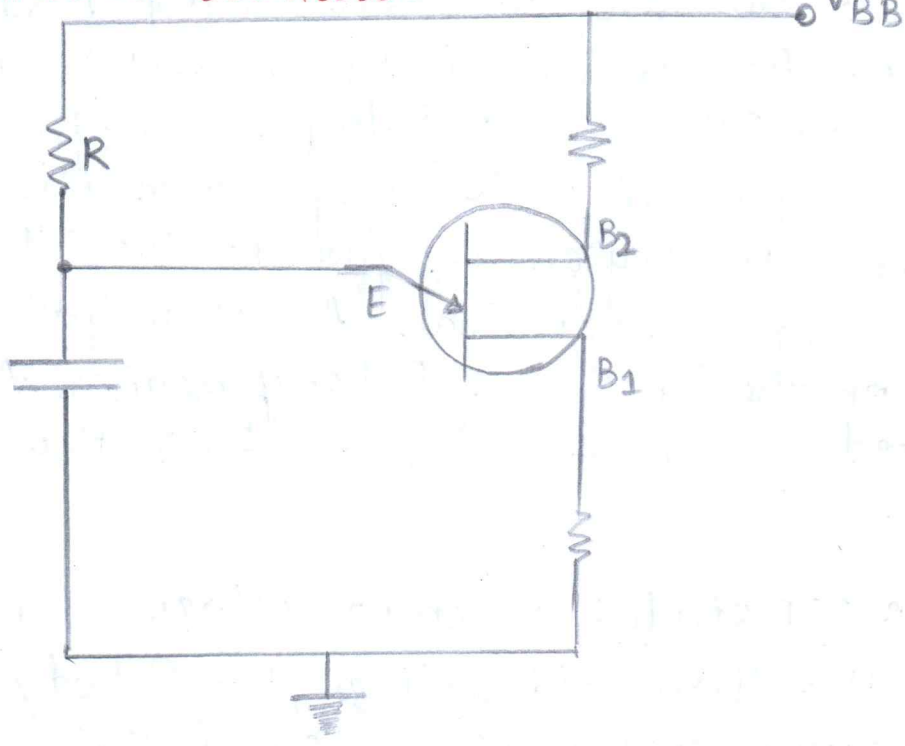
Working: **OFF state:** when no voltage is applied to gate is be low the threshold voltage, the P-body region and N- drift region remain reverse biased. This prevents curr flow from collector to Emitter and IGBT remains in OFF state

ON State: applying + voltage to gate greater than thresh -ld voltage creates an n-channel in P-body region, short- circuiting it to N+ emitter region. This creates a conductive path for electron to flow from N+ to N- drift region. P+ collector injects holes into the N- drift region. Combination of injected holes and electrons from n-channel increases the Conductivity of drift region. This process combined PNP & NP allow a large collector current to flow, and the IGBT turn ON



10 b) With a neat diagram, explain the working of UJT relaxation oscillator. (10 M, L2, CO5)

→



Working: * charging cycle when the Supply voltage is applied the Capacitor begins to charge through the resistor. initially the voltage across the Capacitor is too low to trigger the UJT So it remains in the off state.

* capacitor charges, its voltage increases, when Vc reaches UJT's peak point V_p, Inteinal PN junction become Forward biased. This triggers the UJT causing it to switch from high-impedance state to low impedance.
* UJT's sudden drop in resistance allows the Capacitor to discharge rapidly through the E to B junction. current surges through UJT creating negative-going voltage spike across the optional discharge resistor R_3.
* The Capacitor discharges until its voltage falls below the UJT's (V_v), At E-B_1 junction is no loger forward-biased, and UJT turns off, cutting off the discharge curre
* with UJT off, the Capacitor begins to chargeagain through R and entire cycle repeats, producing a continocus Sawtooth waveform across the Capacitor.