KLS Vishwanathrao Deshpande Institute of Technology

(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Title	:	Analog and Digital Systems Design Laboratory
Course Code	:	BECL305
Year / Semester	:	2nd Year / 3rd Semester
Academic Year	:	2025 – 26

Syllabus :

CLOs	:	• Understand the electronic circuit schematic and its working • Realize and test amplifier and oscillator circuits for the given specifications • Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers. • Study the static characteristics of SCR and test the RC triggering circuit. • Design and test the combinational and sequential logic circuits for their functionalities. • Use the suitable ICs based on the specifications and functions					
COs	:	**CO1:**	Design and analyze the BJT/FET amplifier and oscillator circuits.				
		CO2:	Design and test Op-amp circuits to realize the mathematical computations, DAC and precision rectifiers.				
		CO3:	Design and test the combinational logic circuits for the given specifications.				
		CO4:	Test the sequential logic circuits for the given functionality.				
		CO5:	Demonstrate the basic electronic circuit experiments using SCR and 555 timer.				
CO / PO Mapping	:	**Cos**	**CO1**	**CO2**	**CO2**	**CO4**	**CO5**
		POs / PSOs	1,2,3 / 1,2	1,2,3 / 1,2	1,2,3 / 1,2	1,2 / 1,2	1,2 / 1,2
Course In-Charge	:	**Prof. Deepak Sharma**					

CO-PO Mapping Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
1	2	2	1									1	1
2	2	2	1									1	1
3	2	2	1									1	1
4	2	2										1	1
5	2	2										1	1

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Experiment No: 1

Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances

AIM: Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.

OBJECTIVES:

1. To understand the frequency response characteristics of a BJT common emitter voltage amplifier.
2. To understand the effect of negative feedback on gain-bandwidth product, input and output impedances.

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	1
2	CRO: 20MHz	1
3	Signal generator: 1-1MHz	1
4	Resistors: 1KΩ, 8.2KΩ, 33KΩ,10KΩ, 470Ω	1 each
5	Capacitors: 0.1 μF, 1 μF, 100μF	1 each
6	Transistors: SL100	1
7	Bread board	1
8	CRO Probes and connecting wires	Few

CIRCUIT DIAGRAM:

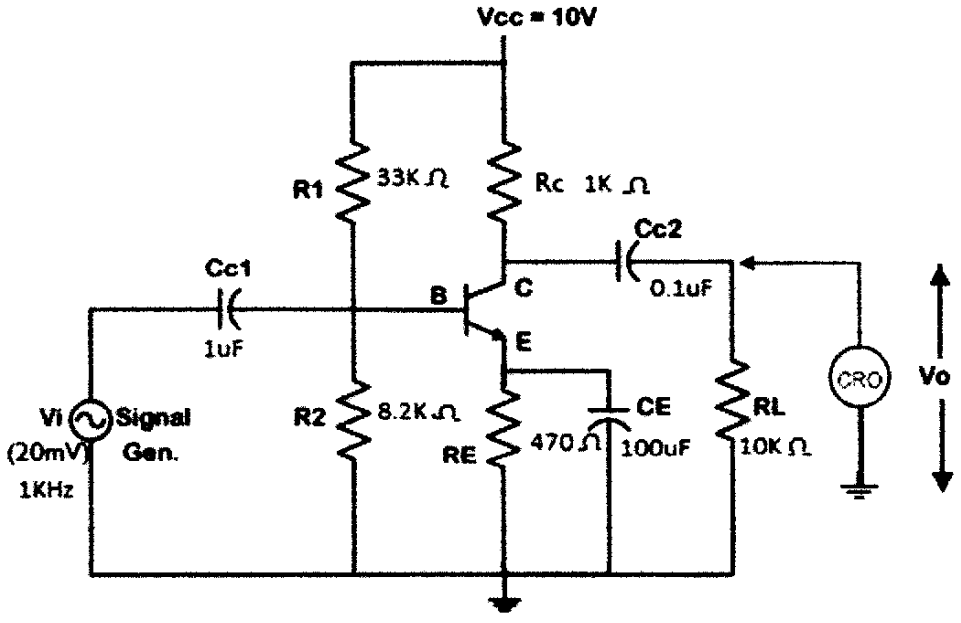


Figure 1a: BJT amplifier without feedback

DESIGN:

Let Vcc = 12V; IC = 4mA; V_E = 2V; V_{CEQ} = 6V; hfe (βDC) = 100.

1. **To find R_E:**

   Given V_E = 2V.

   Therefore, $R_E = V_E / I_E = V_E / I_C = 500\Omega$

   Let **R_E = 470Ω (standard)**

2. **To find R_C:**

   From the collector loop writing KVL we get

   $V_{CC} = I_C R_C + V_{CE} + V_E$

   $R_C = (V_{CC} - V_{CE} - V_E) / I_C$

   R_C = 1kΩ **Therefore, R_C = 1kΩ (standard)**

3. **To find R1 and R2:**

   The base current $I_B = I_C$ / hfe = 4mA / 100 = 0.04mA

   Let I_1 be current through R_1 and I_1 be 10 times of I_B.

   Writing the base loop KVL we get,

   $V_B = V_E + V_{BE}$ = 2 + 0.7= 2.7V **Therefore, V_B = 2.7V**

   Now, $R_1 = (V_{CC} - V_B) / I_1$

   R1 = (12 - 2.7)/0.4m = 23.25 kΩ **Therefore, R1 = 33 kΩ (standard)**

   Also, $R_2 = V_B / (I_1 - I_B)$

   R2 = 2.7/0.36m =7.5 kΩ **Therefore, R2 = 8.2 kΩ (standard)**

4. **Input impedance (Zin):**

   To calculate the input impedance first calculate the value of Zin (base).

   Zin (base) = βr_e where r_e is the resistance of emitter diode.

   re = 25mV / IC = 25mV / 4mA = 6.25 Ω

   Zin(base) = βr_e = 100 * 6.25 = 625 Ω

   The input impedance of an amplifier is the input impedance seen by the A.C. source driving the amplifier. Therefore, the biasing resistor R1 and R2 are included as follows-

   Zin = (1+βre) || R1 || R2 **Zin = 558 kΩ**

5. **Output impedance (Zo):**

   The output impedance is given by,

   Zo = RC || RL

   Let RL = 10 kΩ **Therefore, Zo = 909 Ω**

6. **To find C_{C1}, C_{C2} and C_E:**

   Let F_L = 100Hz (Lower cut-off frequency)

   Input coupling capacitor:

   $C_{C1} = 1 / (2*\pi*Zin*F_L)$

   $C_{C1} = 1/ (2*\pi*558*100)$ =2.85 μF **Therefore, C_{C1}= 4.7 μF (standard)**

Output coupling capacitor:

$C_{C2} = 1 / (2*\pi*(R_C + R_L) *F_{in})$

$C_{C2} = 1/ (2*\pi*(1k + 10k) *100) = 0.144\mu F$ **Therefore, C_{C2}= 0.1μF (standard)**

7. **Design of bypass capacitors, C_E:**

Emitter bypass capacitor, $C_E = 1 / (2*\pi* r_e * F_L)$

$C_E = 1/ (2*\pi* 6.25 * 100) = 254.6\mu F$ **Therefore, CE =100μF (standard)**

PROCEDURE:

1. Rig up the circuit as per the given circuit diagram.
2. Switch on the D.C. power supply = 12V is given to the circuit.
3. Check the D.C. conditions without any input signal and record in table 1.
4. Select sine wave input and set the input signal amplitude to 20mV frequency at 1kHz constant and observe the input / output waves on the CRO and adjust the input amplitude such that the output is undistorted waveform. Calculate mid-band gain using AV = Vo(p-p) / Vin(p-p).
5. Keeping the input amplitude constant, vary the frequency from 100Hz to 2MHz and note down the corresponding output voltage (p-p) in the table 2.
6. Calculate gain in dB and plot the frequency response curve and find the bandwidth.

OBSERVATIONS:

Table 1: D.C. Conditions:

Parameter	V_{RC} (in volts)	V_{CE} (in volts)	V_E (in volts)	V_{BE} (in volts)	V_B (in volts)
Theoretical	4	6	2	0.7	2.7
Practical					

[NOTE: Use the tabular column separately for with and without feedback circuit]

Table 2: Frequency response with feedback and Vin (P-P) = 20mV

Frequency (Hz)	Vo(p-p) (V)	Av = Vo(p-p) / Vin(p-p)	Av (dB) = 20*log Av	Frequency (Hz)	Vo(p-p) (V)	Av = Vo(p-p) / Vin(p-p)	Av (dB) = 20*log Av
100				50K			
200				100K			
300				300K			
500				500K			
700				600K			
1K				700K			
3K				800K			
5K				900K			
10K				1M			
20K				2M			

Measurement of Input Impedance:

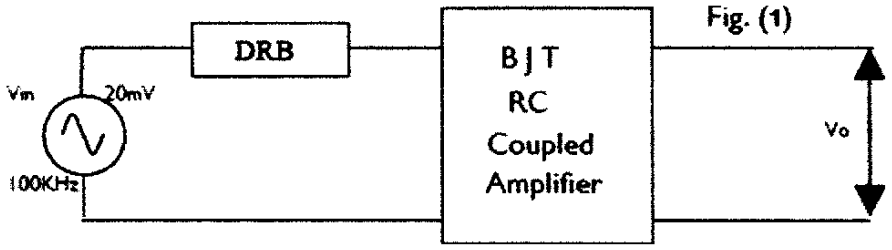


Figure 1b: Measurement of Input Impedance, Z_i

Procedure:

1. Connect the circuit as shown in above figure.
2. Set the following:
   a. DRB to zero.
   b. Input (Vin) sine wave amplitude of 20mV.
   c. Input sine wave frequency to any mid band frequency (say,100 KHz).
3. Measure Vo(p-p).
4. Increase DRB till VO = Vo(p-p)/2.
5. The corresponding DRB value gives the input impedance Zi.

Measurement of Output Impedance:

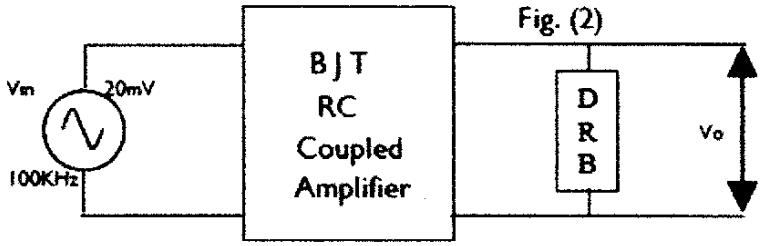
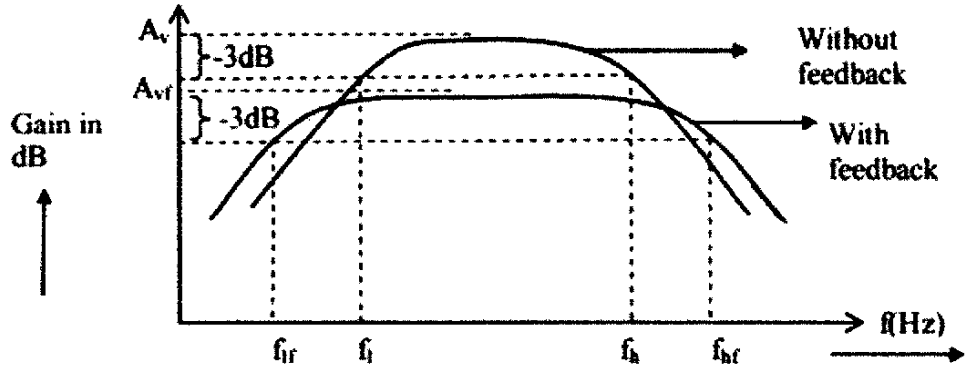


Figure 1c: Measurement of Output Impedance, Zo

Procedure:

1. Connect as in Figure (2).
2. Set the following:
   a. DRB to maximum value
   b. Input (Vin) sine wave amplitude to 20mV.
   c. Input sine wave frequency to any mid band frequency (say, 100 KHz)
3. Measure Vo(p-p).
4. Decrease DRB till Vo = Vo(p-p)/2.
5. The corresponding DRB value gives the output impedance Zo.

MODEL GRAPH:



Bandwidth= f_l-f_h

RESULTS:

With CE (Without feedback):	Without CE: (With feedback):
Av (Mid-band) =.	Av (Mid-band) =. . . . .
Bandwidth = ... Hz	Bandwidth = ... Hz
Input impedance = ... Ω	Input impedance = ... Ω
Output impedance = ... Ω	Output impedance = ... Ω

The RC-coupled amplifier was designed and rigged up and the parameters were found.

PRECAUTIONS:

1. Connections must be made with proper polarity.

2. Avoid loose and wrong connections.

Experiment No: 2

Design and set-up of Colpitt's, Crystal Oscillator using BJT

COLPITT'S OSCILLATOR

AIM: Design and set-up Colpitt's Oscillator using BJT.

OBJECTIVES:

1. To understand the AF oscillator and RF oscillator.
2. To understand the design of Colpitt's and Crystal Oscillator using BJT.

COMPONENTS AND EQUIPMENT'S REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	1
2	CRO: 20MHz	1
3	Discrete inductances 0.5 mH	1
4	Resistors: 1KΩ, 8.2 KΩ, 33KΩ, 470Ω and 1KΩ pot	1 each
5	Capacitors: 0.01 μF, 0.1 μF, 1 μF, 100μF	3, 1, 1 no's
6	Transistors: SL100	1
7	Bread board	1
8	CRO Probes and connecting wires	Few

CIRCUIT DIAGRAM:

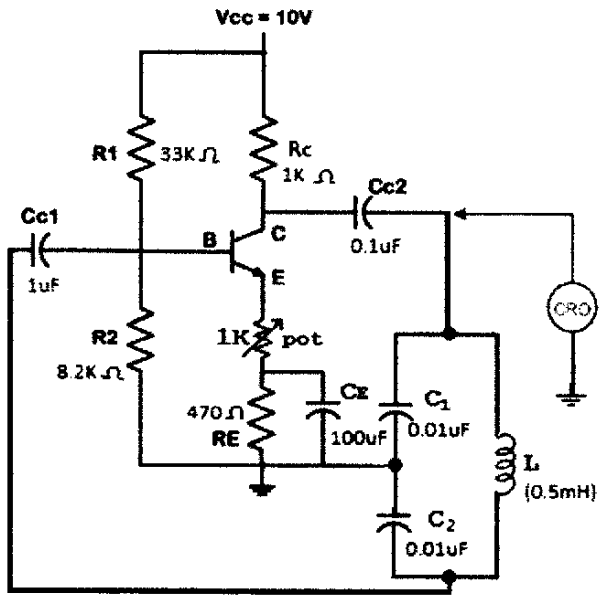


Figure 2a: Colpitt's Oscillator

DESIGN:

Let V_{CC} = 12V; I_C = 4mA; V_E = 2V; V_{CEQ} = 6V; hfe (β_{DC}) = 100.

1. **To find R_E:**

   Given V_E = 2V.

   Therefore, $R_E = V_E / I_E = V_E / I_C$ = 500Ω **Therefore R_E = 470Ω (standard)**

2. **To find R_C:**

   From the collector loop writing KVL we get

   $V_{CC} = I_C R_C + V_{CE} + V_E$

   $R_C = (V_{CC} - V_{CE} - V_E) / I_C$

   R_C = 1kΩ **Therefore, R_C = 1kΩ (standard)**

3. **To find R1 and R2:**

   The base current $I_B = I_C$ / hfe = 4mA / 100 = 0.04mA

   Let I_1 be current through R_1 and I_1 be 10 times of I_B.

   Writing the base loop KVL we get,

   $V_B = V_E + V_{BE}$ = 2 + 0.7= 2.7V **Therefore, V_B = 2.7V**

   Now, $R_1 = (V_{CC} - V_B) / I_1$

   R1 = (12 - 2.7)/0.4m = 23.25 kΩ **Therefore, R1 = 33 kΩ (standard)**

   Also, $R_2 = V_B / (I_1 - I_B)$

   R2 = 2.7/0.36m =7.5 kΩ **Therefore, R2 = 8.2 kΩ (standard)**

4. **To find C_{C1}, C_{C2} and C_E:**

   Let F_L = 100Hz (Lower cut-off frequency)

   Input coupling capacitor:

   $C_{C1} = 1 / (2*\pi*Zin*F_L)$

   C_{C1} = 1/ (2* π *558*100) =2.85 μF **Therefore, C_{C1}= 4.7 μF (standard)**

   Output coupling capacitor:

   $C_{C2} = 1 / (2* \pi *(R_C + R_L) *F_{in})$

   C_{C2} =1/ (2* π *(1k + 10k) *100) = 0.144□F **Therefore, C_{C2}= 0.1μF (standard)**

5. **Design of bypass capacitors, C_E:**

   Emitter bypass capacitor, $C_E = 1 / (2* \pi * re * F_L)$

   C_E = 1/ (2* π * 6.25 * 100) =254.6μF **Therefore, C_E =100μF (standard)**

6. Tank Circuit Design:

   Frequency of oscillation for Colpitt's oscillator is given by,

   $f_O = \frac{1}{2\pi\sqrt{L*C_{eq}}}$, where Ceq = $\frac{C_1 C_2}{C_1+C_2}$

   Let $C_1 = C_2$ = 0.01μF,

   Therefore, Ceq = $\frac{(0.01)(0.01)10^{-12}}{(0.02)10^{-6}}$ = 0.005 μF

   We have f_O= 100kHz, Then L = $\frac{1}{4\pi^2 f_O^2 C_{eq}}$

   L=$\frac{1}{4\pi^2(10000)(10^{3})^{\wedge}2*0.005*10^{-6}}$=5.06*$10^{-4}$H **Therefore, L=0.506mH**

PROCEDURE:

1. Switch on the Power Supply and check the D.C conditions.
2. Check for the sinusoidal waveform at output. If the output is distorted adjust 1KΩ Potentiometer to get perfect SINE wave.
3. Measure the period (T) of oscillation and calculate the frequency (f_o) of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

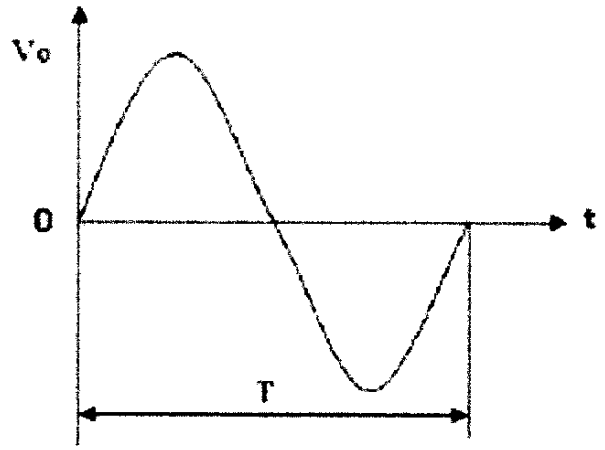
OBSERVATION:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Theoretical	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

TABULATION:

Sl. No.	Inductance, L (H)	Capacitance (F)			Theoretical $f_O = \frac{1}{2\pi\sqrt{L*C_{eq}}}$	Time, T (sec)	$f_o = 1/T$ (Hz)	Amplitude (V)
		C_1	C_2	C_{eq}				
1								
2								
3								

GRAPH:



RESULT:

Performance of the Colpitt's oscillator is tested.

Theoretical frequency f_o = 100kHz.

Practical frequency, f_o = ... kHz.

CRYSTAL OSCILLATOR

AIM: Design and set-up the crystal oscillator and determine the frequency of oscillation.

COMPONENTS AND EQUIPMENT'S REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	1
2	CRO: 20MHz	1
3	Crystal: 2MHz	1
4	Resistors: 1KΩ, 8.2 KΩ, 33KΩ, 470Ω and 1KΩ pot	1 each
5	Capacitors: 0.1 μF, 1 μF, 100μF	1 each
6	Transistors: SL100	1
7	Bread board	1
8	CRO Probes and connecting wires	Few

THEORY:

Crystal oscillators are used in order to get stable sinusoidal signals despite of variations in temperature, humidity, transistor and circuit parameters. A piezo electric crystal is used in this oscillator as resonant tank circuit. Crystal works under the principal of piezo-electric effect. i.e., when an AC signal applied across the crystal, it vibrates at the frequency of the applied voltage. Conversely if the crystal is forced to vibrate it will generate an AC signal. Commonly used crystals are Quartz, Rochelle salt etc.

NOTE: Design of amplifier using BJT is same as Colpitt's oscillator excluding feedback circuit.

CIRCUIT DIAGRAM:

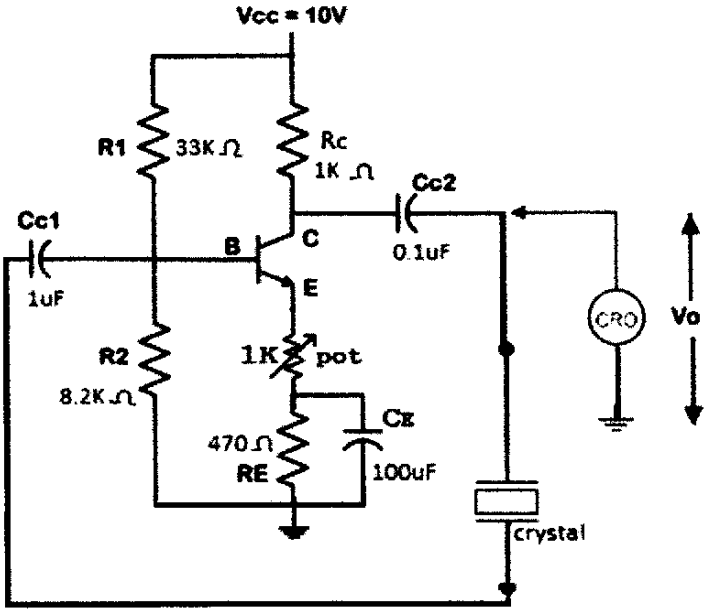


Figure 2b: Crystal Oscillator

PROCEDURE:

1. Switch on the Power Supply and check the D.C conditions.
2. Check for the sinusoidal waveform at output. If the output is distorted adjust 1KΩ Potentiometer to get perfect SINE wave.
3. Measure the period (T) of oscillation and calculate the frequency (fo) of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

OBSERVATION:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Theoretical	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

RESULT:

Performance of the Crystal oscillator is tested.

Theoretical frequency f_o = 2 MHz.

Practical frequency, f_o = ... MHz.

Experiment No: 3

Design Adder, Integrator, Differentiator, and Comparator circuits using Op-Amp

AIM: To design adder, differentiator, integrator, and comparator circuit using Op-Amp.

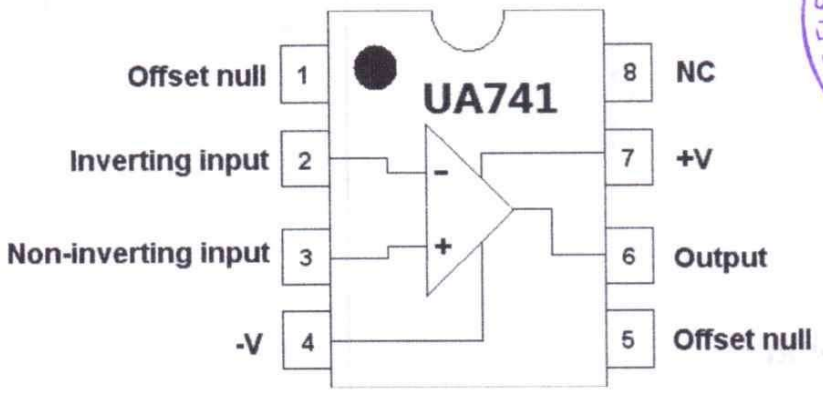
OBJECTIVES:

To design an adder, differentiator, integrator, and comparator circuit using Op-Amp.

COMPONENTS REQUIRED:

1. IC 741
2. Resistors as per circuit design
3. Function generator
4. Regulated power supply
5. Bread board
6. CRO / Patch cards / CRO probes
7. Connecting wires few

PIN DIAGRAM OF OPAMP:



THEORY:

ADDER:

Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non- inverting summer depending on the input applied to inverting & non-inverting terminals respectively. Circuit Diagram shows an inverting summing amplifier with 2 inputs. Here the output will be amplified version of the sum of the two input voltages with 1800 phase reversal.

DIFFERENTIATOR:

It is an op-amp circuit which performs the mathematical operation of differentiation. That is the output waveform is the derivative or differentia l of the input voltage. That is $Vo= - R_fC\ d(Vin)/dt$.

The differentiator circuit is constructed from basic inverting amplifier by replacing the input resistance Ri with capacitor C. This circuit also works as high pass filter.

INTEGRATOR:

It is a closed loop op-amp circuit which performs the mathematical operation of integration. That is the output waveform is the integral of the input voltage and is given by $Vo = (-1/R_fC) \int Vindt$. The integrator circuit is constructed from basic inverting amplifier by replacing the feedback resistance Rf with capacitor C. This circuit also works as low pass filter.

COMPARATOR:

A voltage comparator is a two-input circuit that compares the voltage at one input to the voltage at the other input. Usually, one input is a reference voltage and the other input a time varying signal. If the time varying input is below or above the reference voltage, then the comparator provides a low or high output accordingly (usually the plus or minus power supply voltages, since the op-amp is used in the open loop configuration, a small difference (−) makes the output to saturate).

DESIGN AN ADDER CIRCUIT USING OP-AMP AND VERIFY

Design: $Vo = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$ if $R_1 = R_2 = R_F = R$

$V_o = -(V_1+V_2) \equiv$ output voltage is proportional to the algebraic sum of the input voltages, V_1, V_2

CIRCUIT DIGRAM:

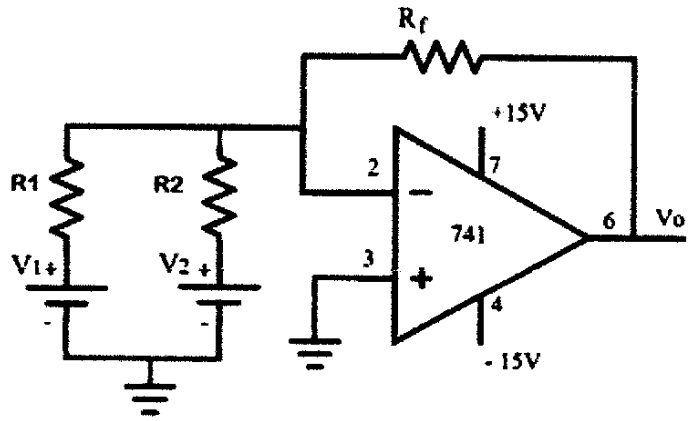


Figure 3a: Adder

PROCEDURE:

Summing/Adder Amplifier:

1. Connections are made as per the circuit diagram.
2. Input DC voltages V1 and V2 are given, and the corresponding output voltage Vo is measured from Multi-meter or CRO.
3. Output varies as $Vo = -(V1 + V2)$, since $R_F = R$.

TABULATION:

Sl. No.	R_1 Ω	R_2 Ω	R_F Ω	V1 volts	V2 Volts	$V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$ volts	Vo (practical) volts
1	1K	1K	1K	1	2		
2	1K	3.3K	2.2K	1	2		

DESIGN AN DIFFERENTIATOR CIRCUIT USING OP-AMP AND VERIFY

Design: $V_{out} = - R_f C \{dV_{in} / dt\}$

The output V_{out} is $R_f C$ times the differentiation of the input voltage. The product $R_f C$ is called as the RC time constant.

Given f = 1 KHz, so that, T = 1/f = 1ms

Design equation is $T = 2\pi R_f C$

Let $C = 0.01\mu F$

Then, $R_f = 15K\Omega$

Let $R_i = R_f/10 = 1.5K\Omega$

CIRCUIT DIGRAM:

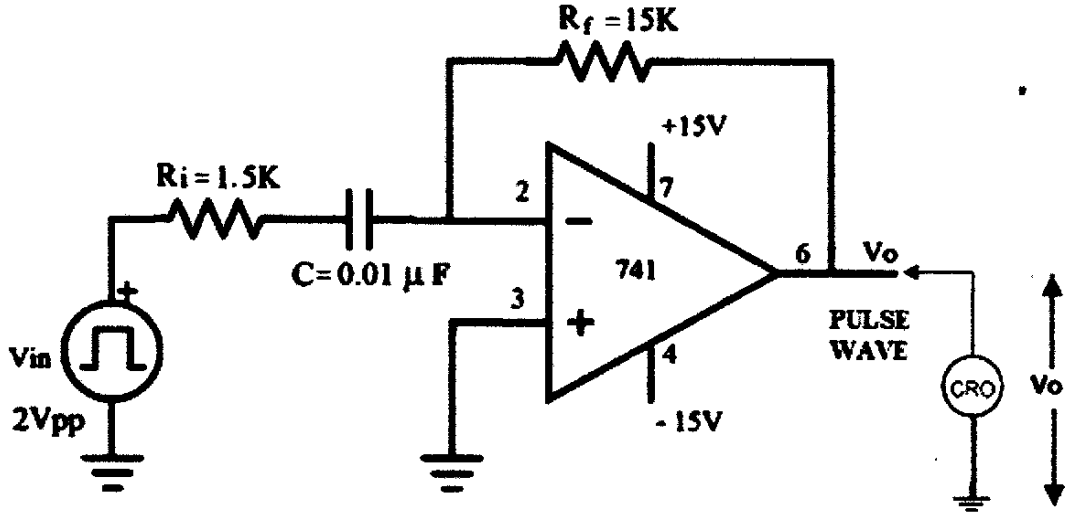


Figure 3b: Differentiator

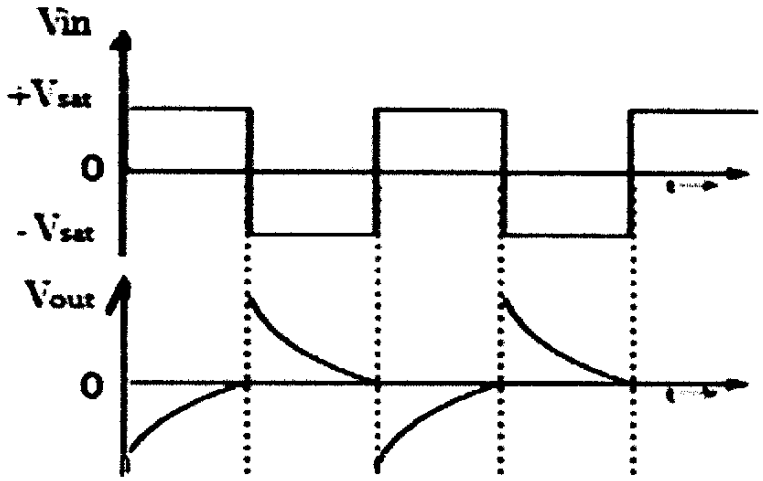
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A square wave/ triangle wave of 4V (p-p) and frequency of 1KHZ from function generator is applied to the inverting terminal (2) as input.
3. Using both channels of CRO, observe and record the corresponding amplitude and time period for input/output for the frequencies of 500 Hz and 1kHz.
4. With the above data plot the output graphs with time on X-axis and voltage on Y-axis. Compare this with the Equations given above.

TABULATION:

Type of circuit ↓	Input Square wave		Output Wave	
	Amplitude	Time period	Amplitude	Time period
Differentiator				

Expected Waveforms:



DESIGN AN INTEGRATION CIRCUIT USING OP-AMP AND VERIFY

Design:

$$V_{out} = -\frac{1}{CR_{in}}\int V_{in}\, dt$$

The output V_{out} is R_iC times the integration of the input voltage V_{in}. The product R_iC is called as the RC time constant.

Given f = 1 KHz, so that, T = 1/f = 1ms

Design equation is $T = 2\pi R_iC$

Let $C = 0.01\mu F$

Then, $R_i = 10K\Omega$ and let $R_f = 10R_i = 100K\Omega$

CIRCUIT DIGRAM:

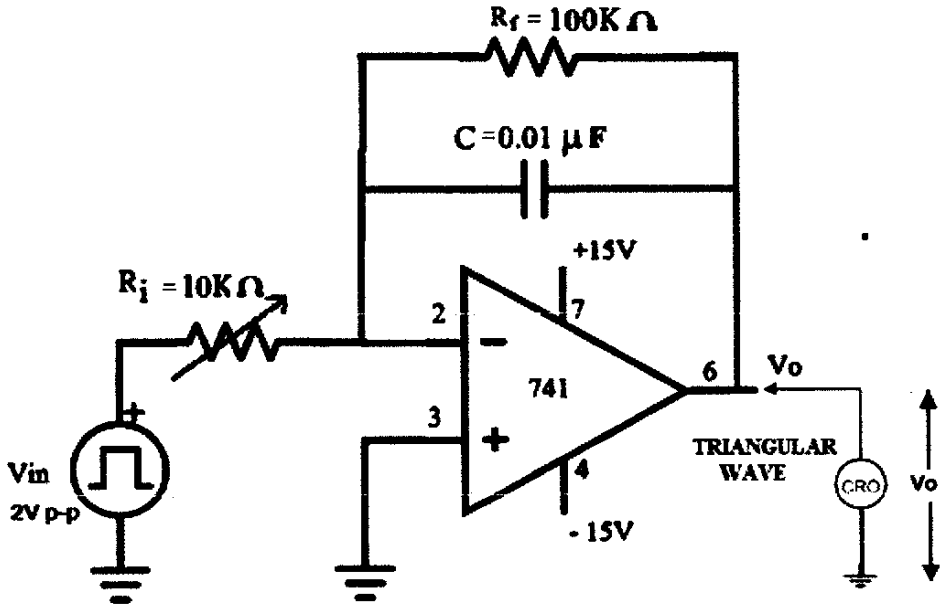


Figure 3c: Integrator

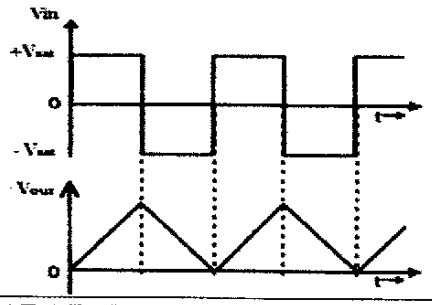
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A square wave/ triangle wave of 4V (p-p) and frequency of 1KHZ from function generator is applied to the inverting terminal (2) as input.
3. Using both channels of CRO, observe and record the corresponding amplitude and time period for input/output for the frequencies of 500 Hz and 1kHz.
4. With the above data plot the output graphs with time on X-axis and voltage on Y-axis. Compare this with the Equations given above.

TABULATION:

Type of circuit ↓	Input Square wave		Output Wave	
	Amplitude	Time period	Amplitude	Time period
Integrator				

Expected Waveforms:



DESIGN AN COMPARATOR CIRCUIT USING OP-AMP AND VERIFY

CIRCUIT DIAGRAM:

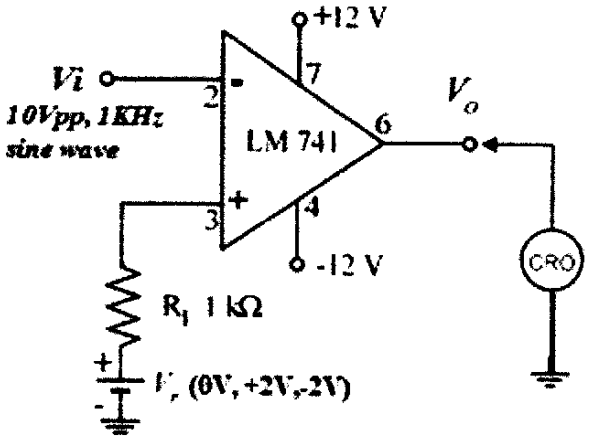
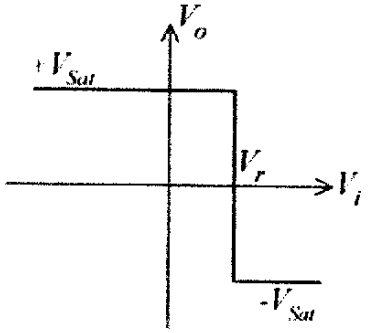


FIGURE 3d: COMPARATOR

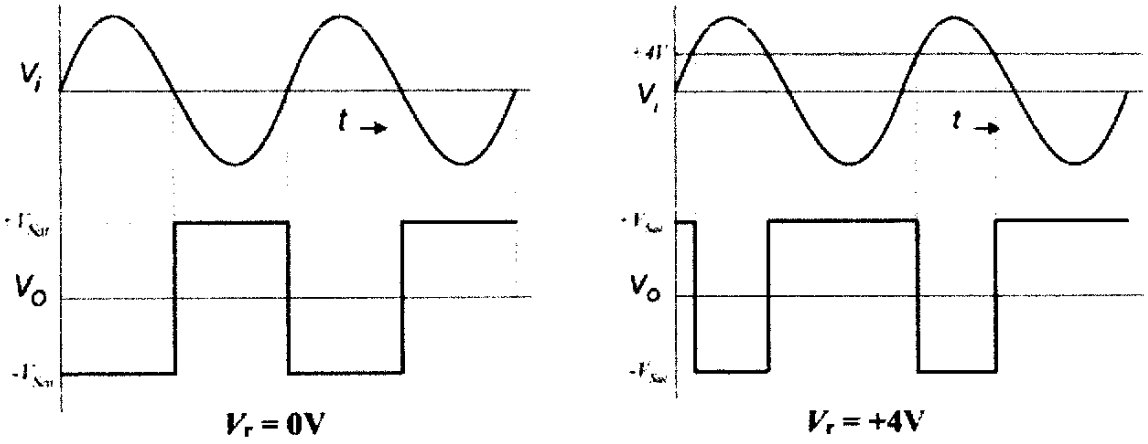
TRANSFER CHARACTERISTICS:



PROCEDURE

1. Set up the circuit as shown in the diagram.
2. Set the input voltage 10 V peak to peak, 1 kHz in function generator, and apply this as input signal to the circuit. Observe the output waveform in CRO.
3. Obtain the response for different Vr (say, Vr = 0V,±2V). Also, obtain the transfer characteristics.

EXPECTED WAVEFORMS:



RESULT:

Theoretical and practical output values for adder and input/output waveforms/values of differentiator, integrator and comparator are observed using op-amp.

Experiment No: 4

Design 4-bit R – 2R Op-Amp Digital to Analog Converter
(i) for a 4-bit binary input using toggle switches
(ii) by generating digital inputs using mod-16

AIM: (i) To design 4-bit R-2R Op-amp DAC for 4-bit binary input using toggle switches.

OBJECTIVE: To design 4bit R-2R ladder DAC using Op-Amp.

COMPONENTS AND EQUIPMENT'S REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	2
2	CRO: 20MHz	1
3	Op-amp IC: μA741	1
4	Resistors: 1KΩ, 2.2 KΩ	3, 5
5	Bread board	1
6	Connecting wires	Few
7	Multimeter	1

THEORY:

What is DAC? Digital to analog converter (DAC) is used to get analog voltage corresponding to an input digital data. Data in binary digital form can be converted to corresponding analog form by using a R-2R ladder (binary weighted resistor) network and a summing amplifier. It is more common and practical. Below is the circuit and output simulated waveform of R-2R ladder network DAC. This circuit also uses an op amp (741) summing amplifier circuit. The resolution of the converter will be equal to the value of the least significant bit (LSB) which is given as:

$$Resolution = V_{LSB} = -\frac{V_{ref}}{2^n}$$

$$\text{For } 4-\text{bit DAC}, \quad V_{ref} = 5V, \quad n = 4, \quad Resolution = V_{LSB} = -\frac{5}{16} = -0.3125V$$

Then the smallest step change of the analogue output voltage, VOUT for a 1-bit LSB change of the digital input of this 4-bit R-2R digital-to-analogue converter example is: 0.3125 volts. That is the output voltage changes in steps or increments of 0.3125 volts and not as a straight linear value.

DESIGN:

To design a 4-bit R-2R DAC for an output voltage, $V_o = 5V$,

Let R_i = Input equivalent resistance of the ladder network and R_F = feedback resistance.

From the circuit diagram,

$$I_{out} = I_0+I_1+I_2+I_3 \text{ (using KCL)}$$

Now, finding each current terms from Ohm's law, we get

$$I_{out} = \left(\frac{V_{ref}}{2R}\right)D_3 + \left(\frac{V_{ref}}{2R}\right)D_2 + \left(\frac{V_{ref}}{2R}\right)D_1 + \left(\frac{V_{ref}}{2R}\right)D_0$$

$$I_{out} = \left(\frac{V_{ref}}{R}\right)\left[\frac{D_3}{2} + \frac{D_2}{4} + \frac{D_1}{8} + \frac{D_0}{16}\right]$$

$$I_{out} = -\left(\frac{V_{out}}{R_F}\right) \quad or \quad V_{out} = I_{out} \cdot R_F$$

Therefore, above equation becomes, $\frac{V_{out}}{R_F} = -\frac{V_{ref}}{16R_i}[8D_3 + 4D_2 + 2D_1 + D_0]$

If $R_i = R_F = 1K\Omega$ then,

$$V_{out} = -\frac{V_{ref}}{16}[8D_3 + 4D_2 + 2D_1 + D_0]$$

For example: $(1010)_2 = (10)_{10}$ is applied from toggle switches then,

$D_3 = 1$ (MSB), $D_2 = 0$, $D_1 = 1$, $D_0 = 0$ (LSB) and $V_{ref} = 5V$, $V_{out} = -3.125V$

CIRCUIT DIAGRAM:

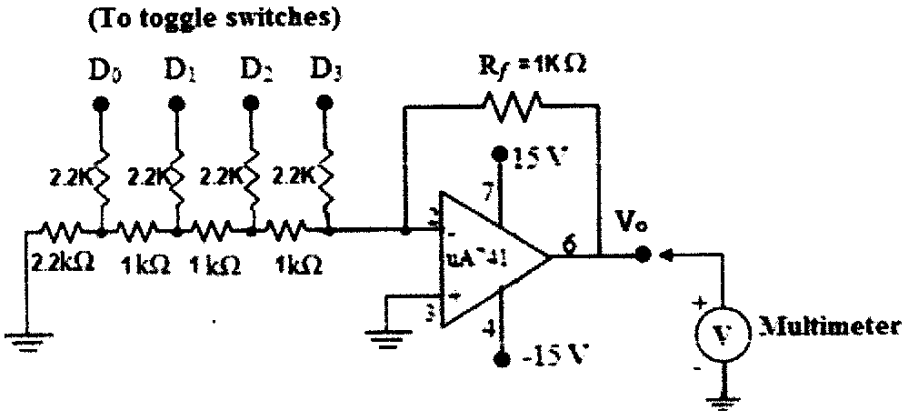


Figure 4b: 4-bit R-2R Ladder Circuit

PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Digital input data is given at D_3, D_2, D_1, D_0 and corresponding analog output voltage V_0 is measured using multimeter.
3. Compare practical and theoretical values of analog output voltage corresponding to binary input combination and find the error value.
4. Tabulate the readings & plot the graph between V_o on y-axis V_{in} on X-axis.

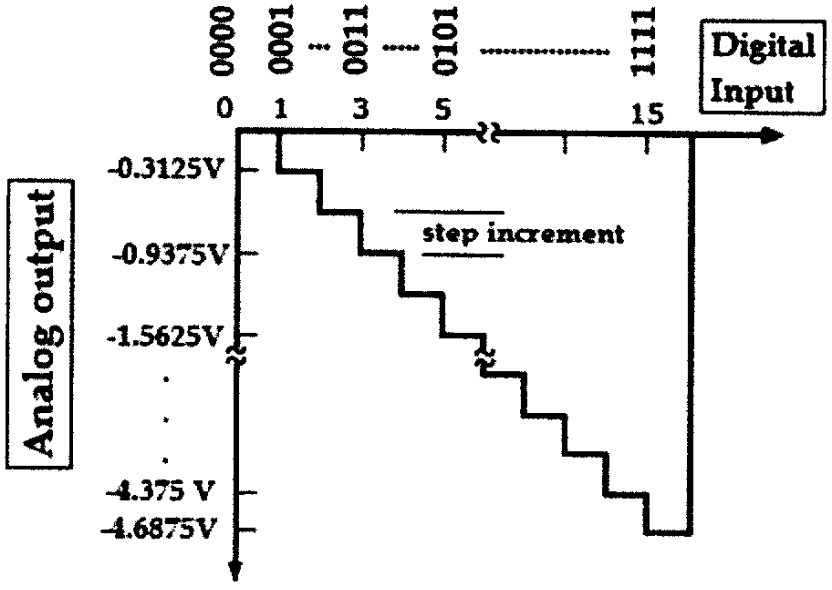
NOTE:

1. D_0, D_1, D_2 & D_3 are binary inputs (digital) applied from toggle switches.
2. V_o is the analog output.
3. Binary inputs D_0, D_1, D_2 & D_3 can take either the value '0' or '1' (Logic 0 → 0 and Logic 1 → +5V).
4. Binary input D_i (i = 0 to 3) can be made '0' by connecting the i/p to ground. It can be made '1' by connecting to +5 V.

TABULATION:

Decimal Value	Binary inputs (switches)				Analog $V_{(Practical)}$ volts (X)	Analog $V_{(Theoretical)}$ volts (Y)	Error X-Y
	D3	D2	D1	D0			
0	0	0	0	0			
1	0	0	0	1			
2	0	0	1	0			
3	0	0	1	1			
4	0	1	0	0			
5	0	1	0	1			
6	0	1	1	0			
7	0	1	1	1			
8	1	0	0	0			
9	1	0	0	1			
10	1	0	1	0			
11	1	0	1	1			
12	1	1	0	0			
13	1	1	0	1			
14	1	1	1	0			
15	1	1	1	1			

Ideal 4-bit R-2R DAC Transfer Characteristics:



AIM: (ii) To design 4-bit R-2R Op-amp DAC for 4-bit binary input using mod-16.

OBJECTIVE: To design 4bit R-2R ladder DAC using Op-Amp.

COMPONENTS REQUIRED:

1. Resistors (1KΩx4, 2KΩx5)
2. 741 Op Amp
3. 7493 Counter IC

In this circuit the IC 7493 is a counter simply it provides digital binary inputs (0000 to 1111) to OPAMP inputs D3D2D1D0 and observe & note down the display on CRO screen.

CIRCUIT DIAGRAM:

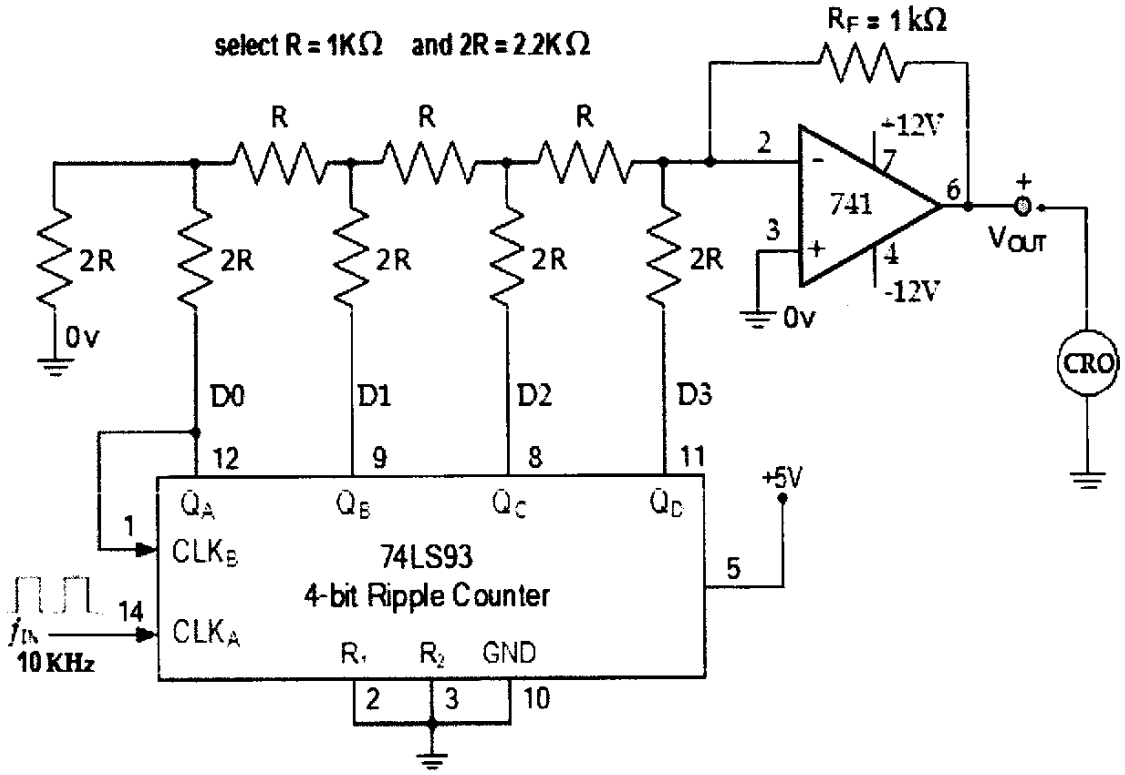
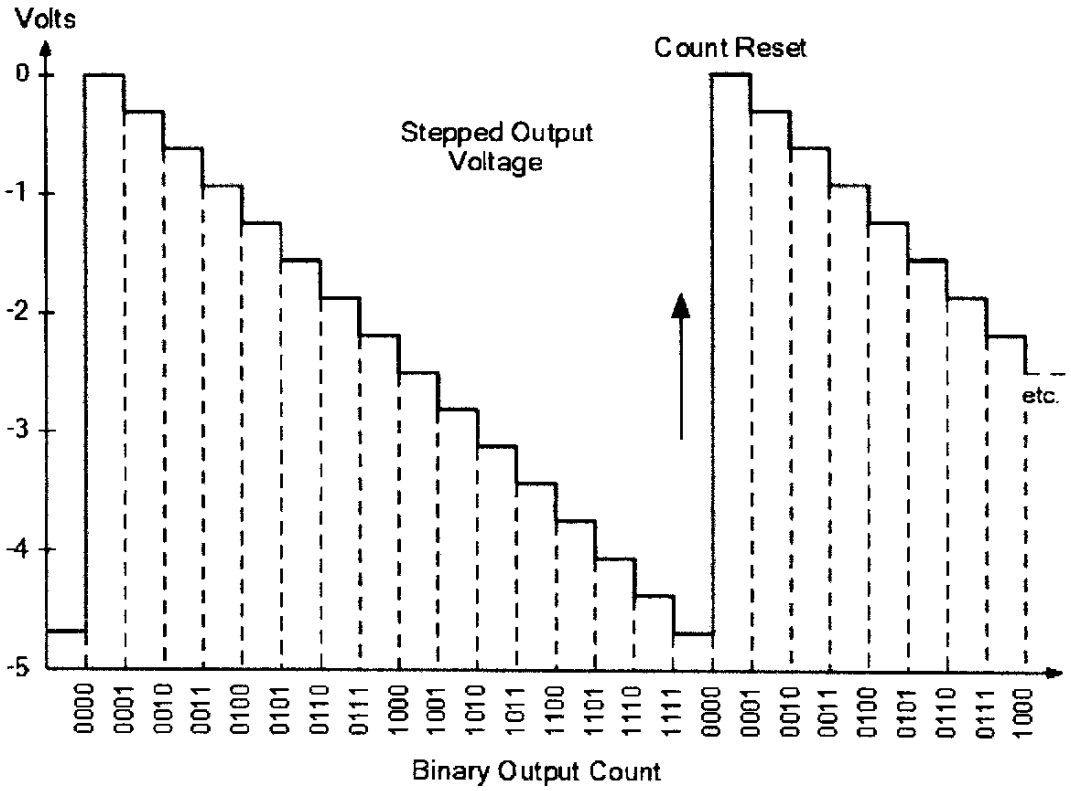


Figure 4b: 4-bit R-2R DAC using mod-16

MODEL GRAPH:



RESULT: 4-bit R-2R DAC is verified using toggle switches and counter IC 7493.

Experiment No: 5

Design and Implement (a) Half Adder & Full Adder using Basic logic gates and NAND gates. (b) Half Subtractor & Full Subtractor using Basic logic gates and NAND gates. (c) 4-variable function using IC74151(8:1 Mux)

AIM:

1. To design and realize Half Adder & Full Adder using Basic logic gates and NAND gates.
2. To design and realize Half Subtractor & Full Subtractor using Basic logic gates and NAND gates.
3. To design and realise 4-variable equation using 8:1 mux IC 74151

OBJECTIVES:

1. To understand Adder and Subtractor concept with the help of basic and universal gates.
2. To understand implementation of 4-variable function (SOP Equation) using 8:1 Mux.

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 7400	1
2.	IC 7408	1
3.	IC 7486	1
4.	IC 7432	1
5.	Patch cards	few
6.	IC Trainer Kit	1

THEORY:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B, is called a half- adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C.

Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called a full-adder.

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e., A –B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor.

Full Subtractor: Subtracting two single-bit binary values, B, Cin from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction.

Design and Implementation of Half and Full Adder and Half and Full Subtractor using Basic Gates and NAND Gates

HALF ADDER:

TRUTH TABLE of HALF ADDER:

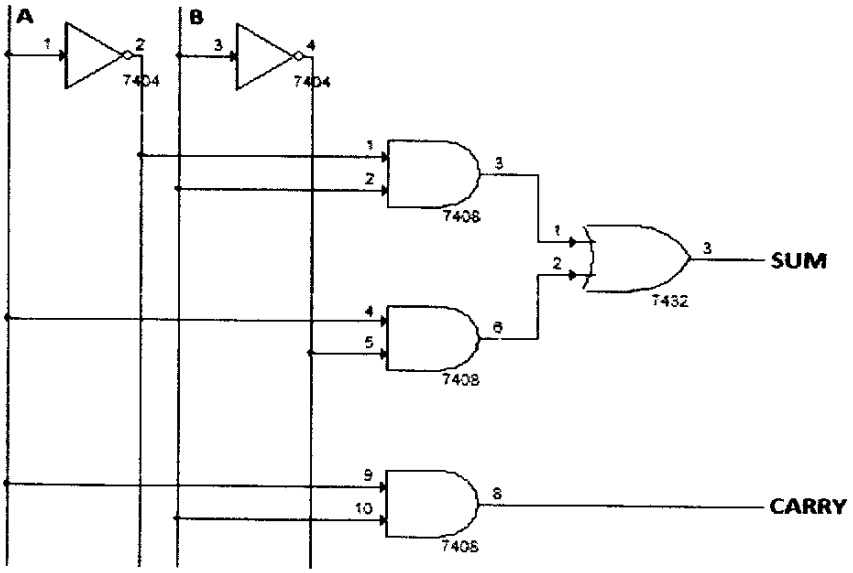
Inputs		Outputs	
A	B	Sum(S)	Carry©
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The Boolean functions describing the half-adder are:

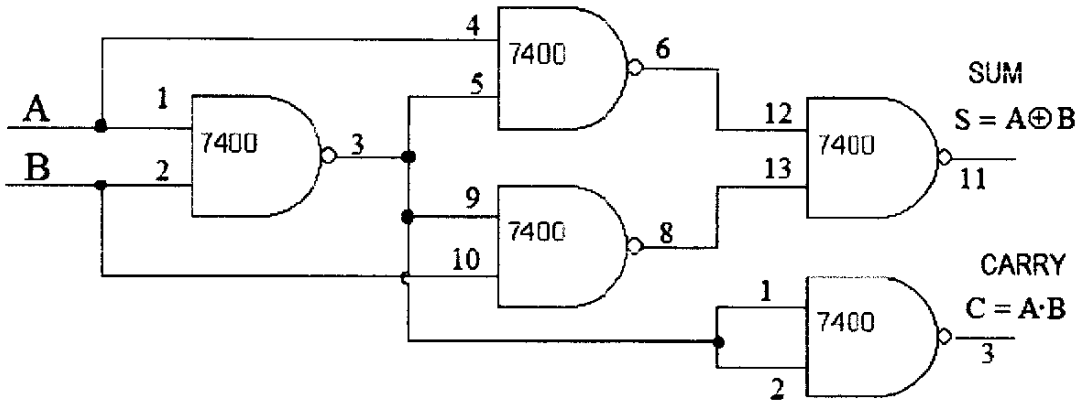
$$S = A \oplus B$$

$$C = A\,B$$

Circuit Diagram of Half Adder using basic gates:



Circuit Diagram of Half Adder using NAND gates:



FULL ADDER:

TRUTH TABLE OF FULL ADDER:

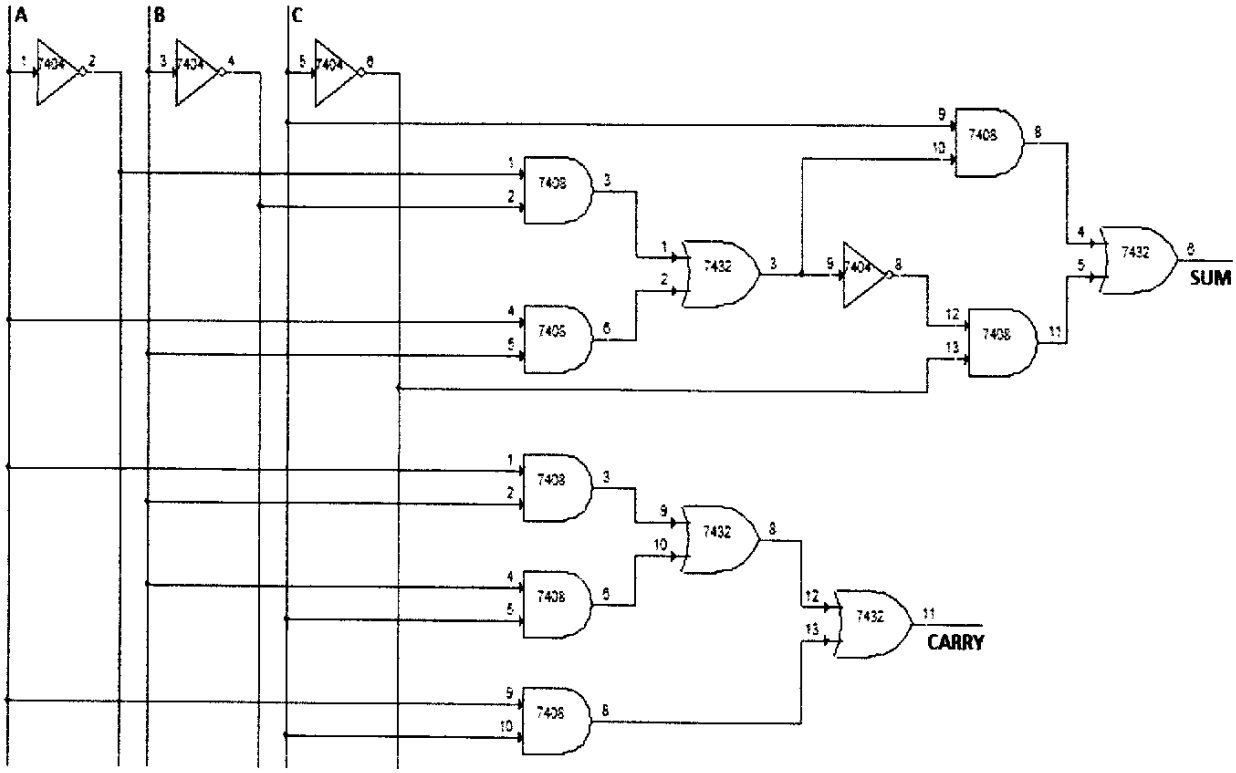
Inputs			Outputs	
A	**B**	**C_{in}**	**Sum (S)**	**Carry (C_{out})**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean functions describing the full adder are:

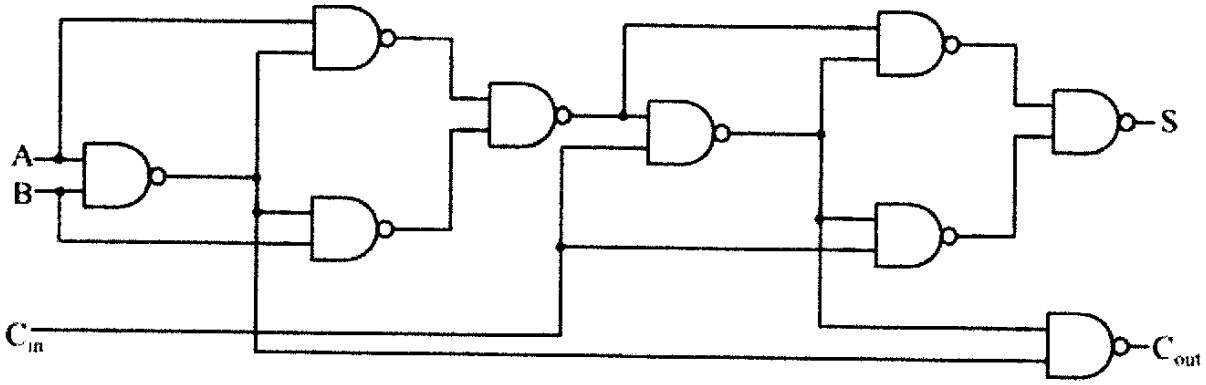
$$S = (x \oplus y) \oplus Cin$$

$$C_{out} = xy + Cin\ (x \oplus y)$$

Circuit Diagram of Full Adder using basic gates:



Circuit Diagram of Full Adder using NAND gates:



HALF SUBTRACTOR:

TRUTH TABLE OF HALF SUBTRACTOR:

Half Subtractor

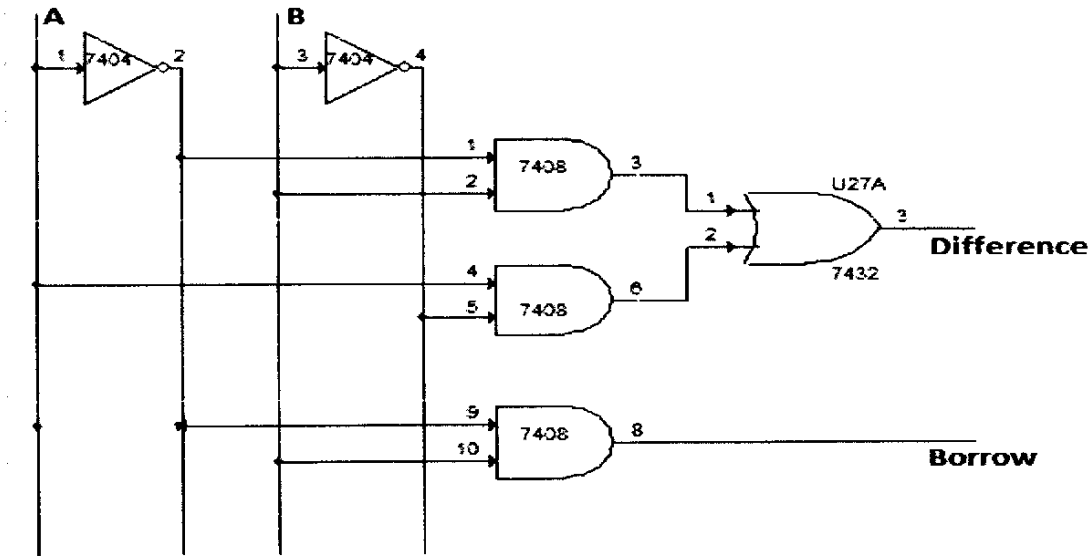
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The Boolean functions describing the half Subtractor are:

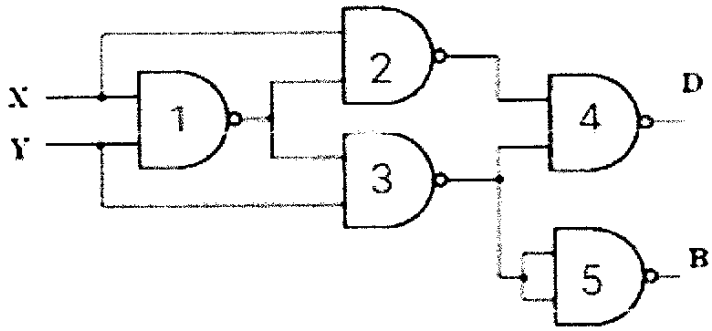
$$D = A \oplus B$$

$$Br = A' B$$

Circuit Diagram of Half Subtractor using basic gates:



Circuit Diagram of Half Subtractor using NAND gates:



Half-Subtractor using NAND gates

FULL SUBTRACTOR

TRUTH TABLE OF FULL SUBTRACTOR:

Full Subtractor

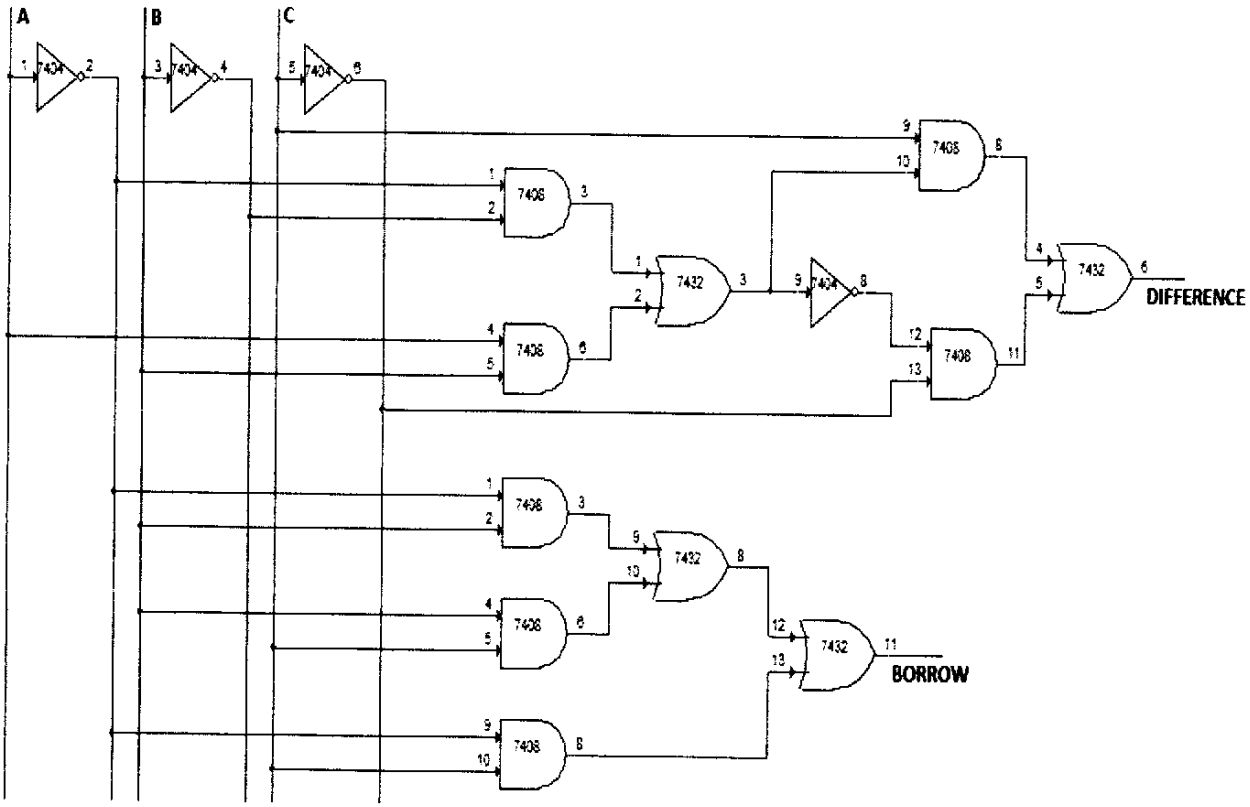
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The Boolean functions describing the full-subtracter are:

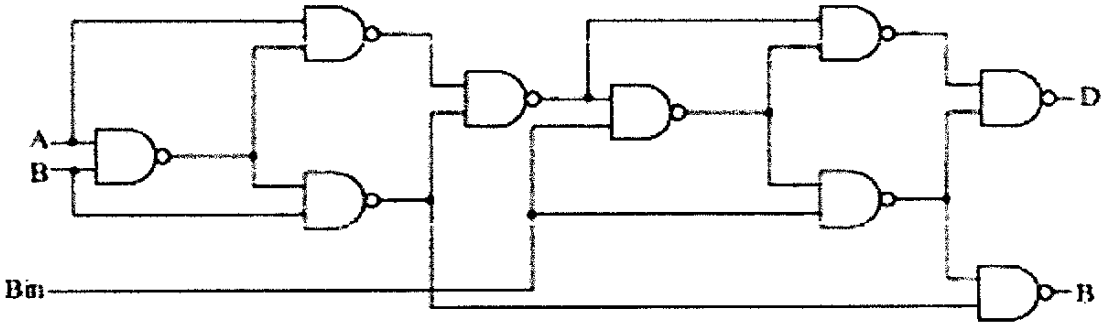
$D = (x \oplus y) \oplus Cin$

$Br = A'B + A' (Cin) + B (Cin)$

Circuit Diagram of Full Subtractor using basic gates:



Circuit Diagram of Full Subtractor using NAND gates:



Full Subtractor with NAND Gates

PROCEDURE:

1. Verify all gates according to respective truth tables.
2. Make the connections as per the circuit diagram.
3. Switch on VCC and apply various combinations of input according to the truth table.
4. Note down the output readings for half and full adder sum and the carry bit for different combinations of inputs.

RESULT: Half adder, Full adder, Half subtractor and Full subtractor using basic/NAND gates are verified.

Design and Implementation of 4-Variable Boolean expression using 8:1 Multiplexer

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 7404	1
2.	IC 74151	1
3.	Patch cards	few
4.	IC Trainer Kit	1

THEORY:

The TTL/MSI SN54/74LS151 is a high speed 8:1 digital multiplexer. It provides, in one DIP package, the ability to select one bit of data from 8 data inputs. The LS151 can be used as a universal function generator to generate any logic function of 4 variables.

Basic multiplexer has several data inputs and a single output line. The selection of a particular input line is controlled by a set of selection line. There are 2n input lines & n is the number of selection line whose bit combinations determines which input is selected.

Example: S2 S1 S0 = 010 code which corresponds to D2 input data line. Now apply D2 =0/1, this data 0/1 is transmitted to Y.

The given function is in terms of min-terms and is to be implemented using a 8:1 MUX. An 8:1 MUX has three select lines, whereas the given function is a 4-variable function. Hence, a logic is needed to give combination of A as inputs while only B, C and D as select line inputs. The method for the same is described below.

Design Example: To implement the following function: F(A,B,C,D) = Σ (0,1,3,4,8,9,15).

Step-1: Using K-map Boolean terms are determined for the variable A as shown below.

	D0	D1	D2	D3	D4	D5	D6	D7
$\bar{A}$	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A

Step-2: Construct digital circuit for the given 4 variable function F(A,B,C,D) = Σ (0,1,3,4,8,9,15), such that a logic is needed to give combination of A as inputs (1, 1, 0, $\bar{A}$, $\bar{A}$, 0, 0, A) while only B, C and D as select line inputs.

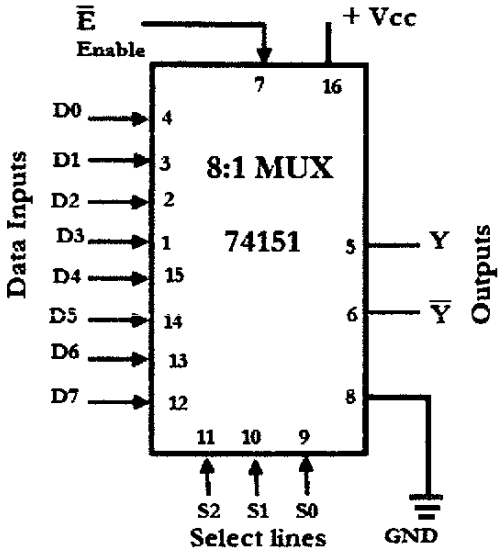


Fig.1 Pin Configuration of 7415

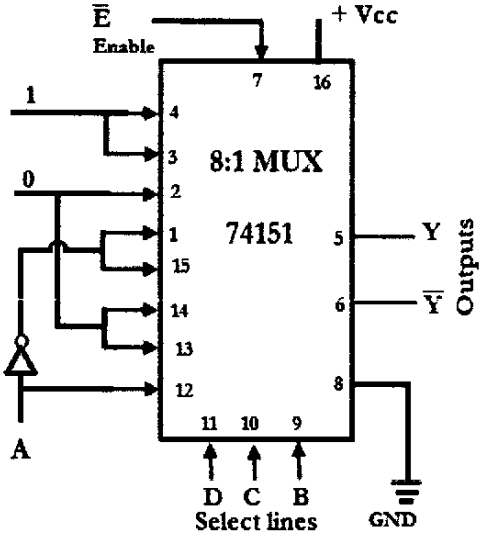


Fig.2 Circuit Diagram of for F(A,B,C,D) = Σ (0,1,3,4,8,9,15)

Step-3: Connect the circuit as shown in the fig. (b) and verify the following truth table.

A	B	C	D	Enable	Decimal	Y = F(A,B,C,D)
0	0	0	0	0	**0**	1
0	0	0	1	0	**1**	1
0	0	1	0	0	2	0
0	0	1	1	0	**3**	1
0	1	0	0	0	**4**	1
0	1	0	1	0	5	0
0	1	1	0	0	6	0
0	1	1	1	0	7	0
1	0	0	0	0	**8**	1
1	0	0	1	0	**9**	1
1	0	1	0	0	10	0
1	0	1	1	0	11	0
1	1	0	0	0	12	0
1	1	0	1	0	13	0
1	1	1	0	0	14	0
1	1	1	1	0	**15**	**1**

RESULT: 4 variable function F(A, B,C,D) = Σ (0,1,3,4,8,9,15) using IC 74151 (8:1 Multiplexer) is realized.

CONCLUSION: Adder and Subtractors are implemented using Basic and Universal logic gates also 4 variable expression is implemented using 8:1 Mux.

Experiment No: 6
Realize (i) Binary to Gray code conversion and vice versa (ii) BCD to Excess-3 code conversion and vice versa

AIM: To realize (i) Binary to Gray code conversion and vice versa (ii) BCD to Excess-3 code conversion and vice versa

OBJECTIVE: To study code conversion

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 7404	1
2.	IC 74139	1
3.	IC 7420	1
4.	Patch cards	few
5.	IC Trainer Kit	1

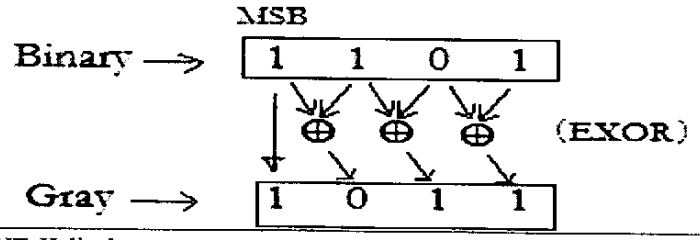
THEORY:

The logical circuit which converts binary code to equivalent gray code is known as binary to gray code converter. The gray code is a non-weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray code can be obtained by reflecting an n-1 bit code about an axis after 2n-1 rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis.

Binary to Gray code Conversion

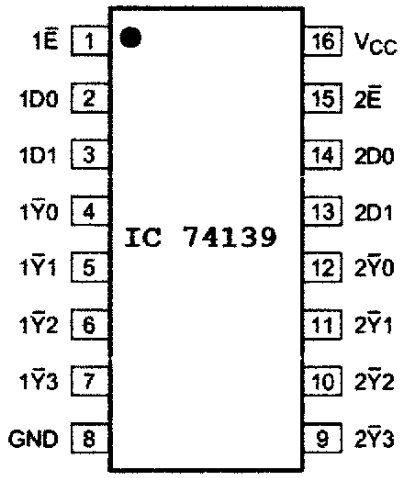
Following steps are required in this conversion:

1. The MSB of the gray code is equal to MSB of binary number.
2. Second bit of the gray code will be exclusive-or of the first and second bit of the given binary number.
3. The third bit of gray code will be equal to the exclusive -or of the second and third bit of the given binary number.
4. The fourth bit of gray code will be equal to the exclusive -or of the third bit and fourth bit of the given binary number.
5. One example given below can make your idea clear on this type of conversion.

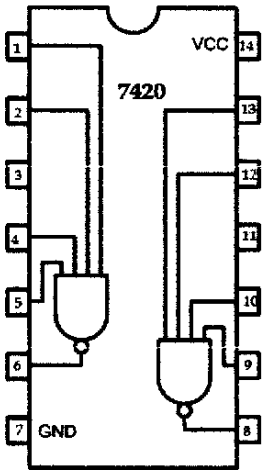


PIN CONFIGURATIONS

1. IC 74139



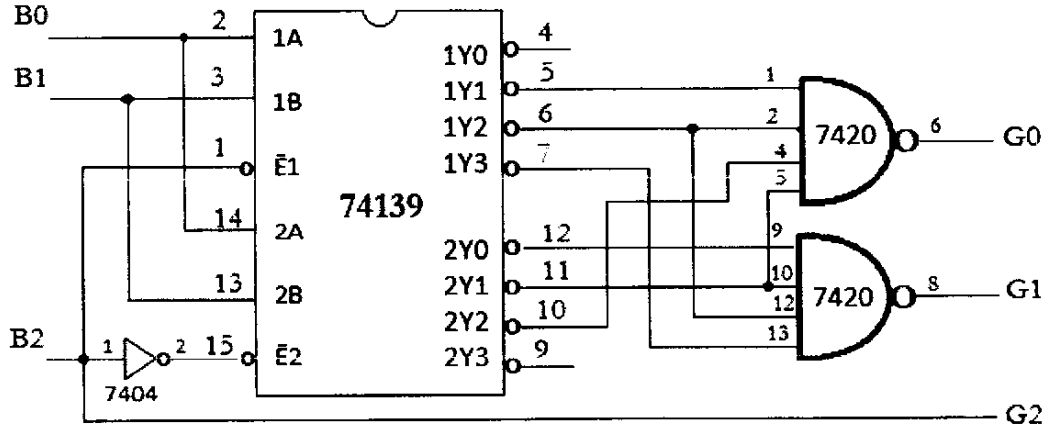
2. IC 7420



Truth Table of Binary to Gray Code Conversion:

Decimal	Binary (Input)			Gray (Output)			Conversion operation	Min-terms
	B2	B1	B0	G2	G1	G0		
0	0	0	0	0	0	0	G2 = B2 G1 = B1 ⊕ B2 G0 = B1 ⊕B0	$G_0 = \Sigma (1,2,5,6)$
1	0	0	1	0	0	1		
2	0	1	0	0	1	1		
3	0	1	1	0	1	0		$G_1 = \Sigma (2,3,4,5)$
4	1	0	0	1	1	0		
5	1	0	1	1	1	1		
6	1	1	0	1	0	1		$G_2 = \Sigma (4,5,6,7)$
7	1	1	1	1	0	0		

Circuit Diagram:

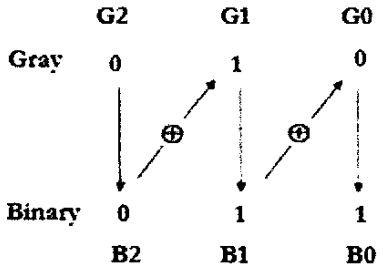


Gray code to Binary conversion

Following steps are required in this conversion:

1. The MSB of the binary number will be equal to the MSB of the given gray code.
2. Start with MSB of Binary number and EXOR it to the second bit of gray number to get next bit of binary.
3. This step is continued for all the bits to do Gray code to binary conversion.

One example given below can make your idea clear on this type of conversion

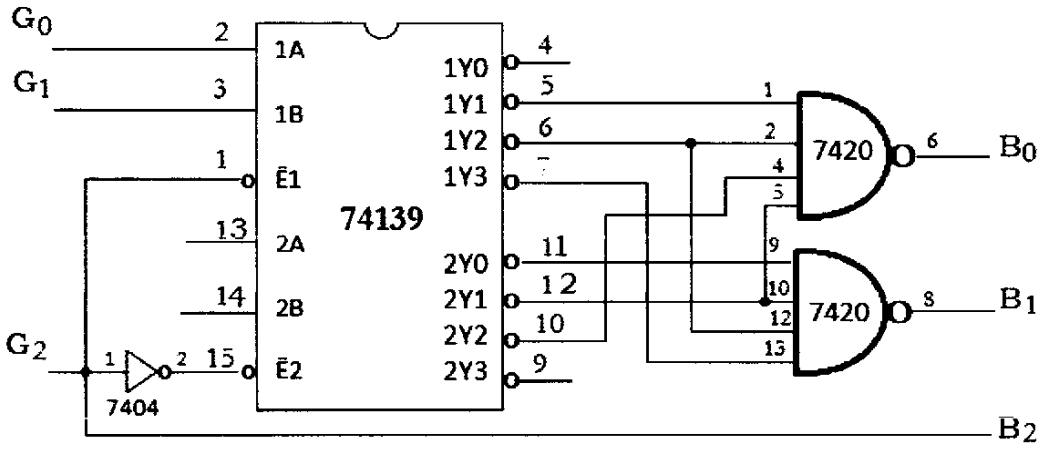


$$B_2 = G_2$$
$$B_1 = G_2 \oplus G_1$$
$$B_0 = G_2 \oplus G_1 \oplus G_0$$
$$(\oplus \Rightarrow Ex - Or\ Operation)$$

Truth Table: Binary to Gray conversion

Decimal	Gray (Input) G2 G1 G0	Binary (Output) B2 B1 B0	Conversion operation	Min-terms
0	0 0 0	0 0 0	$B_2 = G_2$ $B_1 = G_2 \oplus G_1$ $B_0 = G_2 \oplus G_1 \oplus$	$B_0 = \Sigma (1,2,4,7)$
1	0 0 1	0 0 1		
2	0 1 1	0 1 0		
3	0 1 0	0 1 1		$B_1 = \Sigma (2,3,4,5)$
4	1 1 0	1 0 0		
5	1 1 1	1 0 1		
6	1 0 1	1 1 0		$B_2 = \Sigma (4,5,6,7)$
7	1 0 0	1 1 1		

Circuit Diagram



PROCEDURE:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the Truth Table and observe the outputs.

BCD to Excess-3 code conversion and vice versa.

Sl. No.	Component Name	Quantity
1.	IC 7486	1
2.	IC 7483	1
3.	Patch cards	few
4.	IC Trainer Kit	1

THEORY

Code converter is a combinational circuit that translates the input code word into a new corresponding word. In this code each decimal digit is represented by a 4 -bit binary number. BCD is a way to express each of the decimal digits with a binary code. In the BCD, with four bits we can represent sixteen numbers (0000 to 1111). But in BCD code only first ten of these are used (0000 to 1001). The remaining six code combinations i.e., 1010 to 1111 are invalid in BCD.

To Construct a BCD-to-excess-3-code converter with a 4-bit adder feed BCD code to the 4- bit adder as the firstoperand and then feed constant 3 (0011) as the second operand. The output is the corresponding excess-3 code. To make it work as a excess-3 to BCD converter, we feed excess-3 code as the first operand and then feed 2's complement of 3 as the second operand. The output is the BCD code.

Excess-3 Code - It is non-weighted code used to express decimal numbers. The Excess -3 code words are derived from the 8421 BCD code words adding $(0011)_2$ or $(3)_{10}$ to each code word in 8421.

TRUTH TABLE:

Truth Table of BCD to Excess-3 Code Conversions and Vice Versa

BCD to EXCESS-3 code

BCD (input)				BCD code word	Excess -3 (output)			
B3	B2	B1	B0		E3	E2	E1	E0
0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	1	0	0
0	0	1	0	2	0	1	0	1
0	0	1	1	3	0	1	1	0
0	1	0	0	4	0	1	1	1
0	1	0	1	5	1	0	0	0
0	1	1	0	6	1	0	0	1
0	1	1	1	7	1	0	1	0
1	0	0	0	8	1	0	1	1
1	0	0	1	9	1	1	0	0

EXCESS-3 to BCD code

Excess -3 (input)				BCD code word	BCD code (output)			
E3	E2	E1	E0		B3	B2	B1	B0
0	0	1	1	0	0	0	0	0
0	1	0	0	1	0	0	0	1
0	1	0	1	2	0	0	1	0
0	1	1	0	3	0	0	1	1
0	1	1	1	4	0	1	0	0
1	0	0	0	5	0	1	0	1
1	0	0	1	6	0	1	1	0
1	0	1	0	7	0	1	1	1
1	0	1	1	8	1	0	0	0
1	1	0	0	9	1	0	0	1

CIRCUIT DIAGRAM:

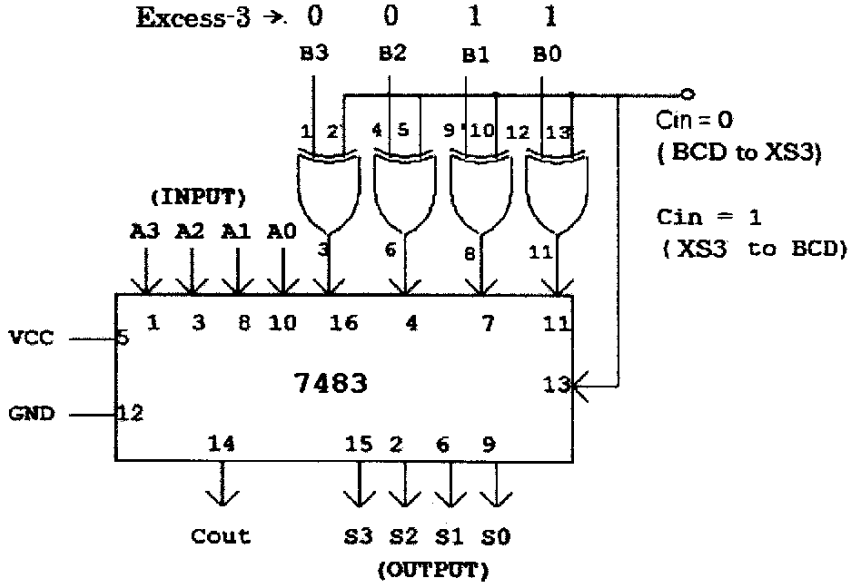


Figure: BCD to EXCESS -3 / EXCESS -3 to BCD Conversion

PROCEDURE:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the Truth Table and observe the outputs.

RESULT: (1) Binary to Gray Code Conversion and vice versa
(2) BCD to Excess-3 code conversion and vice versa, truth tables are verified

CONCLUSION: Code Conversion is designed and implemented.

Experiment No: 7
(a)Realize using NAND Gates i) Master Slave JK flip-flop (ii) D-flip-flop (iii) T-flip-flop using NAND gates (b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring Counter (vi)Johnson Counter

AIM:

1. To Realize i) Master Slave JK flip-flop (ii) D-flip-flop (iii) T-flip-flop using NAND gates.
2. To Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring Counter (vi)Johnson Counter.

OBJECTIVES:

1. To understand working of flip-flop
2. To understand applications of Flip-flops

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 7400	2
2.	IC 7410	1
3.	Patch cards	few
4.	IC Trainer Kit	1

Realize i) Master Slave JK flip-flop (ii) D-flip-flop (iii) T-flip-flop using NAND gates

THEORY:

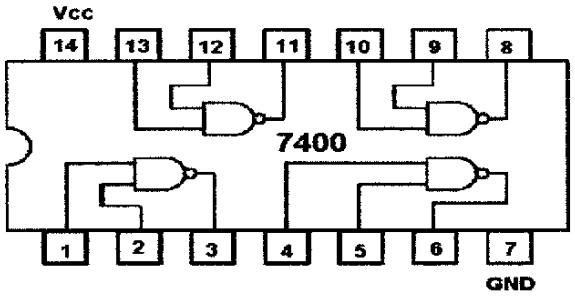
Flip-Flops are binary cells capable of storing one bit of information. A Flip Flop has two outputs, one for the normal value and one for complement value of the bit stored in it.

JK FLIP-FLOP: is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time under normal switching thereby eliminating the invalid condition of SR flip flop. However, if J = K = 1 and clock input is applied the circuit will "toggle" as its outputs switch and change state complementing each other. This timing problem called "race". The master-slave flip- flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. One flip-flop act as the "Master" circuit, which triggers on the leading edge of the clock pulse while the other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. This results in the two sections; the master section and the slave section being enabled during opposite half-cycles of the clock signal.

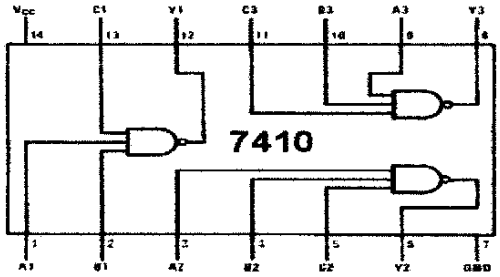
D FLIP-FLOP: It has only one data input (D) and clock input (CP). The outputs are labelled Q and Q'. The data (0 or 1) at the input 0 is delayed one clock pulse from getting to output Q. SD and CD are active low input (Negative edge trigger) to set and reset the Flip-Flop i.e., these inputs will be effective when logic 0 is applied. A D Flip-flop is a bi-stable circuit whose 0 input is transferred to the output after a clock pulse is received.

T FLIP-FLOP: This T Flip-Flop is obtained from a JK type if both inputs are tied together. The designation T shows ability of Flip-Flop to toggle. Regardless of the present state of the Flip-Flop, it assumes the complement state when the clock pulse occurs while input T is logic1. When T=0, both AND gates are disabled and hence there is no change in the previous output. When T=1, (J=K=1) output toggles.

PIN DIAGRAM:

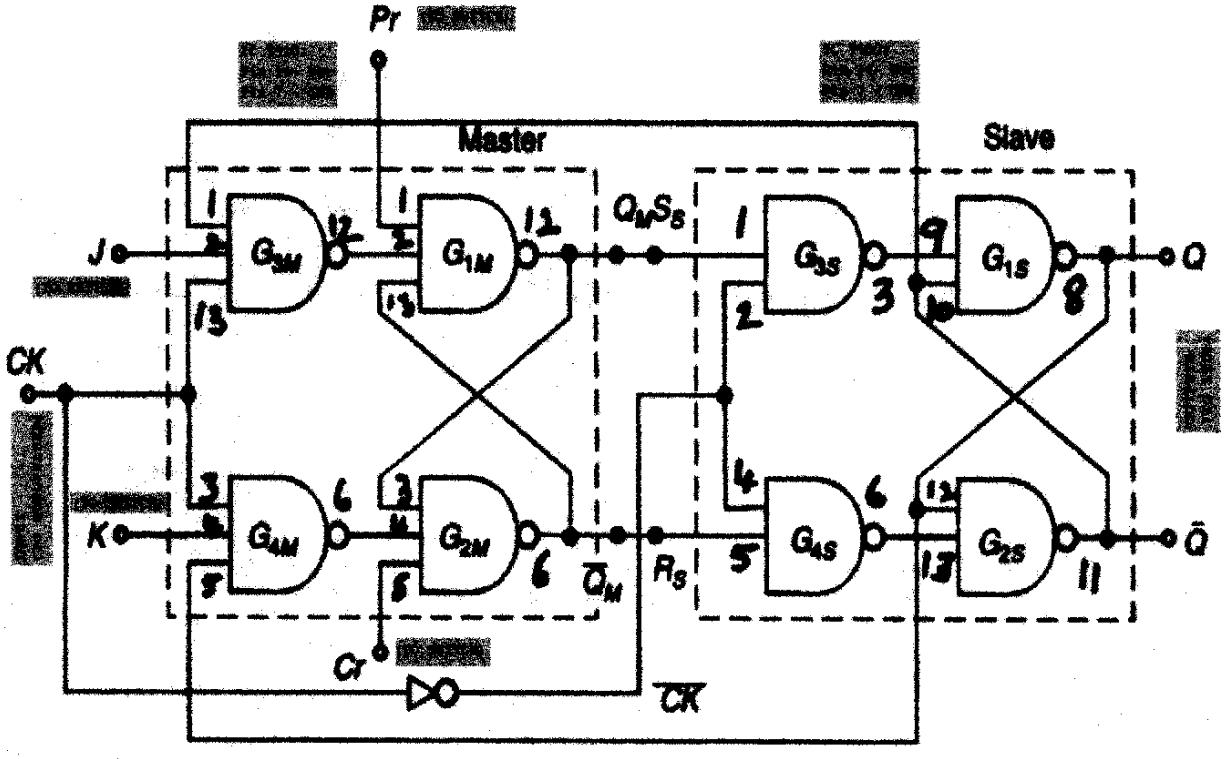


QUAD 2 INPUT NAND GATE



Triple 3 Input NAND GATE

CIRCUIT DIAGRAM FOR MASTER SLAVE JK FF:



OBSERVATION TABLE / LOOKUP TABLE / TRUTH TABLE:

JK-MASTER SLAVE FLIP-FLOP				
INPUTS		Q(t) before Clock Pulse (Establish using Preset & Clear)	OUTPUTS	
J	K		Q(t+1)	Q(t+1)'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

The simple form of function table is given below:

INPUTS		OUTPUT	Status
J	K	Q(t+1)	
0	0	Q(t)	HOLD
0	1	0	RESET
1	0	1	SET
1	1	Q(t)'	TOGGLE

Qnext = JQ' + K'Q

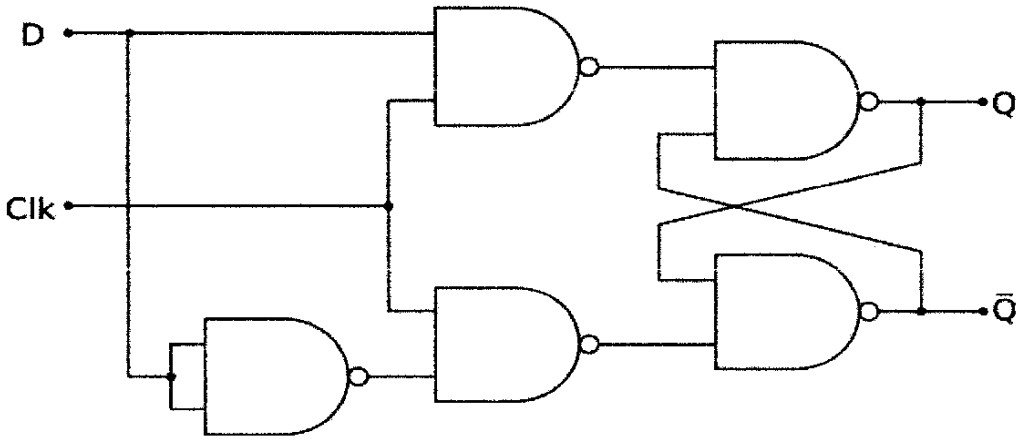
D FLIP-FLOP:

D flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. when D = 1 and CLOCK = HIGH, Output: Q = 1, $\bar{Q}$ = 0. Working is correct.

TRUTH TABLE:

Clock	D	Output Q	Output $\bar{Q}$
0↑1	0	0	1
0↑1	1	1	0
1↑0	X	Q	$\bar{Q}$

CIRCUIT DIAGRAM:



T FLIP-FLOP:

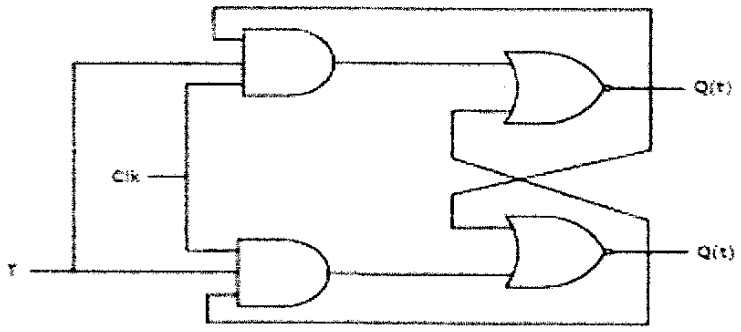
The T flip-flop is a single input version of the JK flip-flop. The T flip-flop is obtained from the

JK type if bothinputs are tied together.

TRUTH TABLE:

Clock	T	Output	
		Q	$\bar{Q}$
0↑1	0	Q	$\bar{Q}$
0↑1	1	$\bar{Q}$	Q
1↑0	X	Q	$\bar{Q}$

CIRCUIT DIAGRAM:



PROCEDURE:

1) Turn on power to the circuit.

2) For each input combination, note the logic state of the normal (Q) and complementary ($\bar{Q}$) outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the results in a table.

3) Compare your results with the truth tables.

RESULT: Master Slave JK flip-flop, D-flip-flop & T-flip-flop using NAND gates are verified.

Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring Counter (vi)Johnson Counter

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 7495	1
2.	IC 7404	1
3.	Patch cards	few
4.	IC Trainer Kit	1

THEORY:

The binary information (data) in a register can be moved within or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers. They are very important in applications involving the storage and transfer of data in a digital system.

Types of shift registers:

Serial In Serial Out [SISO]:

In this type of register, the output of one flip-flop is connected to the input of the next flip-flop. Output of the register is obtained from the last flip-flop. Depending on the direction of the input given shifting takes place in this. Bit by bit loading and shifting takes place with every clock pulse.

Serial In Parallel Out [SIPO]:

This is similar to SISO except that the output is taken from each flip-flop. Thereby the shifted value is shown at once.

Parallel In Parallel Out [PIPO]:

Upon giving clock pulse, data is loaded in parallel in all flip-flops. Output is taken from each of the flip-flop.

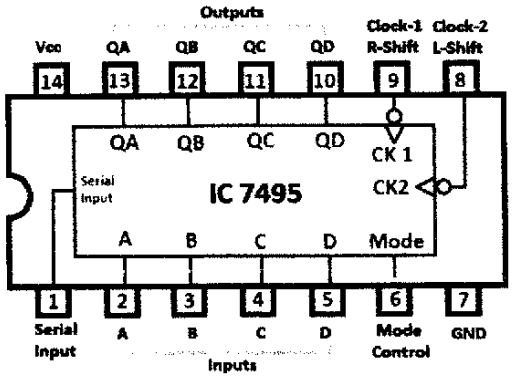
Parallel In Serial Out [PISO]:

Here we use a control input Load/ (Shift) such that if Load/ (Shift) = 1, data is loaded in all flip-flops in parallel and when the Load/ (Shift) = 0, data is shifted with every clock pulse. Output is obtained from the last flip-flop.

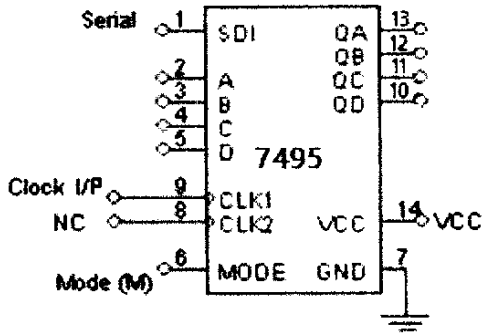
3 Modes of Operation of IC 7495: Parallel, Shift right and Shift Left

Parallel	Shift right	Shift Left
Mode control = 1	Mode control = 0	Mode control = 1
Clock-2 = HIGH to LOW	Clock-1 = HIGH to LOW	Clock-2 = HIGH to LOW

PIN DIAGRAM OF IC 7495:



SIPO (Right Shift)



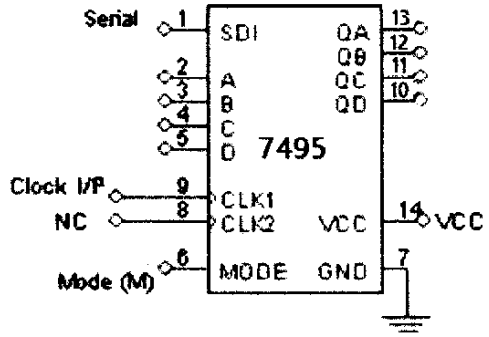
SIPO Function Table

Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p (pin-1)
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new dataapplied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

SISO (Right Shift)



SISO Function Table

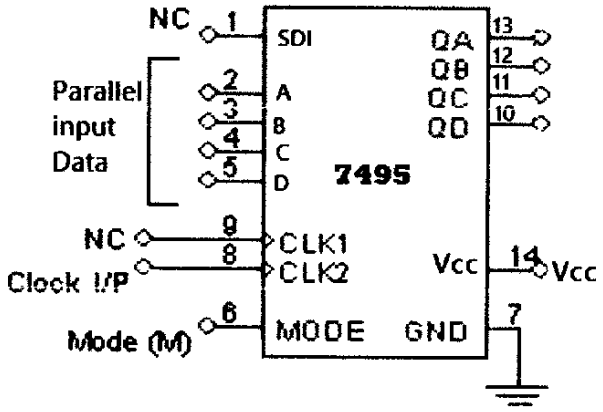
Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data 'd0' appears at QD.
4. Apply 5th clock pulse; the second data 'd1' appears at QD.

5. Apply 6th clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data 'd3' to appear at QD.Thus, the data applied serially at the input comes out serially at QD.

PISO:-



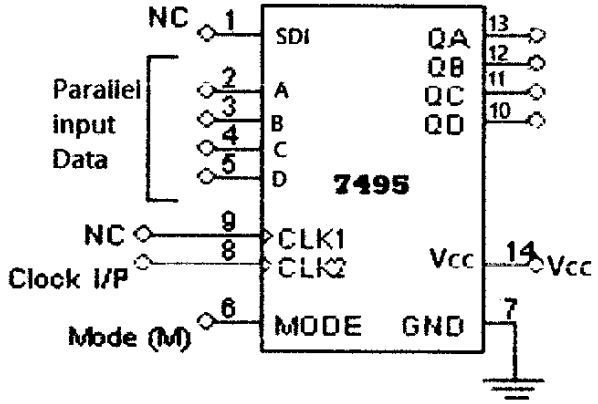
PISO Function Table

Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Apply the desired 4-bit data at A, B, C and D.
3. Keeping the mode control =1 apply one clock pulse. The data applied at A, B, C and D willappear at QA, QB, QC and QD respectively.
4. Now mode control = 0. Apply clock pulses one by one and observe the data coming out serially at QD.

PIPO:-



PIPO Function Table

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Apply the 4-bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control =1).
4. The 4-bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

RESULT: Shift registers using IC 7495 for SIPO/SISO, PISO/PIPO are verified.

Realization of Ring counter and Johnson counter using IC 7495

COMPONENTS REQUIRED:

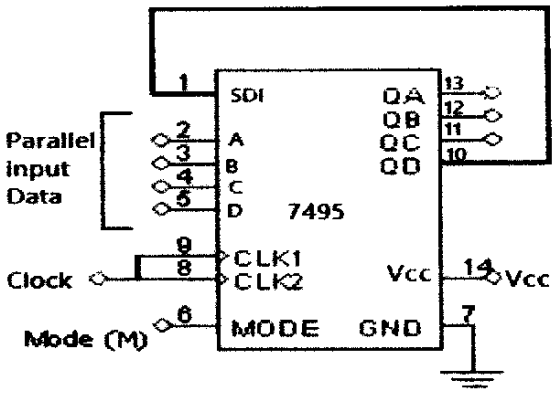
Sl. No.	Component Name	Quantity
1.	IC 7495	1
2.	IC 7404	1
3.	Patch cards	few
4.	IC Trainer Kit	1

THEORY:

A ring counter is a circular shift register which is initiated such that only one of its flip-flops is the state one while others are in their zero states. A ring counter is a Shift Register with the output of the last one connected to the input of the first, that is, in a ring. Typically, a pattern consisting of a single bit is circulated so the state repeats every n clock cycles if n flip-flops are used. It can be used as a cycle counter of n states.

RING COUNTER:

CIRCUIT DIAGRAM:



FUNCTION TABLE:

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	repeats			

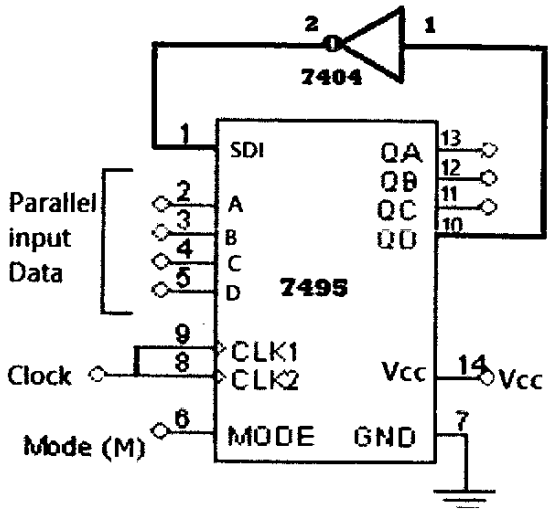
THEORY:

A Johnson counter (or switch tail ring counter, twisted-ring counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the

decade counter, digital-to-analog conversion, etc. They can be implemented easily using D- or JK-type flip-flops.

JOHNSON COUNTER:

CIRCUIT DIAGRAM:



FUNCTION TABLE:

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	repeats			

PROCEDURE:

1. Make the connections as shown in the respective circuit diagram.
2. Initial condition is set by setting up the circuit as shown in the figure.
3. Apply clock and observe the output after each clock pulse, record the observations and verify that they match the expected outputs from the truth table.
4. Verify the operation of ring counter/Johnson counter circuit as per the function tables

RESULT: Ring counter and Johnson counter using IC 7495 are verified

CONCLUSION: Flip-Flops as Ring and Johnson Counter is verified.

Experiment No: 8

Realize (a) Design Mod-N Synchronous Up counter & Down Counter using 7476 JK flip-flop (b) Mod-N counter using IC7490/7476 (c) Synchronous counter using IC74192

AIM:

1. To realize Mod-N Synchronous Up counter & Down Counter using 7476 JK flip-flop
2. To realize Mod-N counter using IC7490/7476
3. To realize Synchronous counter using IC74192

COMPONENTS REQUIRED:

Sl. No.	Component Name	Quantity
1.	IC 74LS76A	1
2.	IC 7408	1
3.	Patch cards	few
4.	IC Trainer Kit	1

(a) Design Mod-N Synchronous Up counter & Down Counter using 7476 JK flip-flop

THEORY:

Counters: counters are logical device or registers capable of counting the no. of states or no. of clock pulses arriving at its clock input where clock is a timing parameter arriving at regular intervals of time, so counters can be also used to measure time & frequencies. They are made up of flip flops. Where the pulse is counted to be made of it goes up step by step & the o/p of counter in the flip flop is decoded to read the count to its starting step after counting n pulse in case of module counters.

Counters are of two types:

1) Asynchronous counter 2) Synchronous counter.

Asynchronous counter commonly called ripple counter, the first flip-flop is clocked by the external clock pulse & then each successive flip-flop is clocked by the Q or Q' output of the previous flip-flop. Therefore, in an asynchronous counter the flip-flops are not clocked simultaneously. When counter is clocked such that each flip flop in the counter is triggered external clock at the same time, the counter is called as synchronous counter. Ex: - Ring counter & Johnson counter

Types of synchronous counter:

1) Up counter 2) Down counter.

Decision for number of flip-flops

Example: If we are designing mod N counter and m number of flip-flops are required then m can be found out by this equation.

$N <= 2m$

Here we are designing Mod-7 counter Therefore, N= 7 and number of Flip flops or bits (m) required is, for m =3, 7<=8, which is TRUE.

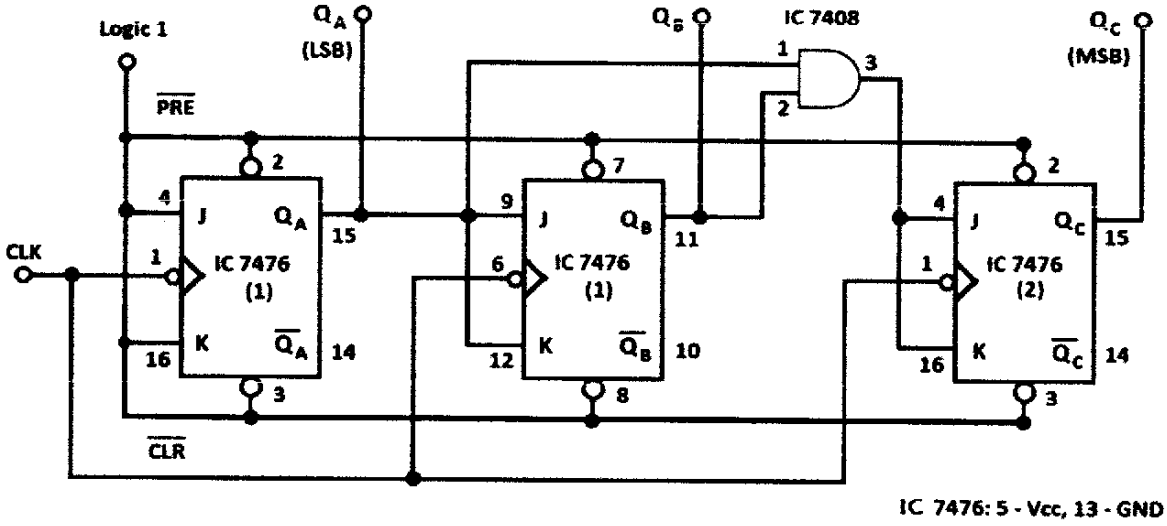
3-bit Synchronous up counter:

The up-counter counts from 0 to7 (000 - 111) for this MS JK flip flop IC 74LS76 is used, 2 MS J-K flip flops are available. It is observed that the AND gate inputs are fed by the non-complement outputs of FFA and FFB. The clock pulse is given at pin 1 & 6 of the 1st IC & pin 1 of 2nd IC, respectively to apply clock to all flip flop at a time.

3-bit Synchronous down counter:

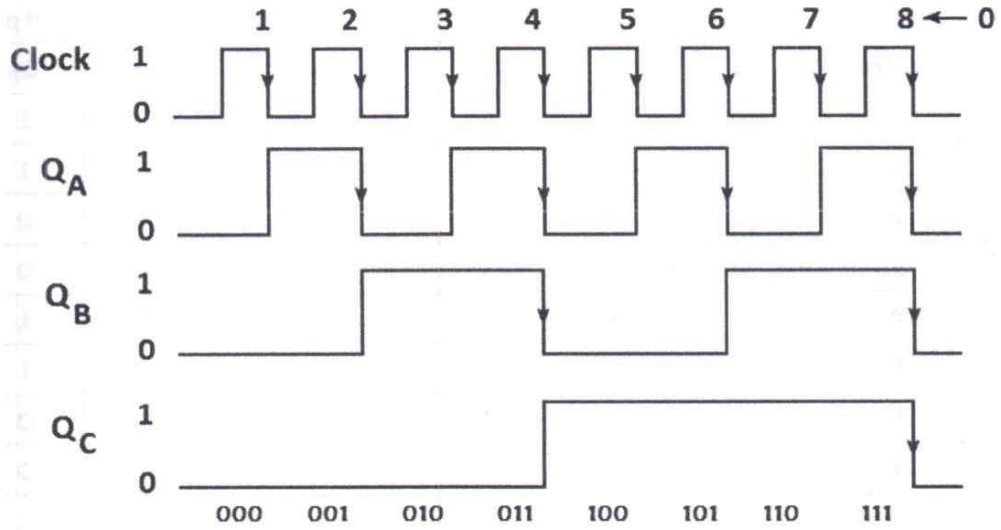
This is used to count from 7 to 0 (111-000) for this also 2 IC's of 74LS76 are required & hence we use 3 MS JK flip flops. It is observed that the AND gate inputs are fed by the complement outputs of FFA and FFB. The clock pulse is given at pin 1 & 6 of the 1st IC & pin 1 of 2nd IC, respectively to apply clock to all flip flop at a time.

UP COUNTER CIRCUIT DIAGRAM:

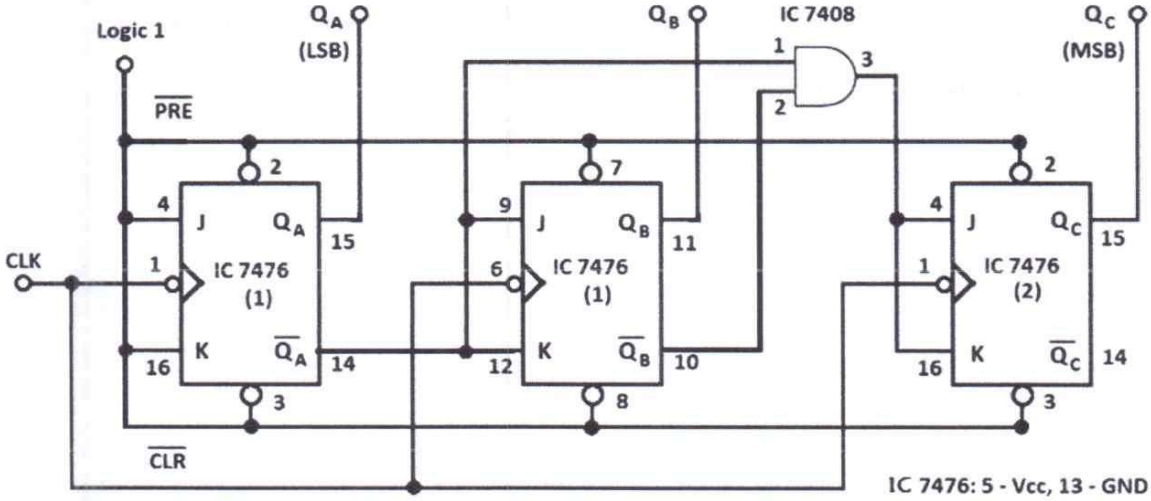


OUTPUT WAVEFORMS:

Timing Diagram:



DOWN COUNTER CIRCUIT DIAGRAM



Observation Table:

Up Counter

Clock Input	Output		
Count	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Down Counter

Clock Input	Output		
Count	Q_C	Q_B	Q_A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

PROCEDURE:

1. Connect the circuit as shown in the diagram.
2. Connect PRE $\overline{\quad\quad}$ input to the logic 1 (+5V).
3. Connect CLR $\overline{\quad\quad}$ input to the logic 0 (0V) or ground to reset counter.
4. Connect CLR $\overline{\quad\quad}$ input to the logic 1.
5. Apply the clock pulse to CLK input.
6. Observe the output and verify the observation table.

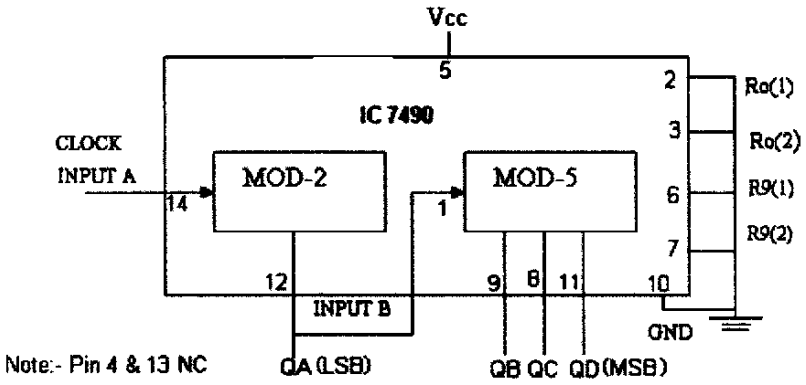
(b) Mod-N counter using IC7490/7476

THEORY:

If N=10, it is said to be a decade counter (MOD-10 counter). Its operation is as follows:

1. The output of MOD-2 is externally connected to the input B which is the clock input of the internalMOD-5 counter.
2. Hence QA toggles on every falling edge of clock input whereas the output QD, QC, QB of the MOD-5 counterwill increment from 000 to 100 on low going change of QA output.
3. Due to cascading of MOD-2 and MOD-5 counter, the overall configuration becomes a MOD-10.
4. The reset inputs Ro(1), Ro(2) and preset inputs R9(1), R9(2) are connected to ground so as to makcit inactivc.

Mod-10 Counter



OBSERVATION TABLE:

CLK	Count	O/p of MOD-5			O/p of MOD-2
		QD	QC	QB	QA
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1

(C) Synchronous Counter Using IC 74192

OBJECTIVE: Students should be able to realize synchronous counter using IC74192

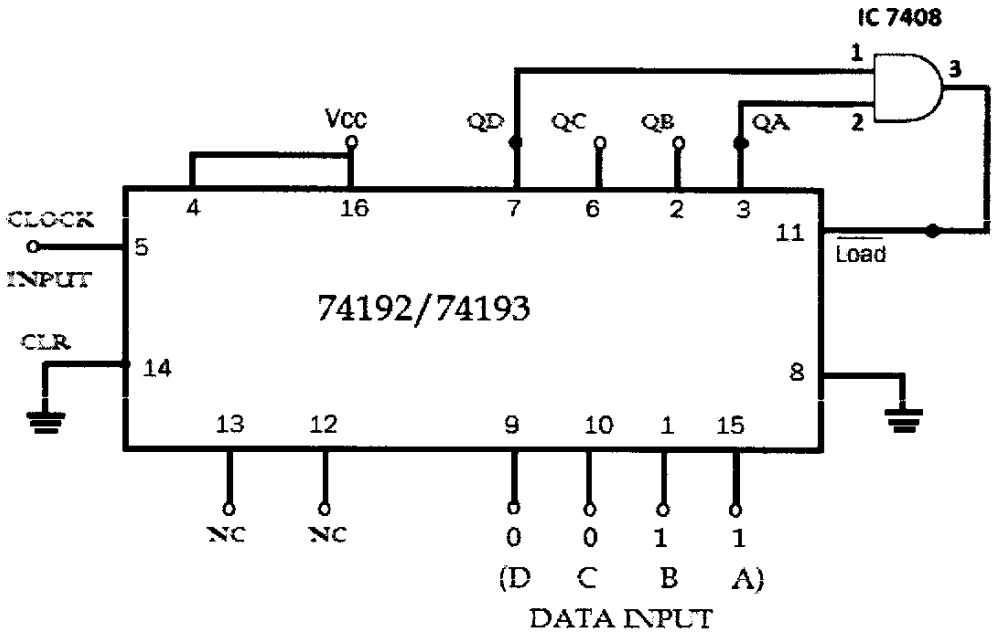
THEORY:

A 74192 IC is a pre-settable synchronous 4-bit Up/Down decimal counter, capable of reset to zero, preloading with a specified value, as well as generating carry and borrow signals that allow one to construct multi-digit counters. The result of the synchronization is that all the individual output bits of each FF changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

PROCEDURE:

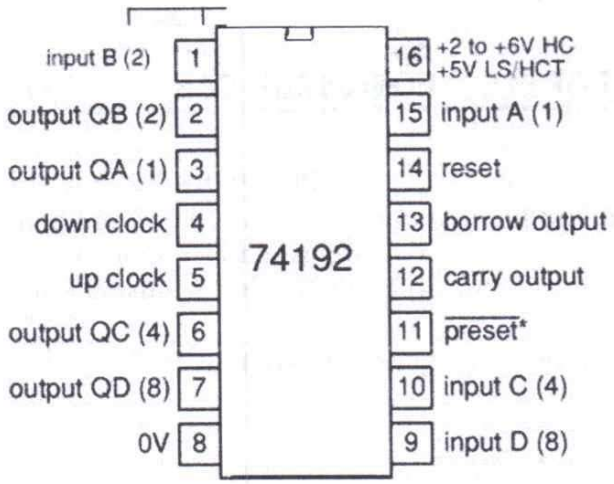
1. Check all the components for their working.
2. Make connections as shown in the circuit diagram.
3. Clock pulses are applied one by one at the clock input and output is observed at QA, QB, QC & QD.
4. Verify the Truth Table from the outputs.

CIRCUIT DIAGRAM: COUNT UP FROM 3 TO 8



OBSERVATION TABLE:

PIN DIAGRAM



RESULT: The functioning of MOD-7using JK FF, MOD-10 using IC 7490 & Synchronous counter using IC74192 are verified.

Experiment No: 9

Design and test the second order Active Filters and plot the frequency response,
i) Low pass and Highpass Filter
ii) Bandpass and Bandstop Filter

9i. Design and test the second order Active Low Pass Filters and plot the frequency response

AIM: To design and obtain the frequency response of the second order Butterworth active low pass filter.

DESIGN STEPS:

1. Choose cut-off frequency $f_c = f_H$.
2. Assume capacitor value C less than or equal to 1uF and calculate R.
3. Calculate the value of Resistance (R) using the formula,

$$R = \frac{1}{2\pi f_c C}$$

$$R = R_2 = R_3$$

4. From the filter circuit analysis, the gain formula is

$$AF = 1 + \frac{R_F}{R_1}$$

where, AF = Gain of Butterworth filter circuit.
Let us assume AF = 1.586 (For Butterworth filter) and using the above equation of gain,

$$1.586 = 1 + \frac{R_F}{R_1}$$

$$R_F = 0.586R_1$$

5. Assume value of R_1 which should be less than 100 KΩ (standard value 27 KΩ) and calculate R_F.

DESIGN WORK:

1. Let us assume the cut-off frequency $f_c = f_H = 10$ KHz.
2. Let us assume the capacitor value C = 0.001uF (which is less than 1uF).
3. Calculate the value of Resistance (R) using the formula,

$$R = \frac{1}{2\pi f_c C}$$

$$R = \frac{1}{2\pi * (10 * 10^3) * (0.001 * 10^{-6})}$$

$$R = R_2 = R_3 = 15.91 \text{ K}\Omega$$

4. Let us assume value of $R_1 = 27$ KΩ (which should be less than 100 KΩ) and substitute it in

$$R_F = 0.586R_1$$

$R_F = 0.586 * 27$ KΩ = 15.822 KΩ (Use 0-22 KΩ pot)

COMPONENTS REQUIRED:

Sl. No	Components	Specification	Quantity
1	Op-Amp	μA-741	1
2	Resistor	15.91 KΩ, 27 KΩ, 10 KΩ, 15.822 KΩ	2, 1, 1, 1(pot of range 0-22 KΩ)
3	Capacitor	0.001 uF	2
4	Bread board	-	1
5	Connecting wire	-	Few

EQUIPMENT REQUIRED:

Sl. No.	Equipment	Specification	Quantity
1	CRO	0-40MHz	01
2	Signal Generator	0-1 MHz	01
3	DC dual Power Supply	±12V	01

CIRCUIT DIAGRAM:

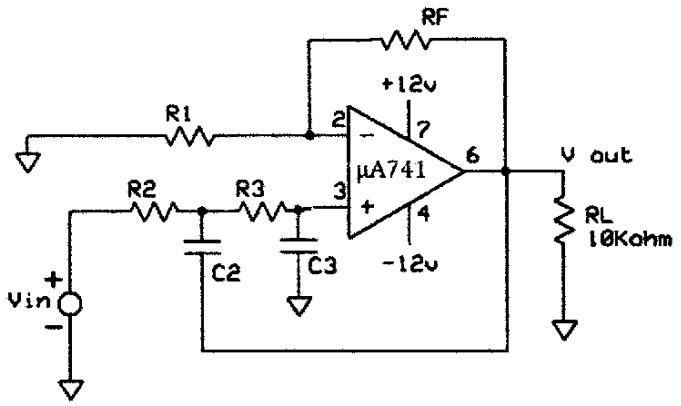


Figure: Circuit diagram of second order active Butterworth LPF

PROCEDURE:

1. Rig – up the circuit as shown in Fig. 1a. $\frac{AF}{\sqrt{2}}$
2. Apply the input voltage Vin =5Vpp
3. Vary the frequency range in appropriate range and note down the output voltage Vo.
4. Calculate gain by using the equation,

   Voltage gain= 20log ($\frac{V_o}{V_{in}}$) dB

TABULATION:

V_{in} (P-P) =_____Volts (Constant)

Sl. No	Frequency in HZ	Vo in Volts	$\frac{Vo}{Vin}$	AF = 20log ($\frac{Vo}{Vin}$)in dB

NATURE OF GRAPH:

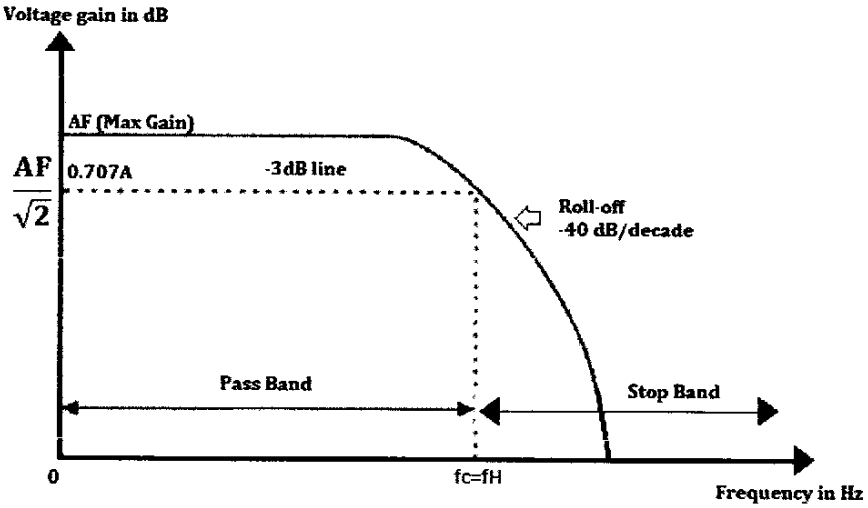


Figure: Frequency response of LPF

CONCLUSION:

Design and test the second order Active High Pass Filters and plot the frequency response

AIM: To design and obtain the frequency domain response of a second order Butterworth active high pass filter.

DESIGN STEPS:

1. Choose cut-off frequency $f_c=f_L$.
2. Assume capacitor value C less than or equal to 1uF and calculate R.
3. Calculate the value of Resistance (R) using the formula,

$$R = \frac{1}{2\pi f_c C}$$

$$R = R_2 = R_3$$

4. From the filter circuit analysis, the gain formula is,

$$AF = 1 + \frac{R_F}{R_1}$$

where, AF = Gain of Butterworth filter circuit.

Let us assume AF = 1.586 (For Butterworth filter) and using the above equation of gain,

$$1.586 = 1 + \frac{R_F}{R_1}$$

$$R_F = 0.586R_1$$

5. Assume value of R_1 which should be less than 100 KΩ (standard value 27 KΩ) and calculate R_F.

DESIGN WORK:

1. Let us assume the cut-off frequency $f_c = f_L = 10$ KHz.
2. Let us assume the capacitor value C = 0.001uF (which is less than 1uF).
3. Calculate the value of Resistance (R) using the formula,

$$R = \frac{1}{2\pi f_c C}$$

$$R = \frac{1}{2\pi*(10*10^3)*(0.001*10^{-6})}$$

$$R = R_2 = R_3 = 15.91\ K\Omega$$

4. Let us assume value of $R_1 = 27$ KΩ (which should be less than 100 KΩ) and substitute it in

$$R_F = 0.586R_1$$

$R_F = 0.586*27$ KΩ = 15.822 KΩ (Use 0-22 KΩ pot)

COMPONENTS REQUIRED:

Sl. No	Components	Specification	Quantity
1	Op-Amp	μA-741	1
2	Resistor	15.91 KΩ, 27 KΩ, 10 KΩ, 15.822 KΩ	2, 1, 1, 1(pot of range 0-22 KΩ)
3	Capacitor	0.001 uF	2
4	Bread board	-	1
5	Connecting wire	-	Few

EQUIPMENT REQUIRED:

Sl. No	Equipment	Specification	Quantity
1	CRO	0-40MHz	01
2	Signal Generator	0-1 MHz	01
3	DC dual Power Supply	±12V	01

CIRCUIT DIAGRAM:

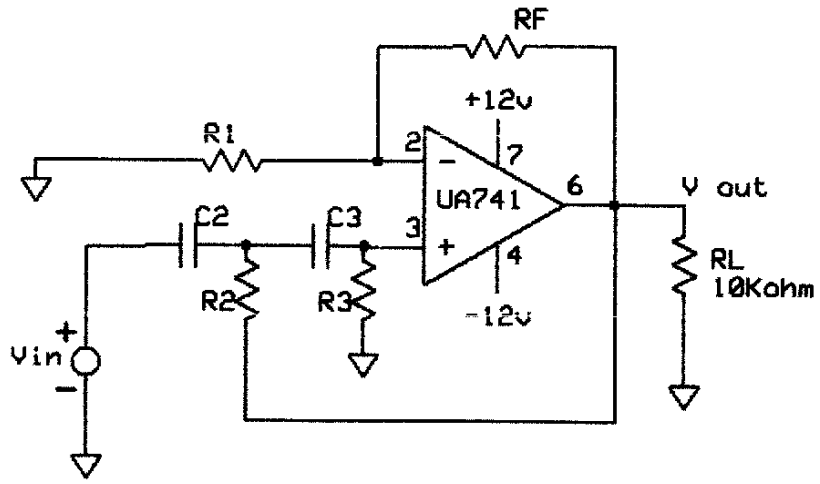


Figure: Circuit diagram of second order active Butterworth HPF

PROCEDURE:

1. Rig – up the circuit as shown in the circuit diagram.
2. Apply the input voltage V_{in}.
3. Vary the frequency range and note down the output voltage.
4. Calculate gain by using given equation,

   Voltage gain= 20log ($\frac{Vo}{Vin}$) in dB

TABULATION:

V_{in} (P-P) =_____Volts (Constant)

Sl. No	Frequency in HZ	Vo in Volts	$\frac{Vo}{Vin}$	AF = 20log ($\frac{Vo}{Vin}$)in dB

NATURE OF GRAPH:

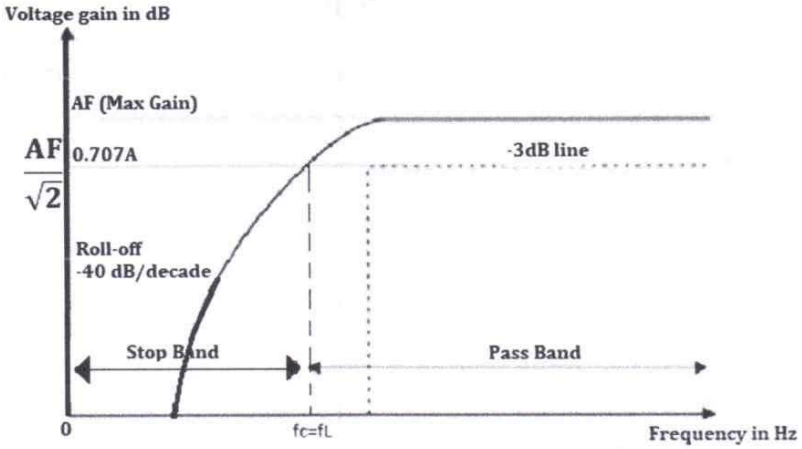


Figure: Frequency response of HPF

CONCLUSION:

9ii) Design and test the second order Active Band Pass Filters and plot the frequency response

AIM: To design an active second order Band pass filter for the given specifications. Conduct an experiment to draw the frequency response graph and verify the design specifications.

DESIGN STEPS:

1. Choose cut-off frequency f_L= 4.6kHz; f_v=5.6kHz.
2. Assume the midband gain A_F=1.
3. Calculate the value of Quality factor (Q) using the formula,

$$Q = \frac{f_c}{\Delta f}$$

f_c is the Centre frequency, Δf is Bandwidth.

where, $f_c = \sqrt{f_L f_v}$ =5kHz

$\Delta f = f_V - f_L$=1kHz

4. Choose C_1=C_2=C=0.01F
5. Resistance values R_1, R_2, and R_f are calculated as follows-

$$R_1 = \frac{Q}{2\pi f_c C A_F} = 0.1591 / \Delta f$$

$$R_2 = \frac{Q}{2\pi f_c C[2Q^2 - A_F]} = R_1 / 2Q^2\text{-}1$$

$$R_f = \frac{Q}{\pi f_c C} = R_f = 2R1$$

R_1 = 15.91KΩ

R_2 = 306.12KΩ

R_f = 30KΩ

COMPONENTS REQUIRED:

Sl. No	Components	Specification	Quantity
1	Op-Amp	μA-741	1
2	Resistor	15.91 KΩ, 306.12 KΩ, 30 KΩ	1, 1, 1
3	Capacitor	0.001 uF	2
4	Bread board	-	1
5	Connecting wire	-	Few

EQUIPMENT REQUIRED:

Sl. No	Equipment	Specification	Quantity
1	CRO	0-40MHz	01
2	Signal Generator	0-1 MHz	01
3	DC dual Power Supply	±12V	01

CIRCUIT DIAGRAM:

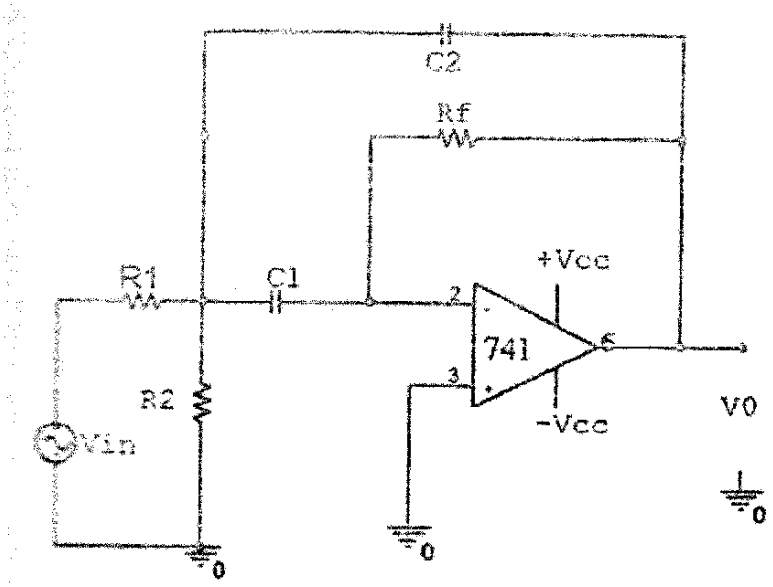


Figure: Circuit diagram of second order active Bandpass filter

PROCEDURE:

1. Make connections as shown in the circuit diagram.
2. Apply the sinusoidal I/P signal of frequency, the filter mid – frequency and amplitude of 1V, (P-P) or any other convenient value (10 V) so that the O/P is undistorted and measure the O/P voltage (P – P). Record this as V_{Max}.
3. Keeping the input signal amplitude constant, decrease the frequency until the O/P voltage reduces to $0.707V_{Max}$. The frequency at which this happens is your f_{c1}, the lower cutoff frequency of the filter.
4. Repeat step 3 but now increase the frequency until the O/P voltage reduces to $0.707V_{Max}$. The frequency at which this happens is your fc2, the upper cutoff frequency of the filter.
5. Keeping the I/P signal amplitude constant at a convenient value, measure and record at least 6 readings below and 6 readings above the filter mid – frequency, fm. (Note: Whenever you change the frequency button /setting, you should check and adjust the I/P to its previous constant value)
6. Plot the graph of Gain in dB V/S frequency.
7. Identify the 3dB points on your graph and identify the mid - frequency. Mark all the salient points on your graph.

TABULATION:

V_{in} (P-P) =_____Volts (Constant)

Sl. No	Frequency in HZ	Vo in Volts	$\frac{Vo}{Vin}$	AF = 20log ($\frac{Vo}{Vin}$)in dB

NATURE OF GRAPH:

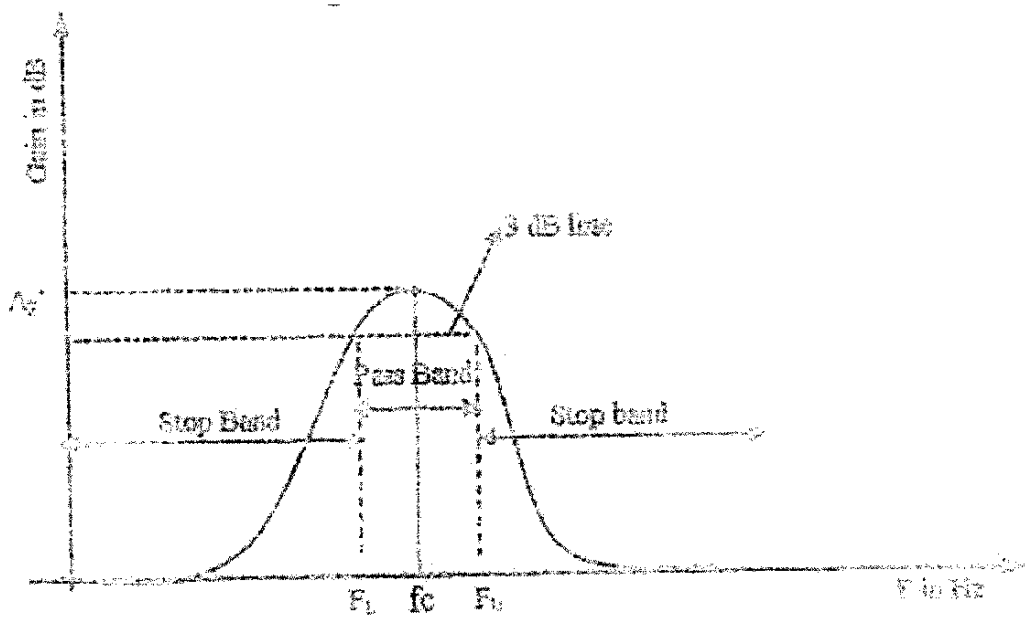


Figure: Frequency response of BPF

CONCLUSION:

Design and test the second order Active Band Stop Filter and plot the frequency response

AIM: To design an active second order Band Stop filter for the given specifications. Conduct an experiment to draw the frequency response graph and verify the design specifications.

DESIGN STEPS:

1. Choose cut-off frequency f_L= 4.6kHz; f_v=5.6kHz.
2. Assume the midband gain A_F=1.
3. Calculate the value of Quality factor (Q) using the formula,

$$Q = \frac{f_c}{\Delta f}$$

f_c is the Centre frequency, Δf is Bandwidth.

where, $f_c = \sqrt{f_L f_v}$ =5kHz

$\Delta f = f_V - f_L$=1kHz

4. Choose C_1=C_2=C=0.01F
5. Resistance values R_1, R_2, and R_f are calculated as follows-

$$R_1 = \frac{Q}{2\pi f_c C A_F} = 0.1591 / \Delta f$$

$$R_2 = \frac{Q}{2\pi f_c C[2Q^2 - A_F]} = R_1 / 2Q^2\text{-}1$$

$$R_f = \frac{Q}{\pi f_c C} = R_f = 2R1$$

R_1 = 15.91KΩ

R_2 = 306.12KΩ

R_f = 30KΩ

COMPONENTS REQUIRED:

Sl. No	Components	Specification	Quantity
1	Op-Amp	μA-741	2
2	Resistor	15.91 KΩ, 306.12 KΩ, 30 KΩ, 10 KΩ	1, 1, 1, 2
3	Capacitor	0.001 uF	2
4	Bread board	-	1
5	Connecting wire	-	Few

EQUIPMENT REQUIRED:

Sl. No	Equipment	Specification	Quantity
1	CRO	0-40MHz	01
2	Signal Generator	0-1 MHz	01
3	DC dual Power Supply	±12V	01

CIRCUIT DIAGRAM:

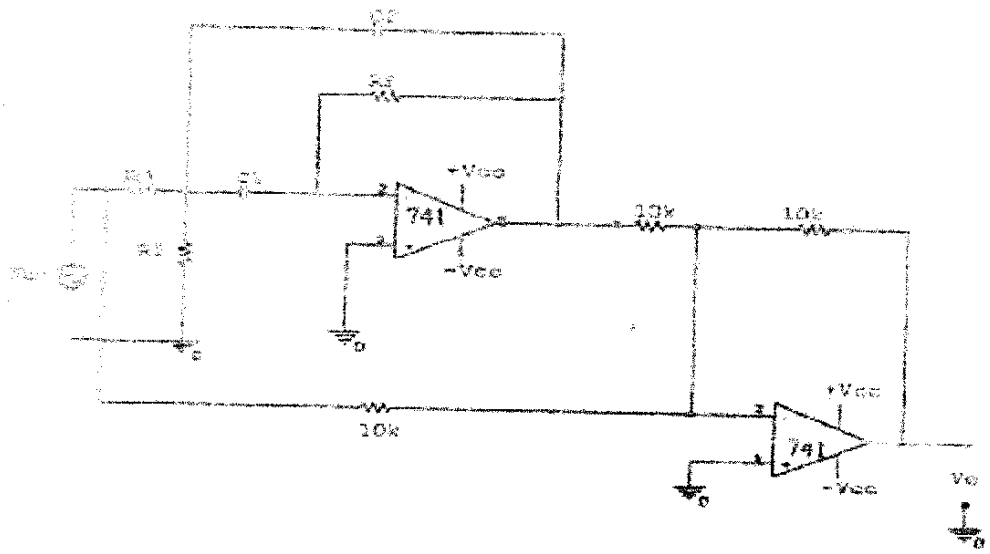


Figure: Circuit diagram of second order active Band Stop filter

PROCEDURE:

1. Make connections as shown in the circuit diagram.
2. Apply the sinusoidal I/P signal of frequency f_m /10, one tenth of the filter mid – frequency and amplitude 1V, (P-P) or any other convenient value (10V or less) so that the O/P is undistorted and measure the O/P voltage (P – P).
3. Keeping the input signal amplitude constant, increase the frequency until the O/P voltage reduces to a minimum value, V_{Min}. The frequency at which this happens is your mid-frequency, f_m.
4. Now increase the frequency until the O/P voltage approaches a constant value. Now you are in the pass band.
5. You can identify the frequencies f_L and f_H as you did in LPF/HPF
6. Keeping the I/P signal amplitude constant at a convenient value, measure and record at least 6 readings below and 6 readings above the filter mid – frequency, f_m. (Note: Whenever you change the frequency button /setting, you should check and adjust the I/P to its previous constant value)
7. Plot the graph of Gain in dB V/S frequency.
8. Identify the 3dB points on your graph and identify the mid - frequency. Mark all the salient points on your graph.

TABULATION:

V_{in} (P-P) =_____Volts (Constant)

Sl. No	Frequency in HZ	Vo in Volts	$\frac{Vo}{Vin}$	AF = 20log ($\frac{Vo}{Vin}$)in dB

NATURE OF GRAPH:

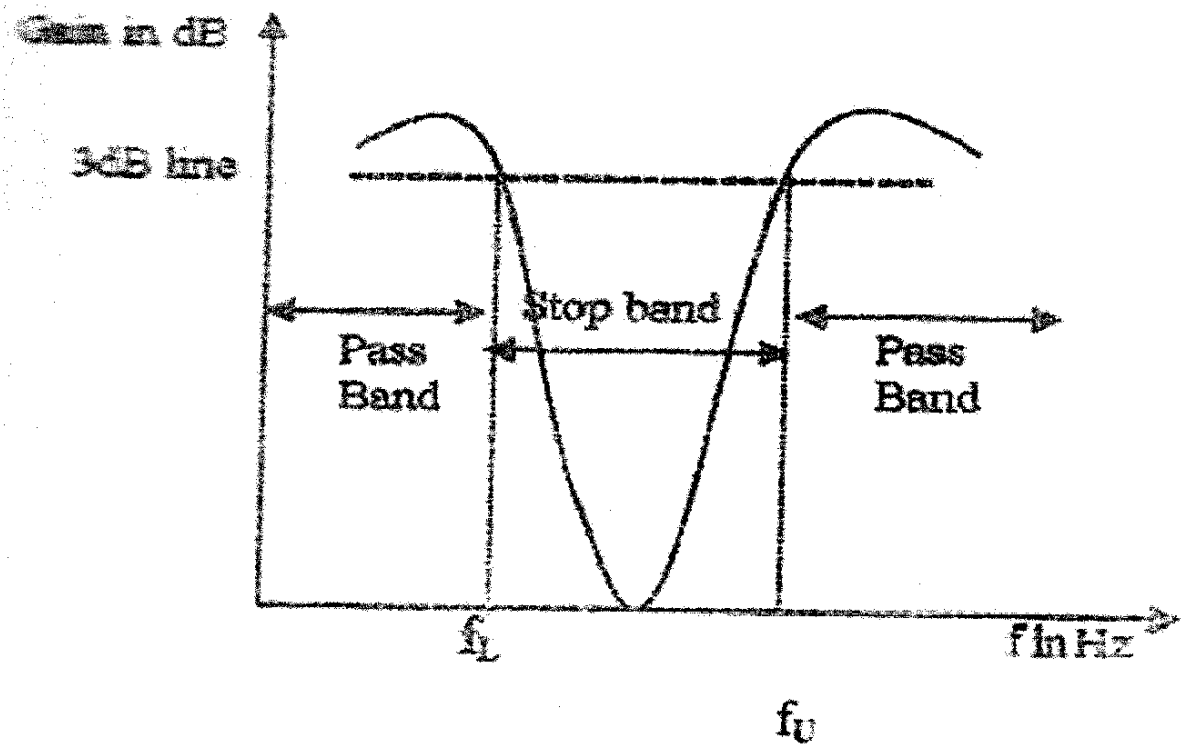


Figure: Frequency response of Band Stop Filter

CONCLUSION:

Experiment No: 10
Design and test the following using 555 timer i) Monostable Multivibrator and ii) Astable Multivibrator

AIM: Design and test Monostable multivibrator using IC 555 timer.

OBJECTIVE: To dcsign and analyse the operation of a monostable multivibrator using 555 IC timer.

COMPONENTS AND EQUIPMENT'S REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	1
2	CRO: 20MHz	1
3	IC 555 timer	1
4	Diode: IN4007	1
4	Resistors: 1 KΩ, 10 KΩ pot, 22KΩ, 33KΩ	1 each
5	Capacitors: 0.047 μF, 0.01 μF, 0.1 μF	2, 1,1
6	Signal generator	1
7	Bread board	1
8	CRO Probes and connecting wires	Few

THEORY:

Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. Timer IC 555 is also used as one shot or monostable operation. Since there are many real-life applications where many applications needs to operate for only specific time interval for such application one shot or monostable operation is suitable. When negative going pulse is applied to pin 2 which leads to output pin 3 goes to high. The negative edge of the trigger pulse causes the internal comparator 2 trigger the flip flops leads to output high at pin 3. The voltage across capacitor rises to 2VCC/3 through supply and resistor R1. When the voltage across capacitor reaches to 2VCC/3 the internal comparator 1 triggers the flip flop from and which send the output from high to low. Figure shows the waveforms associated with the operation of the IC 555 as a monostable. The output waveform shows that the wide range from microsecond to many seconds can be possible with appropriate values of R and C. This flexibility of time period makes IC 555 versatile for many real-life applications. The time period is given by Tp = 1.1 RC.

DESIGN:

Output pulse width (T) = Delay time is given by

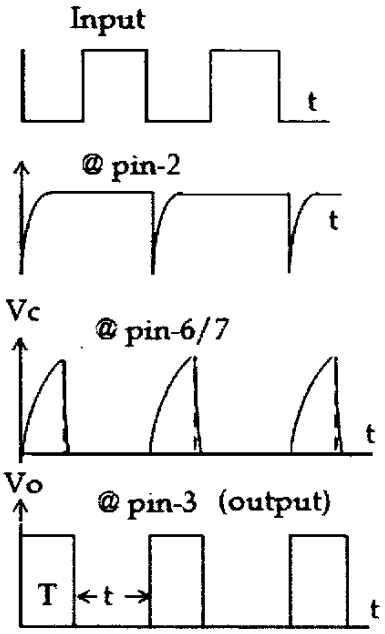
$T = 1.1\ R\ C$ ..... (1)

Let T = 1ms; C = 0.1μF

$$R = \frac{T}{1.1C} = \frac{1x10^{-3}}{1.1x0.1x10^{-6}} = 9.09K\Omega$$

Therefore, R = 10KΩ (std)

Apply input square-wave signal from the signal generator of f = 1KHz (T = 1ms) and V_{pp} =5V



CIRCUIT DIAGRAM:

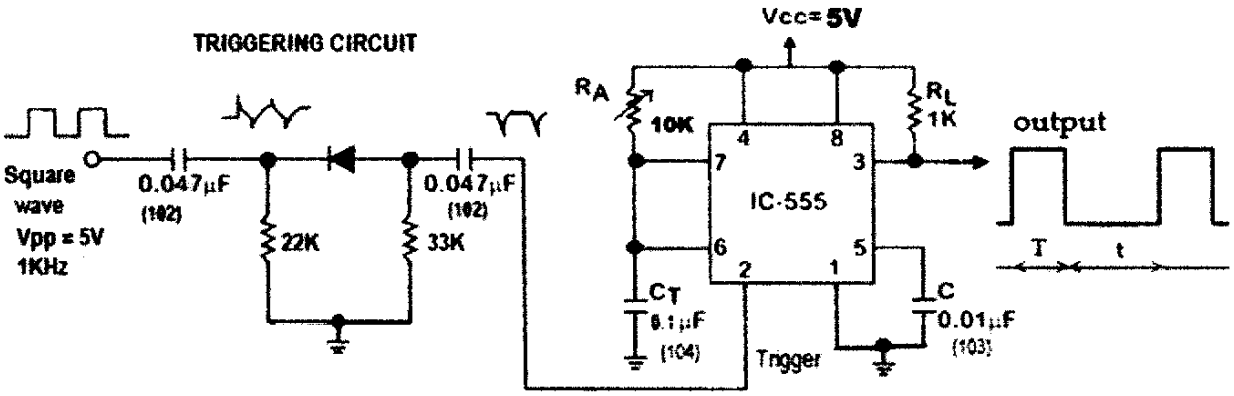


Figure: Monostable multivibrator

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Setup negative triggering using triggering circuit & it is applied at the terminal 2 of IC 555.
3. Observe the output waveforms and measure the output voltage (VO) and voltage across capacitor (V_c). Calculate the theoretical values of above measured parameters.
4. Theoretically the time period (T) is calculated by $T=1.1R_1C_1$ where R_1 =10KΩ C_1=0.1μF.
5. Practical and theoretical charging and discharging timers are measured.
6. Plot the wave forms as per the scale.

TABULATION:

Parameter	Theoretical	Practical
T (ms)	1 m sec	
t (ms)	6 m sec	

RESULT:

Monostable multivibrator using timer IC 555 is designed, setup and the waveforms are obtained.

ASTABLE MULTIVIBRATOR

AIM: To design and setup Astable multivibrator using IC 555 timer.

OBJECTIVE: To design and analyse the operation of a of Astable multivibrator using 555 timer IC.

COMPONENTS AND EQUIPMENT'S REQUIRED:

Sl. No.	Component Name	Quantity
1	Power supply: 0-30V	1
2	CRO: 20MHz	1
3	IC 555 timer	1
4	Diode: IN4007	2
5	Resistors: 1 KΩ, 10 KΩ pot, 2.2 KΩ	2, 1, 1
6	Capacitors: 0.047 μF, 0.01 μF	1 each
7	Bread board	1
8	CRO Probes and connecting wires	Few

THEORY:

The capacitor charges through resistors R_A and R_B the voltage across capacitor rises to $2V_{CC}/3$. This voltage acts as a threshold voltage at pin 6 which is input to internal comparator which finally trigger the internal flip flop so that output pin 3 goes low. Also flip flop drives the internal discharge transistor to ON allowing capacitor to get discharge from R_B this lead to decrease in capacitor voltage to $V_{CC}/3$ and the flip flop get trigger and discharge transistors gets off and output set to high. This leads to charging of capacitor through R_A and R_B to V_{CC}. A diode D_1 is connected between the discharge and threshold terminals (as also across R_B). Thus, the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through R_B. Another optional diode D_2 is also connected in series with R_B in reverse direction for better shorting of R_B.

DESIGN:

The time for charging C from 1/3 to 2/3 Vcc = ON Time = $0.693\ (R_A + R_B)\ C$

The time for discharging C from 2/3 to 1/3 Vcc = OFF Time = $0.693\ R_B\ C$ $f_{osc} = 1/\ T_{osc} = 1.44/(R_A + R_B)C$

Duty Cycle = $R_A/\ (R_A + R_B)$

Min. Duty Cycle = $R_1/(R_1 + RX + R_2)$ Max. Duty Cycle = $(R_1 + RX)/(R_1 + RX + R_2)$

To vary the duty cycle from about 0 to 100%, a potentiometer, RX, is used. Thus, a variable duty cycle is achieved.

CIRCUIT DIGRAM & WAVEFORMS:

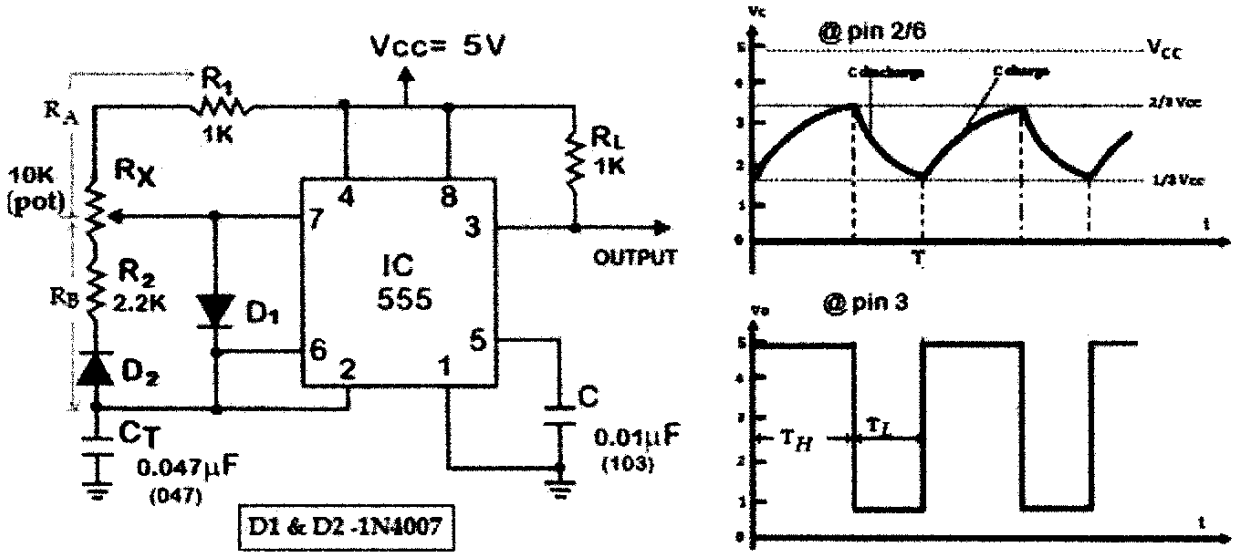


Figure: Astable Multivibrator and waveforms

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Set the DC power supply to provide V_{CC}=5V.
3. Connect output pin (3) of 555 to channel 1 of CRO and pin (2/6) to channel 2 of CRO.
4. Observe the output waveforms and measure the output voltage (V_O) and voltage across capacitor (V_c). Calculate the theoretical values of above measured parameters.
5. Plot the output voltage waveforms for output voltage and voltage across capacitor. Frequency, f= $1.45/ (R_A+2R_B)C$ and % of Duty cycle = $(T_H/ (T_H+T_L))*100$
6. Practically T_L and T_H are measured, and theoretical values are verified with practical values.

TABULATION:

T_H (ms)		T_L (ms)		T (ms)		F (Hz)		Duty Cycle
Theoretical	Practical	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical	
								60%
								50%
								40%

RESULT:

Astable multivibrator using timer IC 555 is designed, setup and the waveforms are obtained.

Experiment No: 11
Design and Test a Regulated Power supply

AIM: Design and test a regulated power supply.

OBJECTIVES:

1. To understand the working of Zener diode.
2. To understand the working of Regulated power supply.

COMPONENTS REQUIRED:

1. Diode: IN4007
2. Resistance: 10Ω
3. Zener diode:
4. Capacitor: 0.01μF
5. Multimeter

CIRCUITDIAGRAM:

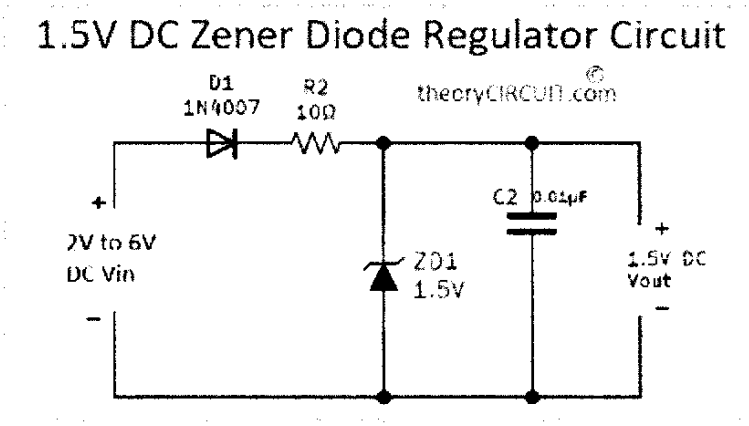


Figure 11a: Circuit diagram of 1.5V DC Regulated Power Supply

THEORY:

The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum I_Z (min) value in the reverse breakdown region. It permits current to flow in the forward direction as normal but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the Zener voltage. The Zener diode is specially made to have a reverse voltage breakdown at a specific voltage. Its characteristics are otherwise very similar to common diodes. In breakdown the voltage across the Zener diode is close to constant over a wide range of currents thus making it useful as a shunt voltage regulator.

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current. A typical Zener diode shunt regulator is shown in Figure 3. The resistor is selected so that when the input voltage is at V_{IN} (min) and the load current is at I_L (max) that the current through the Zener diode is at least Iz(min). Then for all other combinations of input voltage and load current the Zener diode conducts the excess current thus maintaining a constant voltage across the load. The Zener conducts the least current when the load current is the highest and it conducts the most current when the load current is the lowest.

PROCEDURE:

1. Rig up the circuit as per the given circuit diagram.
2. Switch on the power supply.
3. Observe the regulated output using multimeter.

CONCLUSION:

Experiment No: 12

Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker

AIM: Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.

OBJECTIVES:

1. To understand the working of microphone
2. To understand the response of audio amplifiers

COMPONENTS REQUIRED:

1. LM386
2. 10uF / 16V capacitor
3. 470uF / 16V
4. 0.047uF / 16V Polystar Flim Capacitor
5. 10R ¼ Watt
6. 12V Power Supply unit
7. 8 Ohms / .5 Watt Speaker
8. Capsule or Electret Microphone
9. 0.1uF capacitor
10. 10k 1/4th Watt Resistor
11. Bread Board
12. Hook up wires

CIRCUIT DIAGRAM

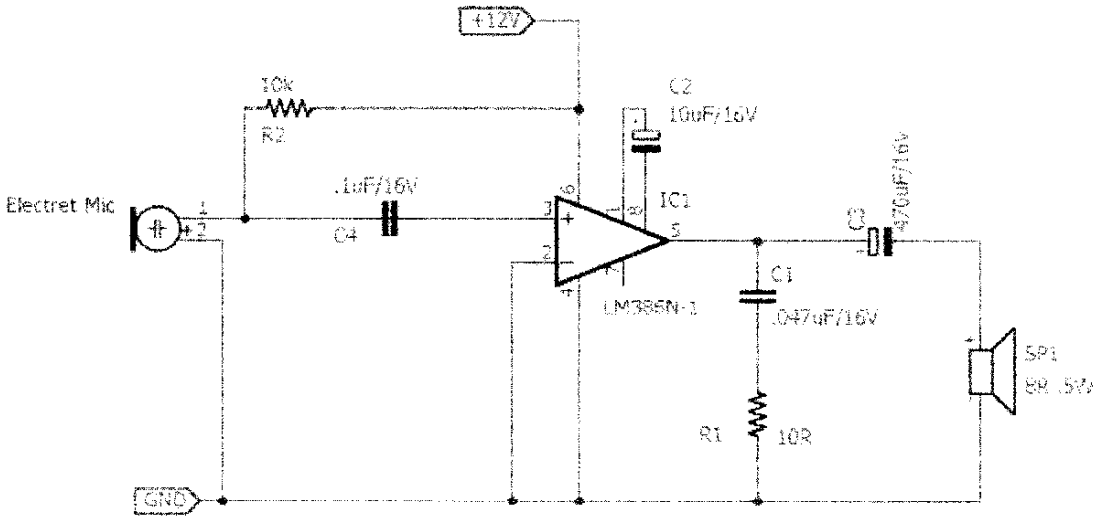


Figure 12a: Audio Amplifier Circuit

THEORY:

In the circuit diagram, the Amplifier is shown with the respective pin diagrams. The amplifier will provide 200x gain at output depending on the input. The 10uF capacitor across pin 1 and pin 8 is responsible for the 200x gain of the amplifier. We did not change the gain of the amplifier in our circuit construction. Also, the 250uF capacitor is connected across the Speaker. We have changed the value and used 470uF instead of 250uF capacitor. There is a 0.05uF capacitor along with a 10R resistor. This RC combination is called snubber or clamp circuit which protects the amplifier from back EMF, produced by the speaker. We used a common but close value of 0.047uF instead of 0.05uF. Other circuitry and connections remain the same in our construction.

Also, the power amplifier can drive a wide range of loads, from 4 Ohms to 32 Ohms and can be powered using 5V to 12V. We need to be careful about this rating otherwise we could damage the power amplifier or the output speaker.

PROCEDURE:

1. Rig up the circuit as per the given circuit diagram.
2. Switch on the D.C. power supply
3. Provide voice input.
4. Observe the amplified voice output.

CONCLUSION:

Experiment No: 13
Virtual Lab

AIM: To study astable and monostable multivibrator using IC 555.

LINK: https://ae-iitr.vlabs.ac.in/exp/astable-monostable-multivibrator/

THEORY: A multivibrator is a one type of electronic circuit, that is used to implement a two state system like flip-flops, timers and oscillators. Multivibrators are categorized by two amplifying devices like electron tubes, transistors and other devices like capacitors and cross coupled by resistors. Multivibrators are classified into three types based on the circuit operation, namely Astable multivibrators, Bistable multivibrators and Monostable multivibrators. The astable multivibrator is not stable and it repeatedly switches from one state to the other. In monostable multivibrator, one state is stable and remaining state is unstable. A trigger pulse is the root to the circuit to enter the unstable state. When the circuit enters into the unstable state, then it will return to the normal state after a fixed time. A bistable mutivibrator circuit is stable that can be changed from one stable to other stable by an external trigger pulse. This multivibrator circuit is also called as flip-flop which can be used to store one bit of data.

CIRCUIT CONNECTIONS OF MONOSTABLE MULTIVIBRATOR WITH 555 TIMER:

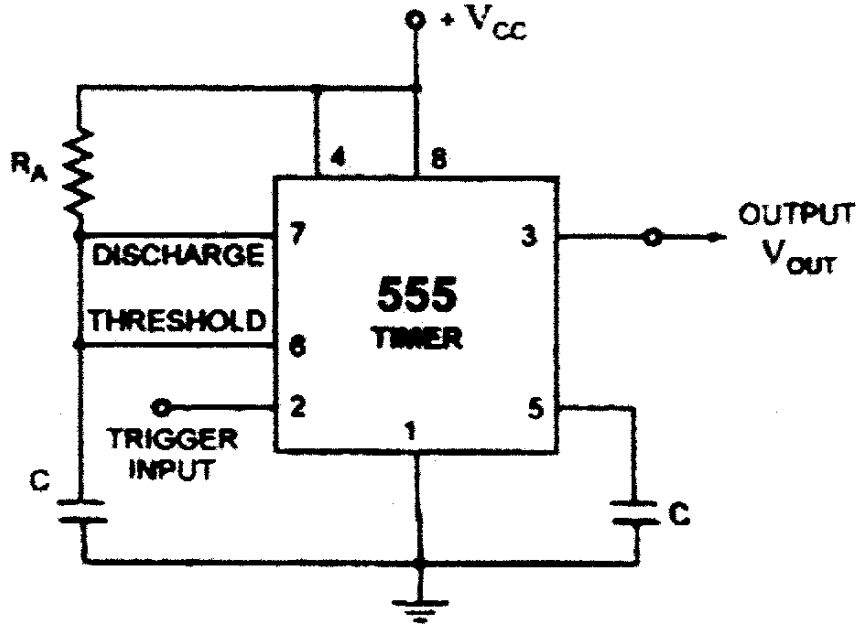
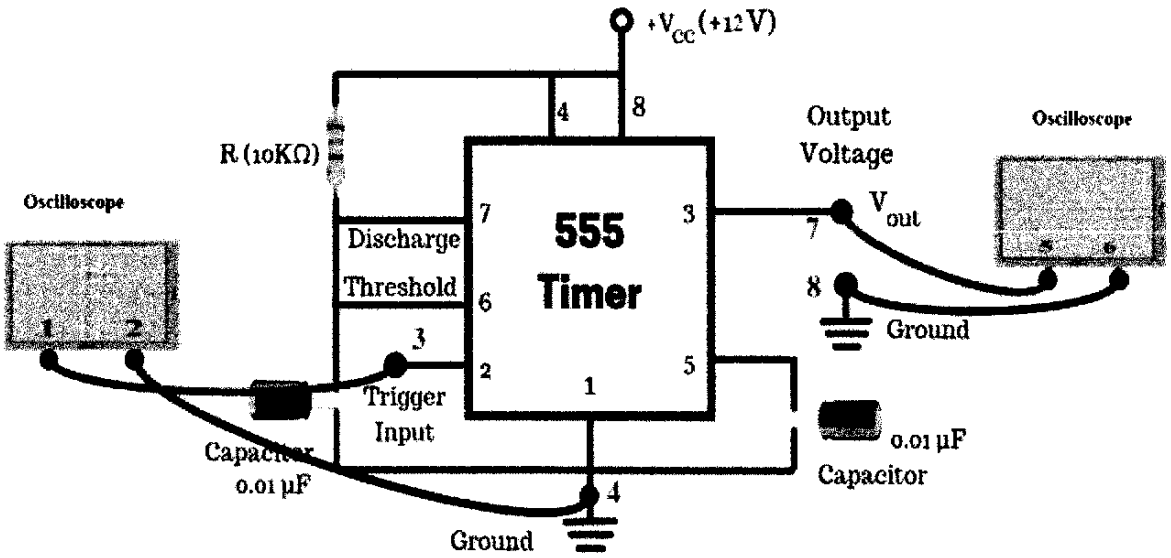


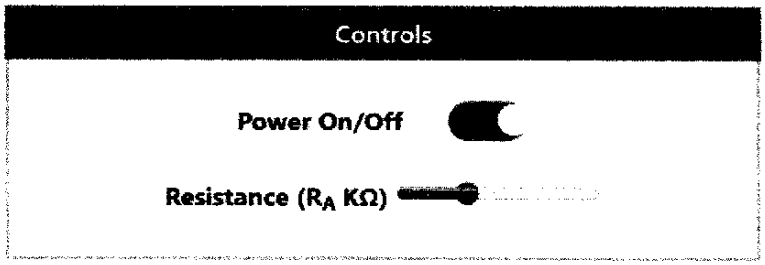
Figure 13a: Monostable Mutivibrator using 555 IC Timer

PROCEDURE:

1. In the above circuit, the pin1 is connected to the ground and the trigger input is given to the pin2.
2. In inactive condition of o/p, this i/p is kept at +VCC. To get transition of the output from a stable state to unstable state, a negative going pulse of narrow width and amplitude of greater than +2/3 VCC is applied to pin2.
3. The o/p is taken from pin3 and pin4 is connected to +VCC to avoid accidental reset. Pin5 is connected to the ground via a 0.01uF capacitor to avoid noise. Pin6 and pin7 are shorted and a resistor is connected between pins 6 and 8.
4. A discharge capacitor is connected to pin7 while pin8 is connected to VCC.

SIMULATION IN VIRTUAL LAB:



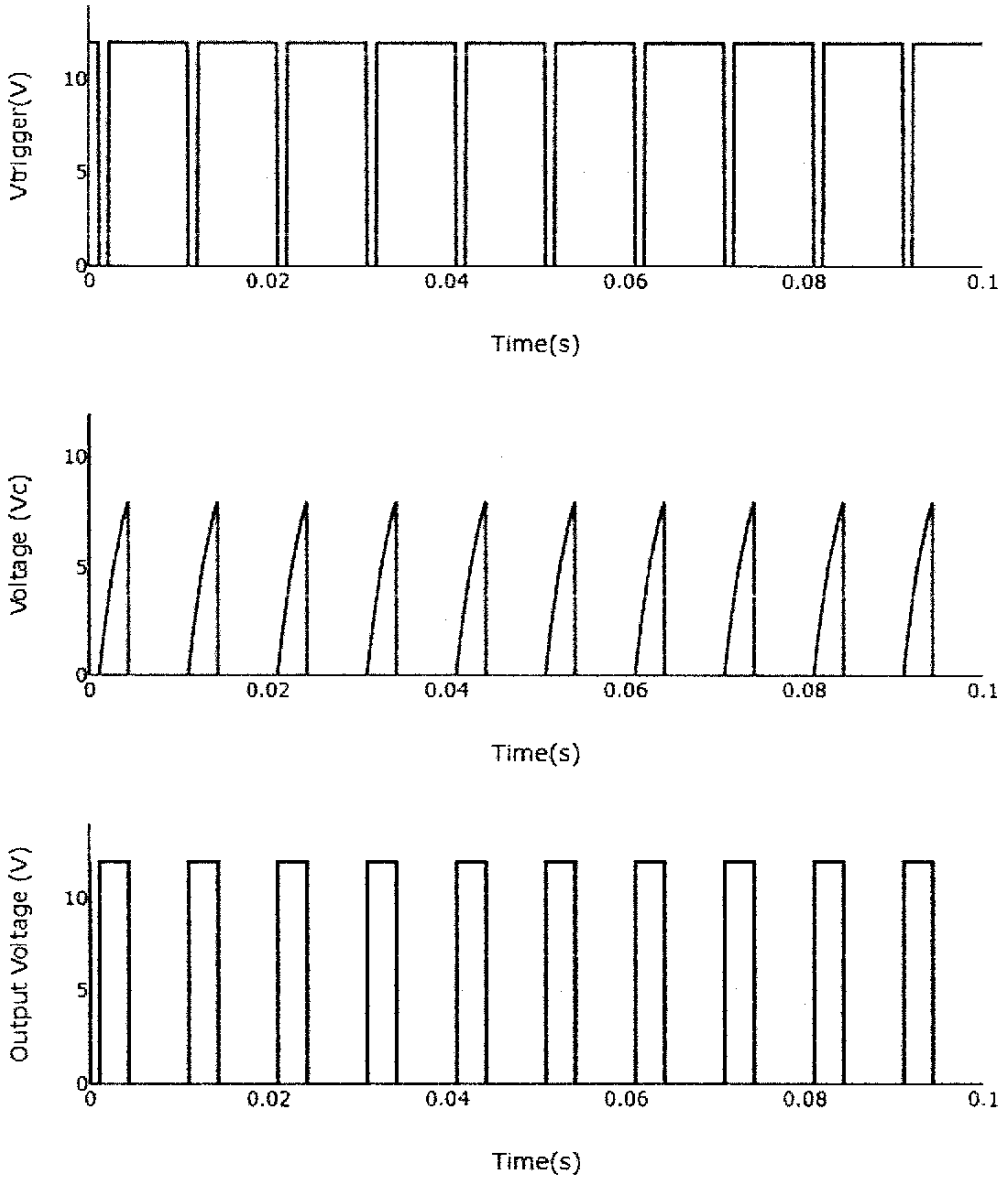


Plot Print Reset

Experimental Readings

S.No	Resistor (R KΩ)	Capacitance (C μF)	Pulse width (τ_{on} msec)	Duty Cycle (D %)
1	30	0.1	3.3	33

Graph


Vtrigger(V)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)
Voltage (Vc)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)
Output Voltage (V)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)

WORKING OF ASTABLE MULTIVIBRATOR WITH 555 TIMER CIRCUIT:

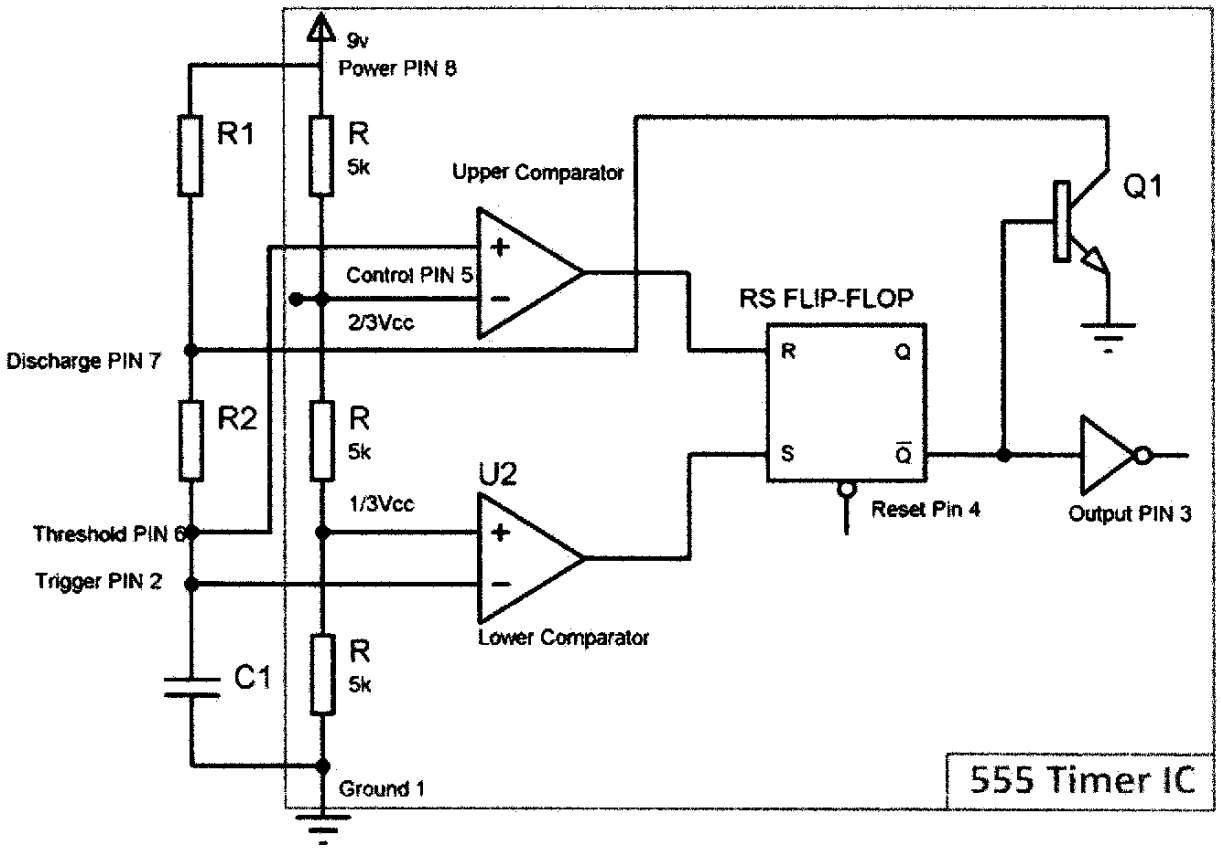


Figure 13b: Astable Mutivibrator using Timer IC 555

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Set the DC power supply to provide V_{CC}=5V.
3. Connect output pin (3) of 555 to channel 1 of CRO and pin (2/6) to channel 2 of CRO.
4. Observe the output waveforms and measure the output voltage (V_O) and voltage across capacitor (V_c). Calculate the theoretical values of above measured parameters.
5. Plot the output voltage waveforms for output voltage and voltage across capacitor. Frequency, f= $1.45/ (R_A+2R_B)C$ and % of Duty cycle = $(T_H/ (T_H+T_L))*100$
6. Practically T_L and T_H are measured, and theoretical values are verified with practical values.

WAVEFORM of ASTABLE MULTIVIBRATOR:

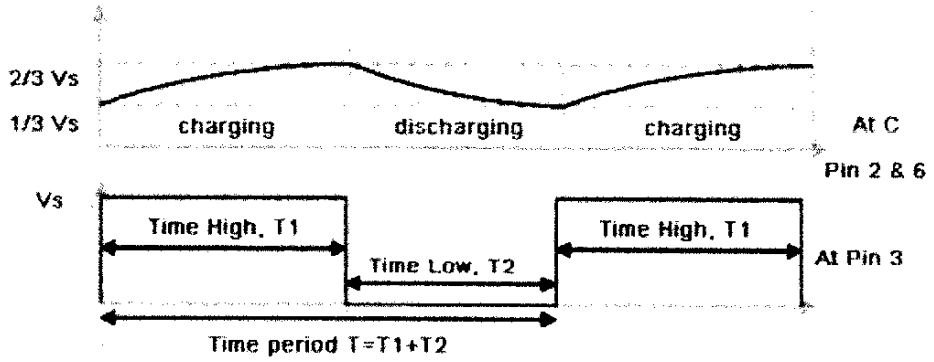
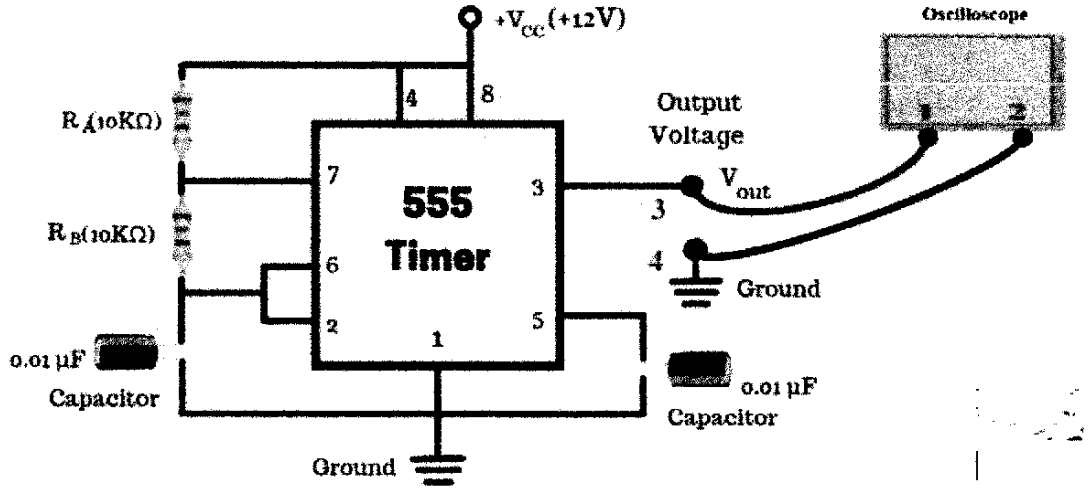


Figure 13c: Waveform of Astable Mutivibrator

SIMULATION IN VIRTUAL LAB:



Controls

Power On/Off

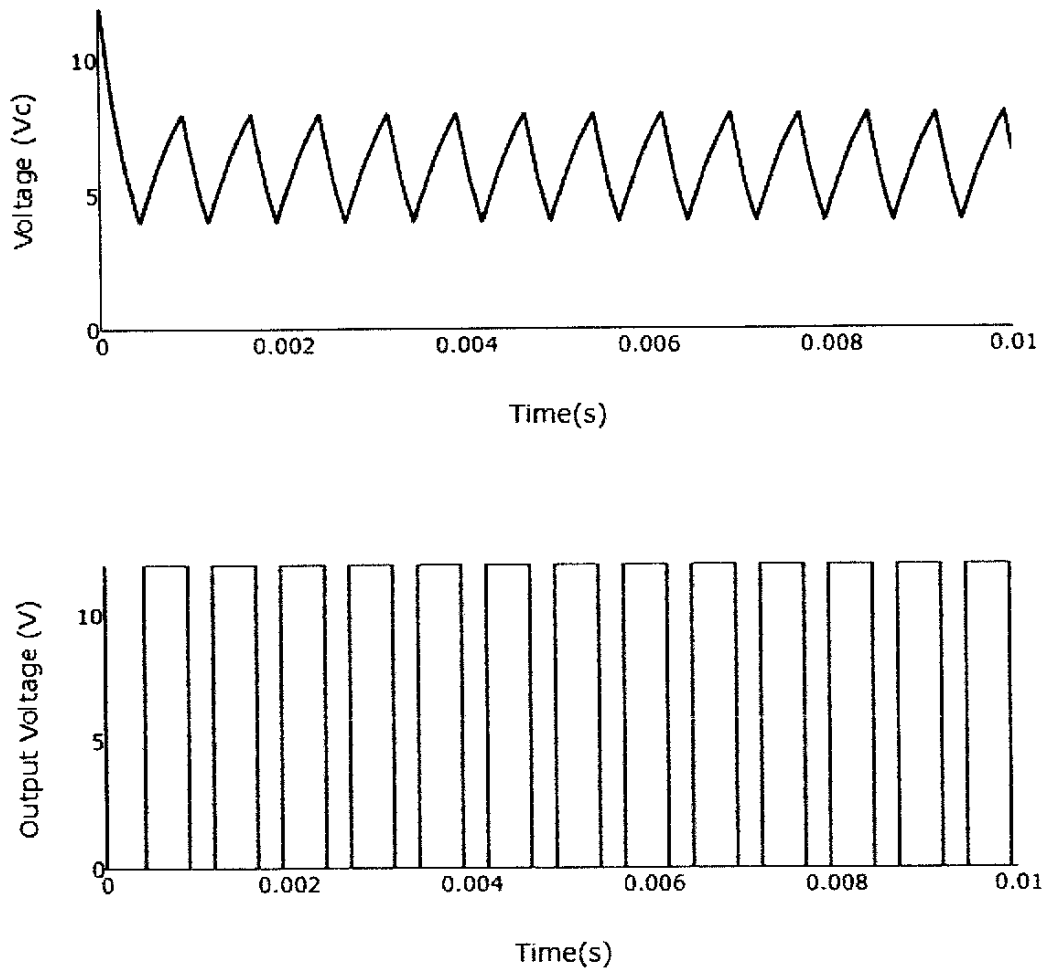
Resistance (R_A KΩ)

Plot | Print | Reset

Experimental Readings

S.No	Resistance (R_A KΩ)	Resistance (R_B KΩ)	Capacitance (C µF)	Pulse width (τ_p msec)	Time constant (T msec)	Duty cycle (D %)	Freq (F Hz)
1	3	3.9	0.1	0.476	0.745	63.89	1.34

Graph



CONCLUSION: