

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY,  
Jnana Sangama, Belagavi – 590018**



**KLS VISHWNATHRAO DESHPANDE INSTITUTE OF TECHNOLOGY,  
Haliyal – 583 219, Uttara Kannada  
(Accredited by NAAC with “A” Grade)**

**LABORATORY MANUAL**

---

**Course Title : Electronic Principles and Circuits**  
**Course Code : BEC303**  
**Year / Semester : 2<sup>nd</sup> Year / 3<sup>rd</sup> Sem**  
**Academic Year : 2025-26**  
**Course In-Charge : Prof. Rohini Kallur**

---



**Department of Electronics and Communication  
Engineering**

*P. Kallur* 12/9/2025  
Signature of the Faculty with Date

*Amrutesh*  
HoD

Head of the Department  
Dept. of Electronic & Communication Engg.  
KLS V.D.I.T. HALIYAL (U.K.)

# KLS Vishwanathrao Deshpande Institute of Technology



(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(F) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 179, Dist - Uttara Kannada

Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodese@klsvdit.edu.in



## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### College Vision and Mission Statements

#### Vision

To nurture talent & enrich society through excellence in technical education, research & innovation.

#### Mission

1. To augment innovative pedagogy & kindle quest for interdisciplinary learning & to enhance conceptual understanding.
2. To build competence, professional ethics & develop entrepreneurial thinking.
3. To strengthen industry institute partnership & explore global collaborations.
4. To inculcate culture of socially responsible citizenship.
5. To focus on holistic & sustainable development.

### Department Vision, Mission, PEOs and PSOs Statements

#### Vision

To bring out talented, skilled, and sustainable Electronics and Communication Engineering Graduates through strong domain expertise to serve the Society with greater Professional Ethics.

#### Mission

1. To create and impart an active learning ambience to accomplish a high degree of Professional competencies
2. To inculcate innovative research and developmental thinking in effective Teaching and Learning processes for solving Societal challenges
3. To deliver the needs and requirements of the latest state of art of the Industry through quality multidisciplinary internship and training programs

#### PEOs

- |        |   |
|--------|---|
| PEO 1: | To be successful in professional career in electronics, communication and allied industries by acquiring the knowledge in the fundamentals of Electronics and Communication Engineering principles and professional skills. |
| PEO 2: | To be in a position to analyze real life problems and design socially accepted and economically feasible solutions in the respective fields.  |
| PEO 3: | To exhibit good communication skills in their professional career, lead a team with good leadership traits and good interpersonal relationship with the members related to other engineering streams.                       |
| PEO 4: | To involve themselves in lifelong learning and professional development by pursuing higher education and participation in research and development activities.  |
| PEO 5: | To demonstrate professional and ethical responsibilities towards their profession, society and the environment.   |

#### PSOs

- |        |  |
|--------|--|
| PSO 1: | An ability to use appropriate modern techniques for analysis, design and development of VLSI and Embedded Systems. |
| PSO 2: | Understand the architectural specifications of a communication system and determine their performance.             |

# KLS Vishwanathrao Deshpande Institute of Technology



(Accredited by NAAC with "A" Grade)  
 (Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)  
 (Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist. Uthara Kannada  
 Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodce@klsvdit.edu.in



## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

<b>Course Title</b>	: Electronic Principles and Circuits						
<b>Course Code</b>	: BEC303						
<b>Year / Semester</b>	: 2 <sup>nd</sup> Year / 3 <sup>rd</sup> Semester						
<b>Academic Year</b>	: 2025-26						
<b>Syllabus</b>	<b>Sl. No.</b>	<b>Content</b>	<b>Page No.</b>				
	1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator.	1				
	2	Design and Test Biased Clippers – a) Positive, b) Negative, c) Positive-Negative Positive and Negative Clampers with and without Reference	6				
	3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.	13				
	4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely, drain resistance, mutual conductance and amplification factor.	16				
	5	Design and test Emitter Follower	19				
	6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier	22				
	7	Test the Op-amp Comparator with zero and non-zero reference and obtain the Hysteresis curve.	24				
	8	Design and test Full wave Controlled rectifier using RC triggering circuit.	26				
	9	Design and test Precision Half wave and full wave rectifiers using Op-amp	28				
	10	Design and test RC phase shift oscillator	31				
	11	Virtual Lab	33				
<b>CLOs</b>	: <ul style="list-style-type: none"> <li>• Understand the electronic circuit schematic and its working</li> <li>• Realize and test amplifier and oscillator circuits for the given specifications</li> <li>• Realize the Op-Amp circuits for applications such as DAC, implement mathematical functions and precision rectifiers.</li> <li>• Study the static characteristics of SCR and test the RC triggering circuit.</li> <li>• Design and test the combinational and sequential logic circuits for their functionalities. Use suitable ICs based on the specifications and functions</li> </ul>						
<b>COs</b>	: <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%; text-align: center;"><b>CO1:</b></td> <td>Understand the characteristics of BJTs and FETs for switching and amplifier circuits.</td> </tr> <tr> <td style="text-align: center;"><b>CO2:</b></td> <td>Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.</td> </tr> </table>			<b>CO1:</b>	Understand the characteristics of BJTs and FETs for switching and amplifier circuits.	<b>CO2:</b>	Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
<b>CO1:</b>	Understand the characteristics of BJTs and FETs for switching and amplifier circuits.						
<b>CO2:</b>	Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.						





## 1. Evaluation:

**Students Assessment through CIE (50%) + SEE (50%)**

Parameter	Particulars	Marks	Total	Scale Down Marks
CIE	Performance	05	110 (10*11 Expt.)	15
	Viva-Voce	02		
	Journal	03		
LAB IA	Write-up + Conduction + Result	30	50	10
	Viva	20		
<b>Total Marks</b>				<b>25</b>

### Note:

1. CIE for each lab session will be for 10 Marks.
2. Total CIE marks scale down to 15 Marks.
3. One lab Internals to be conducted for 50 Marks.
4. Lab Internal marks to be scale down to 10 Marks.



### Experiment: 01

#### Design and test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator

#### Aim:

- i. Construct Bridge Rectifier with Capacitor Input Filter and determine ripple factor & analyse wave form.

#### Equipment Required:

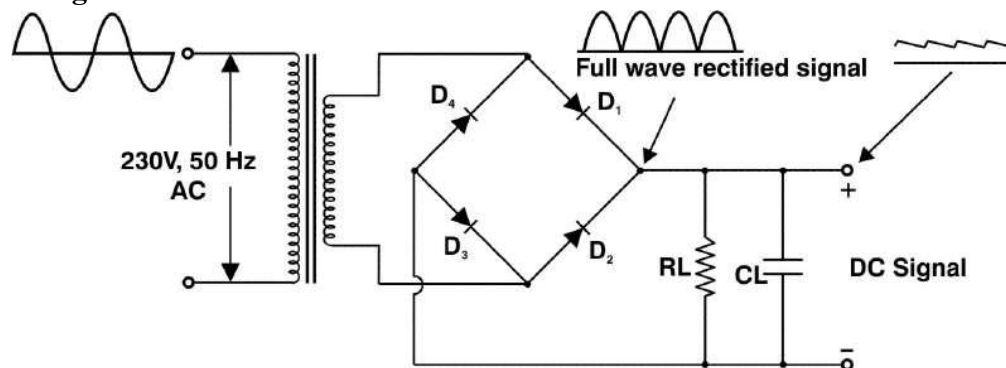
Hardware- Computer, Software- MultiSim software

#### Theory:

In a full wave rectifier, current flows through the load in the same direction for both half cycles of input ac voltages. Full wave bridge rectifiers employ 4 diodes. Full wave rectifiers are classified into: -

1. Full wave center tap rectifier
2. Full wave bridge rectifier

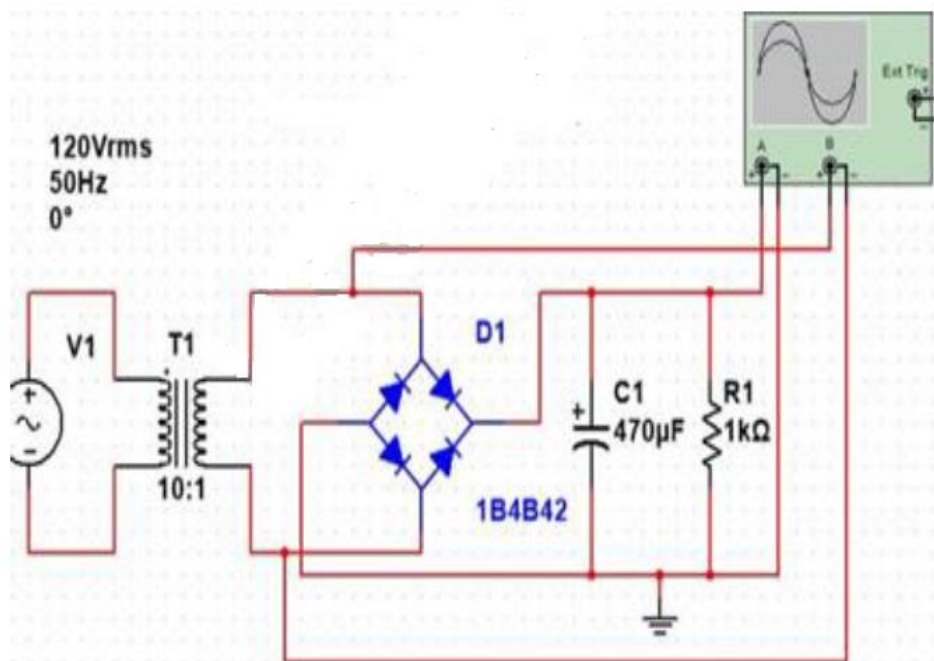
#### Full wave bridge rectifier: -



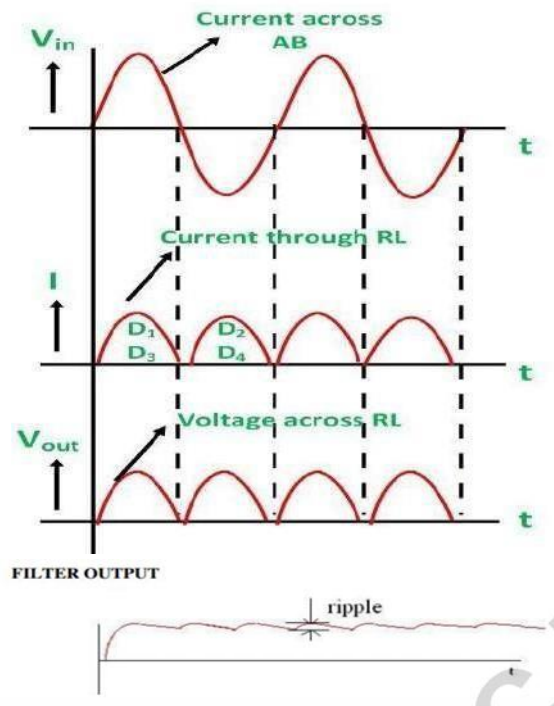
This rectifier employs 4 diodes i.e. D1, D2, D3 & D4. During the +ve half cycle of the input ac voltage, end A of secondary winding becomes +ve & end B becomes -ve. This makes diode D1 & D3 forward biased while diode D2 & D4 becomes reverse biased. Thus, only diode D1 & D3 conducts. The conventional current flow is shown by dotted arrows. During the -ve half cycle of input voltage, end A becomes -ve & end B becomes +ve. This makes diode D2 & D4 forward biased while diode D1 & D3 reverse biased. Thus, only diode D2 & D4 conducts. The conventional current flow is shown by solid arrows.

**Procedure:**

1. Open MULTISIM Software.
2. Click=> New => Design1
3. Click save as in Desktop rename the Design1 to your circuit name.
4. Go to Component tool bar and select the components.
5. Draw the above circuits using the components that are available in the tool bar and then save the circuit.
6. Double click AC\_POWER set its value above mentioned.
7. Click simulate button or press F5 key => RUN
8. Then double click connected in the output of the Oscillo scope and measure input and output waveforms.
9. Then Change input Frequency and voltage, again measure and print the output waveforms.

**Circuit Diagram:**

**Input & Output Waveforms of Voltage & Current: -**



**Conclusion: -** Verification of Bridge Rectifier with Capacitor Input Filter is completed.

**Aim:**

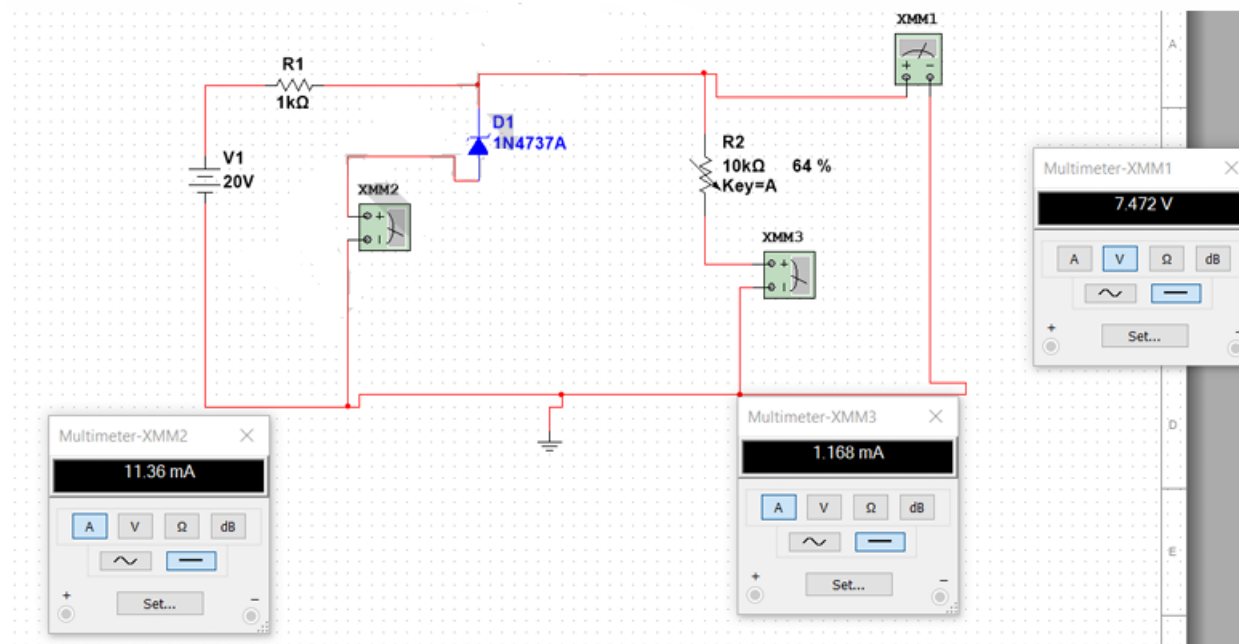
- ii. Construct & test the Zener diode as voltage regulator.

**Equipment Required:**

Hardware- Computer, Software- MultiSim software

**Theory:**

Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. It is acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode breaks down while reverse biased. In the case of normal diodes, the diode damages at the break down voltage. But Zener diode is specially designed to operate in the reverse breakdown region. The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, it's depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction. And the electron hole pair generation takes place. Thus, heavy current flows. This is known as Zener break down. So, a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage across it remains constant. This principle is used in voltage regulator using Zener diodes.

**Circuit Diagram:****Procedure:**

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component tool bar.
2. Using a component tool bar, place all the components on the circuit window and wire the circuit.
3. Connect the circuit as shown in circuit diagram.

### Input Characteristics:

1. Varying the input voltage keeping load constant: Connect the circuit as show in in figure. Keep supply control at minimum.
2. Keep the load  $R_L$  at 750ohms for Q-point. Increase the input voltage  $V_S$  in step of 1Volt and note  $V_1$  and  $V_2$ . Where  $V_1$  is the input and  $V_2$  is the output voltage across Zener.
3. Plot the curves between input –output at load constant. Find out the  $\delta V_1$  and  $\delta V_2$  from the plot and calculate the line regulation.

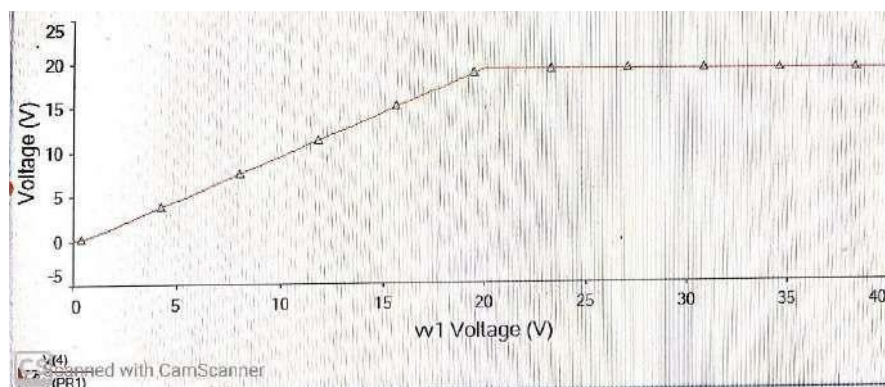
### Output characteristics:

1. Varying the load keeping input voltage constant: Connect the circuit as show in in figure.
2. Keep supply control at minimum. 2. Keep load  $R_L$  at 3000ohms. Increase the input voltage  $V_1$  to 12 Vdc.
3. Decrease the load and note the voltage  $V_2$  with load value.
4. Plot the curves between load and output voltage at input constant. Find out the  $\delta V_2$  and
5.  $V_Z$  at Q point at set load value from the input plot and calculate load regulation.

### Observation-

Sl.No.	$V_1$ (in V)	O/P Voltage

### Graph-



**Conclusion:** Verification of Zener diode as voltage regulator is completed.



### Experiment: 02

#### Design and Test:

1. Biased Clippers – a) Positive, b) Negative, c) Positive-Negative
2. Positive and Negative Clampers with and without Reference

**Aim 1:** To design and test the clipping circuits using MultiSim.

#### Equipment Required:

Hardware- Computer, Software- MultiSim software

#### Theory:

Clipping circuits (also known as limiters, amplitude selectors, or slicers), are used to remove the part of a signal that is above or below some defined reference level. We've already seen an example of a clipper in the half-wave rectifier –that circuit basically cut off everything at the reference level of zero and let only the positive-going (or negative-going) portion of the input waveform through. To clip to a reference level other than zero, a dc source is put in series with the diode. Depending on the direction of the diode and the polarity of the battery, the circuit will either clip the input waveform above or below the reference level.

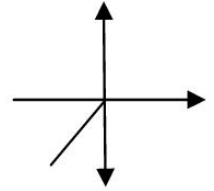
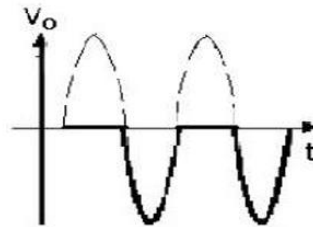
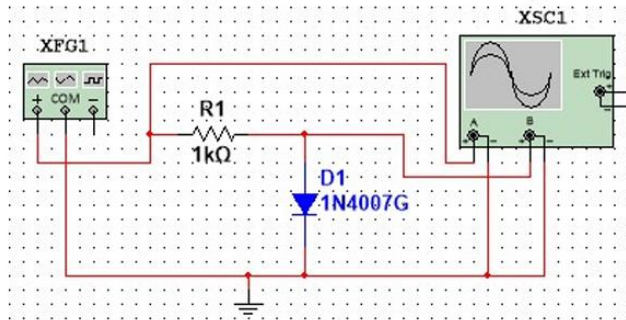
- **Positive Clipping (Without the battery):** When  $V_i > 0$  the diode is ON  $V_i$  dropped across R &  $V_o = 0$ . When  $V_i < 0$  the diode is OFF voltage across R is Zero &  $V_o = V_i$ .
- **Positive Clipping (With Battery):** The will not turn ON until  $V_i > V_B$  This shifts the reference level up and clips the input at  $+V_B$  and passes everything  $V_i < V_B$ .
- **Negative Clipping (With Battery):** If the polarity of the Diode is changed without the battery the positive portion of input is passed & Negative part is clipped. With battery the diode conducts for  $V_i < V_B$  the reference level shifted to  $+V_B$  only  $V_i > V_B$  appears at output. If the battery polarity also changed, then the reference level shifted to  $-V_B$  output will be  $V_i > -V_B$ .
- **Double Sided Clipping:** This circuits clips both positive & negative portions of input signal simultaneously.

**Procedure:**

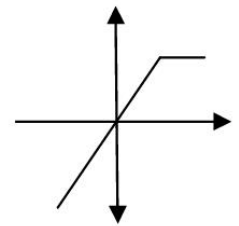
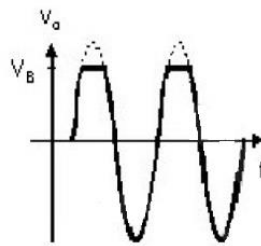
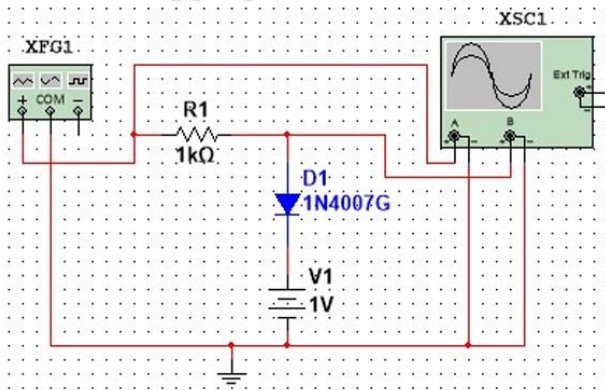
1. All the connections are made as per the circuit diagram.
2. Apply the sine wave input with frequency 1kHz and 10Vpp and observe the different clipping output.
3. Observe the various transfer characteristics on CRO.

**Circuit diagram:**

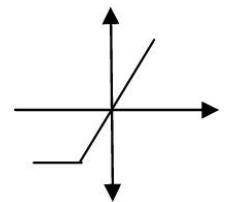
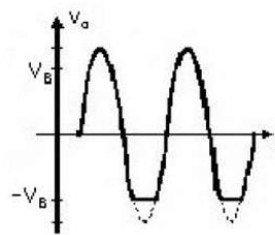
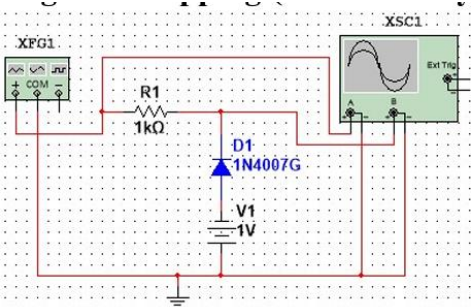
**Positive Clipper (Without bias):**



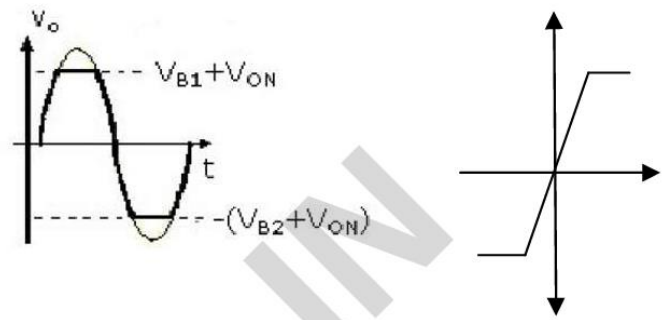
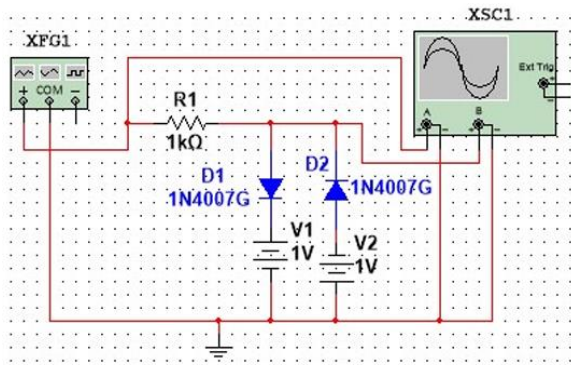
**Positive Clipper (With bias)**



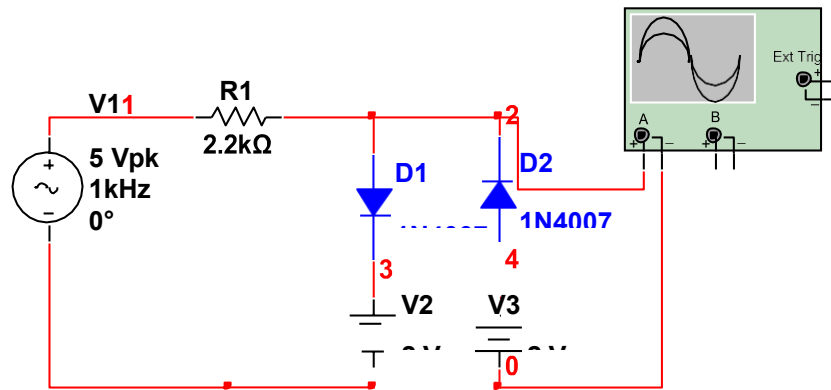
**Negative Clipping (with bias)**



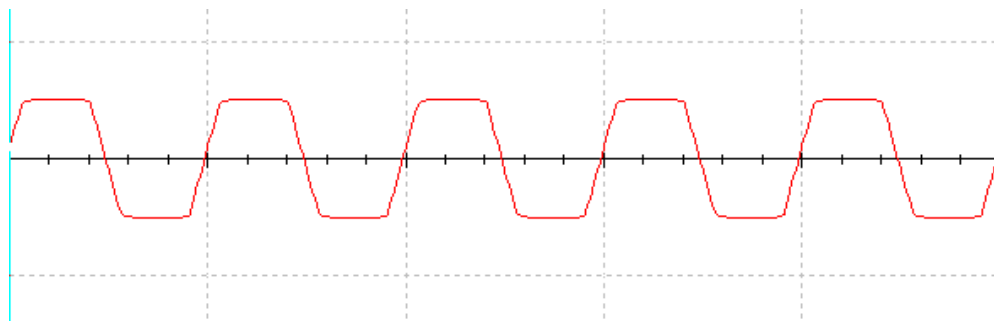
### Two-Sided Clipping (with bias):



### Slicer:



### Output Waveform:



**Aim 2:** To design and test the clamping circuits using MultiSim.

**Theory:**

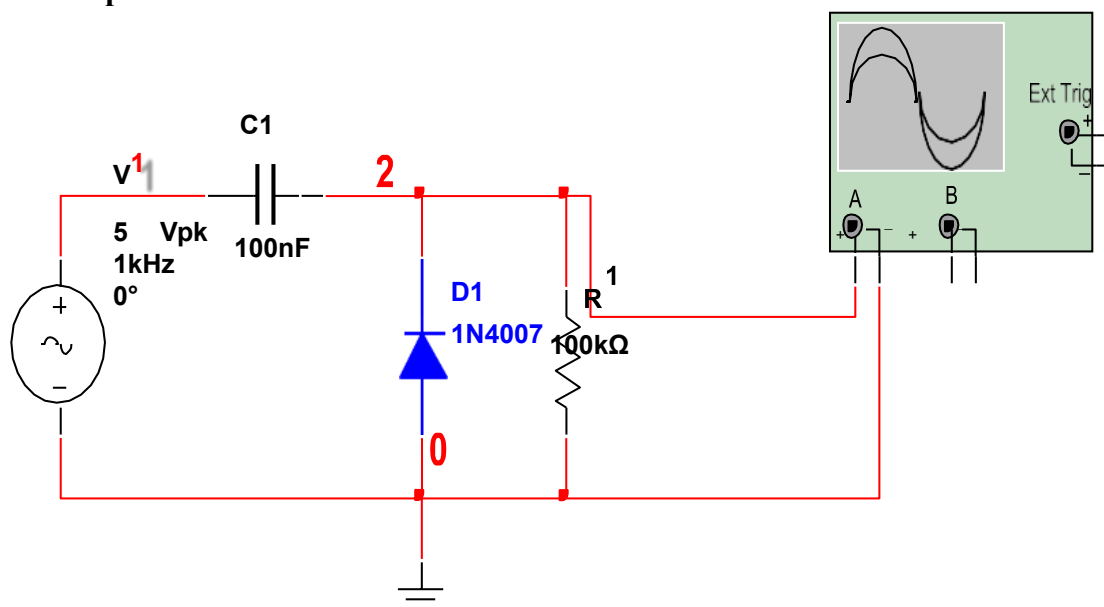
Clamping circuits, also known as dc restorers or clamped capacitors, shift an input signal by an amount defined by an independent voltage source. While clippers limit the part of the input signal that reaches the output according to some reference level(s), the entire input reaches the output in a clamping circuit – it is just shifted so that the maximum (or minimum) value of the input is clamped” to the independent source.

Negative clamping circuit is a circuit that shifts the original signal in a vertical downward direction. The diode D1 will be forward biased, and the capacitor C is charged when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrier potential of the diode,  $V_0$  and the capacitor is charged to  $(V - V_0)$ . During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus, during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to  $-V - (V - V_0)$  or  $-(2V - V_0)$ . The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to  $V_0 - [-(2V - V_0)]$ .

In Positive Clamping the diode polarity is reversed and hence the effect will be reversed in the positive clamping. During Negative half cycle capacitor charges & in positive half cycle capacitor C discharges hence the  $V_0$  will be shifted in the positive half.

**Circuit Diagram:**

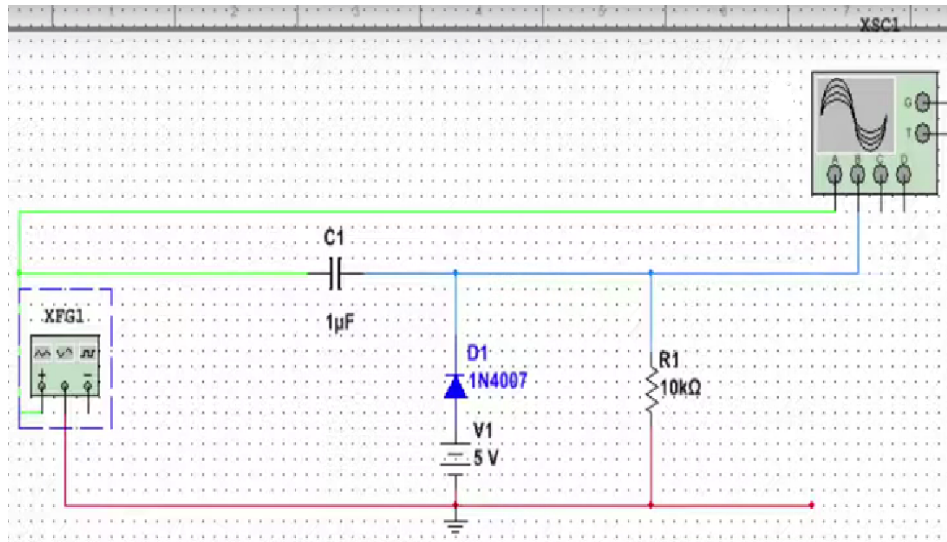
**Positive clamper without reference:**



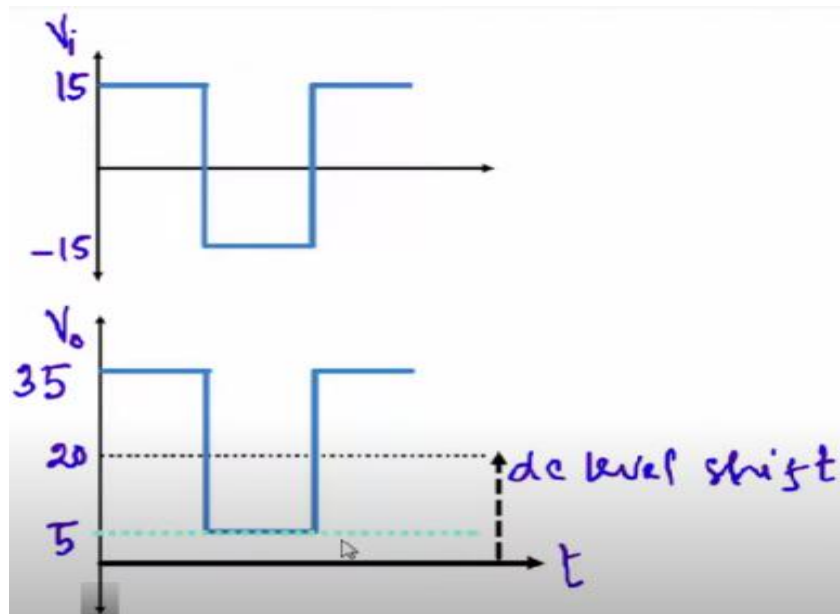
**Output Waveform:**



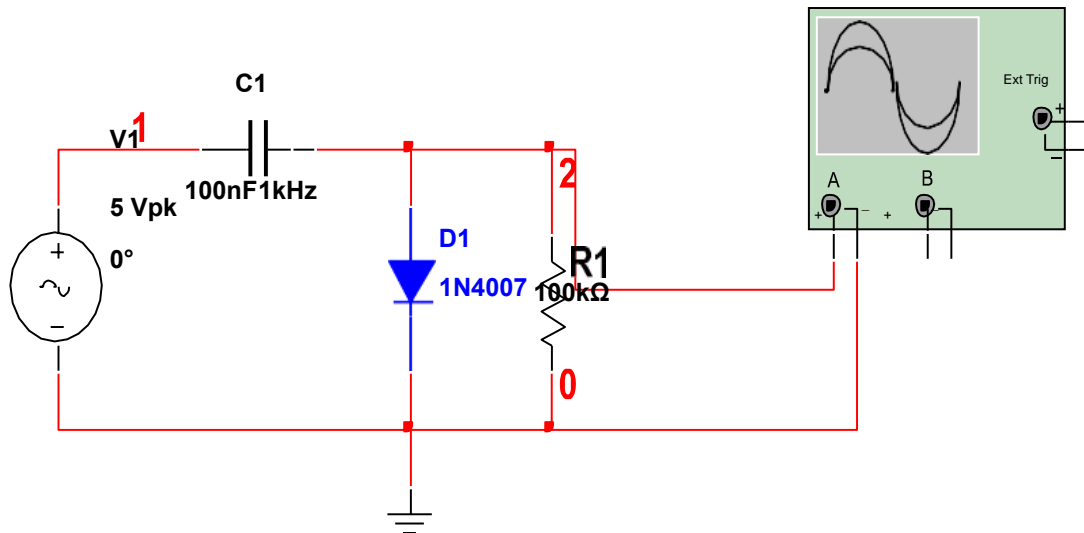
**Positive Clamper with reference:**



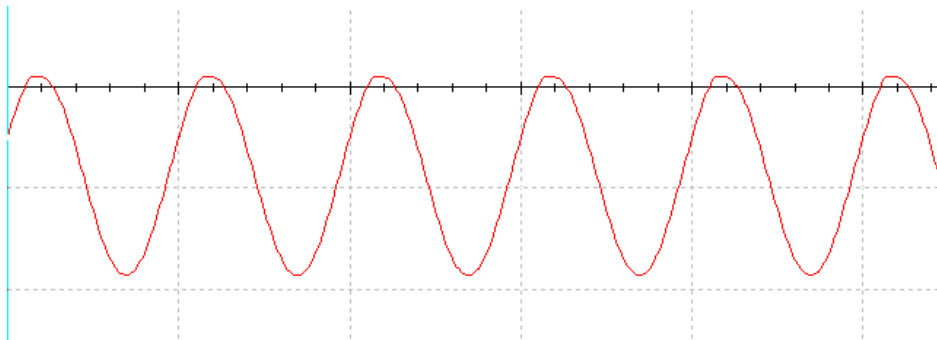
**Output Waveform:**



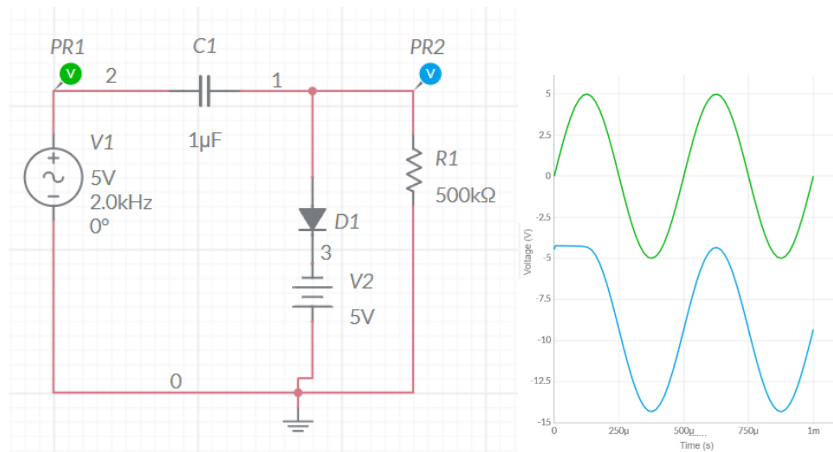
**Negative Clamper without reference:**



**Output Waveform:**



**Negative clamper with reference:**



**Procedure:**

1. Open new schematic capture in Multisim.
2. Connect the circuit as shown in figure above.
3. Now apply a sine/square wave of frequency 1KHz and amplitude 10V(P-P) using function generator available in Multisim.
4. Now click on Simulate and then RUN the circuit.
5. Now observe the output waveform using oscilloscope.

**Conclusion:** Different types of clamping circuits are studied and observed the response for different combinations of  $V_R$  and diodes using Multisim.



### Experiment: 03

Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.

**Aim:** Determine drain & Transfer characteristics of JFET.

#### Equipment Required:

Hardware- Computer, Software- Multisim

#### Theory:

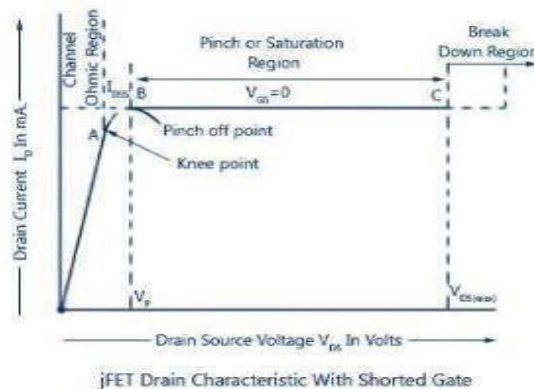
Characteristics of JFETS

There are two types of characteristics.

- 1) Output or drain characteristics and
- 2) Transfer characteristic.

#### 1) Output or Drain Characteristic:

The curve drawn between drain current  $I_D$  and drain-source voltage  $V_{DS}$  with gate-to source voltage  $V_{GS}$  as the parameter is called the drain or output characteristic. This characteristic is analogous to collector characteristic of a BJT:

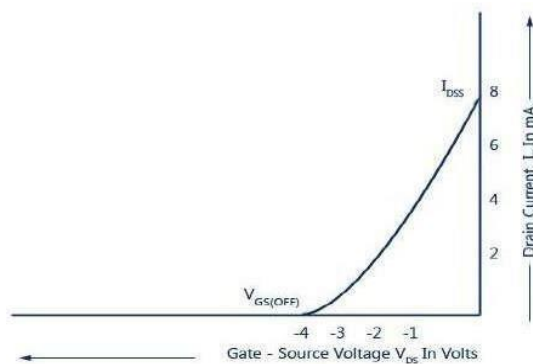


#### 2) Transfer Characteristics of JFET

The transfer characteristic for a JFET can be determined experimentally, keeping drain- source voltage,  $V_{DS}$  constant and determining drain current,  $I_D$  for various values of gate-source voltage,  $V_{GS}$ . The curve is plotted between gate-source voltage,  $V_{GS}$  and drain current,  $I_D$ , as illustrated in fig. It is similar to the Transconductance characteristics of a vacuum tube or a transistor. It is observed that:

- (i) Drain current decreases with the increase in negative gate-source bias
- (ii) Drain current,  $I_D = I_{DSS}$  when  $V_{GS} = 0$
- (iii) Drain current,  $I_D = 0$  when  $V_{GS} = V_D$

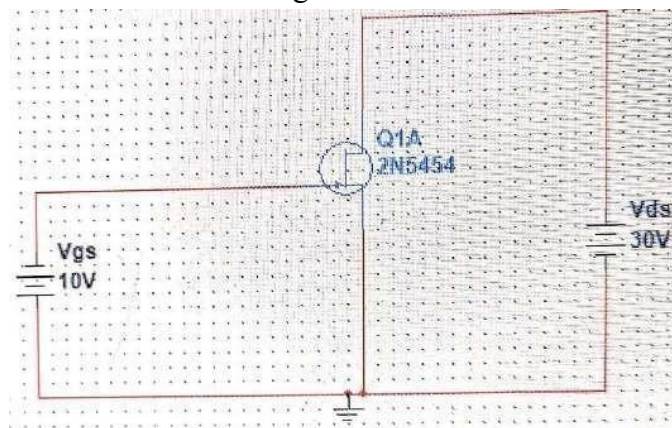
The transfer characteristic can also be derived from the drain characteristic by noting values of drain current,  $I_D$  corresponding to various values of gate-source voltage,  $V_{GS}$  for a constant drain-source voltage and plotting them.



Transfer Characteristics of JFET

#### Procedure -

1. Start MULTISIM. A blank circuit window will appear on the screen along with a component tool bar.
2. Using component tool bar, place all the components on the circuit window and wire the circuit.
3. Connect the circuit as shown in circuit diagram.



#### 4. Components Required-

- a. JFET (2N5454)
- b.  $V_{gs}$  (V1)- 10V
- c.  $V_{ds}$  (V2)- 30V

#### For Drain Characteristic:

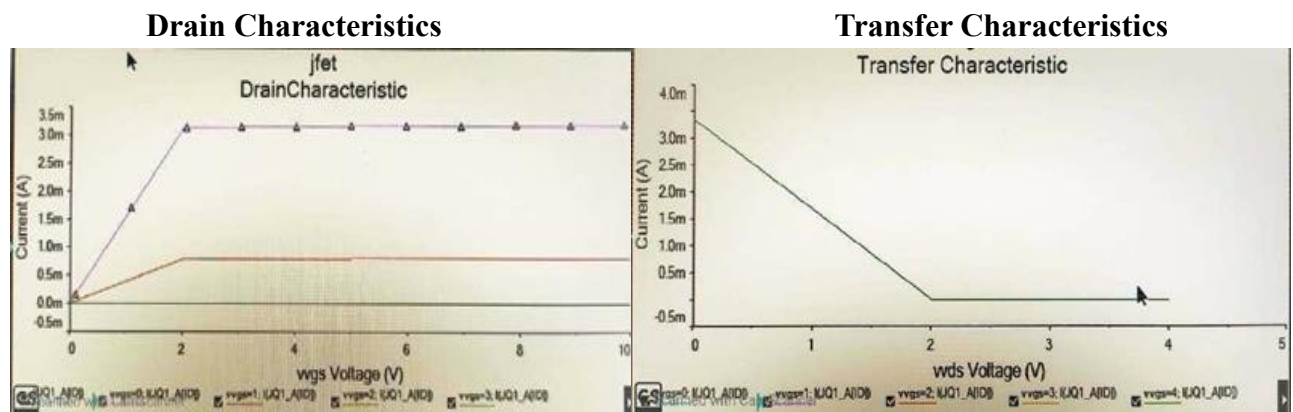
1. Go to analyses and simulation- DC sweep. In the DC sweep window set the following values:  
 Source1:  
 Source:  $V_{ds}$   
 Start Value: 0

- Stop Value: 10  
 Increment: 2
2. Tick out the “use source 2” and set the following values:  
 Source2:  
 Source: Vgs  
 Start Value: 0  
 Stop Value: 5  
 Increment: 1
  5. Then save it.
  6. Go to analyses and simulation- DC sweep and select the value I(JQ1\_A[ID]) and click on add option.
  7. Then run the simulation and observe the Drain characteristic.

**For Transfer Characteristic:**

1. Go to analyses and simulation-DC sweep.
2. In the DC sweep window set the following values:  
 Source1:  
 Source: Vgs  
 Start Value: 0  
 Stop Value: 5  
 Increment: 2
3. Then save it.
4. Go to analyses and Simulation DC sweep – Output and select the value I(JQ1\_A[ID]) and click on add option.
5. Then run the simulation and observe the transfer characteristics.

**Characteristics:**



**Conclusion:** - Drain & Transfer characteristics of JFET are verified.



### Experiment: 04

Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely, drain resistance, mutual conductance and amplification factor.

**Aim:** Determine Drain & Transfer characteristics of MOSFET.

#### Equipment Required:

Hardware- Computer

Software- Multisim Software

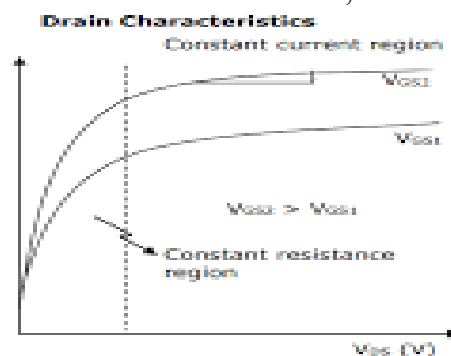
#### Theory:

There are two types of characteristics

- 1) Drain Characteristics
- 2) Transfer Characteristics

#### Drain Characteristics

- In Drain Characteristics, the output current is plotted with respect to the Drain to source voltage  $V_{DS}$ . We make  $V_{GS}$  (Gate to source voltage constant). It helps us in understanding three regions of operation.
- On the X-axis we plot Drain to Source voltage while on Y- Axis we plot  $I_D$  (Drain current).
- We plot the current values for different values of  $V_{GS}$ .
- As we can see, the current remains constant after some drain voltage. Hence, minimum drain to source voltage is needed for MOSFET to work.
- Hence, as we increase  $V_{GS}$  the channel width increases, and it results in more drain current  $I_D$



#### Transfer Characteristics

- Transfer characteristics is the graph of output current to input voltage.
- Hence, we plot current (output) with respect to input voltage  $V_{GS}$ .
- The above figure shows transfer characteristics. It is also known as Transconductance curve.

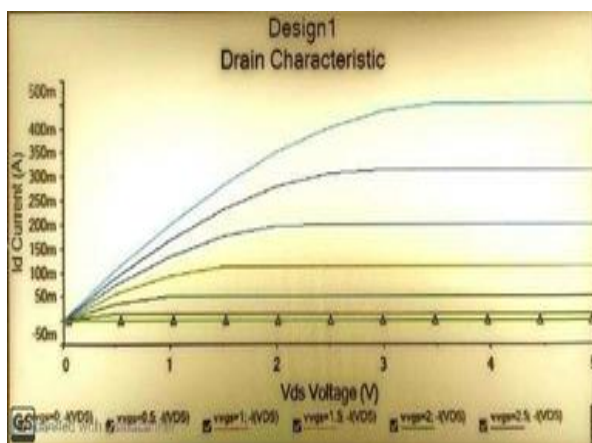


### For Transfer Characteristic:

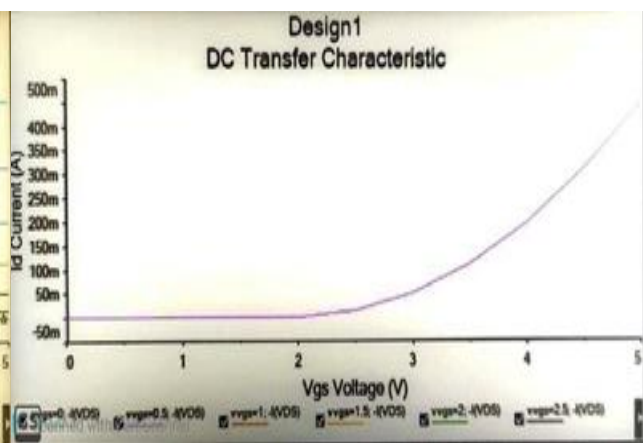
- 1) Go to analyses and simulation- DC sweep.
- 2) In the DC sweep window set the following values:  
Source1:  
Source: Vgs  
Start Value: 0  
Stop Value: 5  
Increment: 0.5
- 3) Then save it.
- 4) Go to analyses and simulation – DC sweep output
- 5) In output window click on add expression and select “-” and I (Vds).
- 6) Then run the simulation and observe the transfer characteristics.

### Characteristics:

**Drain Characteristics**



**Transfer Characteristics**



**Conclusion:** Drain & Transfer characteristics of MOSFET are verified.



### Experiment: 05

#### Design and test Emitter Follower

**AIM:** To study the input and output characteristics of common emitter connection.

#### Equipment Required:

Hardware- Computer

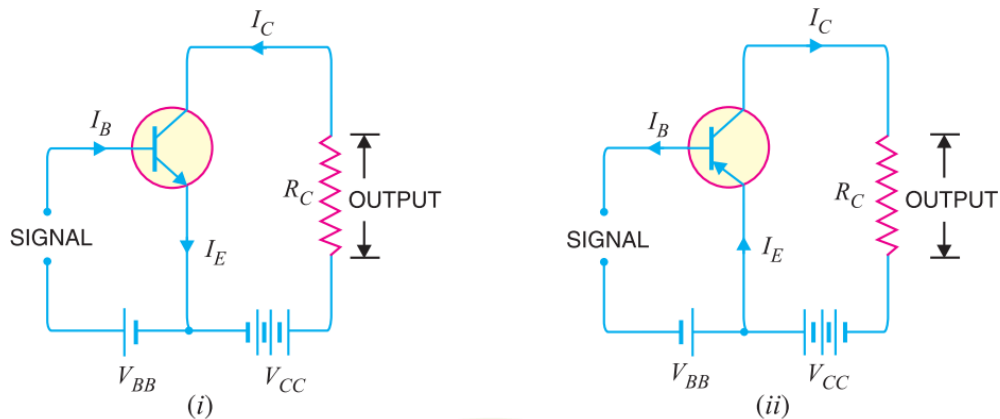
Software- Multisim Software

#### Theory:

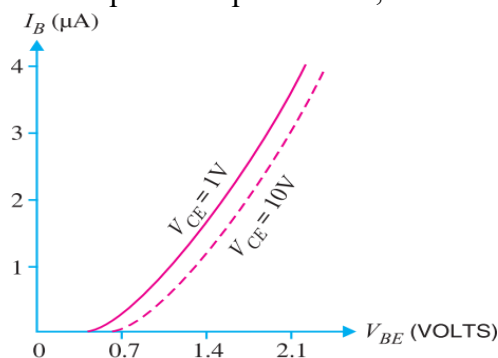
A transistor can be connected in a circuit in the following three ways:

- 1) Common base connection
- 2) Common emitter connection
- 3) Common collector connection

#### Common Emitter Connection:



- In the above circuit arrangement, input is applied between base & emitter & output is obtained from collector & emitter.
- Here, emitter is common to both input & output circuits, hence named CE connection.



## Current Amplification Factor ( $\beta$ )

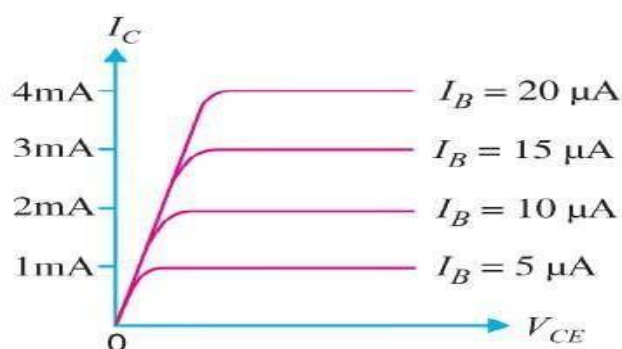
It is the ratio of the change in  $I_C$  to change in  $I_B$ .  $\beta = \Delta I_C / \Delta I_B$

## Input Characteristics

- It is the curve between  $I_B$  and  $V_{BE}$ .
- Keeping  $V_{CE}$  constant, when  $V_{BE}$  is increased,  $I_B$  increases less rapidly. This means that it has high input resistance than that of CB circuit.
- Input Resistance ( $r_i$ ) is the ratio of the change in  $V_{BE}$  to change in  $I_B$  at constant  $V_{CE}$ .
- Input resistance ( $r_i$ ) =  $\Delta V_{BE} / \Delta I_B$  at constant  $V_{CE}$ .

## Output Characteristics

- It is the curve drawn between  $I_C$  and  $V_{CE}$  at constant  $I_B$ .
- By keeping  $I_B$  constant when  $V_{CE}$  is increased,  $I_C$  also increases slowly up to knee voltage.
- When  $V_{CE}$  is increased beyond knee voltage, the collector current becomes almost constant.
- Output resistance ( $r_o$ ) is the ratio of the change in  $V_{CE}$  to change in  $I_C$ . Output resistance ( $r_o$ ) =  $\Delta V_{CE} / \Delta I_C$  at constant  $I_B$ .



## Procedure For Input Characteristics:

- 1) Adjust collector to emitter voltage  $V_{CE}$  (using VR2) at some suitable value (say at -2 v) and keep it constant.
- 2) Adjust base to emitter voltage  $V_{BE}$  (using VR1) so that base current shows value  $20 \mu A$ .
- 3) Note down base to emitter voltage  $V_{BE}$ .
- 4) Increase  $V_{BE}$  in small steps and note the corresponding base current  $I_B$ .
- 5) Repeat step number 1, 2, 3 and 4 for other values of  $V_{CE}$  (say at -4v, -6v, -8v).
- 6) Plot a graph by taking base voltage  $V_{BE}$  along X axis and base current along Y axis as shown in the figure.
- 7) Draw tangent  $V_{BE}$ - $I_B$  curve and determine its slope.

## Procedure For Output Characteristics:

- 1) Set collector voltage  $V_{CE} = 0.5$  v.
- 2) Adjust the base current  $I_B$  to  $50 \mu A$  using VR1.
- 3) Note down the corresponding collector current  $I_C$ .
- 4) Gradually increase the collector voltage in small steps (i.e., say -2v, -2.5v, -3.0v ...-8v).

- 5) Note the corresponding collector current  $I_C$  keeping the base current  $I_B$  constant.
- 6) Repeat step number 6 and 7 for other values of base current  $I_B$  (say  $75 \mu A$ ,  $100 \mu A$  etc).
- 7) Plot a graph by taking collector voltage  $V_{CE}$  along X axis and collector current  $I_C$  along Y axis.
- 8) Draw a tangent  $V_{CE}$ -  $I_C$  curve and determine its slope.

**Observations for Input Characteristics:**

S. No	Collector base voltage ( $V_{CE}$ in volts)	Base current in ( $I_B$ ) $\mu A$	Collector emitter voltage ( $V_{BE}$ in volts)
1	-2V / -4V / -6V		
2			
3			
4			
5			

**Observations for Output Characteristics:**

S. No	Base current ( $I_B$ ) in $\mu A$	Collector current in ( $I_C$ ) $\mu A$	Collector emitter voltage ( $V_{CE}$ in volts)
1			
2			
3			
4			
5			

**Conclusion:** Verification of Emitter Follower is done.

# KLS Vishwanathrao Deshpande Institute of Technology

(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada

Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in



## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### Experiment: 06

#### Design and plot the frequency response of Common Source JFET/MOSFET amplifier

**Aim:** To obtain the frequency response of MOSFET amplifier in common source configuration with given specifications.

#### Equipment Required:

Hardware- Computer

Software- Multisim Software

#### Theory:

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary n- channel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology. Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown below. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by the bias resistors R1 and R2). Normally the value of the bias resistors is chosen as high as possible. However, too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the active region of the characteristics.

#### Procedure:

1. Set up the circuit as shown in the figure with an input signal of 0.2V (peak-to-peak) at 1000 Hz.
2. Observe the output on the CRO.
3. Vary the frequency of the input signal over a range of values (from 50Hz to a few MHz) to obtain the frequency response which is a graph between  $\log f$  (x-axis) and gain in dB (y-axis).

**Circuit Diagram:**

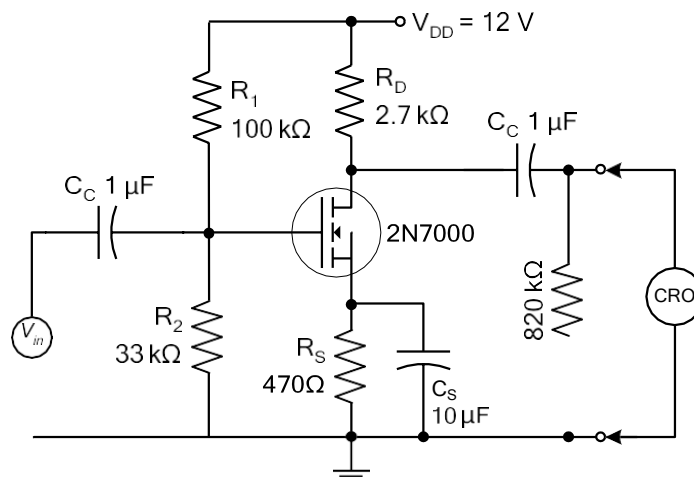


Fig. 1 Circuit diagram of MOSFET amplifier

**Observation:**

Frequency $f$ Hz	Input voltage $V_i$ V	Output voltage $V_o$ V	Gain ( $V_o/V_i$ )	Gain $20 \log(V_o/V_i)$ dB

**Graph (to be obtained):**

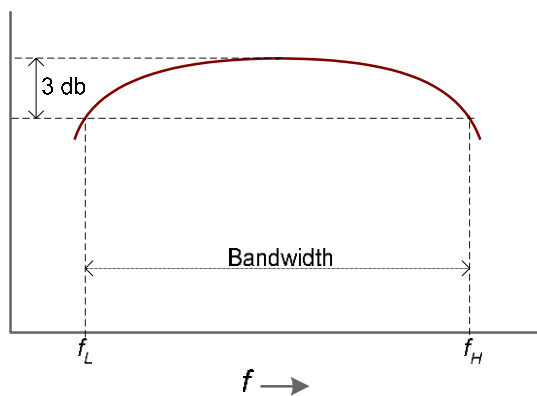


Fig 2. Frequency response

**Result:** The required common source MOSFET amplifier was designed and set up to obtain the required frequency response.

# KLS Vishwanathrao Deshpande Institute of Technology

(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada

Phone: 08284 - 220861, 220334, 221409, Fax: 08284 - 220813

www.klsvdit.edu.in | principal@klsvdit.edu.in | hodece@klsvdit.edu.in



## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### Experiment: 07

#### Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve

**Aim:** Verify the operation of an op – amp as (a) voltage comparator circuit and (b) Zero Crossing Detector.

#### Equipment Required:

Hardware- Computer

Software- Multisim Software

#### Theory:

**Voltage Comparator:** The circuit diagram shows an op-amp used as a comparator. A fixed reference voltage  $V_{ref}$  is applied to the (-) input, and the other time-varying signal voltage  $V_{in}$  is applied to the (+) input; Because of this arrangement, the circuit is called the non-inverting comparator. Depending upon the levels of  $V_{in}$  and  $V_{ref}$ , the circuit produces output. In short, the comparator is a type of analog-to- digital converter. At any given time, the output waveform shows whether  $V_{in}$  is greater or less than  $V_{ref}$ . The comparator is sometimes also called a voltage-level detector because, for a desired value of  $V_{ref}$ , the voltage level of the input  $V_{in}$  can be detected.

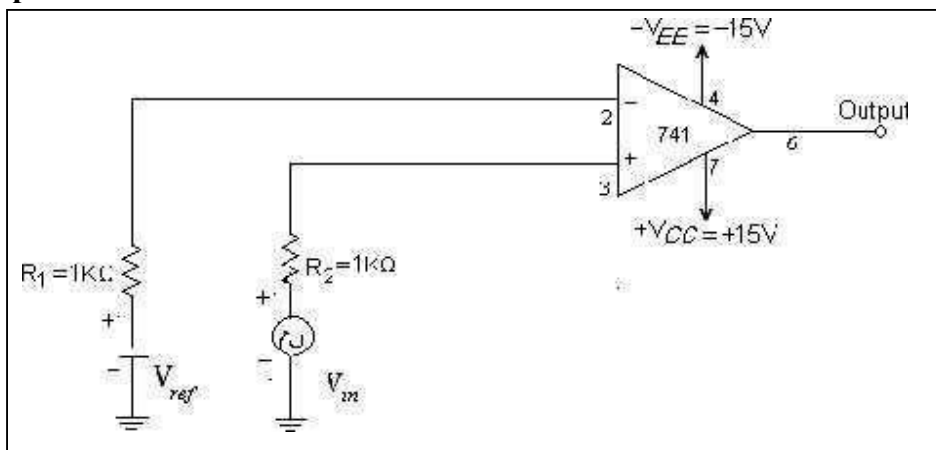
**Zero crossing detector:** ZCD is a voltage comparator that switches the output between  $+V_{sat}$  and  $-V_{sat}$  ( $V_{sat}$ : Saturation voltage almost equal to 14V) when the input crosses zero reference voltage. Then what is a comparator? In simple words comparators are basic operational amplifier circuits that compare two voltages simultaneously and switches the output according to the comparison. We can say zero crossing detection circuit is a comparator example. Inverting zero cross detector circuit schematic using op amp 741 IC is shown below along with working, input output wave forms.

#### Procedure:

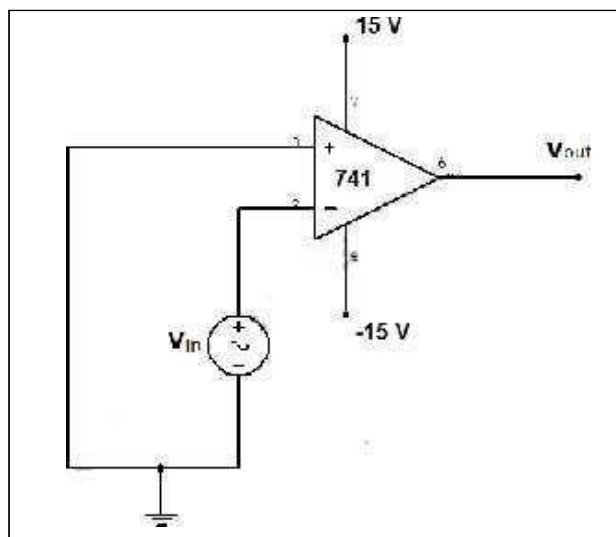
1. Set up circuit as shown in the connection diagram.
2. Set the input voltage 20 V peak to peak, 1 kHz in function generator, and apply input signal to the circuit.
3. Observe the output waveform in CRO.
4. Obtain the response for different  $V_r$  (for comparator circuit only).

#### Circuit Diagram:

### Voltage Comparator Circuit



### Zero Crossing Detector



### Observation table:

Sl. No	V <sub>in</sub>	V <sub>ref</sub>	V <sub>o</sub>
1			
2			
3			

**Conclusion:** The Opamp Comparator with zero and non zero reference is tested and verified.

**Experiment: 08**  
**Design and test Full wave Controlled rectifier using RC triggering circuit**

**Aim:** To design and test Full Wave Controlled Rectifier by using RC Triggering Circuit.

**Equipment Required:**

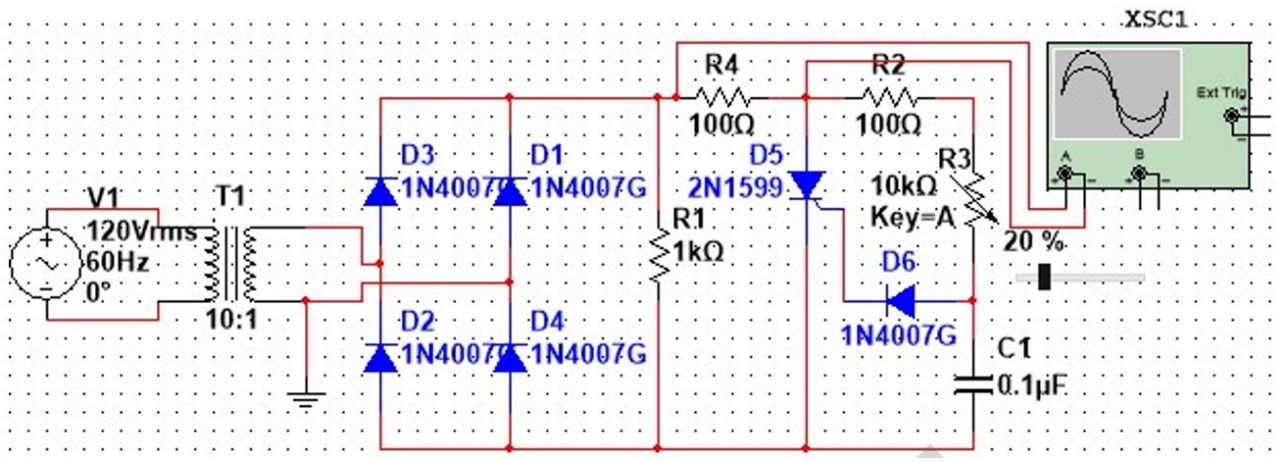
- Hardware- Computer
- Software- Multisim Software

**Theory:**

A thyristor is a four-layer 3 junction p-n-p-n semiconductor device consisting of at least three p-n junctions, functioning as an electrical switch for high power operations. It has three basic terminals, namely the anode, cathode and the gate mounted on the semiconductor layers of the device.

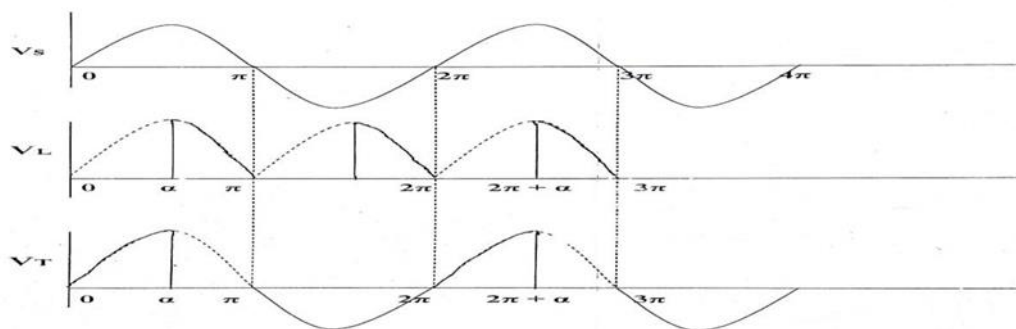
On giving the supply, we get the required V-I characteristics of a thyristor show in the figure below for anode to cathode voltage  $V_a$  and anode current  $I_a$  as we can see from the circuit diagram. A detailed study of the characteristics reveal that the thyristor has three basic modes of operation, namely the reverse blocking mode, forward blocking (off-state) mode and forward conduction (on-state) mode. Which are discussed in great details below, to understand the overall characteristics of a thyristor.

**Circuit diagram:**



### Waveforms:

VARIOUS WAVEFORMS FOR FULLY CONTROL



### Tabulation:

SL NO.	FIRING ANGLE ( $\alpha$ )	VDC

### Procedure:

1. Connect the circuit as per circuit diagram.
2. Make sure that R position must be High level before turn ON the power supply 3.
3. Turn ON the power supply and vary the firing angle (R value) step by steps and note down the reading of alpha vs Vdc.
4. Find the resistance value by using ohm's law.

**Conclusion:** Design and testing of Full Wave Controlled Rectifier by using RC Triggering Circuit is completed.



### Experiment: 09

#### Design and test Precision Half wave and full wave rectifiers using OpAmp

**Aim:** Design and verify a precision full wave rectifier. Determine the performance parameters.

#### Equipment Required:

Hardware- Computer

Software- Multisim Software

#### Theory

The use of Operational amplifiers can improve the performance of a wide variety of signal processing circuits. In rectifier circuits, the voltage drop that occurs with an ordinary semiconductor rectifier can be eliminated to give precision rectification.

The below shown circuit is the precision full wave rectifier. It consists of following sections:

1. Precision half-wave rectifier
2. Inverting summing amplifier

The input voltage  $V_{in}$  is applied to one terminal of the summing amplifier along with resistor R3 and to the input of the precision rectifier. The output of precision rectifier is applied to another terminal of summing amplifier. The precision half-wave rectifier circuit uses an inverting amplifier configuration.

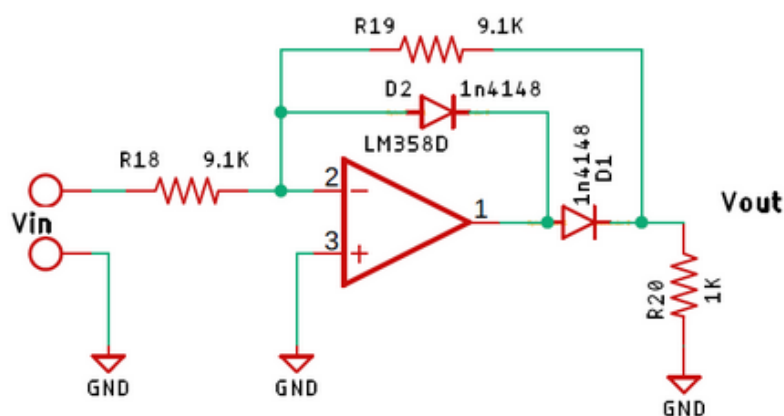


Fig 1. Precision Half Wave Rectifier circuit

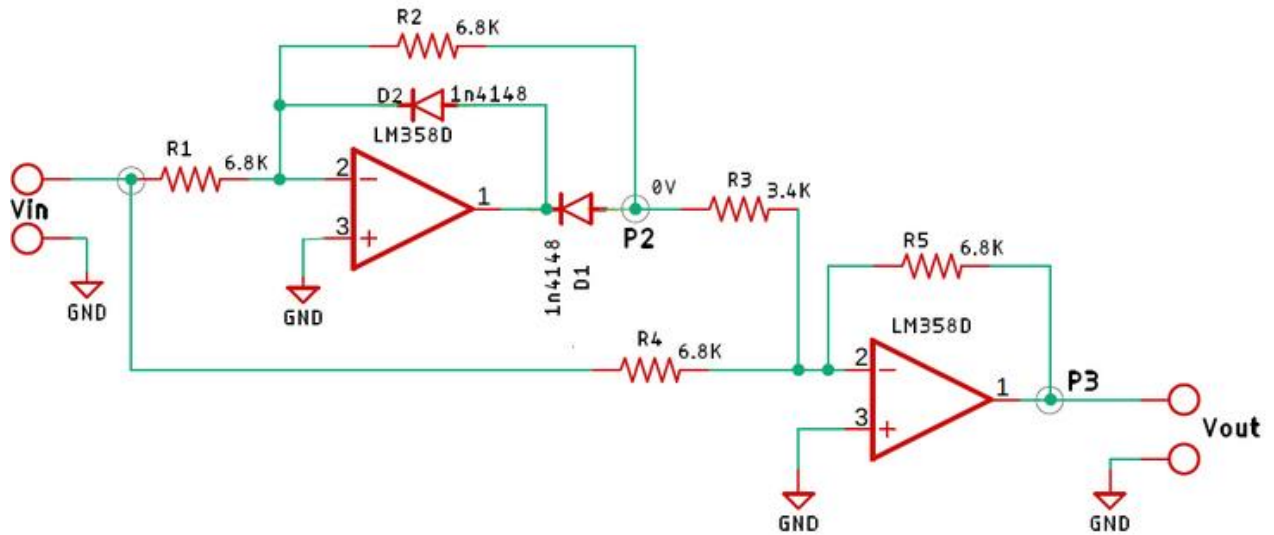


Fig 2. Precision Full Wave Rectifier circuit

### Procedure

1. Connections are made as per the circuit diagram shown in Fig. 1 and Fig. 2
2. Apply sinusoidal input of 0.5V peak to peak at the inverting terminal of the op-amp.
3. Note down the output voltage and observe the direction of the output on the CRO.
4. Calculate the output voltage and the gain of the circuit.
5. Draw the graph.

### Output

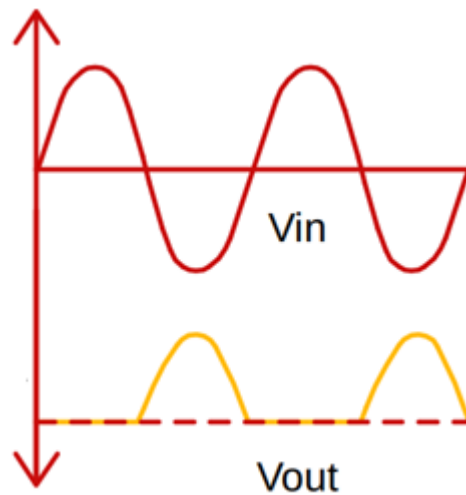


Fig 3. Precision Half Wave rectifier circuit

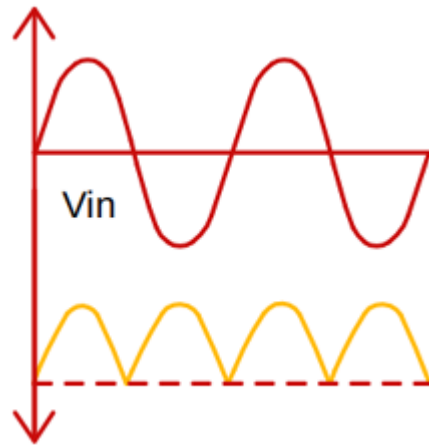


Fig 4. Precision Full Wave rectifier circuit

**Conclusion:** Design and verification of a Precision full wave rectifier is completed.



### Experiment: 10

#### Design and test RC phase shift oscillator

**Aim:** To design and study the working of an RC Phase Shift oscillator using BJT.

#### Equipment Required:

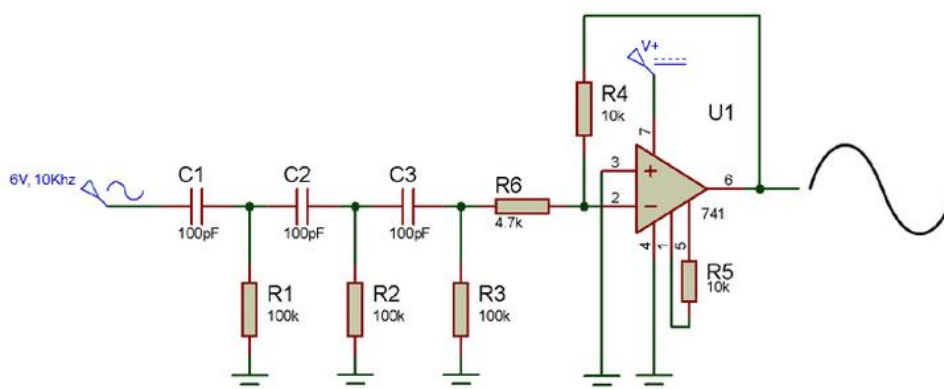
Hardware- Computer

Software- Multisim Software

#### Theory:

RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feedback Networks; the output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is  $60^\circ$ . Thus the RC ladder network produces a total phase shift of  $180^\circ$  between its input and output voltage for the given frequencies. Since CE Amplifier produces  $180^\circ$  phases shift the total phase shift from the base of the transistor around the circuit and back to the base will be exactly  $360^\circ$  or  $0^\circ$ . This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations.

#### Circuit Diagram:



**Output:**



**Conclusion:** Design and testing of RC phase shift oscillator is verified.



### Experiment: 11(Virtual Lab)

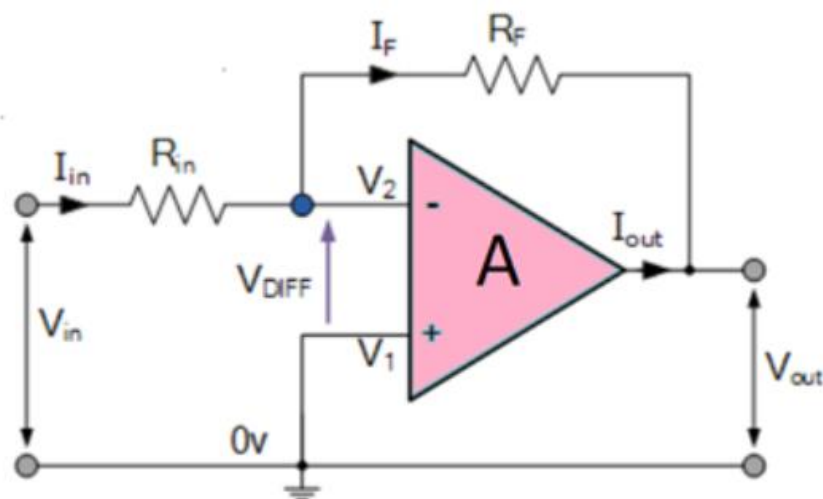
#### Design and test Inverting Amplifier using OP Amp

**AIM:** To design and study the working of an Inverting Amplifier using OP Amp.

**Components/ Equipment's Required:**

Sl.No	Component	Quantity	Specification
1	Capacitor	3	100pF
2	Resistors	5	100kΩ, 10KΩ
3	OP Amp	1	μA 741
5	CRO	1	40 M Hz, 1MΩ, 25pF
6	DC source	1	+12V
7	Connecting wires	Few	
8	Probes	2	

**Circuit Diagram:**



**Design:**


$$\frac{R_F}{R_{in}} = -\frac{V_{out}}{V_{in}}$$

The close loop gain ( $A_{cl}$ ) is given by,


$$A_{cl} = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_{in}}$$

Output voltage ( $V_{out}$ ) is given by,

$$V_{out} = -\frac{R_F}{R_{in}} \times V_{in}$$

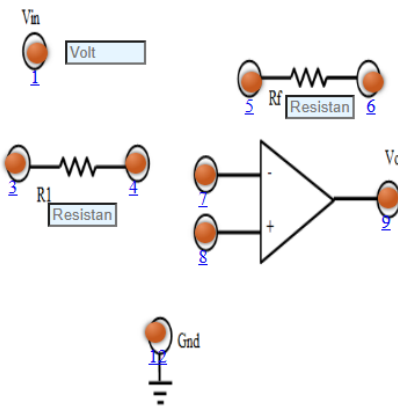


**Virtual Labs**  
An MoE Govt of India Initiative



INSTRUCTION

### Inverting Opamp



CONTROLS

EXPERIMENTAL TABLE

Resistance:  KΩ

Serial No.	Input Voltage V	Output Voltage V	Current mA

Input volt :

Volt

Resistance (R<sub>1</sub>) :

Kohms

Resistance (R<sub>f</sub>) :

Kohms

Add to Table

Plot

Clear

Volt

Amp

Gain

Check connection

Delete all connection

**Virtual Lab Link :**

[https://be-iitkgp.vlabs.ac.in/exp/non-inverting-amplifiers/simulation/inverting\\_opamp.html](https://be-iitkgp.vlabs.ac.in/exp/non-inverting-amplifiers/simulation/inverting_opamp.html)

**Conclusion:** Design and study of an Inverting Amplifier using OP Amp is verified.