

KLS Vishwanathrao Deshpande Institute of Technology



(Accredited by NAAC with "A" Grade)

(Approved by AICTE, New Delhi, Affiliated to VTU, Belagavi)

(Recognized Under Section 2(f) by UGC, New Delhi)

Udyog Vidya Nagar, Haliyal - 581 329, Dist.: Uttara Kannada

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Date: 10.012.2025

Report on Industrial Visit to Kirloskar Electric Company Ltd. Hubballi

Academic Year	2025-26
Date of Workshop	09-12-2025
Program /Activity Name	Hands-on Workshop
Organized By	Department of E&CE in Association with IIC, ECDC and BIS Club
Resource Person / Guest Speaker	Mr. Ravishankar Holla, Assistant Professor, RVCE Bengaluru
Start Date	09-12-2025
End Date	09-12-2025
Number of Students Participants	130
Number of Faculty Participants	04
Location	Department of Electronics and Communication Engineering, KLS VEDIT, Haliyal
Attendee	3 rd Semester Students
Program Name	CPU Design using LogiSim
Mode of Session Delivery	Offline
Objectives	<ul style="list-style-type: none">• Understand the fundamentals of CPU architecture, including ALU, registers, control unit, and data paths.• Identify and explain the role of basic digital components such as multiplexers, decoders, adders, and memory elements in CPU design.• Design and simulate simple combinational and sequential circuits using LogiSim software.
Benefit in terms of Learning / Skill / Knowledge Obtained	<ol style="list-style-type: none">1. Learning Benefits: Gained a clear understanding of CPU architecture and digital system fundamentals.2. Skill Development: Developed skills to construct and test a functional mini-CPU.3. Knowledge Gained: Understood instruction execution flow, data paths, and control signals in CPU operations.

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A hands-on workshop on “CPU Design Using LogiSim Software” was conducted on 9th December 2025 for the 3rd Semester Electronics & Communication Engineering (E&CE) students. The workshop was led by Prof. Ravishankar Holla, who served as the resource person for the session. The primary objective of the workshop was to provide students with practical exposure to 1-bit CPU design using the LogiSim simulation tool.

The session began with an introduction to the fundamental concepts of digital circuits, including logic gates, combinational circuits, and sequential elements that form the basis of CPU architecture. Prof. Ravishankar Holla explained essential CPU components such as the Arithmetic Logic Unit (ALU), registers, control unit, buses, and data paths, ensuring that students developed a clear conceptual understanding before moving to hands-on design.

During the workshop, students were guided through the step-by-step process of constructing a 1-bit CPU, starting with the design of the ALU, implementing register blocks, and developing basic control logic. The resource person demonstrated how these individual modules could be connected and integrated within LogiSim to create a fully functional 1-bit CPU capable of performing simple arithmetic and logical operations.

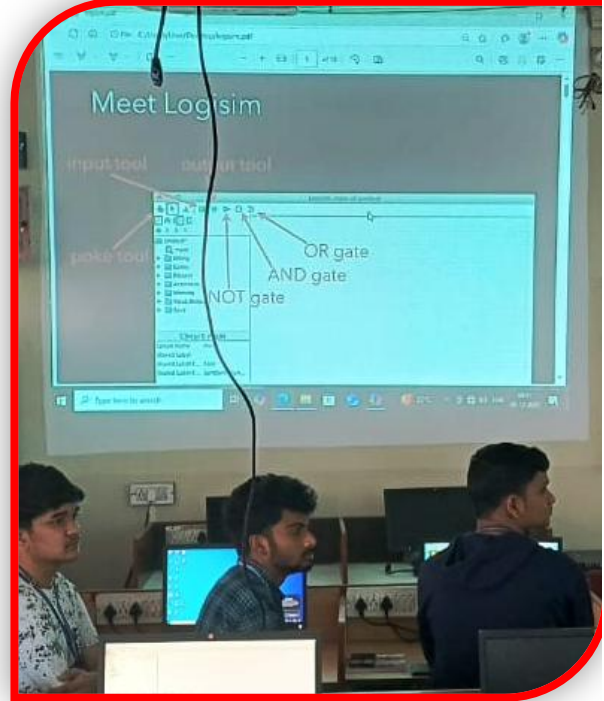
The hands-on nature of the session enabled students to actively engage with LogiSim, experiment with circuit layouts, and debug their designs in real time. This practical experience significantly enhanced their understanding of digital system design and strengthened their analytical and problem-solving skills.

Overall, the workshop proved to be highly beneficial and informative. It provided students with valuable insights into CPU architecture and hands-on proficiency with simulation tools. The department extends its sincere gratitude to Prof. Ravishankar Holla for delivering an interactive, insightful, and effectively structured workshop.

The visit was Organized by Dr. Mahendra Dixit, Head of the Electronics and Communication Department, with coordination from Dr. Nagaraj Bhat and Prof. Nikhil Kulkarni. The event provided valuable industry insights for the students, enriching their academic experience.



Glimpses of Event



Coordinators

HoD

Principal