KLS Vishwanathrao Deshpande Institute of Technology

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

University / Model Question Paper
Scheme & Solution

Faculty Name	:	Prof. Deepak. S. Sharma.
Course Name	:	VLSI Design & Testing
Course Code	:	BEC602.
Year of Question Paper	:	2025
Date of Submission	:	12/02/2026.

Faculty Member

HoD

Dean (Acad.)

CBCS SCHEME

USN

BEC602

Sixth Semester B.E/B.Tech. Degree Examination, June/July 2025
VLSI Design and Testing

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
1	a.	Compare CMOS and NMOS logic.	5	L3	CO1
	b.	With neat diagram, explain the physical representation of transmission gate.	5	L2	CO1
	c.	Design CMOS compound gate for the functions : i) $Y = \overline{A(B+C)+D\bar{E}}$ ii) $Y = \bar{A}B + A\bar{B}$.	10	L3	CO1
		OR			
2	a.	Design D-flip-flop using transmission gates and explain its operation with necessary conditions on LD input.	7	L3	CO1
	b.	Illustrate different alternate circuit representations used in digital circuit designs with an example for each.	6	L2	CO1
	c.	With a neat diagram, explain the physical representation of CMOS inverter.	7	L2	CO1
		Module – 2			
3	a.	With neat diagram, explain the working of nMOS enhancement mode transistor under various voltage conditions.	6	L2	CO2
	b.	How does body effect influences threshold voltage? What are the design strategies to minimize body effect?	6	L2	CO2
	c.	For an nMOSFET, derive the equation for drain current in linear and saturation region.	8	L3	CO2
		OR			
4	a.	Explain the working of pseudo nMOS inverter. Find the output voltage equation for pseudo nMOS inverter.	6	L3	CO2
	b.	Find the expression for V_{out} in region C of CMOS inverter transfer characteristics.	8	L3	CO2
	c.	Illustrate with suitable sketch, latup phenomenon in CMOS circuits and also explain its prevention.	6	L2	CO2
		Module – 3			
5	a.	Illustrate with neat diagram wafer processing and selective diffusion.	6	L2	CO3
	b.	Derive the equation for rise time, fall time and delay time.	8	L3	CO3
	c.	Explain with neat diagram, the process flow of fabricating inverter (CMOS) using Twin-tub process.	6	L2	CO3

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		OR			
6	a.	What is sheet resistance? Estimate the sheet resistance for a given layer having length 'L' and width 'W'.	7	L4	CO3
	b.	Explain the various capacitances in MOS transistor.	6	L2	CO3
	c.	Estimate the total capacitance for the structure as shown in below Fig.Q6(c).	7	L4	CO3

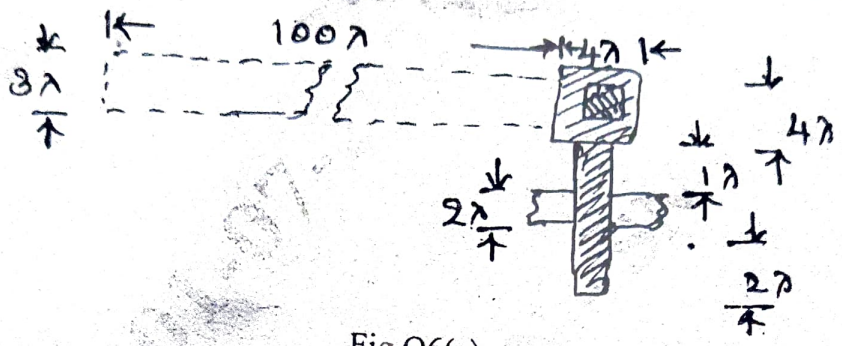


Fig.Q6(c)

Module – 4

7	a.	Differentiate static and dynamic CMOS circuit with relevant diagrams.	7	L3	CO4
	b.	Explain the percharge and evaluate phase in dynamic logic.	6	L2	CO4
	c.	Design a CVSL (Cascade Voltage Switch Logic) based XOR gate.	7	L3	CO4
		OR			
8	a.	Design a 2 : 1 multiplexer using pass transistor logic.	7	L3	CO4
	b.	Draw and explain the layout diagram of a 2 input NAND gate.	6	L2	CO4
	c.	Design a schematic and layout for $Z = (\overline{A + B + CD})$ using Euler's graph.	7	L3	CO4

Module – 5

9	a.	With appropriate neat diagram of two inverter bistable element, explain in detail the voltage transfer characteristics (VTC) and potential energy analogy.	7	L2	CO5
	b.	Explain the operation of SR latch using CMOS NAND2 gates and switch level diagram.	6	L2	CO5
	c.	With neat appropriate diagrams, explain the clocked JK – Latch using NOR2 gates.	7	L2	CO5
		OR			
10	a.	What is structured design strategy? Explain the factors modularity, regularity and locality.	7	L2	CO5
	b.	Distinguish self-test and built-in test with examples.	6	L3	CO5
	c.	Explain with neat diagram, Gate Array Design flow.	7	L2	CO5

* * * * *

1a Compare CMOS and NMOS logic.

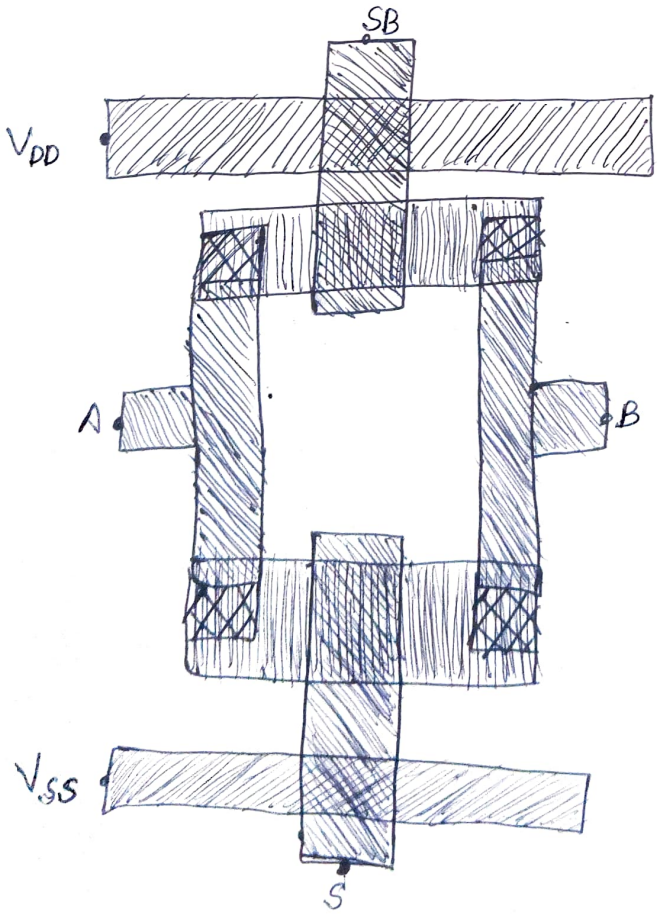
CMOS	NMOS
* Uses both n-type and p-type MOSFETs	* Uses only n-type MOSFET's
* Uses complementary pairs (PMOS+NMOS)	* Requires pullup resistors or load transistor.
* Very low power consumption	* High power consumption
* Degraded logic '0' is good.	* Degraded logic '1' is good '0'
* T_r & T_f are same.	* T_r is slower than T_f
* 2N transistor / gate.	* (N+1) transistor / gate

5M
1m x5

1b). With neat diagram explain physical representation of transmission gate.

5m

Soln:-



3m

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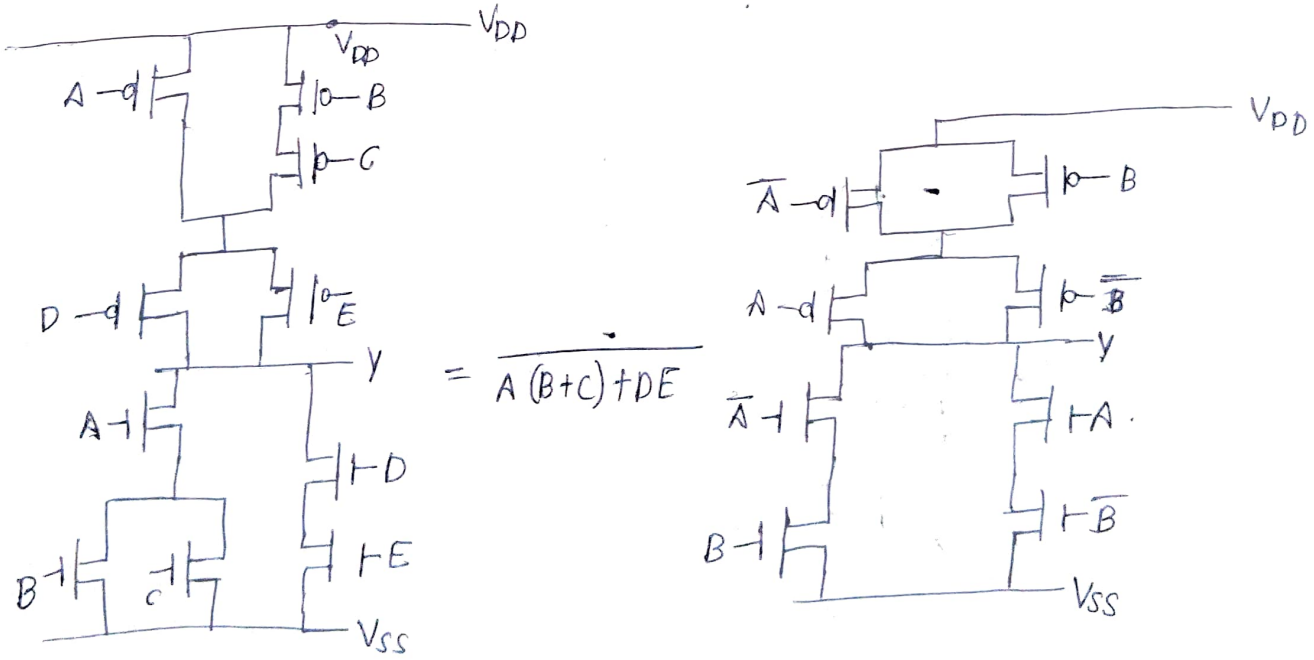
* nMOS & pMOS connected in parallel
* nMOS gate ⟶ control (C)
* pMOS gate ⟶ complement control ($C \bar{C}$) 2m
* Source & drain connected together

Working

* When C=1, both transistors ON that is signal passes.
* When C=0, both OFF that is high impedence.
* Passes both logic '1' & '0' without threshold loss.

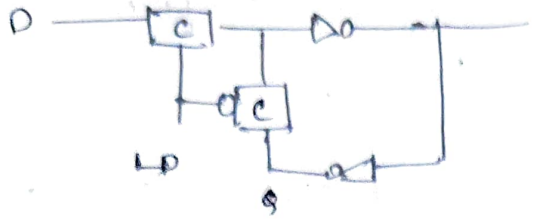
c) Design CMOS Compound Gates. 10m

i) $Y = \overline{A(B+C)+DE}$ 5m ii) $Y = \bar{A}B + B\bar{B}$ 5m



2a) Design D-flip flop using transmission gates. & explain its operation with necessary conditions. on LD input.

7m



LD = 0 & LD = 1.

3m

* consists two latches. in master slave form
* Each gate with one transmission & 2 inverters.

* CLK = 1.
  master transmission gate is ON & slave is OFF.
  Input D is stored the master latch while output unchanged.

4m

* CLK = 0.
  the master transmission gate turns OFF slave turns ON.
  stored value from master latch is transferred to slave.
  appears output Q.

2b) Illustrate different alternate circuit representations used in digital circuit design with an example for each. 6m

3m x 3

⇒ 1) Behavioural representation.
→ This describes what circuit ~~does~~ like does, not how it's built.
→ Expresses input-output relationship using Boolean equivalent or truth tables.
Eg :- NAND gate $Y = \overline{AB}$

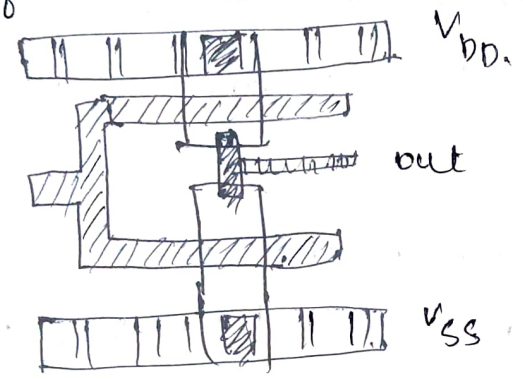
2) Structural Representation.
→ this shows the circuit is built using gates or transistors.
→ It specifies how components are interconnected.
Example :- NAND gate implemented by 2 NMOS & PM

3. Physical Representation.

-> This shows how circuit is laid out on silicon.

-> It includes stick diagrams & layout diagrams showing diffusion polysilicon & metal layers.

20) Explain with neat diagram explain physical representation of CMOS Inverter. 7M



3M

4M

The physical representation of CMOS inverter. shows how the nMOS & pMOS transistors are placed on silicon chip.

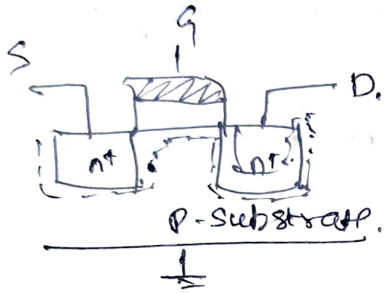
The pMOS transistor is fabricated inside an n-well & placed at top while nMOS transistor is fabricated p-substrate & placed at bottom.

Both transistors have gates connected by common polysilicon line, which forms input of inverter.

The drain terminals of both transistors are connected together using metal to form output & source of PMOS is connected to V_{DD} & source of nMOS is connected to ground.

Module-2

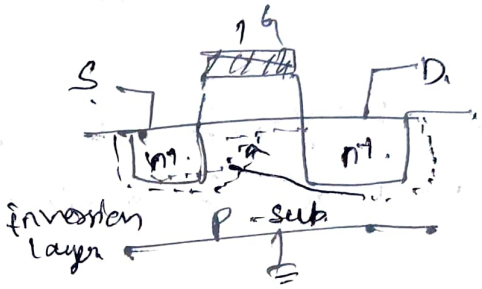
3a) With neat diagram explain working of nMOS enhancement mode transistor under various voltage conditions. 6m



2m

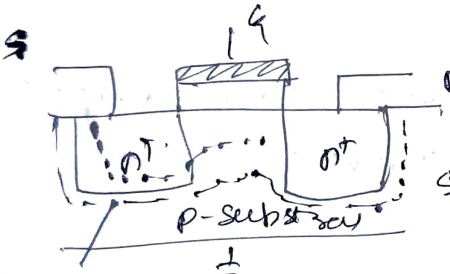
Cutoff.

$V_{GS} \geq V_t$ & $V_{DS} = 0$.



2m

$V_{DS} < V_{GS} - V_t$



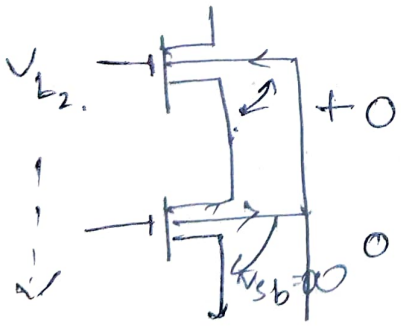
2m

Saturation region

$V_{DS} > V_{GS} - V_t$.

explain

3b) How does body effect influences threshold voltage? What are design strategies to minimize body effect? 6m



3m

$$V_t = V_{t(0)} \pm \sqrt{V_{sb}}.$$

Body effect is the increase in threshold voltage when the source at higher potential than the substrate.

As source to body voltage increases the depletion region widens requires higher gate voltage to turn ON transistor.

3m

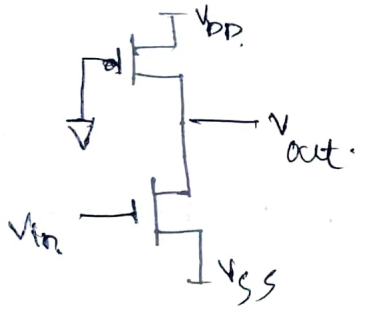
3c) For nMOSFET derive the equation for drain current for linear & saturation region. 8m

$$I_{ds} = \begin{cases} \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] & \text{--> Linear region} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & \text{--- Saturation region.} \end{cases}$$ 4m

* Linear region :- drain current increases both gate voltage & drain voltage.

* Saturation region drain current depends mainly $V_{gs} - V_t$ & becomes independent of V_{DS}. 4m

4a) Explain working of pseudo nMOS inverter. Find output voltage equation for pseudo nMOS inverter. 6m



2m

A pseudo nMOS inverter consists of an always-ON pMOS transistor acting as load & an nMOS transistor driven by input

When input is low the nMOS is OFF & pMOS pulls output high.

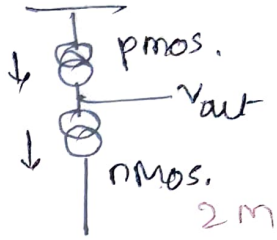
When input high the nMOS turns ON & pulls output low.

$$V_{inv} = V_{tn} \left[\frac{2\beta_p}{\beta_n} \right]^{1/2} \left[(V_{DD} - V_{tp}) V_{sp} - \frac{V_{sp}^2}{2} \right]^{1/2}$$ 4m

4b). Find the expression for V_{out} in region C of CMOS inverter transfer characteristics. 8m

⇒ Drain current nMOS saturation

$$I_{Dn} = \frac{1}{2} \beta_n (V_{in} - V_{tn})^2$$



pMOS saturation.

$$I_{DP} = \frac{1}{2} \beta_p (V_{DD} - V_{in} - |V_{tp}|)^2.$$

2m

At equilibrium

$$I_{Dn} = I_{DP}.$$

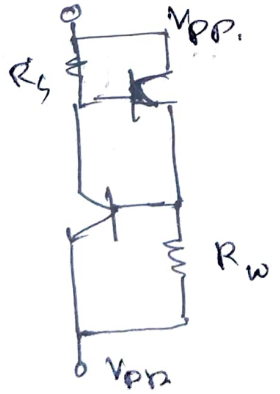
$$\frac{1}{2} \beta_n (V_{in} - V_{tn})^2 = \frac{1}{2} \beta_p (V_{DD} - V_{in} - |V_{tp}|)^2.$$

$$\beta (V_{in} - V_{tn})^2 = \beta_p (V_{DD} - V_{in} - |V_{tp}|)^2. \quad 6m$$

4c) Illustrate with neat diagram ~~wafer processing of~~ selective diff.

4c) Illustrate with suitable sketch. Latch up phenomenon in CMOS circuits & explain prevention 6m

⇒



2m.

Latch-up is caused by parasitic pnp npn transistor pair inside CMOS forming silicon controlled rectifier (SCR) once triggered it creates low resistance path between V_{DD} & GND leading to large current & possible chip damage.

2m

Prevented using

→ rings

→ low resistance substrates.

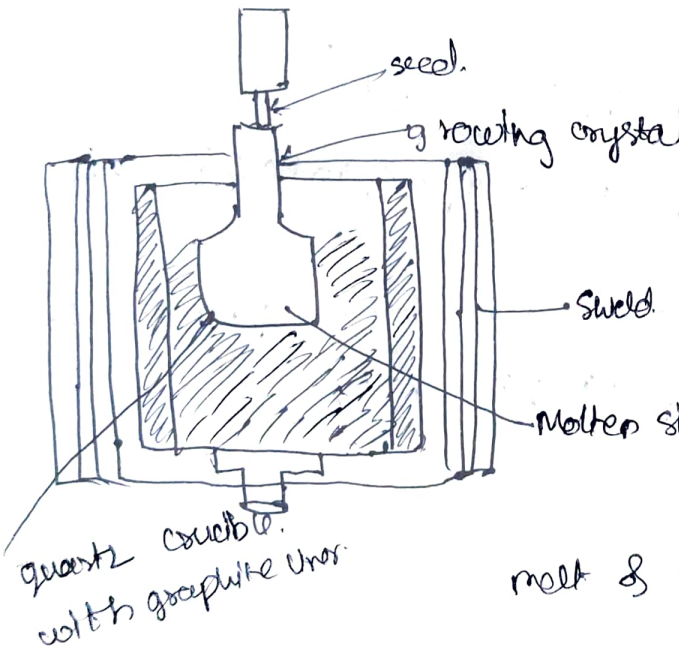
→ Twin tub technologies.

2m

Module-3

5a) Illustrate with neat diagram wafer processing & selective diffusion. 6m

2m



* High purity silicon is melted in quartz crucible. surrounded by graphite radiator & heated using radio frequency induction.

* The temperature maintained slightly above 1425 C with inert gas

* seed crystal is dipped into melt & slowly withdrawn while rotating

* Molten silicon solidifies maintaining single crystal structure of seed.

* The ingot diameter is controlled by withdrawal rate & rotation speed. with growth rates ranging from 30mm h-1 to 180 mm h-1.

2m

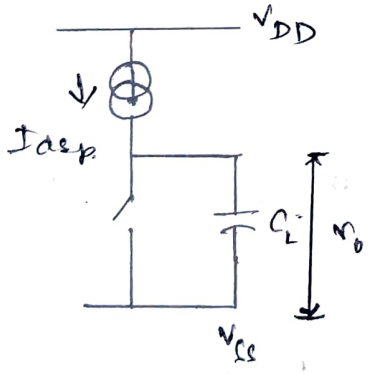
ii) Selective diffusion process 2m

* Selective process used to introduce controlled amounts of donor or acceptor impurities into specific areas of silicon wafer
* The ability of silicon dioxide (SiO_2) to act as diffusion barrier allows precise patterning of doped region.
* Selective diffusion involves the following steps.
* Opening windows in an SiO_2 layer grown on wafer surface
* Removing SiO_2 selectively using a suitable etching technique
* Exposing silicon to controlled dopant to alter its electrical properties.

8m

5b) Derive equation for rise time fall time & delay time.

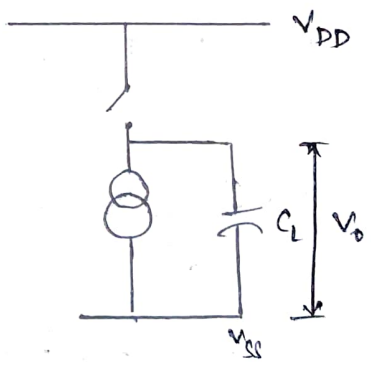
4m



$$t_r \simeq \frac{4 C_L}{\beta_p V_{DD}}$$

$$t_{ar} = \frac{t_r}{2}$$

4m



$$t_f \simeq \frac{4 C_L}{\beta_n V_{DD}}$$

$$t_{af} = t_f / 2.$$

$$\text{delay} = \frac{t_r + t_f}{4}.$$

7c. 5c). Explain with neat diagram process flow of fabricating inverter CMOS using Twin-tub process. 6M

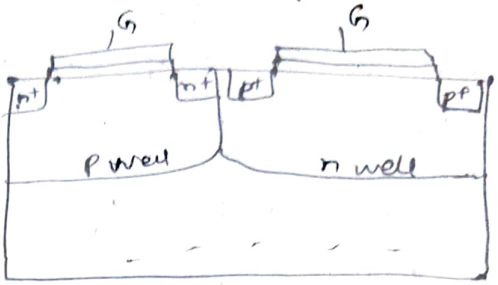
Tub formation 3m

Twin oxide etching

Source & drain Implantation

Contact cut definition

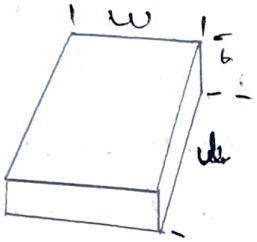
metallization.

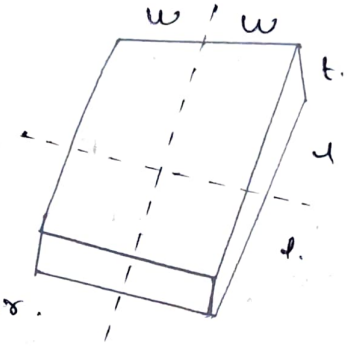


dig 6c) 3m

7m

6a)





$R = \rho \frac{L}{A}$.

$A = W \times t$.

$R = \frac{\rho}{t}\left(\frac{L}{W}\right)$.

$R_S = \frac{\rho}{t}$.

for smaller conductor.

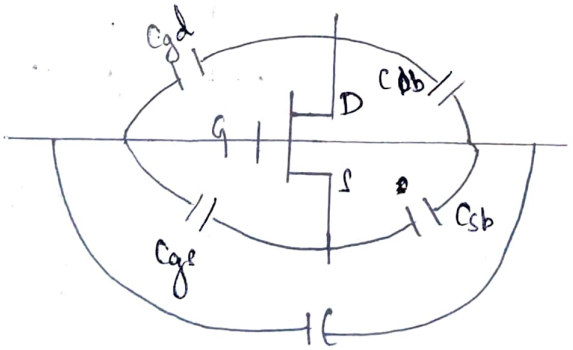
$R = R_S \frac{L}{W} \Omega$.

3rm

for longer conductor

$R = R_S \frac{L}{W} \Omega$. 4m

6b) Explain various capacitances in MOS transistor 6m



3m

$C_g = C_{gb} + C_{gs} + C_{gd}$.

C_{gs} → This capacitance exists between the gate & source.

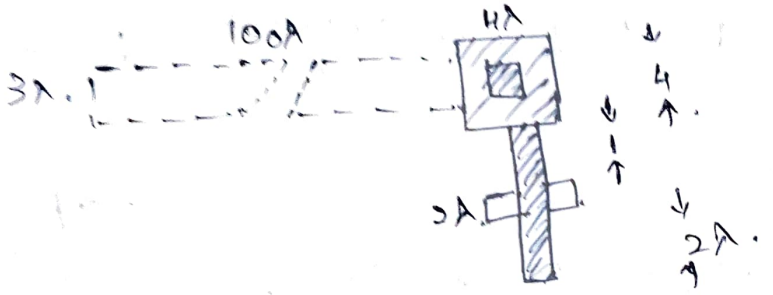
C_{gd} → Gate to drain Capacitance.

C_{gb} → Gate to body Capacitance.

C_{db} → Source to body Junction Capacitance. 3m

7m

6c] Estimate total capacitance for structure. as shown.



3m

$C_{mg} = (3\lambda \times 100\lambda)\, 0.3 \times 10^{-4} = 0.036\text{pF}$.

$C_p = [[(4\lambda \times 4\lambda) + (\lambda \times 2\lambda) \times 2\lambda] \times 0.6 \times 10^{-4}$

$= 0.0053\text{pF}$.

$C_g = (2\lambda \times 2\lambda) \times 5.0 \times 10^{-4}$

$= 0.008\text{pF}$.

$C_T = C_{mg} + C_p + C_p$

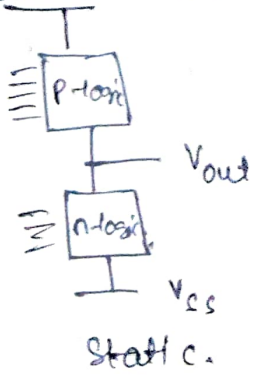
$= 0.049\text{pF}$.

4m

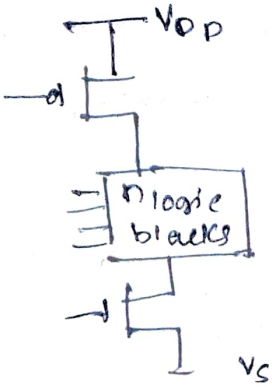
Module-4

7m

7a) Differentiate static & dynamic CMOS circuit.



Static.



4m

3m

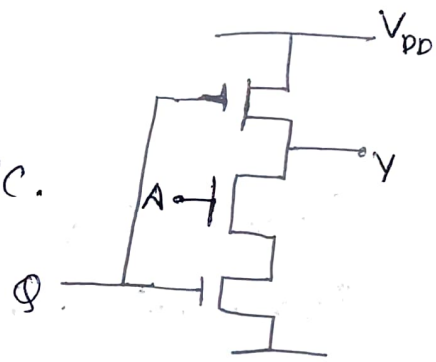
Output is always connected to VDD or GND.	Output is stored as charge.
Does not require clock.	Requires clock.
Maintains output permanently	Stores output temporarily
Very low static power.	Higher leakage power.

7b.) Explain the precharge & evaluate phase in dynamic logic.

6m

Precharge phase.

The clock signal is at logic. low.



* PMOS precharge transistor is turned ON & the dynamic output node is connected to supply voltage (VDD).

3m

As result output node gets charged to high logic level At same time the nMOS evaluation transistor is transistor. is turned OFF. so there is no path between output node & ground

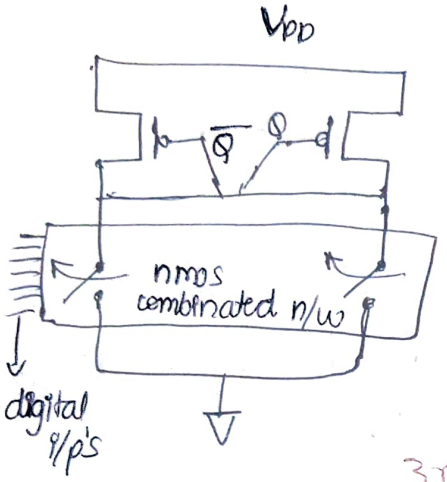
Precharge phase is to initialize the output node or to a known logic value usually logic 1. before evaluation begins.

Evaluation

3m

* Precharge pMOS turns OFF
* The evaluation nMOS turns ON.
* Pull down network becomes active.

7c. 7m



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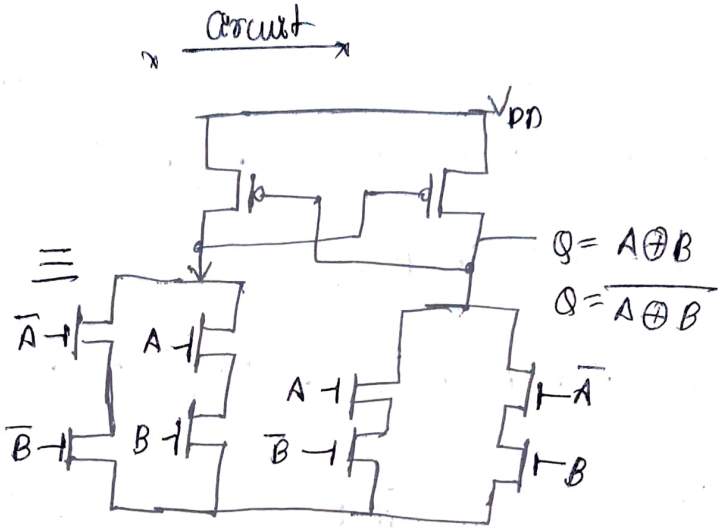
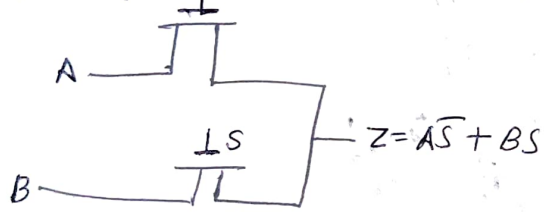


4m

8a. Design $\overline{S}$ 2:1 multiplexer using pass transistor logic. 7m



circuit diagram.

B	Z
0	A
1	B

3m

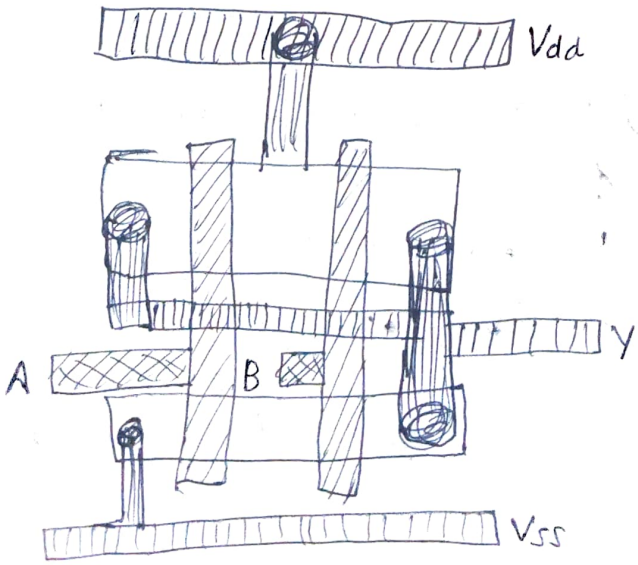
* When S=0 → $\overline{S}$=1 → D0 is passed to output Y
* When S=1 → D1 is passed to output Y.
* Only one pass transistor conducts at time.

4m

6m

8b). Draw & explain the layout diagram of a 2 input NAND.

b.



4m

$Y = \overline{A \cdot B}$

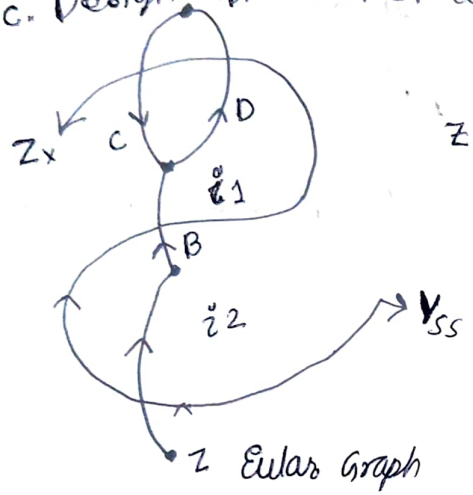
* A 2-input NAND gate is built using 4 transistor.
* 2 PMOS & 2 NMOS (pull down network)
* PMOS transistors are connected in parallel to V_{DD} → output goes HIGH if any input is 0.

2m

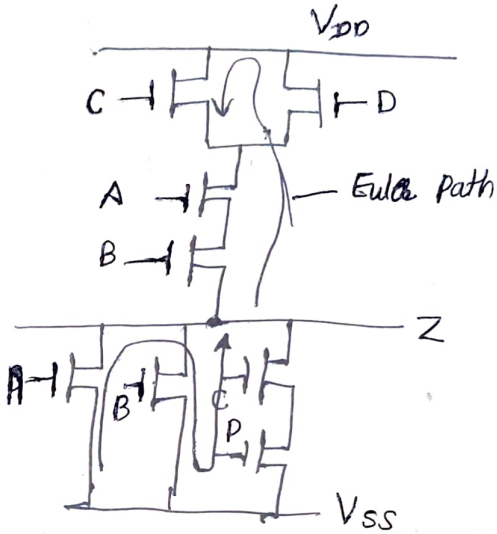
* NMOS transistors are connected in series to GND <-> output goes LOW only when both inputs are 1

* output = NOT (A · B).

c. Design V_{DD} Schematic & layout $Z = \overline{(A+B+CD)}$ using Euler. 7m



$Z = \overline{(A+B+CD)}$



3m

$Z = \overline{(A+B+CD)}$

$Z = \bar{A}\,\bar{B} \cdot (\bar{C} \cdot \bar{D})$.

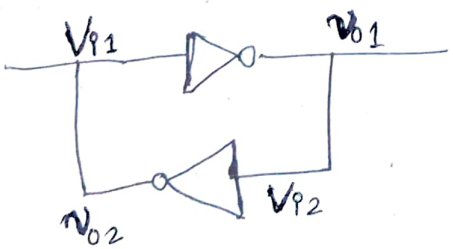
4m

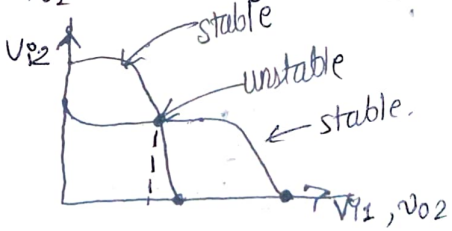
$Z = \bar{A}\,\bar{B}\,C\,(\bar{C}+\bar{D})$.

Module-5

7m

9. a. With appropriate neat diagram of two inverters.





4m

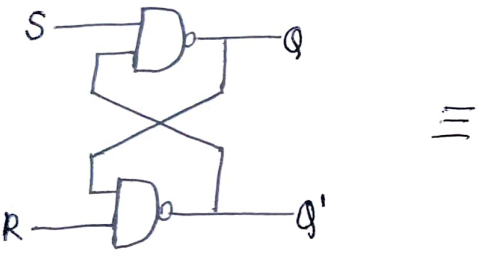
Two inter section points correspond to stable states

One intersection point corresponds to unstable state

Logic 0 stored
Logic 1 stored. 3m

Small disturbances do not change output so ckt remains in that state.
Potential Energy Analogy stable state is represented by peak.

b. SR Latch using NAND:- 6m



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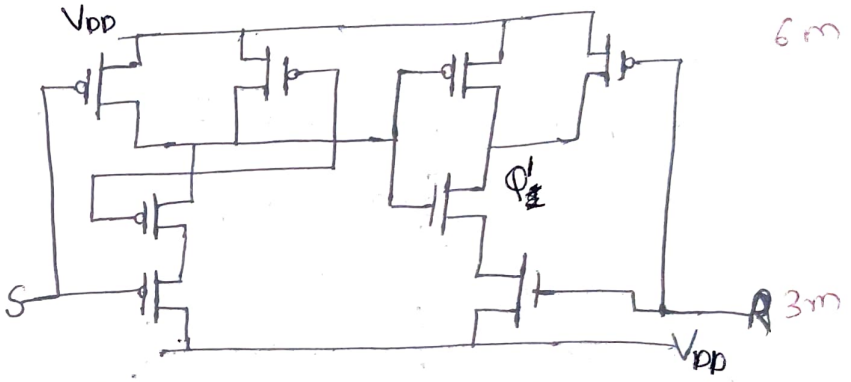


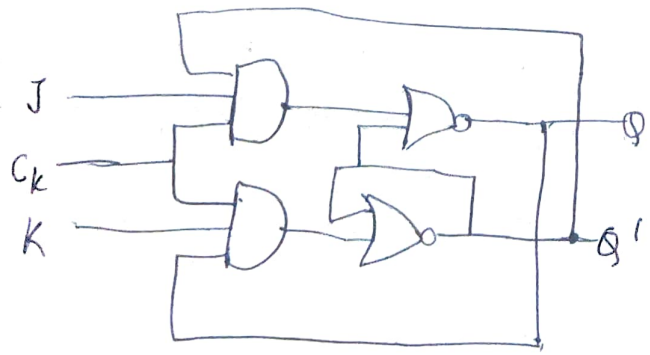
3m

1) $\bar{S}=0$, $\bar{R}=1$. ⇒ As result, Q becomes 1 & $\bar{Q}$ becomes 0

2) Reset $\bar{S}=1$ $\bar{R}=0$
$Q=0$ & $\bar{Q}=1$ The latch is Reset state 3m

3) Hold condition ($\bar{S}=1$ $\bar{R}=1$);
when both inputs are high the outputs remain unchanged & Invalid when. $Q \neq \bar{Q}$.

c. Clocked JK latch using NOR gates. 7m



* Two cross coupled NOR gates forming an SR latch.
* Two additional NOR gates at the input stage.
* A clock input (CLK) that controls the operation.
* J & K two inputs.
* Outputs Q & $\bar{Q}$. 4m

Clk = 0 (Low).

When clock is Low, both Input NOR gates are disabled.

No signal from J or K reaches the latch.

Clk = 1 (High)

Clock is High, the Input NOR gates become active.

Latch responds to J & K.

J=0 K=0. (No change)

J=1 K=0 (Set state) 3m

J=0 K=1 (Reset state)

J=1 K=1. (Toggle state)

10a) What is structured design strategy? Explain the factors modularity regularity & locality. 7m

⇒ ~~Modularity means dividing large system.~~

Structured design strategy is systematic approach used in VLSI system design to handle complexity by organising circuit into well defined & manageable parts. It helps designers develop large & complex systems in efficient reliable & scalable manner. 2m

Modularity :- dividing large & complex VLSI system into smaller, independent functional blocks called modules. Each modules perform specific task & can be designed tested & verified. separately
These modules are then connected to form complete system.
Simplifies design, reduces complexity, improves reliability & makes debugging & modification easier. 2m

Locality :- Means placing related & frequently interacting components close to each other on chip By keeping connected modules nearby the length of interconnections is reduced & noise, delay power consumption. 1 m

Regularity

Refers to use of repeated & uniform structure in VLSI design In regular design the same circuit blocks & layout patterns the same circuit blocks & layout patterns are used many times throughout chip. 2m

10b) Distinguish self-test & built-in test. 6m

⇒ Self test refers to testing method in which IC is tested using external test equipment.

-> The test patterns are generated outside the chip & applied through input pins. The output response is then observed using external instruments.

-> Requires ATE & depends on external instruments for fault

⇒ Built-In Test :- Is testing technique in which testing circuitry is included inside the chip itself

-> The circuit generates own test patterns applies them internally & analyses out put response without external equipment

10 c). Explain Gate Array Design flow

⇒ Gate array design flow. Is semi custom VLSI. design approach is which prefabricated. transistor arrays used. & only metal interconnections are customised.

the design process starts with logic design & verification the circuit is mapped onto predefined. gate array Placement & routing of interconnection. are customized.

the design process starts with logic design & verification Next, the circuit is mapped onto predefined gate. array. Placement & routing of interconnection are. then performed. After this design rule checking & layout rectification are carried out. Finally chip is fabricated. by metal layers.

This reduces design time & cost compared to full custom design & is. suitable for medium-complexity circuit.