CBCS SCHEME

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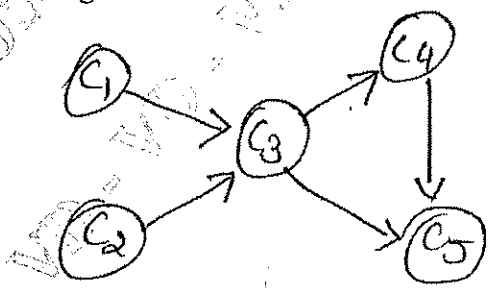
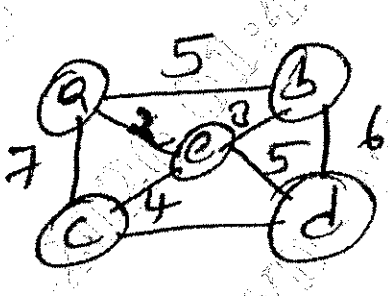
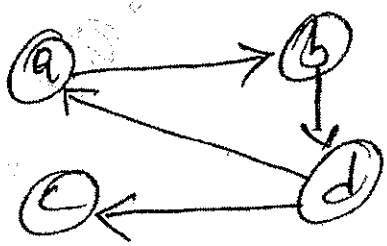
BCS401

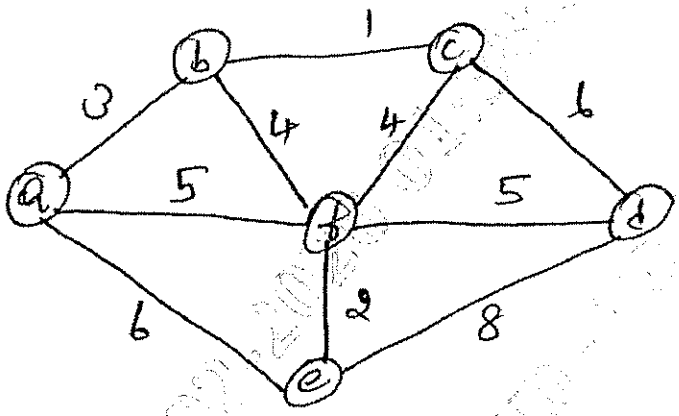
Fourth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Analysis and Design of Algorithms

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define algorithm with the help of flow chart, explain the various stages of algorithm's design and analysis process.	10	L2	CO1
	b.	Compare the order of 1/2 .n (n-1) and n^2.	4	L3	CO1
	c.	List and explain asymptotic notations used to compare the orders of growth of an algorithm, with an example each.	6	L3	CO1
		OR			
Q.2	a.	Give the general plan for analyzing the time efficiency of recursive algorithm show that efficiency of tower of Hanoi is exponential.	10	L2	CO1
	b.	Prove that if $t_1(n) \in 0(g_1(n))$ and $t_2(n) \in 0(g_2(n))$, then $t_1(n) + t_2(n) \in 0\{\max g_1(n), g_2(n)\}$.	4	L3	CO1
	c.	Solve the following recurrence $x(n) = x(n-1) + 5$ for $n > 1$, $x(1) = 0$	6	L3	CO1
		Module – 2			
Q.3	a.	Define Divide and Conquer. Design an algorithm for merge sort and sort the list "EXAMPLE" in alphabetical order using merge sort.	10	L3	CO2
	b.	Design an algorithm for quick sort. Sort the list 65, 70, 75, 80, 85, 60, 55, 50, 45. Also derive the worst case complexity of quick sort.	10	L3	CO2
		OR			
Q.4	a.	Define decrease and conquer technique. What are the three major variations of decrease and conquer technique? Obtain the topological ordering for the following graph. Using source removal method.  Fig.Q.4(a)	10	L3	CO2

	b.	Design an algorithm to sort N number of elements using insertion sort. Illustrate the tracing of insertion sort algorithm for the following set of numbers 25, 10, 72, 18, 40, 11, 64, 58, 32, 9.	10	L3	CO2
		Module – 3			
Q.5	a.	What is heap? Design an algorithm to construct a heap for the elements of the given array by bottom up approach. Show heap construction of the given list 2, 9, 7, 6, 5, 8 by successive insertion using bottom up procedure.	10	L2	CO3
	b.	What is AVL tree? Explain the four types of rotations used to construct the AVL tree. Construct AVL tree for the set 5, 6, 8, 3, 2, 4, 7 by successive insertion.	10	L3	CO3
		OR			
Q.6	a.	Apply Horse Pool's algorithm to search for the pattern DEMOCRATIC from the text INDIA_IS_A_DEMOCRATIC_COUNTRY. Explain its working along with a neat shift table and algorithm to find the pattern string.	10	L3	CO3
	b.	Design an algorithm for comparision counting sort. Apply the same to sort the list 62, 31, 84, 96, 19, 47.	10	L3	CO3
		Module – 4			
Q.7	a.	Apply Kruskal's algorithm to find minimum cost spanning tree to the graph shown below source = a ;  Fig.Q.7(a)	10	L3	CO4
	b.	Explain the Warshall's algorithm to find the transitive closure of a directed graph. Apply it to the following graph.  Fig.Q.7(b)	10	L3	CO4

		OR			
Q.8	**a.**	Construct a minimum cost spanning tree using prims algorithm for the following graph source = 'a'.  Fig.Q.8(a)	**10**	**L3**	**CO4**
	b.	What is Huffman Tree? Explain the algorithm to construct the Huffman tree. Construct the Huffman tree for the following data: Character: A, B, C, D, - Probability: 0.35, 0.1, 0.2, 0.2, 0.15	**10**	**L3**	**CO4**
		Module – 5			
Q.9	**a.**	Using Branch and Bound technique solve the below instance of knapsack problem. Item / Weight / Value: 1 / 2 / 12; 2 / 1 / 10; 3 / 3 / 20; 4 / 2 / 5 Capacity = 5	**10**	**L3**	**CO6**
	b.	Define Backtracking. Apply backtracking to solve the instance of the sum of subset problem s = {3, 5, 6, 7} and d = 15.	**10**	**L3**	**CO6**
		OR			
Q.10	**a.**	Explain the concept of P, NP, NP – complete and NP-Hard problem.	**10**	**L2**	**CO5**
	b.	What are Decision Trees? Explain with example, how decision trees are used in sorting algorithms.	**10**	**L2**	**CO6**

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BCS402

Fourth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Mention the difference between : i) Microprocessor and Microcontroller ii) CISC and RISC architectures	8	L2	CO1
	b.	With a neat diagram, explain ARM core dataflow model.	6	L2	CO1
	c.	With a neat diagram, explain embedded system hardware.	6	L2	CO1
		OR			
Q.2	a.	Explain the various modes of operation of ARM processor and banked registers.	8	L2	CO1
	b.	What is a pipeline? With neat diagram explain the various blocks in a 3-stage pipeline of ARM processor organization.	6	L2	CO1
	c.	Discuss the various fields in CPSR with neat sketch.	6	L2	CO1
		Module – 2			
Q.3	a.	With example illustrate how following instructions work. i) MLA ii) MUL iii) SMLAL iv) UMULL.	8	L3	CO2
	b.	Explain Single register load store addressing mode syntax, table index mode with an example.	8	L2	CO2
	c.	Explain Barrel shifter operation in ARM processor with neat diagram. If $r_5 = 5$, $r_7 = 8$ using the following instructions, write values of r_5, r_7 after execution of MOV r_7, r_5, LSL # 2.	4	L2	CO2
		OR			
Q.4	a.	Along with suitable examples describe various logical and comparison instructions.	8	L2	CO2
	b.	Discuss the Branch instructions and SWAP instructions with example.	8	L2	CO2
	c.	Explain briefly co-processor instructions of ARM processor.	4	L2	CO2
		Module – 3			
Q.5	a.	Explain basic C-Data types with example codes.	10	L2	CO3
	b.	Discuss how Registers are allocated to optimize the program.	10	L2	CO3

		OR			
Q.6	**a.**	Explain C looping structures with example codes.	**10**	**L2**	**CO3**
	b.	Explain function calls and pointer Aliasing with example codes.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With a neat sketch, explain exceptions and associated modes.	**10**	**L2**	**CO4**
	b.	With the help of vector table, explain processor modes. Also mention the exception priority levels.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain interrupt latency, IRQ and FIQ exceptions in detail with neat sketches.	**10**	**L2**	**CO4**
	b.	Explain Firmware and bootloader, with sand stone example, explain detail directory layout.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	With neat diagram, explain the relationship of cache between processor core and main memory.	**8**	**L2**	**CO5**
	b.	With neat sketch, explain set associatively.	**8**	**L2**	**CO5**
	c.	Explain logical and physical cache with neat diagram.	**4**	**L2**	**CO5**
		OR			
Q.10	**a.**	Briefly, explain cache policies.	**8**	**L2**	**CO5**
	b.	Explain direct mapped cache and thrashing.	**8**	**L2**	**CO5**
	c.	Write short note on co-processor 15.	**4**	**L2**	**CO5**

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CBCS SCHEME - Make-Up Exam

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BCS402

Fourth Semester B.E/B.Tech. Degree Examination, June/July 2025
Microcontrollers

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Differentiate between RISC and CISC processors.	4	L2	CO1
	b.	Explain ARM core data flow model with neat diagram.	8	L2	CO1
	c.	Explain different processor modes provided by ARM7.	8	L2	CO1
		OR			
2	a.	Explain the architecture of a typical embedded device based in ARM core, with a neat diagram.	8	L2	CO1
	b.	Explain the various fields in the current program status register with a neat layout.	6	L2	CO1
	c.	What is pipeline in ARM? Explain the different pipeline stages of ARM9 processor.	6	L2	CO1
		Module – 2			
3	a.	Discuss the load-store instruction with respect to, (i) Single Register Transfer (ii) Multiple Register Transfer	8	L2	CO2
	b.	Explain different arithmetic instructions in ARM processor with an example.	8	L2	CO2
	c.	Explain the multiply instructions of ARM processor.	4	L2	CO2
		OR			
4	a.	Write a ALP to find the Sum of first 10 integer numbers.	6	L3	CO2
	b.	Explain the ARM single-Register and Multiple-Register load-store addressing modes with example.	8	L2	CO2
	c.	Explain the different branch instructions of ARM processor.	6	L2	CO2

		Module – 3			
5	a.	Write a program in C for ARM microcontroller to find factorial of a number.	**6**	**L3**	**CO3**
	b.	Explain why we should avoid using char data type for local variables, with suitable example.	**8**	**L3**	**CO3**
	c.	List and explain different portability issues.	**6**	**L2**	**CO3**
		OR			
6	a.	Discuss how registers are allocated to optimize the program.	**6**	**L3**	**CO3**
	b.	Explain the concept of Loop unrolling with suitable example.	**6**	**L3**	**CO3**
	c.	Explain four register rule used in function calls and also explain the benefits of using a structure pointer in code taking a suitable example.	**8**	**L3**	**CO3**
		Module – 4			
7	a.	With a neat diagram, explain ARM processor exceptions and modes.	**10**	**L2**	**CO4**
	b.	Explain assigning interrupts and interrupt latency.	**10**	**L2**	**CO4**
		OR			
8	a.	Briefly explain what happens when an IRQ and FIQ exception is raised, with an ARM processor.	**10**	**L2**	**CO4**
	b.	Explain firmware execution flow and explain Red Hat Red Boot.	**10**	**L2**	**CO4**
		Module – 5			
9	a.	Explain the basic architecture of cache memory.	**10**	**L2**	**CO5**
	b.	Explain how main memory maps to a cache memory.	**5**	**L2**	**CO5**
	c.	Explain the basic operation of a cache controller.	**5**	**L2**	**CO5**
		OR			
10	a.	Briefly explain Cache line replacement policies.	**8**	**L2**	**CO5**
	b.	Explain briefly the allocation policy on a Cache Miss.	**6**	**L2**	**CO5**
	c.	Explain the following : (i) Write Buffers (ii) Measuring Cache efficiency (iii) Write policy	**6**	**L2**	**CO5**

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BCS402

Fourth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Mention the difference between : i) Microprocessor and Microcontroller ii) CISC and RISC architectures	8	L2	CO1
	b.	With a neat diagram, explain ARM core dataflow model.	6	L2	CO1
	c.	With a neat diagram, explain embedded system hardware.	6	L2	CO1
		OR			
Q.2	a.	Explain the various modes of operation of ARM processor and banked registers.	8	L2	CO1
	b.	What is a pipeline? With neat diagram explain the various blocks in a 3-stage pipeline of ARM processor organization.	6	L2	CO1
	c.	Discuss the various fields in CPSR with neat sketch.	6	L2	CO1
		Module – 2			
Q.3	a.	With example illustrate how following instructions work. i) MLA ii) MUL iii) SMLAL iv) UMULL.	8	L3	CO2
	b.	Explain Single register load store addressing mode syntax, table index mode with an example.	8	L2	CO2
	c.	Explain Barrel shifter operation in ARM processor with neat diagram. If $r_5 = 5$, $r_7 = 8$ using the following instructions, write values of r_5, r_7 after execution of MOV r_7, r_5, LSL # 2.	4	L2	CO2
		OR			
Q.4	a.	Along with suitable examples describe various logical and comparison instructions.	8	L2	CO2
	b.	Discuss the Branch instructions and SWAP instructions with example.	8	L2	CO2
	c.	Explain briefly co-processor instructions of ARM processor.	4	L2	CO2
		Module – 3			
Q.5	a.	Explain basic C-Data types with example codes.	10	L2	CO3
	b.	Discuss how Registers are allocated to optimize the program.	10	L2	CO3

		OR			
Q.6	**a.**	Explain C looping structures with example codes.	**10**	**L2**	**CO3**
	b.	Explain function calls and pointer Aliasing with example codes.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With a neat sketch, explain exceptions and associated modes.	**10**	**L2**	**CO4**
	b.	With the help of vector table, explain processor modes. Also mention the exception priority levels.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain interrupt latency, IRQ and FIQ exceptions in detail with neat sketches.	**10**	**L2**	**CO4**
	b.	Explain Firmware and bootloader, with sand stone example, explain detail directory layout.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	With neat diagram, explain the relationship of cache between processor core and main memory.	**8**	**L2**	**CO5**
	b.	With neat sketch, explain set associatively.	**8**	**L2**	**CO5**
	c.	Explain logical and physical cache with neat diagram.	**4**	**L2**	**CO5**
		OR			
Q.10	**a.**	Briefly, explain cache policies.	**8**	**L2**	**CO5**
	b.	Explain direct mapped cache and thrashing.	**8**	**L2**	**CO5**
	c.	Write short note on co-processor 15.	**4**	**L2**	**CO5**

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USN | | | | | | | | | | |

BAD402

Fourth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Artificial Intelligence

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define AI. Explain the foundation of AI in detail.	10	L2	CO1
	b.	Explain the historical development of AI, highlighting key milestones and breakthroughs.	10	L2	CO1
		OR			
Q.2	a.	Briefly explain the properties of Task Environment.	10	L2	CO1
	b.	Explain the following with respect to structure agents: (i) Simplex reflex (ii) Model based reflex (iii) Utility based	10	L2	CO1
		Module – 2			
Q.3	a.	Discuss how problem solving agents interact with their environments.	10	L2	CO2
	b.	Explain the principles of breadth-first search as a problem solving strategy with an example.	10	L2	CO2
		OR			
Q.4	a.	Discuss the different solutions and metrics for searching.	10	L2	CO2
	b.	Explain Goal Formulation and Problem Formulation with examples.	10	L2	CO2
		Module – 3			
Q.5	a.	Define informed search strategies in the context of AI. Difference between Informed and Uninformed search strategies.	10	L2	CO3
	b.	Explain A^* algorithm. Give one example where A^* is suitable is suitable to apply.	10	L2	CO3
		OR			
Q.6	a.	Describe the principles of greedy best first search as an informed search strategy. How does it make use of heuristic information?	10	L2	CO3
	b.	Explain the following with examples: (i) Logical Equivalence (ii) Inference Rules (iii) Horn Clauses	10	L2	CO3
		Module – 4			
Q.7	a.	Provide examples of how inference can be applied to draw conclusions in a given knowledge base represented FOL.	10	L2	CO4
	b.	Explain the propositional syntax and semantics of First Order Logic (FOL).	10	L2	CO4
		OR			
Q.8	a.	Describe the principles of forward chaining in FOL. Provide examples to illustrate how forward chaining works in practice.	10	L2	CO4
	b.	Outline the process of backward chaining in FOL. Provide examples to illustrate how forward chaining works in practice.	10	L2	CO4
		Module – 5			
Q.9	a.	Explain the inference using full joint distribution.	10	L2	CO5
	b.	Explain Baye's rule and its use in detail.	10	L2	CO5
		OR			
Q.10	a.	Define Expert Systems. Explain the components of Expert System with a neat diagram. Also list its capabilities and incapabilities.	10	L2	CO5
	b.	Explain: (i) Knowledge Shell (ii) Knowledge Acquisition.	10	L2	CO5

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