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Report on Two-Day Hands-on Workshop on VLSI Design

Date: 27th & 28th November 2025
Participants: 5th Semester Students, Department of E&EE

- A two-day hands-on workshop on **VLSI Design** was organized for the 5th semester students of the E&EE branch on 27th and 28th November 2025.

- The workshop aimed to introduce students to the fundamentals of **Very Large-Scale Integration (VLSI)** and provide practical exposure to industry-standard design methodologies.

- Prof. Deepak Sharma delivered structured sessions covering **basic concepts of VLSI**, including CMOS logic, design flow, and an overview of fabrication processes.

- Participants gained hands-on experience in using **Cadence Design Suite**, a widely used professional EDA tool in semiconductor industries.

- Students practiced the complete **schematic design flow**, including symbol creation, circuit connectivity, parameter entry, and schematic verification through Design Rule Checks (DRC) and simulation.

- The sessions guided students through the **layout design flow**, enabling them to draw custom layouts, understand design layers, and validate their work using Layout Versus Schematic (LVS) checks.

- Attendees reported improved understanding of the **overall VLSI design pipeline**, from concept to layout validation.

- The workshop was useful to the Students which

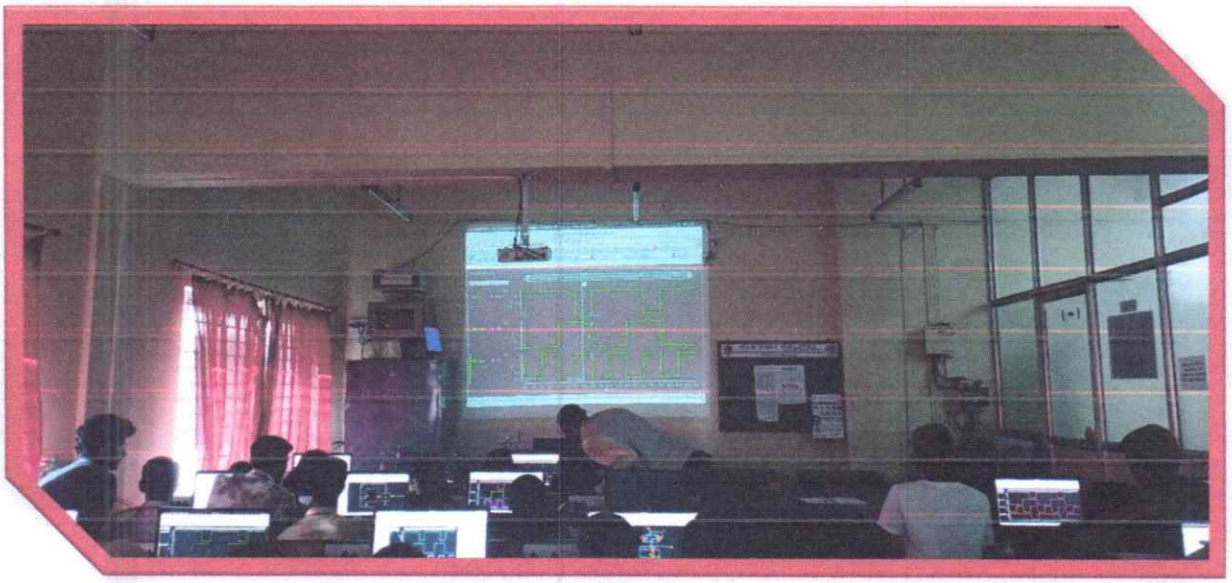
  - Helped them understand the **basics of VLSI design**.
  - Provided meaningful **hands-on exposure to Cadence** industrial tools.

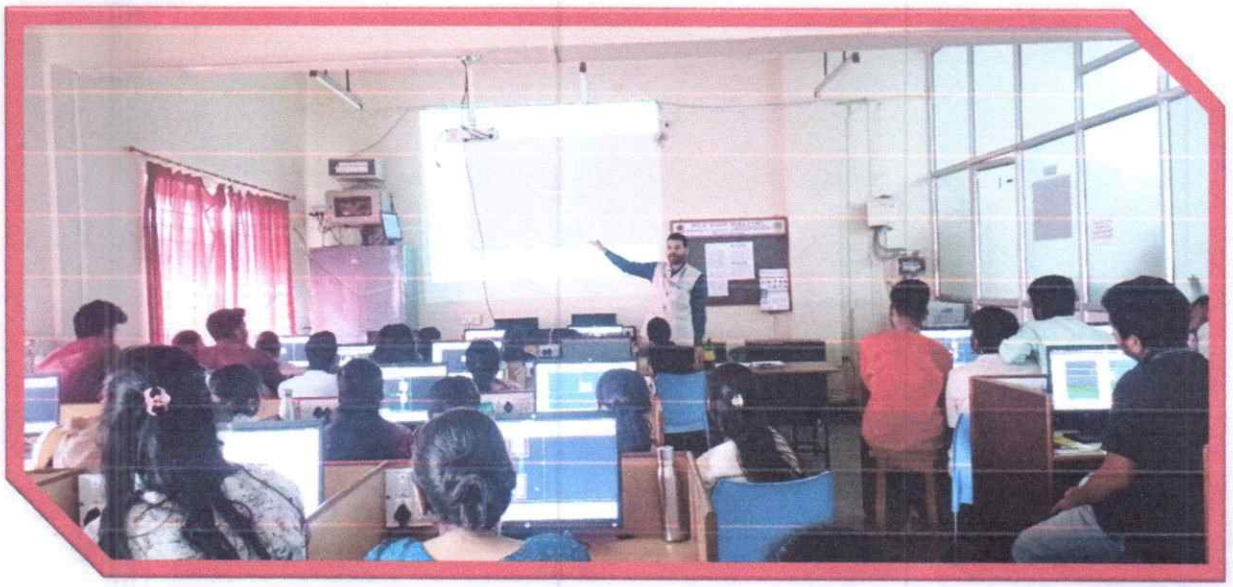
- Enabled clear understanding of the **schematic creation and verification flow**.
- Clarified the steps involved in **layout design and its validation** using Cadence.

- The workshop enhanced design skills, improved tool familiarity, and motivated students to explore advanced concepts in VLSI and semiconductor technology.

- The event concluded with positive feedback, with students expressing interest in **advanced-level workshops and project-based training** in VLSI.

Glimpses of the Event





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