CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define the following : i) Canonical SOP ii) Canonical POS iii) Essential Prime Implicant (EPI) iv) Prime Implicant (PI) v) Min term and Max term with a table of two input variable representation	10	L1	CO1
	b.	Using Quine Mccluskey method and PI reduction table, determine the minimal SOP expression for the following function. $Y = f(a, b, c, d) = \Sigma(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$	10	L3	CO1
		OR			
Q.2	a.	Explain the procedure to place SOP and POS equations into canonical form convert the following equations into canonical forms i) $T = f(a, b, c) = (a + b')(b' + c)$ ii) $G = f(w, x, y, z) = w'x + yz'$	10	L3	CO1
	b.	Solve the given functions using Kamangh Map i) $F = f(w, x, y, z) = \Sigma(0, 7, 8, 9, 10, 12) + \Sigma d(2, 5, 13)$ ii) $G = f(a, b, c, d) = \pi(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ Also identify the prime implicants.	10	L3	CO1
		Module – 2			
Q.3	a.	Implement the function using multiplexers i) $f(x, y, z) = \Sigma m(0, 2, 3, 5)$ using 4 × 1 multiplexer ii) $f(w, x, y, z) = \Sigma m(0, 1, 5, 6, 7, 9, 12, 15)$ using 8 × 1 multiplexer.	10	L2	CO2
	b.	Explain the concept of carry look ahead adder with related equation and block diagram.	10	L2	CO2
		OR			
Q.4	a.	Using a 4-bit binary adder, design a logic to convert a decimal digit in 8421 code into a decimal adder.	10	L3	CO2
	b.	Implement the following functions using 3 : 8 decoder. i) $P = f(w, x, y, z) = \Sigma(1,4, 8, 13)$ $Q = g(w, x, y, z) = \Sigma(2, 7, 13, 14)$ ii) $A = f(x, y, z) = \pi(0, 1, 3, 5)$ $B = f(x, y, z) = \Sigma(1, 4, 5, 7)$	10	L3	CO2

		Module – 3			
Q.5	**a.**	Explain master slave JK flip-flop with the help of circuit diagram and timing diagrams.	**10**	**L2**	**CO3**
	b.	Design a synchronous Mod -6 counter with sequence 0-2-3-6-5-1 using JK flip-flop.	**10**	**L3**	**CO3**
		OR			
Q.6	**a.**	Design a 4-bit binary ripple up counter with logic diagram and counting sequence and explain its operation.	**10**	**L3**	**CO3**
	b.	With the help of logic diagram and counting sequence, explain. i) Ring counter ii) Mod – 8 twisted ring counter.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	What are the different data types in verilog. Explain with examples.	**10**	**L2**	**CO4**
	b.	i) Develop a verilog program to implement 2×1 multiplexer using conditional operator. Also write the truth table of 2×1 mux ii) Design a 2×1 multiplexer using dataflow verilog description draw a logic diagram and logic gate level circuit for it.	**4** **6**	**L3** **L3**	**CO4** **CO4**
		OR			
Q.8	**a.**	Discuss in detail different description styles in verilog.	**8**	**L2**	**CO4**
	b.	Let A = 5' b11011, B = 5' b 10101 C = 4' d3 Determine the output the following verilog statements. i) d = & A ii) e = ~^ 4' b1011 iii) f = ~ (A & (~B)) iv) g= A| |B v) b = 3** 2 vi) i = {2{A}}	**12**	**L3**	**CO4**
		Module – 5			
Q.9	**a.**	Design a 4-bit counter with synchronous hold using verilog. Also draw the simulation waveform.	**10**	**L3**	**CO5**
	b.	Explain the operation of positive edge triggered JK flip-flop by using a verilog code using case statement. Write truth table and timing diagram.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain the operation of half adder and implement using structural description in verilog.	**6**	**L2**	**CO5**
	b.	Write the verilog format of case statement and explain.	**4**	**L2**	**CO5**
	c.	Develop a verilog behavioral description for 3 bit binary up counter.	**6**	**L3**	**CO5**
	d.	Develop a verilog program for D latch using behavioral description style.	**4**	**L3**	**CO5**

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CBCS SCHEME

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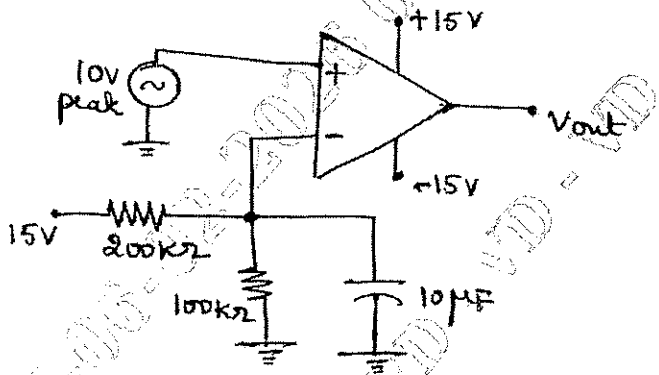
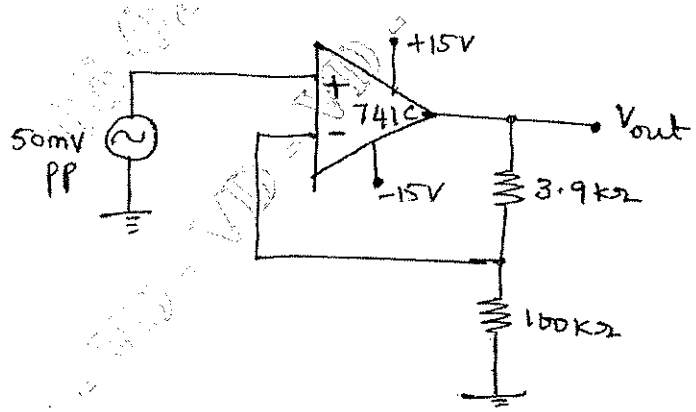
BEC303

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Electronic Principles and Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Develop an expression for the operating point I_C and V_{CE} for the voltage divider bias circuit using approximate analysis. Hence calculate the operating point for the VDB circuit given : $V_{CC} = 10V$, $R1 = 10K\Omega$, $R2 = 2.2\ K\Omega$, $R_C = 3.6K\Omega$, $R_E = 1\ K\Omega$.	10	L3	CO1
	b.	For the voltage divider biased amplifier, derive the expression for the voltage gain from i) π –Model ii) T –Model.	10	L2	CO1
		OR			
Q.2	a.	Develop an expression for voltage gain and input impedance for an emitter follower with neat circuit diagram.	10	L2	CO1
	b.	Determine the operating point for two supply emitter bias circuit given : $V_{CC} = 10V$, $R_C = 3.6\ K\Omega$, $R_B = 2.1\ K\Omega$, $R_E = 1\ K\Omega$ and $-V_{EE} = -2V$.	5	L2	CO1
	c.	Develop an expression for the operating point I_C and V_{CE} for collector feedback bias circuit.	5	L2	CO1
		Module – 2			
Q.3	a.	With neat circuit diagrams, explain biasing of MOSFET by fixing the gate voltage.	10	L2	CO2
	b.	With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common source amplifier with source resistance.	10	L2	CO2
		OR			
Q.4	a.	With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common gate amplifier.	10	L2	CO2
	b.	Define transconductance and hence develop any three expressions for transconductance.	10	L2	CO4

		Module – 3			
Q.5	**a.**	With neat circuit diagram, explain the operation of R-2R digital to analog converter.	**6**	**L2**	**CO4**
	b.	For the circuit shown in Fig.Q5(b) the input voltage is a sine wave with peak value of 10V. What is the trip point of the circuit? Determine the cut off frequency of bypass capacitor. Also draw the input output waveform.  Fig.Q5(b)	**6**	**L3**	**CO4**
	c.	Explain the operation of inverting Schmitt-trigger with neat circuit diagram and waveform.	**8**	**L2**	**CO4**
		OR			
Q.6	**a.**	Make use of the concept of lead-lag circuit to explain the operation of Wein bridge oscillator.	**10**	**L2**	**CO4**
	b.	Explain the operation of Astable Multi-Vibrator using 555 timer with internal block diagram and waveforms.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With neat block diagram, explain four types of negative feedback circuit.	**8**	**L2**	**CO3**
	b.	For the circuit shown in Fig.Q7(b), calculate the feedback fraction, the ideal closed loop voltage gain, the percent error and the exact closed loop voltage gain, use the open loop gain of 741C as 100,000.  Fig.Q7(b)	**6**	**L2**	**CO3**
	c.	With neat circuit diagram and equations, explain the operation of a current amplifier.	**6**	**L2**	**CO3**

		OR			
Q.8	**a.**	Classify filters and explain each filter with its ideal frequency response.	**10**	**L2**	**CO3**
	b.	What is First Order Filters? Explain the various implementation of first order low pass and high pass active filters with expressions.	**10**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Explain the operation of class–B push pull emitter follower amplifier with its advantages and disadvantages.	**10**	**L2**	**CO5**
	b.	Discuss the concepts of DC and AC load line taking voltage divider bias amplifier as an example.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain the working of SCR phase control with the help of circuit and waveform.	**10**	**L2**	**CO5**
	b.	Explain the construction, control and advantages of Insulated-Gate Bipolar Transistor (IGBT).	**10**	**L2**	**CO5**

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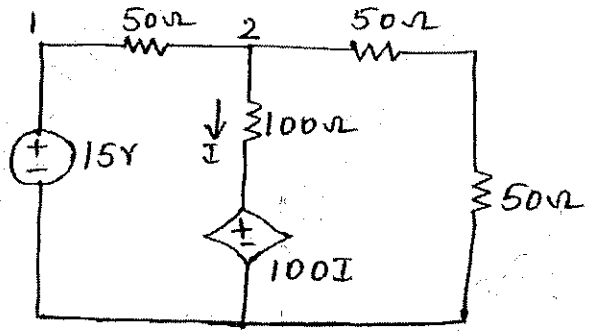
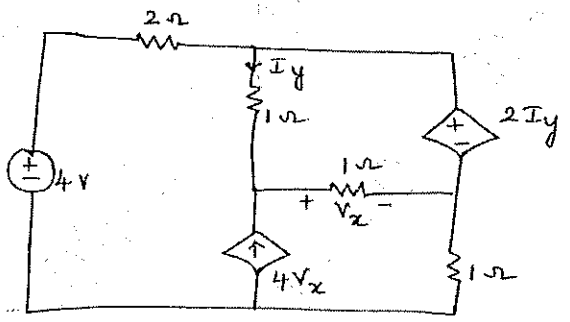
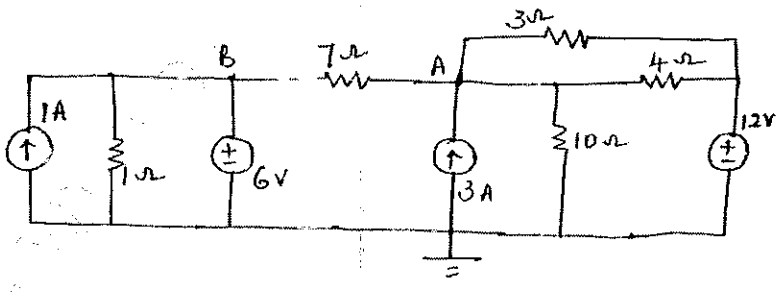
BEC304

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Network Analysis

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	**a.**	Make use of source transformation technique, to find the voltage V_2 at node 2 in the circuit shown in Fig.Q1(a).  Fig.Q1(a)	**5**	**L3**	**CO1**
	b.	Using Mesh analysis, find the power absorbed by 2 Ω resistor in the circuit shown in Fig.Q1(b).  Fig.Q1(b)	**8**	**L3**	**CO1**
	c.	Apply node analysis to find V_A for the network shown in Fig.Q1(c).  Fig.Q1(c)	**7**	**L3**	**CO1**

OR

Q.2	**a.**	Find the equivalent resistance, between A and B using star – delta transformation for the circuit shown in Fig.Q2(a).	**7**	**L3**	**CO1**

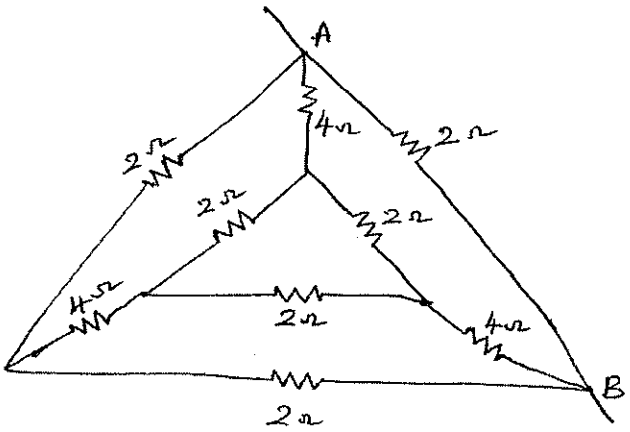


Fig.Q2(a)

	b.	Reduce the network shown in Fig.Q2(b), to find the current 'I' using source shifting and source transformation.	**7**	**L3**	**CO1**

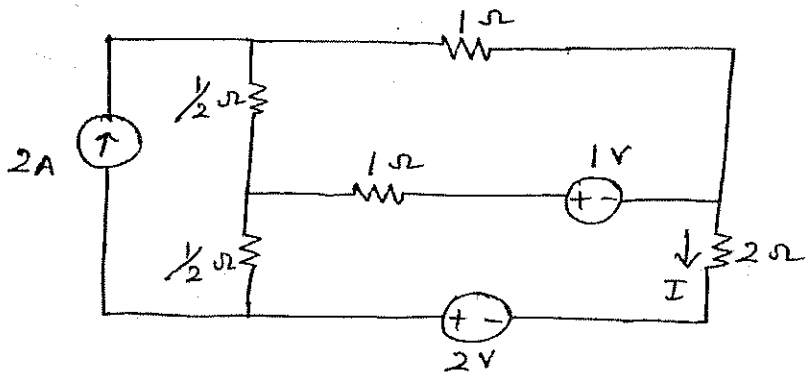


Fig.Q2(b)

	c.	Find the power delivered by the dependent voltage source in the network shown in Fig.Q2(c) using Node analysis.	**6**	**L3**	**CO1**

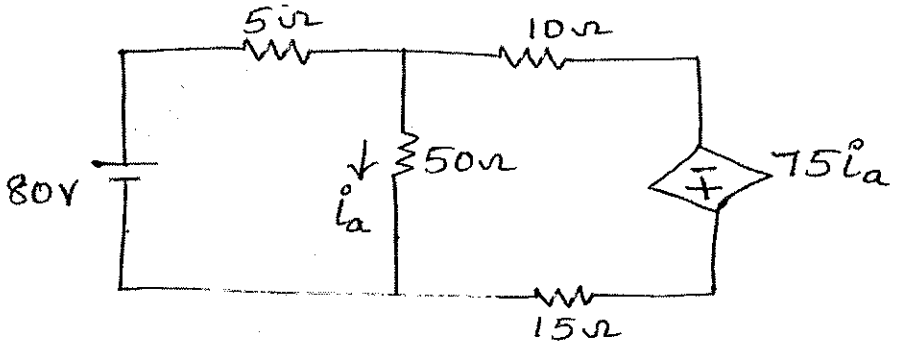
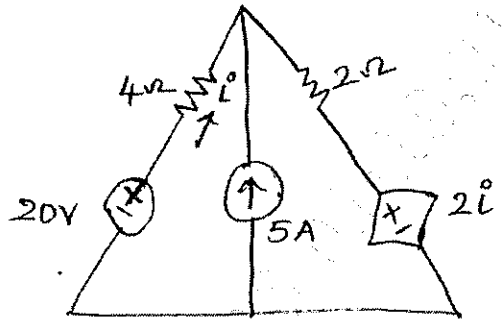
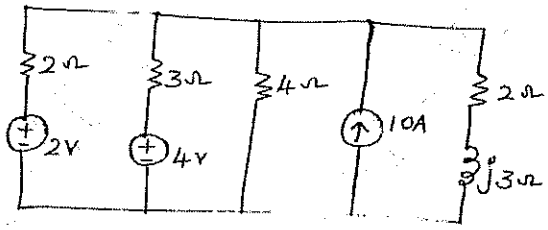
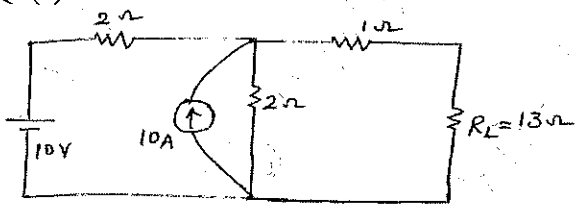
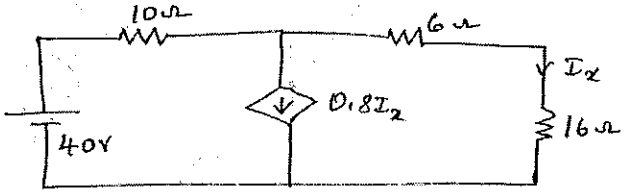
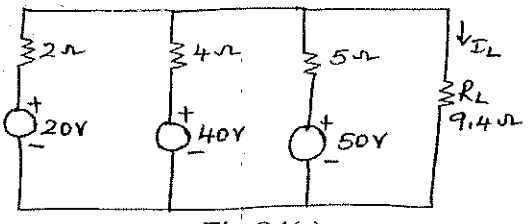
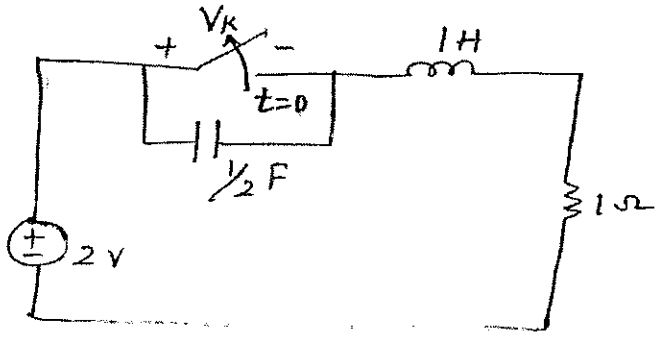
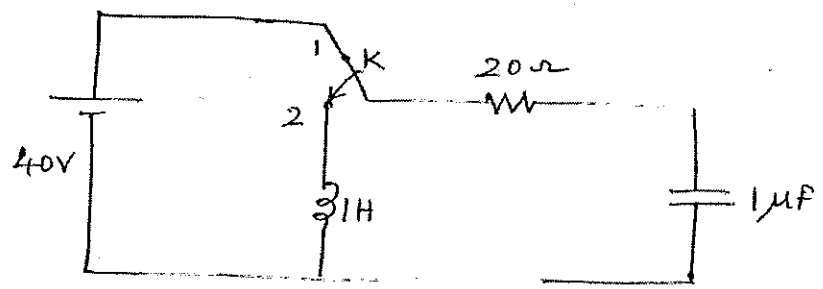
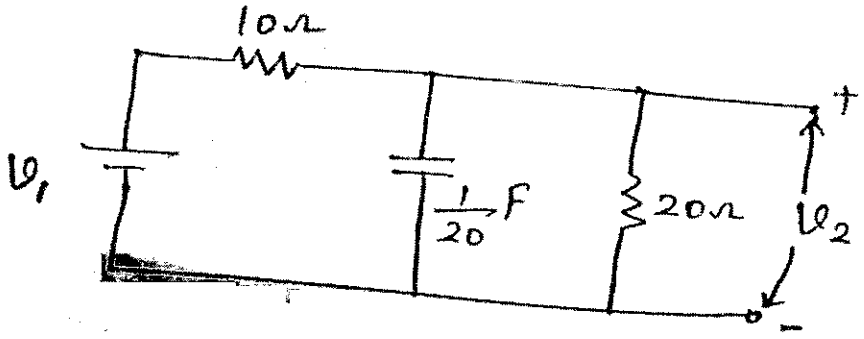


Fig.Q2(c)

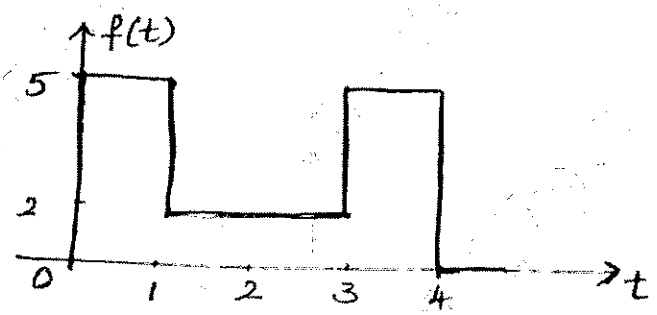
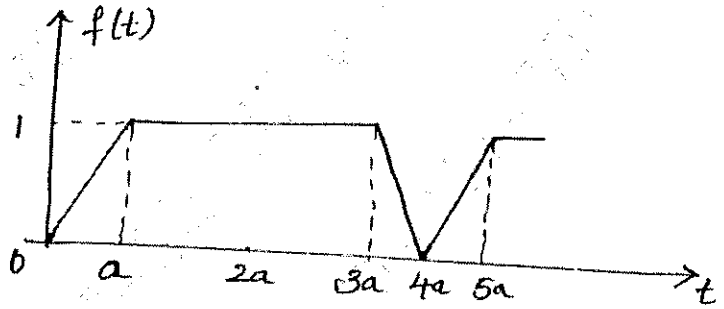
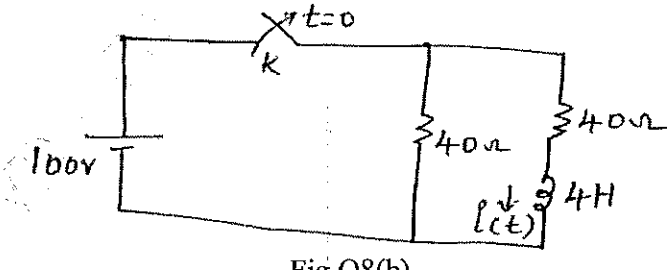
Module – 2

Q.3	**a.**	Use superposition theorem, to find the current 'i' for the circuit shown in Fig.Q3(a).  Fig.Q3(a)	**6**	**L3**	**CO2**
	b.	Use Millman's theorem, to find current flowing through (2 + j3)Ω impedance, for the circuit given in Fig.Q3(b).  Fig.Q3(b)	**6**	**L3**	**CO2**
	c.	State and find the condition for maximum power transfer in a AC circuit when load impedance is the invariable (Z_L).	**8**	**L2**	**CO2**
		OR			
Q.4	**a.**	Use Thevenin's theorem, to find the current through 'R_L' for the network shown in Fig.Q4(a).  Fig.Q4(a)	**7**	**L3**	**CO2**
	b.	Apply Norton's theorem to find the current through 16Ω resistor for the circuit shown in Fig.Q4(b).  Fig.Q4(b)	7	**L3**	**CO2**
	c.	Using Millman's theorem, find I_L through R_L for the network shown in Fig.Q4(c).  Fig.Q4(c)	**6**	**L3**	**CO2**

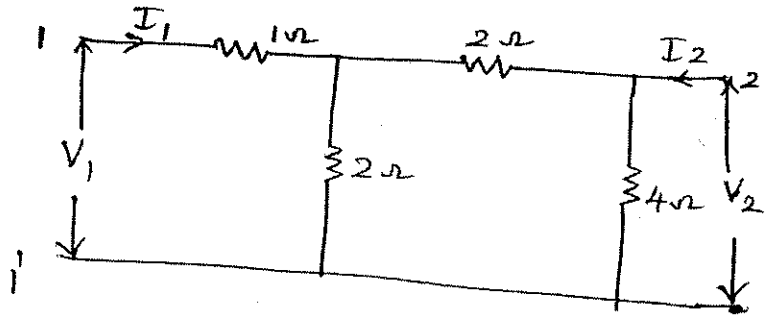
Module – 3

Q.5	**a.**	Explain the transient behavior of the Resistance, Inductance and Capacitor.	**10**	**L2**	**CO3**
	b.	The circuit is in steady state with switch K closed for the circuit shown in Fig.Q5(b). At t = 0, the switch is opened. Find the voltage across the switch V_K, $\frac{dV_K}{dt}$ at t = 0+.  Fig.Q5(b)	**10**	**L3**	**CO3**
		OR			
Q.6	**a.**	In the circuit shown in Fig.Q6(a), the switch K is changed from Position-1 to Position-2 at t = 0, steady state having been reached before switching. Evaluate i, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at t = 0+.  Fig.Q6(a)	**10**	**L3**	**CO3**
	b.	In the circuit shown in Fig.Q6(b), $V_1(t) = e^{-t}$ for t ≥ 0 and is zero for all t < 0. If the capacitor is initially uncharged, determine the value of $\frac{dV_2}{dt}, \frac{d^2V_2}{dt^2}, \frac{d^3V_2}{dt^3}$ at t = 0+.  Fig.Q6(b)	**10**	**L3**	**CO3**

Module – 4

Q.7	**a.**	Find the Laplace transform of the following functions : i) $t.e^{-at}$ ii) $\cos^3 3t$ iii) $\frac{1}{2a^2}\sin h\, a\, t \sin a\, t$.	**6**	**L3**	**CO3**
	b.	Find the Laplace transform of the following functions : i. Unit step function ii. Ramp function.	**6**	**L3**	**CO3**
	c.	Obtain the Laplace transform of the f(t) shown in Fig.Q7(c).  Fig.Q7(c)	**8**	**L3**	**CO3**
		OR			
Q.8	**a.**	Find the Laplace transform of the periodic waveform shown in Fig.Q8(a).  Fig.Q8(a)	**10**	**L3**	**CO3**
	b.	Find the current i(t) when switch K is opened at t = 0 having reached steady state before the switching and the circuit is as shown in Fig.Q8(b). Also find the current at t = 0.5 sec.  Fig.Q8(b)	**10**	**L3**	**CO3**

Module – 5

Q.9	**a.**	Define Z and Y – parameters. Express Z-parameters in terms of Y.	**10**	**L2**	**CO4**
	b.	Obtain h – parameters for the network shown in Fig.Q9(b).  Fig.Q9(b)	**10**	**L3**	**CO4**
		OR			
Q.10	**a.**	Derive the expressions for Half-power frequencies for a series RLC circuit.	**10**	**L3**	**CO4**
	b.	A series RLC circuit has R = 10 Ω, L = 0.3H and C = 100 μF. The applied voltage is 230 V, find : i. The resonant frequency ii. The quality factor iii. Lower and upper cut-off frequency iv. Bandwidth.	**10**	**L2**	**CO4**

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CBCS SCHEME

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat diagram, describe the functional units of a computer.	8	L2	CO1
	b.	Explain following with an example: i) One address instruction ii) Two address instruction iii) Three address instruction	6	L2	CO1
	c.	Write a short note: i) Basic Performance equation ii) Clock rate	6	L2	CO1
		OR			
Q.2	a.	With a neat diagram, explain basic operational concept of computer.	7	L2	CO1
	b.	With help of example, explain little Endian and Big Endian byte assignment with a neat diagram.	6	L2	CO1
	c.	Explain memory operations.	7	L2	CO1
		Module – 2			
Q.3	a.	Define Assembler Directives. Explain various assembler directives used in Assembly language program.	10	L2	CO2
	b.	Define subroutine and parameter passing. Explain how to pass the parameter by value and by reference.	10	L2	CO2
		OR			
Q.4	a.	Define stack, explain PUSH and POP operations on stack with neat diagram.	10	L2	CO2
	b.	Explain shift and rotate operations with examples.	10	L2	CO2
		Module – 3			
Q.5	a.	Define Interrupt. Explain the various ways of enabling and disabling interrupts.	10	L2	CO3
	b.	Explain DMA technique and its importance.	10	L2	CO3

		OR			
Q.6	**a.**	Explain different ways of handling multiple I/O devices.	**10**	**L2**	**CO3**
	b.	Illustrate interrupt priority scheme with neat diagram.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Explain the principle of working of magnetic disk.	**10**	**L2**	**CO4**
	b.	Explain the internal organization of 1K × 1 dynamic memory chip with neat diagram.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain the interfacing of the main memory to the processor.	**10**	**L2**	**CO4**
	b.	Explain virtual memory organization with a neat diagram.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Explain single bus organization of the datapath inside a processor with neat diagram.	**10**	**L2**	**CO5**
	b.	Discuss hardwired control unit organization relevant diagram.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain complete processor with neat diagram.	**10**	**L2**	**CO5**
	b.	Develop the complete control sequence for the executing instruction Add (R_3), R_1.	**10**	**L2 L3**	**CO5**

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